USB hardware and PCB guidelines using STM32 MCUs

Introduction

The STM32 MCU family includes a group of products embedding a USB (Universal Serial Bus) controller and a PHY (physical layer of the open systems interconnection model); the list of applicable products is detailed in *Table 1*.

The USB controller and the PHY features enable the support of full speed (FS) USB 2.0 with a data rate of 12 Mbit/s. This application note provides guidelines for PCB (printed circuit board) design to help ensure electrical compliance with the USB standards.

Some high performance STM32 MCUs propose also a ULPI (USB 2.0 transceiver macro cell interface and low-pin interface), which allows to have a USB 2.0 with high-speed data compatibility by connecting an external ULPI HS PHY. Refer to *Table 4* for the list of STM32 devices featuring the ULPI capability. This application note also covers details about this configuration.

Table 1. Applicable products

Type	Part numbers, product lines and product series
Microcontrollers	STM32F2 Series, STM32L1 Series, STM32F0x2, STM32F102, STM32F103, STM32F105/107, STM32F302, STM32F303, STM32F373, STM32F401, STM32F405/415, STM32F407/417, STM32F411, STM32F412, STM32F427/437, STM32F429/439, STM32F446, STM32F469/479, STM32F7x5, STM32F7x6, STM32F7x7, STM32F7x8, STM32F7x9, STM32L0x2, STM32L0x3, STM32L4x2, STM32L4x3, STM32L4x5, STM32L4x6, STM32F070C6, STM32F070CB, STM32F070F6, STM32F070RB, STM32F048C6, STM32F048G6, STM32F048T6, STM32F078CB, STM32F078RB, STM32F078VB

Contents

List of tables

List of figures

1 Layout guidelines for USB FS devices

All of the STM32 MCUs embedding a USB PHY (refer to *Table 1*) are full speed capable.

The USB full speed data is 12 Mbit/s, and while this speed does not represent a high data rate itself, successful and compliant operations are guaranteed by following the basic rules explained in this section.

A platform supporting USB full speed devices must ensure a PCB trace routing achieving 90 ohms +/-15% differential and having a common mode impedance of 30 ohms +/-30%.

1.1 PCB track impedance and routing on FS data lines

The full speed USB driver impedance on STM32 MCUs is guaranteed by design to be between 28 ohms and 44 ohms. The result is that these products do not need an external resistor on the board for the output driver impedance.

The track routing should respect 90 ohm +/-15% differential from the STM32 MCU's package to the receptacle. It is important to route the two data lines in parallel to ensure the best impedance matching. A 45 ohm +/-15% single ended trace is recommended.

Routing USB signals using a minimum of vias and corners reduces the signal reflections and the impedance changes. When it becomes necessary to turn by 90°, it is preferred to use two 45° turns or an arc instead of making a single 90° turn. This action reduces the reflections on the signal by minimizing the impedance discontinuities.

1.2 Protection against electrostatic discharge (ESD) and electromagnetic interference (EMI)

A protection against ESD and EMI is needed. The system should comply with both the JESD22-A114D standard (also known as the human body model standard) and with the IEC 61000-4-2 standard.

The HBM requires that the USB pins of the component device are tolerant to up to 2 kV discharge, this is the case for the STM32 MCUs. Refer to *Figure 1* and *Table 2* for JESD22-A114D standard test waveform and class levels. For more details on this topic please refer to the document *System Level ESD -expanded* available at www.jedec.org.

The system should also comply with the IEC 61000-4-2 standard on USB lines when they are connected to the receptacle. This standard is far from the HBM standard. Refer to *Figure 2* and *Table 3* for IEC 61000-4-2 standard test waveform and class levels.

To see the current pulse difference between the two tests, compare the *Figure 1* and *Figure 2* below.

Figure 1. JESD22-A114D standard test waveform

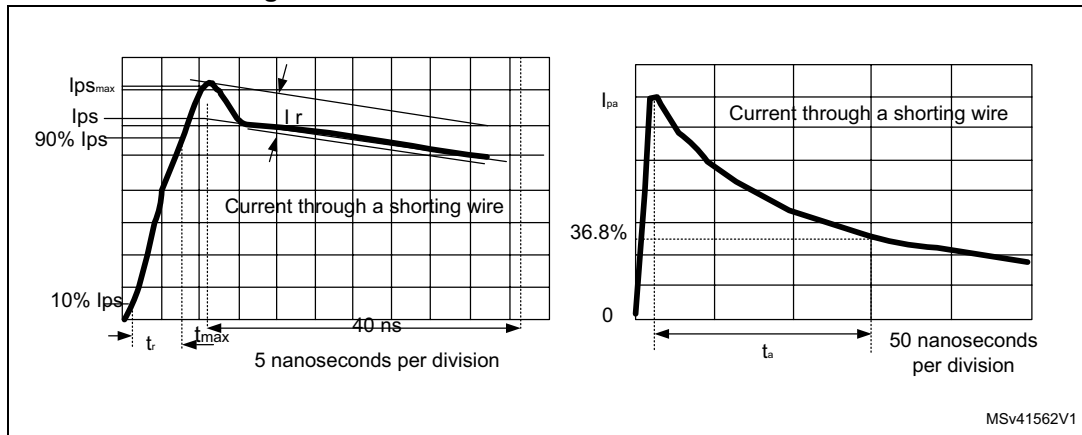

Table 2. JESD22-A114D standard class levels

Class	Voltage range	Current range
Class 0	V < 250 V	I < 0.17 A
Class 1A	250 V < V < 500 V	0.17A < I< 0.33 A
Class 1B	500 V < V < 1000 V	0.33 A < I < 0.67 A
Class 1C	1 kV < V < 2 kV	0.67 A < I < 1.33 A
Class 2	2 kV < V < 4 kV	1.33 A < I < 2.67 A
Class 3A	1 kV < V < 8 kV	2.67 A < I < 5.33 A
Class 3B	V > 8kV	I > 5.33 A

Figure 2. IEC 61000-4-2 standard waveform
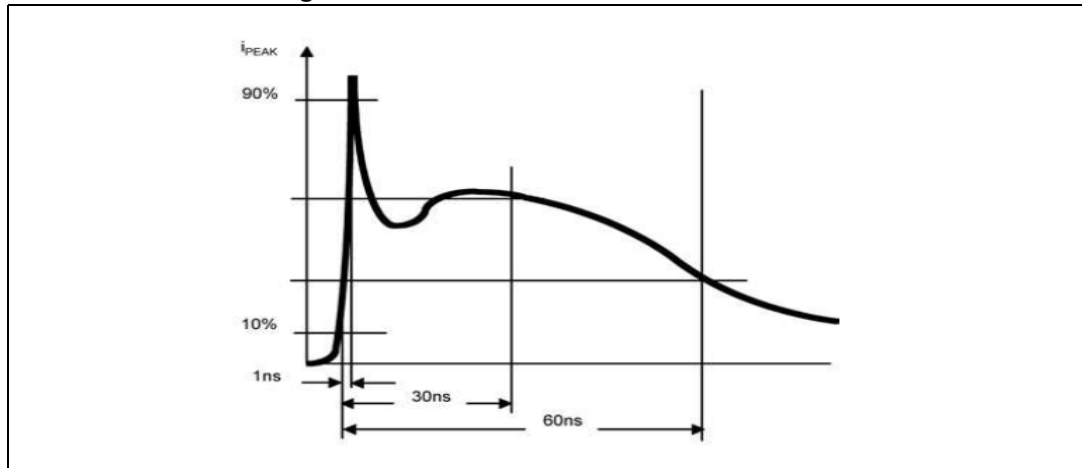
Table 3. IEC 61000-4-2 standard class levels

Level	Contact	Air	Peak current
	indicated voltage (kV)		(A)
1	2	3	7.5
2	4	4	15
3	6	8	22.5
4	8	15	30

The component needs to be placed as close as possible to the receptacle to add ESD protection against high ESD surge. The USBLC6 component is recommended for such protection on VBUS and USB data lines. For OTG (on-the-go) use cases, the ID pin should also be protected against high ESD surge.

2 Hardware guideline for FS upstream port implementation

In peripheral mode, VBUS power is always provided through the cable. The USB FS impedance driver is always managed internally to avoid the need to add external serial resistors on the dataline path.

There are two main use cases:

- Self-powered applications: a platform with a power source that needs the ability to act as an upstream port on the cable insertion.
- Bus-powered applications: a platform supplied only through VBUS and acting as an upstream port.

2.1 Upstream port in self-powered applications

In order to optimize the platform power consumption on self-powered platforms, only a USB PHY and a controller should be started on the VBUS detection.

It is recommended to implement a resistor bridge to lower the voltage used for VBUS detection. This recommendation is even more important when VDD on the STM32 MCU is not present while VBUS is supplied from the connector.

The output of the resistor bridge must be connected to a FT IO on the STM32 MCU. Note that no power is sunk from VBUS and that the USBLC6 should be placed as close as possible to the USB receptacle.

Figure 3. Upstream self-powered platform based - USB PHY with DP pull-up
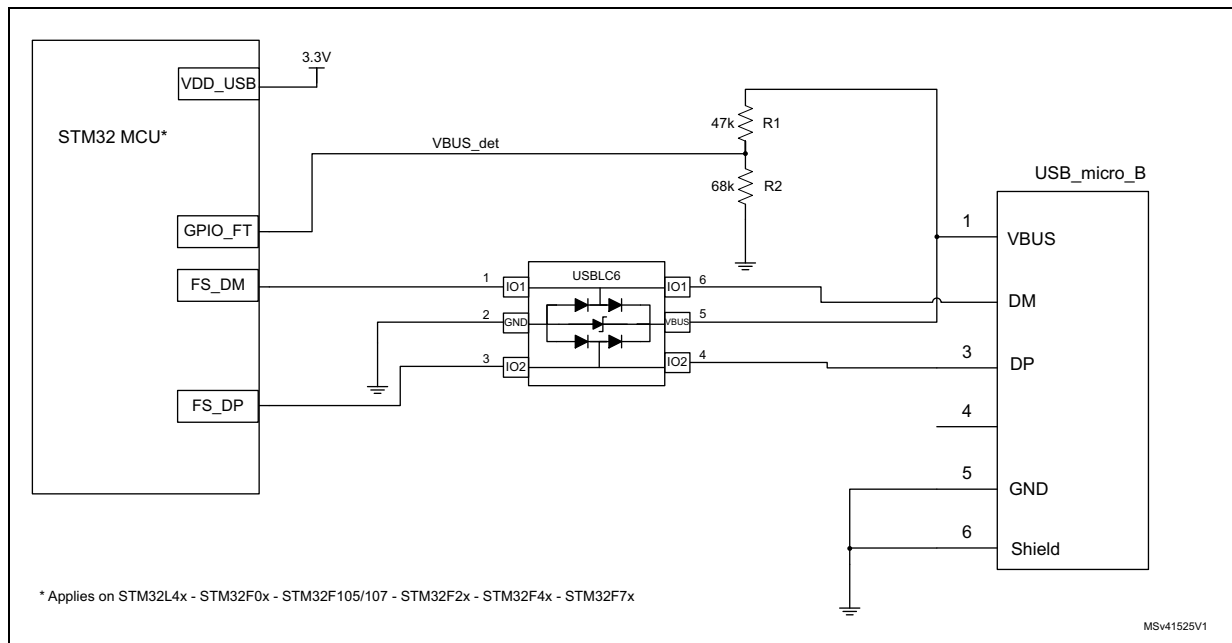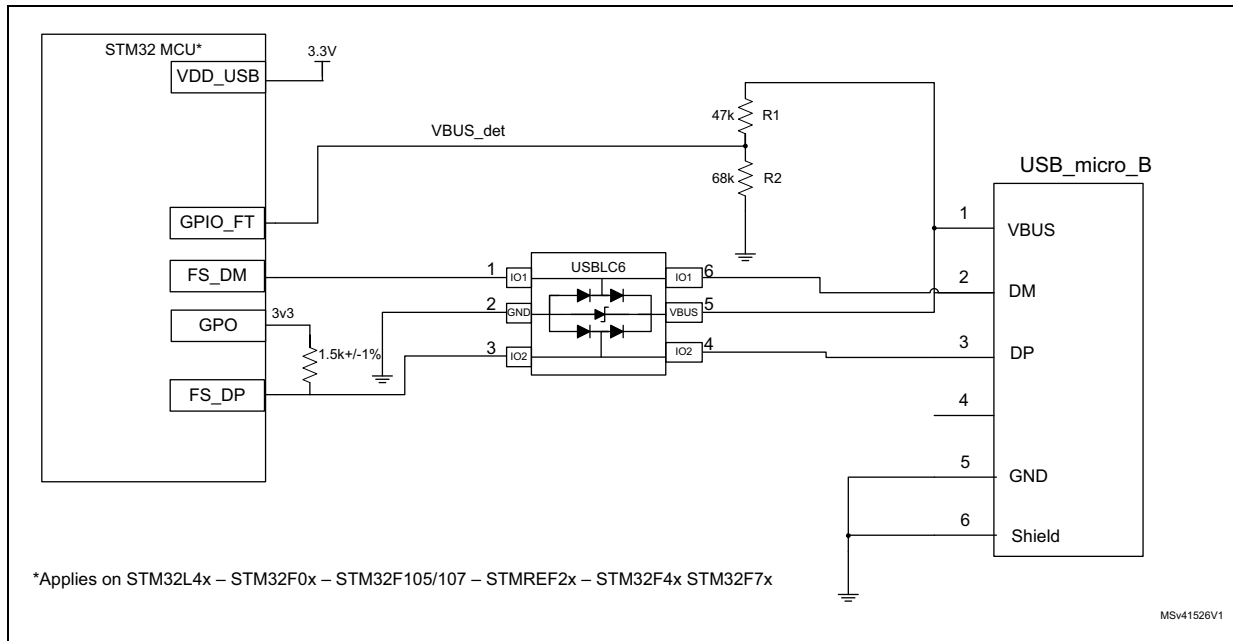
Figure 4. Upstream self-powered platform based - USB PHY without DP pull-up

1. As DP pull-up should be connected only when VBUS is plugged, a GPO from the MCU is used to drive it after the VBUS detection.

2.2 Bus-powered applications

A bus-powered application is an application where the platform supply comes exclusively from VBUS. The LDO (low-dropout) is mandatory to lower the input supply of the STM32 MCU.

The PHY and the controller must be active all the time to keep the host alive and to keep VBUS available. The protection chip USBLC6 should be as close as possible to the USB connector.

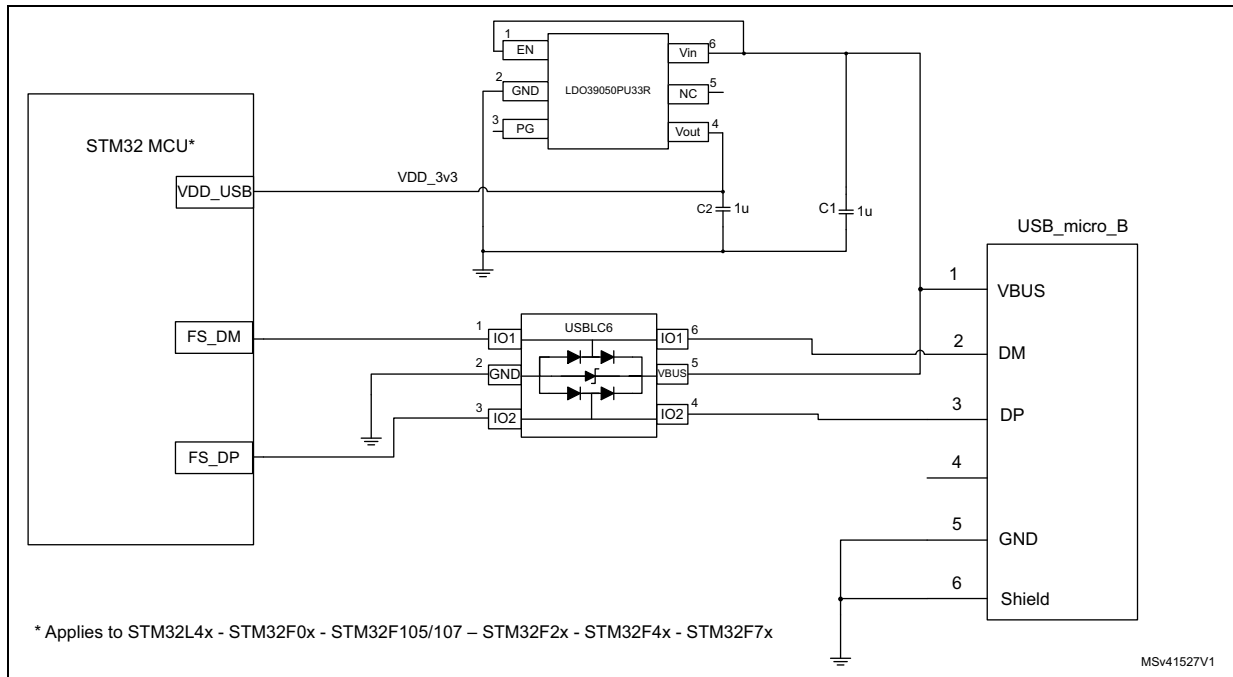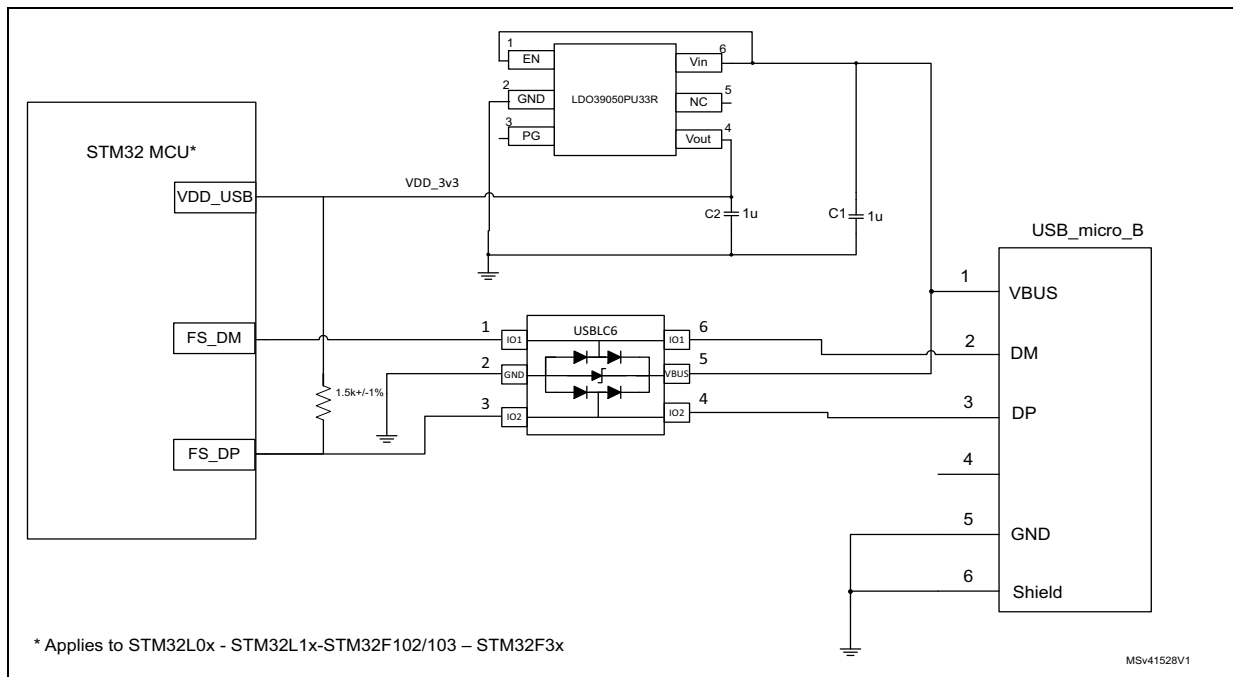## Figure 5. Bus-powered application - USB PHY with DP pull-up

* Applies to STM32L4x - STM32F0x - STM32F105/107 – STM32F2x - STM32F4x - STM32F7x

MSv41527V1

Figure 6. Bus-powered application - USB PHY without DP pull-up

* Applies to STM32L0x - STM32L1x-STM32F102/103 – STM32F3x

MSv41528V1

3 Hardware guideline for FS and LS downstream port implementation

The USB specification allows the system to turn OFF the VBUS generation in the System Suspend mode in order to implement a switch.

The USB specification requires that if an overload on VBUS occurs, it is indicated to the user. A switch with over-current protection provides the information on the VBUS overload to the STM32 MCU.

An example of a USB FS downstream implementation that allows a maximum current of 500 mA on VBUS and uses a STMPS2151STR switch is illustrated in *Figure 7* below. The ESD protections are required and should be placed as close as possible to the USB receptacle.

Figure 7. USB FS downstream implementation
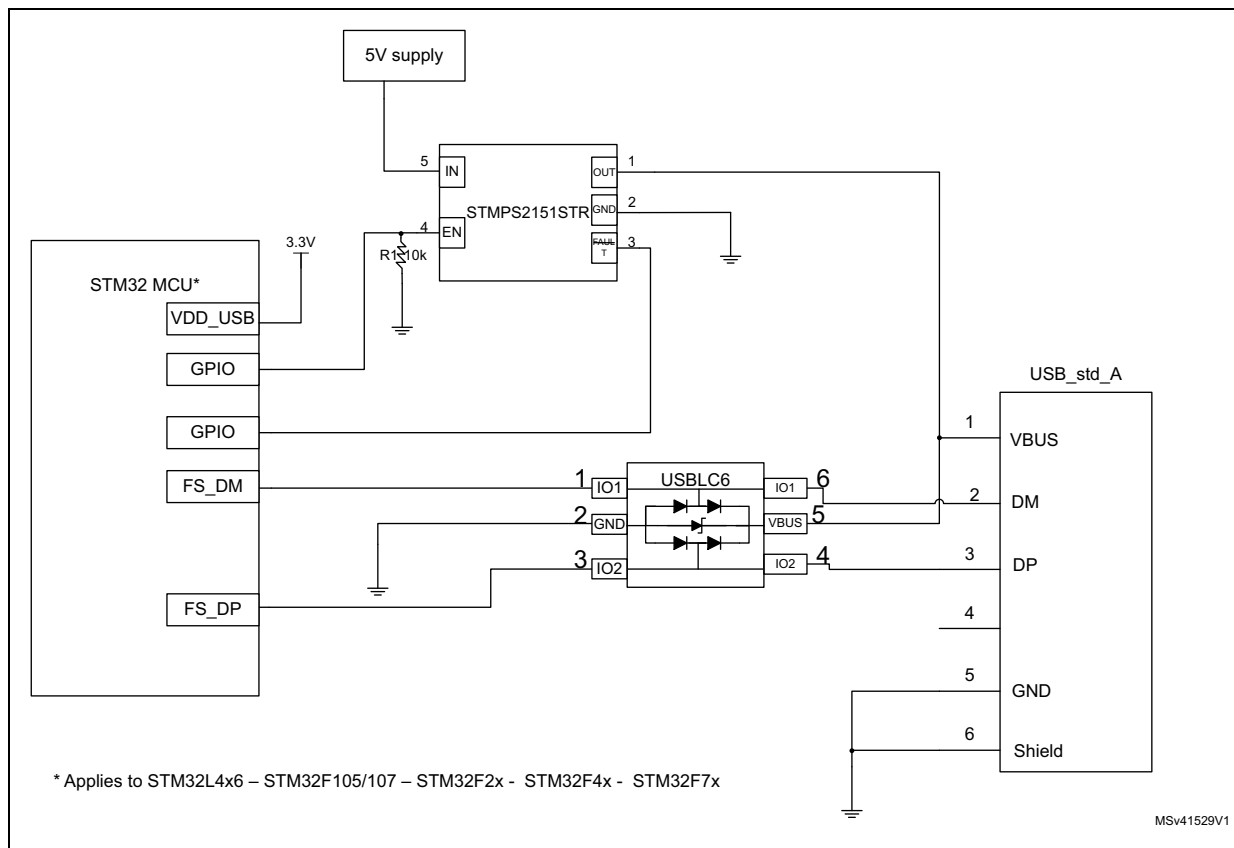
4 Hardware guideline for OTG product implementation

The USB on-the-go products address scenarios that allows portable devices and non-PC hosts to have the following enhancements:

- targeted host capability to communicate with a list of selected USB peripherals
- support for direct connections between OTG devices
- power saving features to preserve battery life

A new pin on connector, named ID, identifies the USB power role.

Consequently, the OTG platforms should implement the following features:

- an STM32 MCU supporting the OTG feature
- a Micro AB connector: the USB role is identified through the ID pin
- a VBUS generation when the OTG device acts as a downstream facing port
- a VBUS current overflow both monitoring and acting as a downstream facing port

Figure 8. OTG schematic implementation on battery-powered application
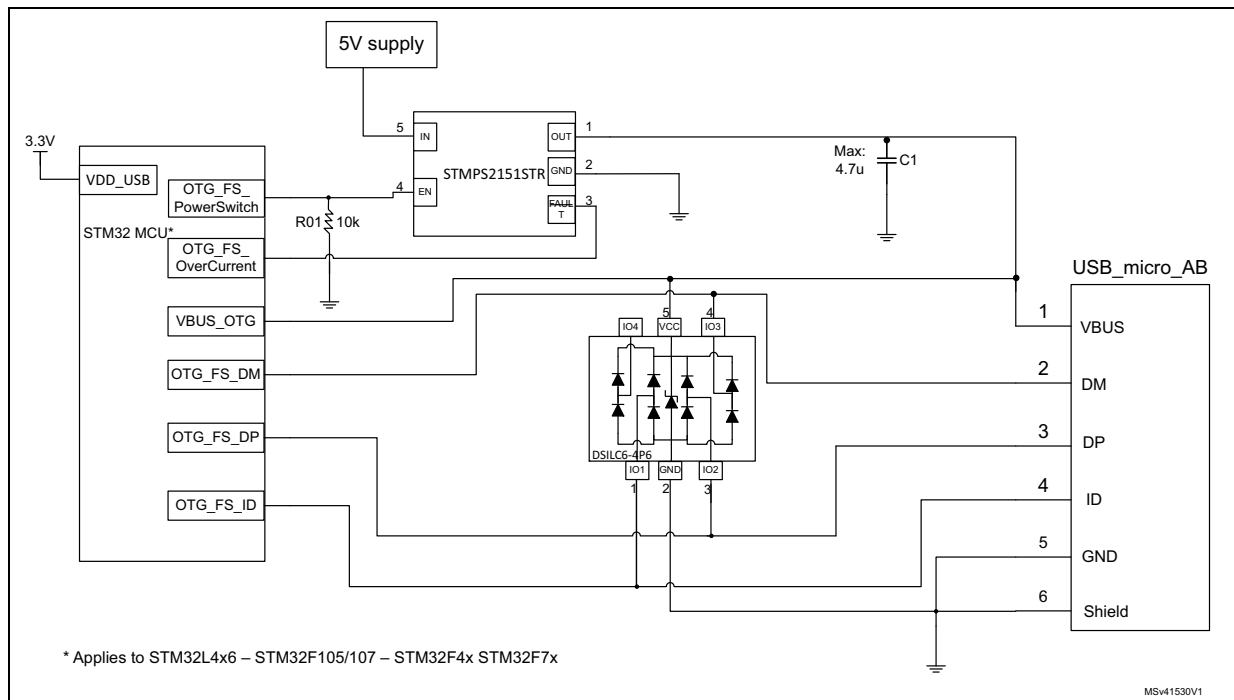
Note that the DSILC6-4P6 should be placed as close as possible to the receptacle and that the STMPS2151STR switch allows up to 500 mA output current.

When an over-current is detected, the information is sent to the STM32 software that alerts the user about the issue. It is recommended to route VBUS far from a DP/DM.

The STM32 MCU must always be supplied when the platform is connected as device to a host. In the case of dead battery support, the VBUS divider must be used as shown in *Figure 3: Upstream self-powered platform based - USB PHY with DP pull-up on page 8*.

5 OTG USB high speed PHY connected to STM32 through the ULPI link

The USB standards propose routing guidelines for high speed USB platforms in the *High Speed USB Platform Design Guidelines* document available on USB-IF website.

Note that for a full speed driver that is part of high speed driver, the impedance is 45 ohms +/- 10%.

A crystal oscillator is required to guarantee a clock precision for the ULPI sampling and for the USB HS data sampling. This requirement is due to the ULPI PHY being master of a ULPI CLK. It is recommended to use a common ESD mode filter for the USB HS data and it must be placed as close as possible to the connector. The OTG specification requires a 4.7 uF maximum on VBUS.

Figure 9 shows an example of an USB HS using the STM32 ULPI link. Refer to *Table 4* for the list of STM32 devices featuring the ULPI capability.
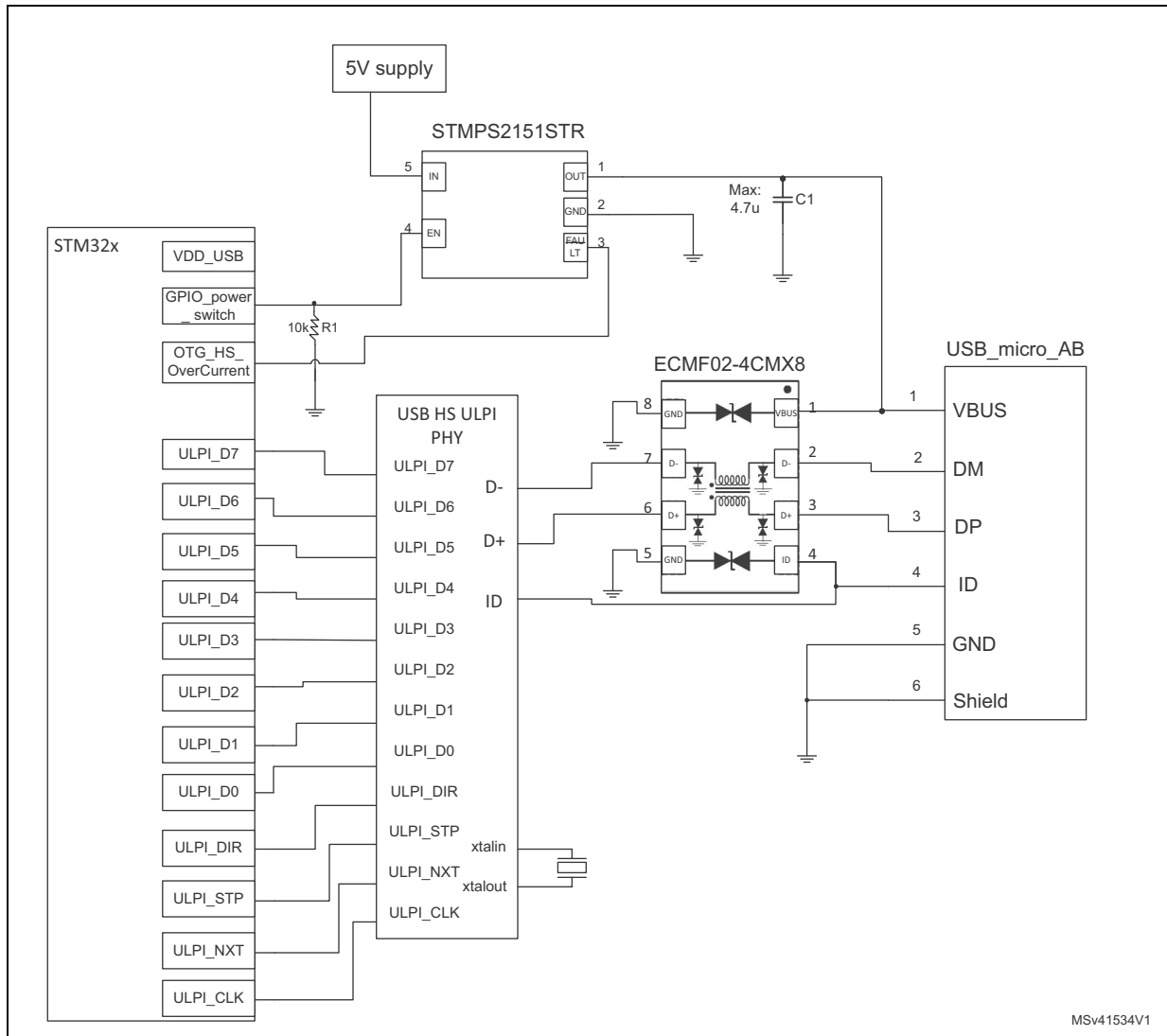
Figure 9. USB HS using STM32 ULPI link configuration

MSv41534V1

Table 4. STM32 products with USB HS ULPI capability

Type	Product series and lines
Microcontrollers	STM32F2 Series STM32F405/415, STM32F407/417, STM32F427/437, STM32F429/439, STM32F446, STM32F469/479 STM32F7x5, STM32F7x6, STM32F7x7, STM32F7x8, STM32F7x9

6 References

System Level ESD-expanded, JEDEC, September 2013.

Improve System ESD Protection While Lowering On-Chip ESD Protection, *www.*mobiledevdesign.com, February 2009.

USB 2.0 specification, revision 2.0, April 2000, available at www.usb.org.

On The Go and Embedded Host Supplement to the USB revision 2.0 specification, revision 2.0, July 2012 available at www.usb.org.

High Speed USB Platform Design Guidelines available at www.usb.org.

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
10-Aug-2016	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY