NAND

Date

* ISE design suite 14.7 —— clk. (app)

file
new project
Name —— NANDing
location —— make new folder — ok
working directory — —
Description — —

Next

Next

Finish

Hierarchy
xc6slx9 — right clk — new source

VHDL module
filename - nandi
location — —
Next

Port name	Direction
a	in
b	in
y	out

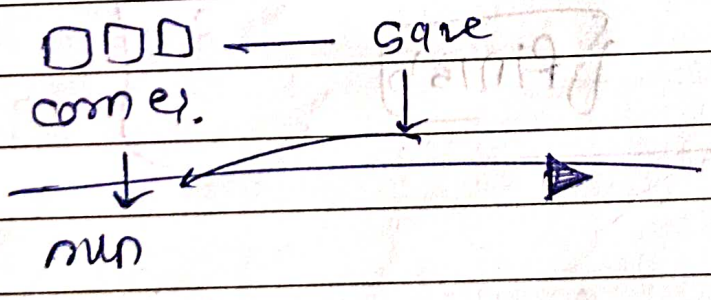
next

finish

code येती.

Nand gate formula →

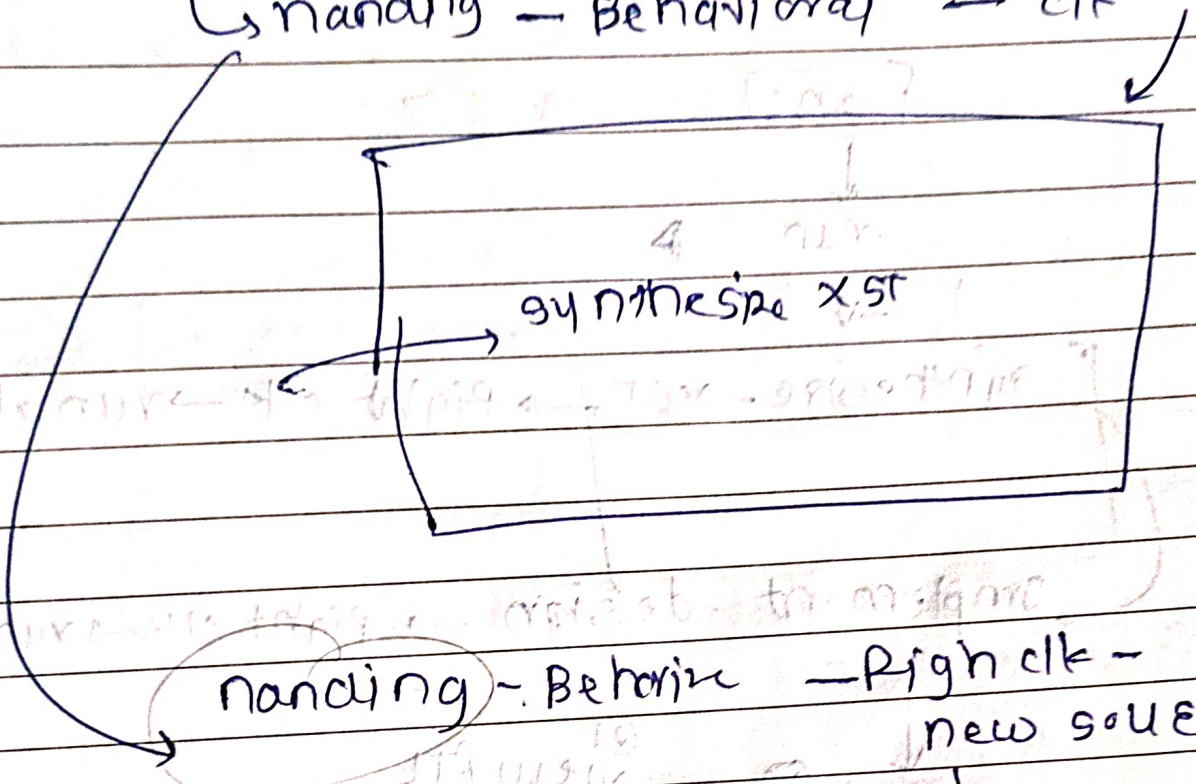
```
begin
    y <= not (A and B);
```



Hierachy

└ xc6

└ nanding — Behavioral — clk



nanding - Behavior — Right clk -

new source

↓

implementation constraints

file

↓

filename - nanding

↓

Next

↓

finish

↓

(program - निर्देश)

Date

NET "A" LOC = "P6";
—"— B ——"—— "P58";
—"— Y ——" ——"P5";

Save
↓
run
↓
synthesize - XST → Right clk → run all

Implement design → Right clk → run all.
↓
② view RTL
① synthesize ← Right click ← Rerun all
↓
ok

diagram होता
double clk करके screen करती

Date

Implement design — Right click - runall

[] generate programming
↓ Right clk — Run

✓ green tick generate pr

Stepup joint karaycha.
Hiaeachy

⊕ — nanding - Behavioral
click → (file दिसते) — nanding.ucf
(user contract file)

configure target device → Right clk → run
[ok]

new file open होते.

↳ Boundary scan → double click
Right click to add device or Initialize

Right click — initialize chain
↓
diagram yete
[NO]

diagram वरती click करायचे.

| double click

↓

foldee ↓

· bit file select

↓

open

↓

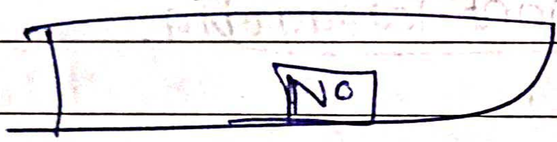
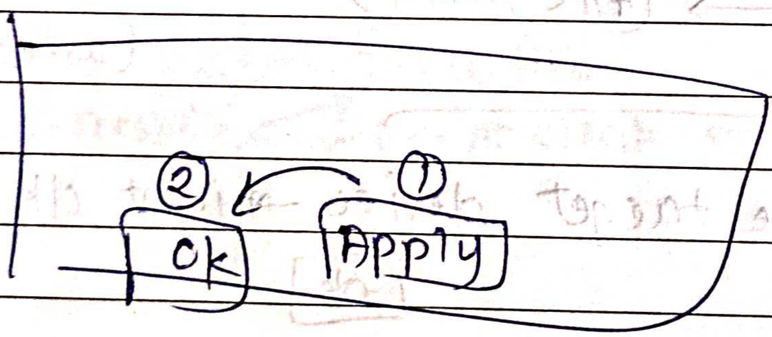


diagram — Right clk — program



Program successed.