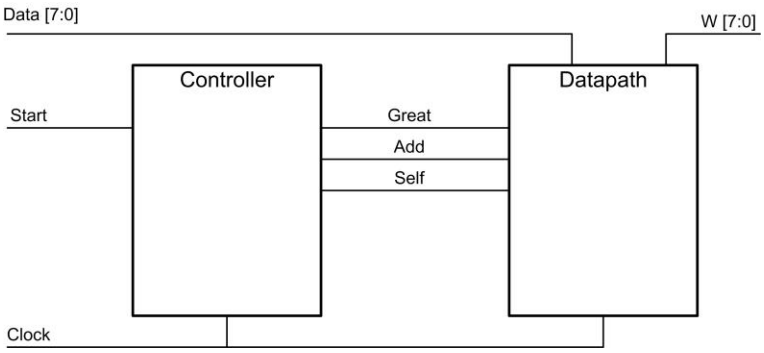
TEHRAN UNIVERSITY
Electrical and Computer Engineering Department
Digital System Design with Hardware Description Languages
Fall 1389 / *Homework 2 – RT Level Synthesis*

Design a data collection system with *Start* and *Data [7:0]* inputs. The System has a *W [7:0]* output that is either the largest of data on *Data*, the accumulative add of data on *Data*, or the same as the data on *Data*. Always after a **1***01*, **1***10*, or **1***00* on *Start*, the sequence of 8-bit data vectors begins on *Data*. The end of data is indicated when a sequence of **1***11* is detected on *Start*. The first bit on *Start* is considered the marker and the next two bits are the instruction. *01* is for *Greater*, *10* is for *Add*, *00* is for *Self*, and *11* is for *End*. The circuit behaves as follows:

- After **1***01* and before **1***11* on *Start*, the largest of data on *Data* will appear on *W*.
- After **1***10* and before **1***11* on *Start*, the sum of all data on *Data* will appear on *W*.
- After **1***00* and before **1***11* on *Start*, the same data that appears on *Data* will appear on *W*.

A. Design the controller of this system. The controller has *Start* and *Clock* inputs, and three outputs for *Greater*, *Add*, and *Self*. The outputs become **1** and stay **1** depending on the sequence received on *Start*. Show a complete state diagram and show one-hot implementation.
B. Write VHDL description of the controller.
C. Write VHDL code for the datapath of this system. The datapath behaves according to the instruction it receives from the controller. Show the complete block diagram of the datapath. Show complete VHDL code of the datapath in accordance you're your block diagram.
D. Show a diagram that shows the details of wiring and interconnections of the datapath and the controller.
E. Write complete VHDL code of the data collection system.
F. Develop a testbench for a comprehensive testing of the circuit.


Data [7:0]
W [7:0]
Controller
Datapath
Start
Great
Add
Self
Clock