TEHRAN UNIVERSITY
Electrical and Computer Engineering Department
Digital System Design with Hardware Description Languages
Fall 1389 / *Homework 6 – VHDL Channels*

NOC Switch

In this homework you are to design a switch that can be used as the building block of a Network on Chip (NoC). The switch has 5 pairs of input and output ports. Four of these pairs are used for communicating with four neighbor switches and the fifth pair for communicating with a local Processing Element (PE). There is a buffer capable of storing multiple flits each of 8 bits length corresponding to each input port that stores the incoming flits. Each input port has a port controller handling the buffer and handshaking with the data sending element. There are two lines between each port and its neighboring element for handshaking, *Req* and *Ack*. A data sending neighbor puts a flit on the Data_in parallel lines and asserts *Req*. The port controller that continuously monitors the *Req* line loads the flit into its buffer and asserts the *Ack* line. When the buffer is full the sending neighbor is informed via *full* signal. In this situation the neighbor suspends the data sending process until the buffer has some empty place. The switch has a routing table that is used to determine the output port corresponding to a packet target address. Figure 1 shows this signaling.

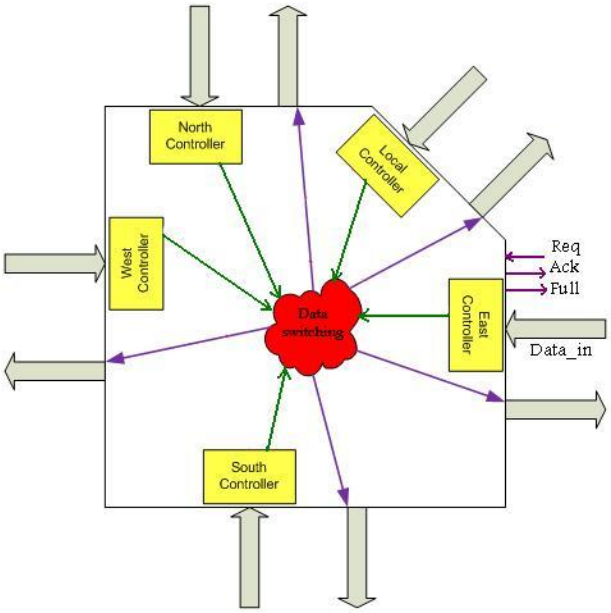

Figure 1. Block diagram of a sample switch

Assume that each packet of data is composed of a header flit, 6 data flits, and a tail flit. Each flit is 8 bits wide. The header flit is an 8 bit number representing the target PE number. Assume that the switching protocol is wormhole. In this protocol when a switch receives a header flit, it tries to reserve the corresponding output port according to the target address. The reserved output port remains in this state until all data flits are transferred and the tail flit is received that causes the reserved port to be released.

- Design a switch with the above specification. All the must be synthesizable.
- Use 9 of these switches to construct a 3 by 3 mesh connecting 9 PEs. You can describe your PEs using high level constructs not necessarily synthesizable.
- Write a thorough testbench to show the correctness of your design in all the ordinary and corner cases. The correct use of testbenches and its comprehensiveness is a part of your final grade.