JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

Homework 6

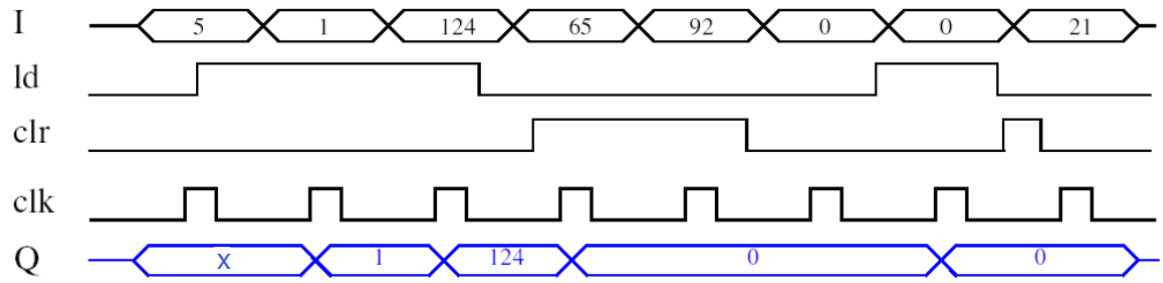
Assigned: June 28, 2018

Due: July 5, 2018, 2:00pm.

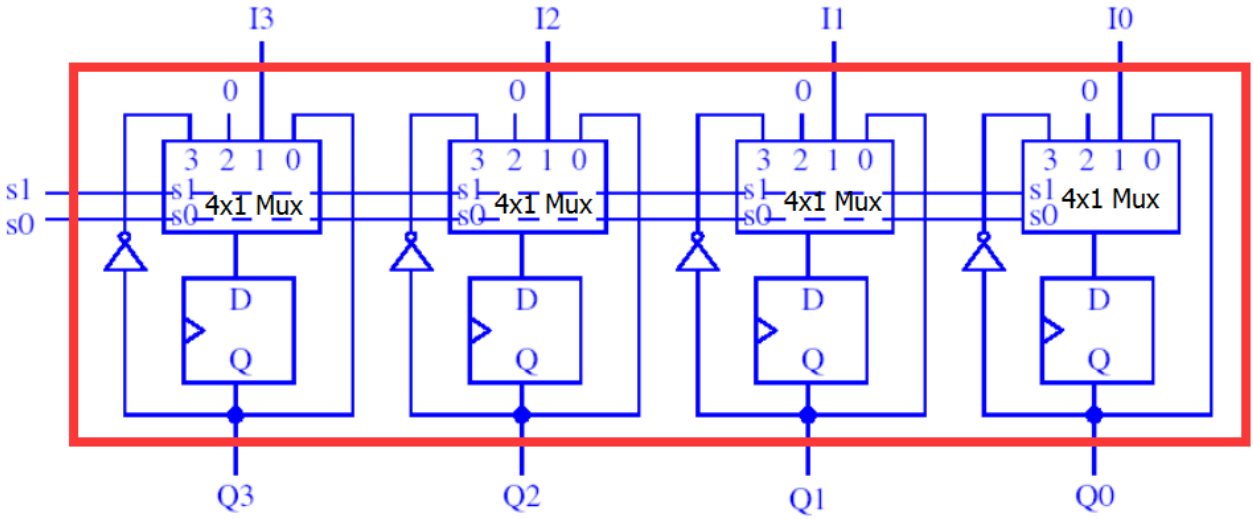
The homework should be submitted in hard copies.

1. Problem 4.2 (10 points)

4.2 Trace the behavior of an 8-bit parallel load register with input I, output Q, load control input *ld*, and synchronous clear input *clr* by completing the following timing diagram.

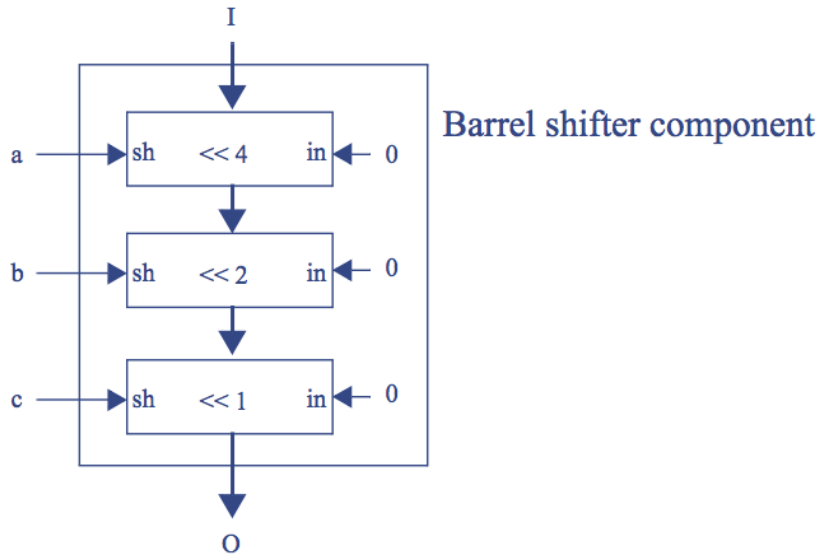


2. Problem 4.3, using components to draw schematic (20 points)

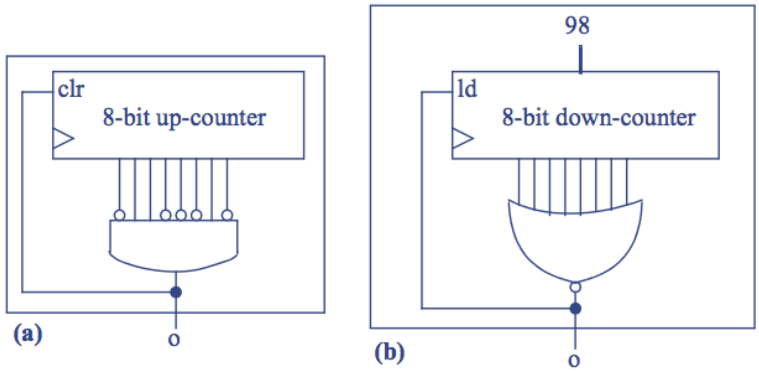


3. Problem 4.46. Draw schematic. (20 Points).

The solution just uses a single barrell shifter component. The internals of such a component are shown below for convenience.

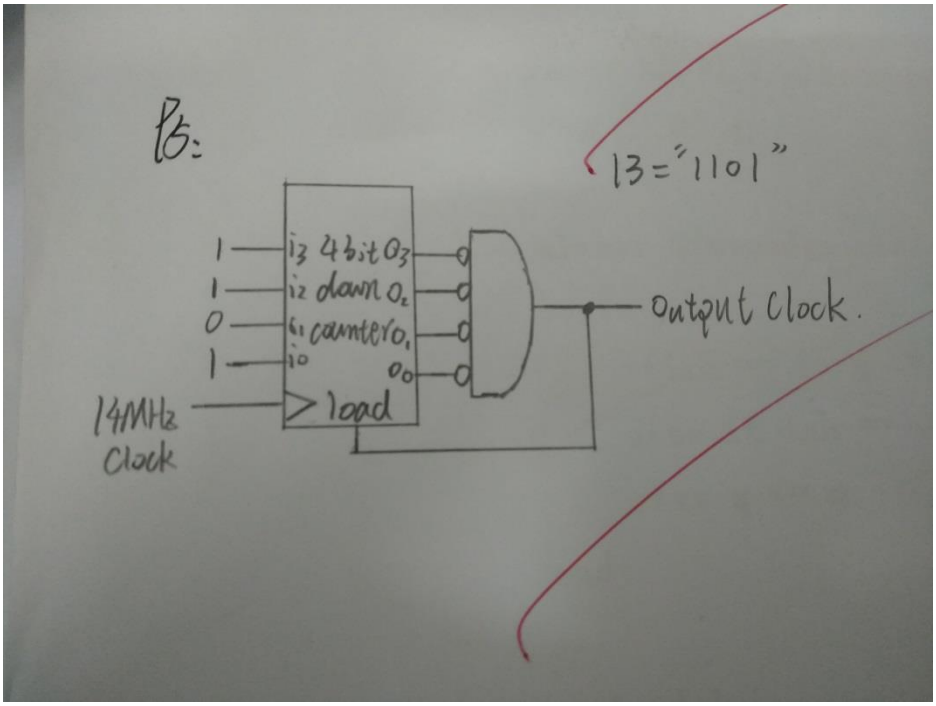


4. Problem 4.57. Draw schematic (a), (b). (20 points)



(c) The circuit implemented in (a) is smaller, while the circuit implemented in (b) is easier to modify to pulse at a different rate.

5. Problem 4.59. Draw schematic (10 Points)



6. Model a Universal Shift Register (shown below) with Verilog. Simulate your design. (20 Points)

```
23  module Q6(Q, SI, D, Sh, L, CLK);
24    input SI, Sh, L, CLK;
25    input [3:0] D;
26    output [3:0] Q;
27
28    reg [3:0] Q;
29
30    always @ (negedge CLK)begin
31      if (Sh) begin
32          Q[2:0] <= Q[3:1];
33          Q[3] <= SI;
34          end
35      else if (L) Q <= D;
36      else Q <= Q;
37    end
38
39  endmodule
```