Introduction

VE311 Electronic Circuits (Summer 2019)

Dr. Chang-Ching Tu

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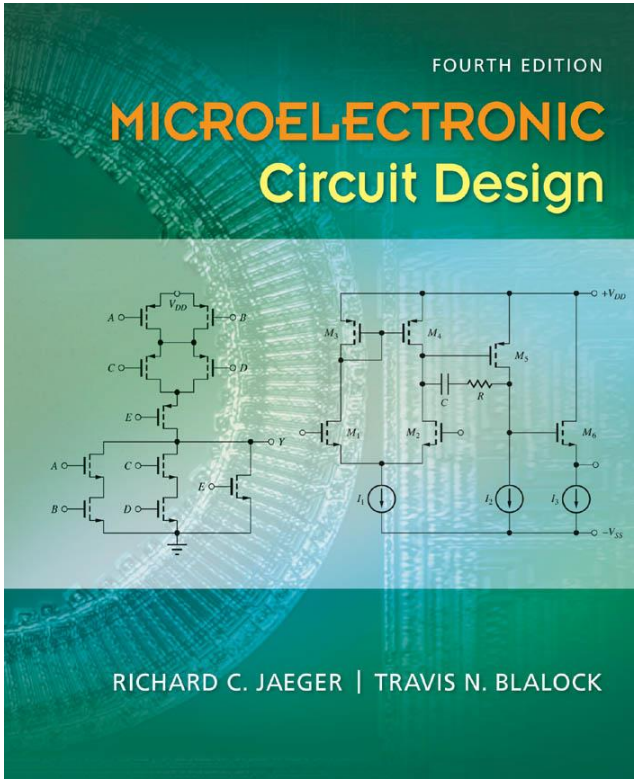
Last Updated on **May 13, 2019**

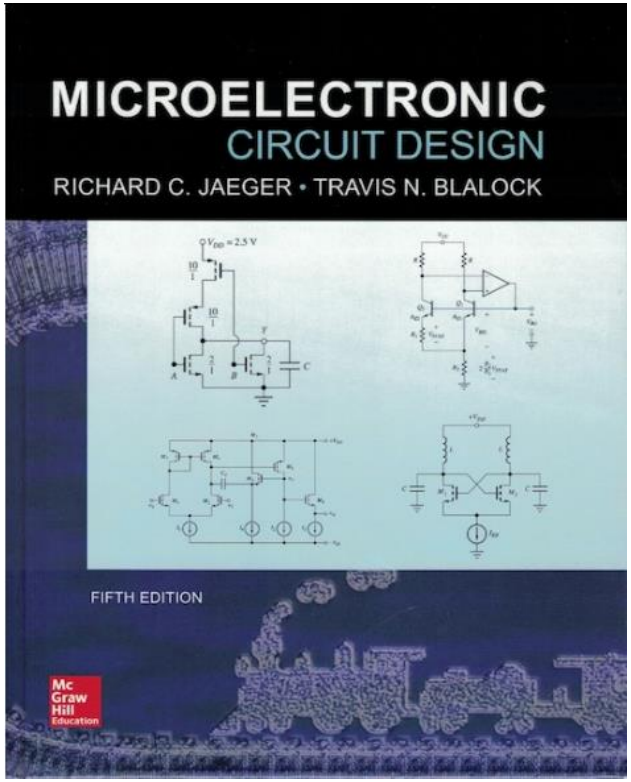
Instructor Short Biography

- **台湾交通大学** (1998 – 2002)
  电子工程学系 B.S.
- **台湾交通大学** (2002 – 2004)
  电子工程学系 M.S.
- **University of Washington, Seattle** (2006 – 2011)
  Electrical Engineering, Ph.D.

- **UW MSE Postdoc** (2011 – 2012)
- **LumiSands, Inc. Co-Founder / CEO** (2013 – 2017)
- **NCTU Applied Chemistry Postdoc** (2014 – 2017)
- **UM-SJTU JI Assistant Professor** (2017 –)

Textbook I

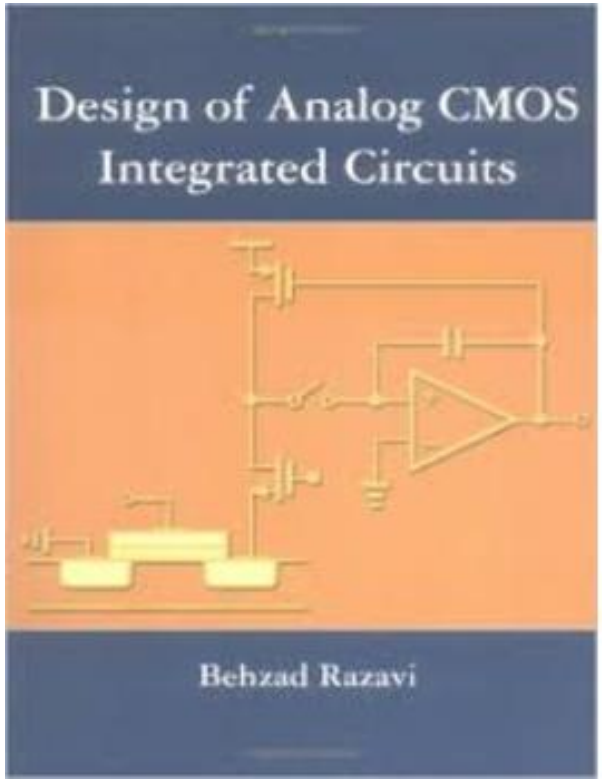


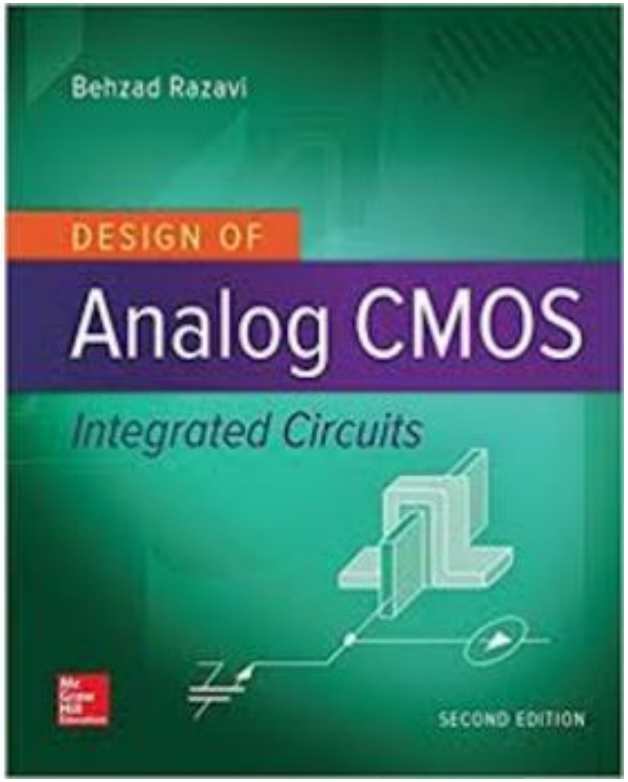


Richard C. Jaeger
Distinguished University Professor Emeritus
ECE Department
Auburn University

Travis N. Blalock
Visiting Associate Professor
ECE Department
University of Virginia

Textbook II





Behzad Razavi
ECE Department
UCLA

Syllabus

Midterm Exam

- **Diode**
- **Diode Circuit**
- **BJT**
- **BJT Circuit**
- **MOSFET**
- **MOSFET Single Stage Amplifiers**
- **MOSFET Differential Amplifiers**
- **MOSFET Current Mirrors**
- **Feedback Circuits**

Final Exam

Grading

- **8 × Assignments (with Pspice) (16%)**
- **4 × Quizzes (4%)**
- **1 × Midterm Exam (30%)**
- **1 × Final Exam (38%)**
- **4 × Lab Reports (12%)**

Schedule

	May				Jun				Jul					Aug				Sep
Mon	6	13	20	27	3	10	17	24	1	8	15	22	29	5	12	19	26	2
Tue	7	14	21	28	4	11	18	25	2	9	16	23	30	6	13	20	27	3
Wed	8	15	22	29	5	12	19	26	3	10	17	24	31	7	14	21	28	4
Thu	9	16	23	30	6	13	20	27	4	11	18	25	1	8	15	22	29	5
Fri	10	17	24	31	7	14	21	28	5	12	19	26	2	9	16	23	30	6
	11	18	25	1	8	15	22	29	6	13	20	27	3	10	17	24	31	7
	12	19	26	2	9	16	23	30	7	14	21	28	4	11	18	25	1	8
		1	2	3	4	5	6	7	8	9	10	11	12	13				
	Spr. Break	**Summer Semester**												**Summer Break**				

Lecturing:
Tue 10:00 to 11:40
Thu 10:00 to 11:40
Fri 16:00 to 17:40
East Lower Hall 205

Lab Sessions:
JI Circuits/Electronics Lab (3F)
TBD

Midterm/Final Exam

Instructor Office Hours:
JI Building Room 508
Wed 10:00 to 12:00

TA Office Hours:
JI Building YLM Center
Mon 19:00 to 21:00
Thu 19:00 to 21:00

Contact Info

- Instructor:

  Chang-Ching Tu
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- Teaching Assistants:

  JIANG Yicheng

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  WANG Yiqin
  Email: wangyiqin@sjtu.edu.cn
  CHEN Ziyang
  Email: czyang@sjtu.edu.cn

Labs

Lab 1

Diode Circuit (Rectifier)

Lab 2

BJT Circuit (Single-stage amplifier)

Lab 3

MOSFET Circuit (Single-stage amplifier, Differential pair)

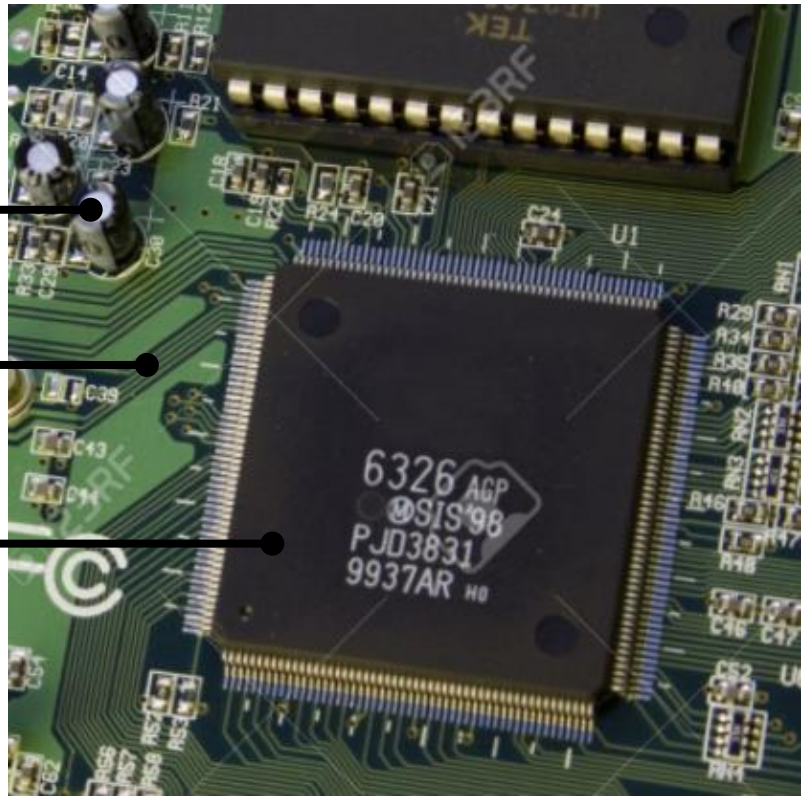
Lab 4

OP Amp Circuit + Feedback

IT Hardware Industry Ecosystem

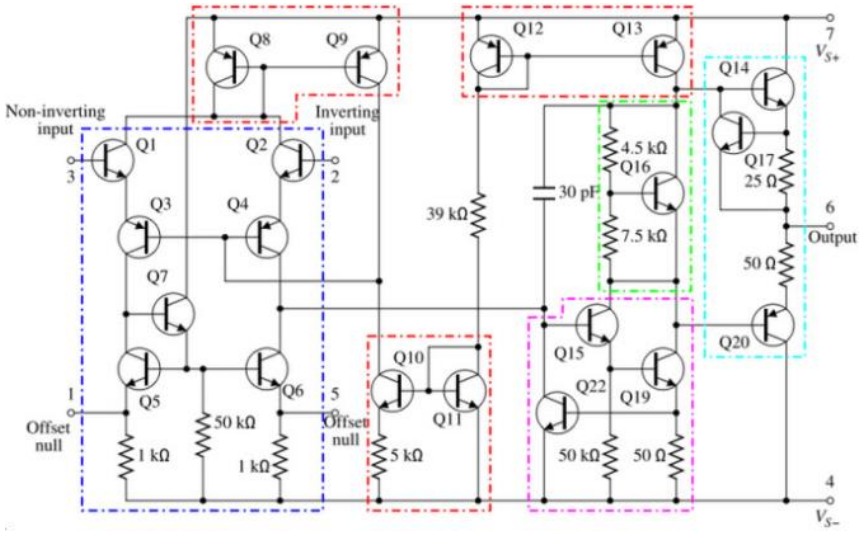
Apple
HP
Sony
Huawei
Samsung

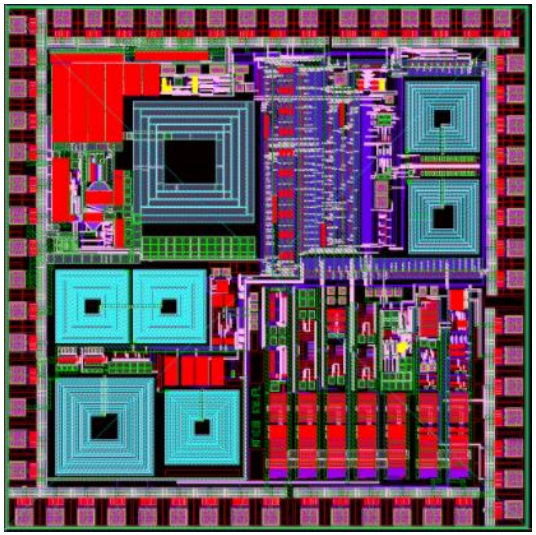
Apple
Microsoft
Google
Amazon
腾讯
百度
阿里巴巴



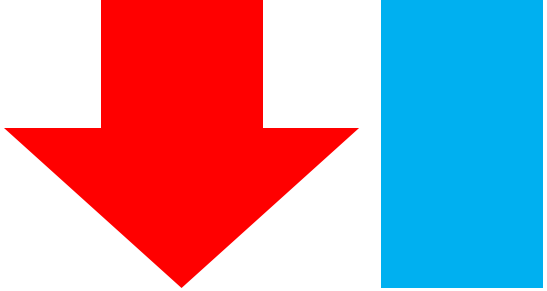
Foxconn
Huawei
Samsung

Qualcomm
Broadcom
MediaTek
NVIDIA
Marvell
Apple
Intel
Huawei (海思)
Samsung

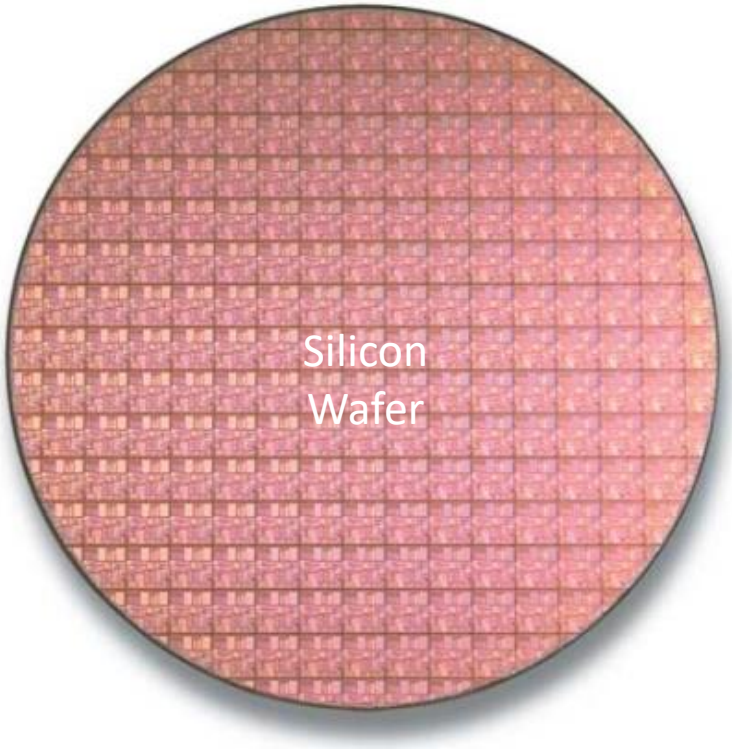


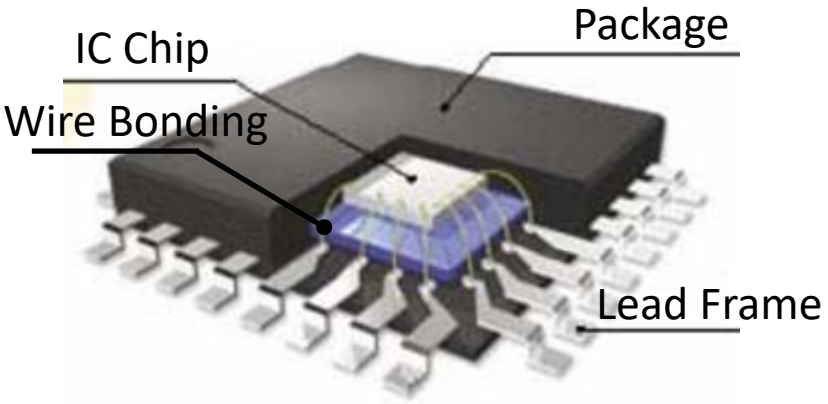


[VE215](): Introduction to Circuits
[VE311](): Electronic Circuits
[VE312](): Digital Integrated Circuits
[VE413](): Monolithic Amplifier Circuits



TSMC
Intel
GlobalFoundries
Samsung
中芯半导体





ZTE Event in May 2018

One of the World's Biggest Phone Firms Is Stopping Operations Because of a Ban on Buying U.S. Parts

- *Fortune*, May 10th, 2018

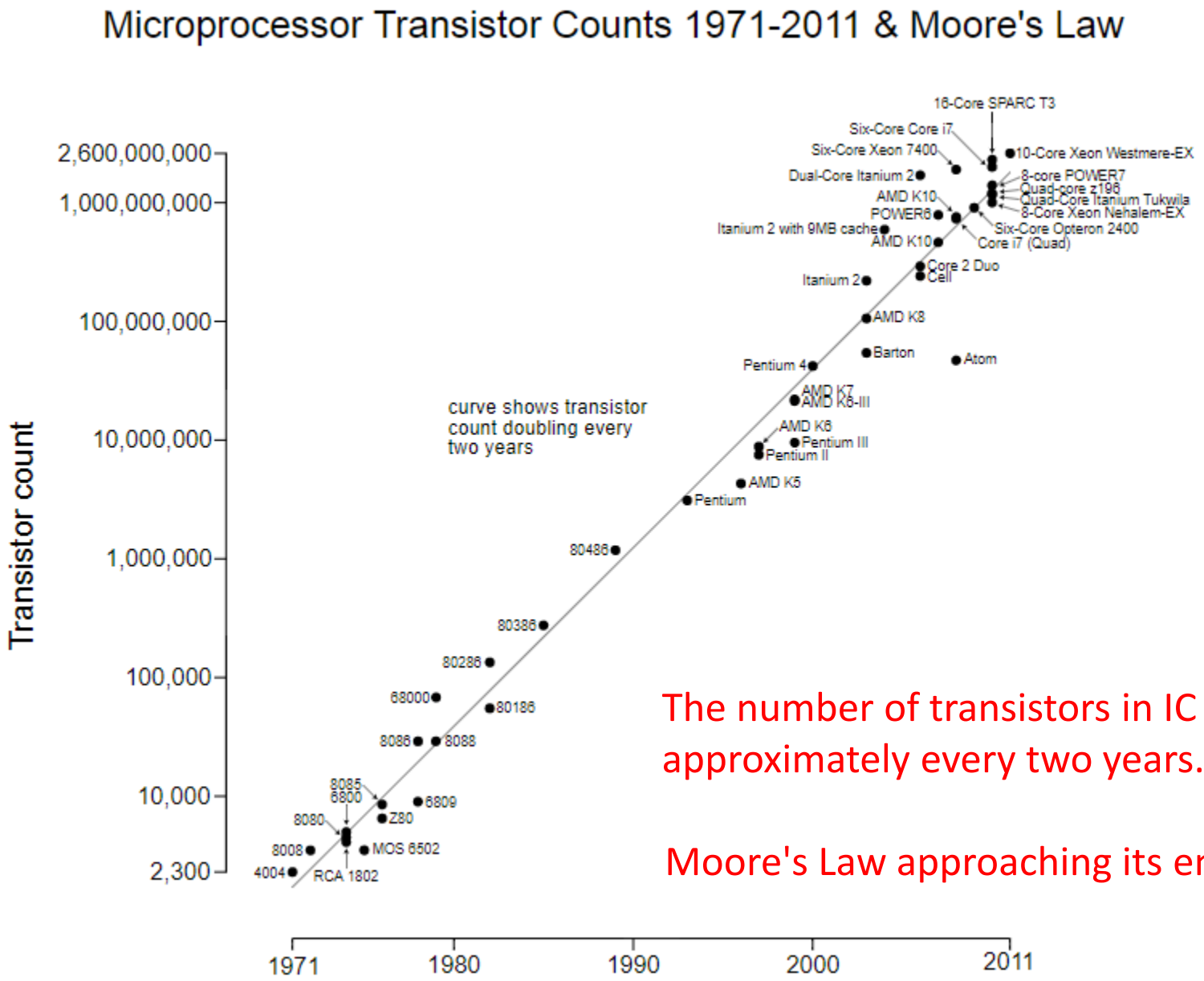
China's ZTE may be first major casualty of trade war with US

- *The Guardian*, May 10th, 2018

China's ZTE says main operations have ceased after US ban

- *CNN*, May 9th, 2018

Moore's Law



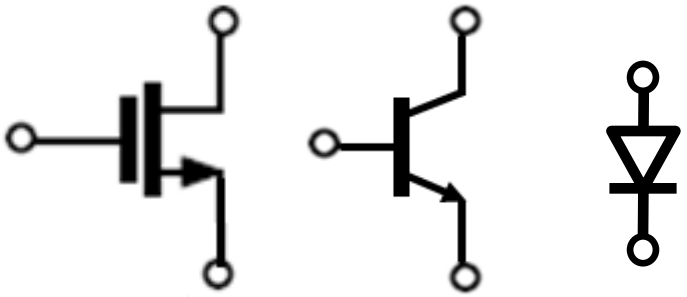
The number of transistors in IC doubles approximately every two years.

Moore's Law approaching its end now?

Active vs Passive Components

Active Components

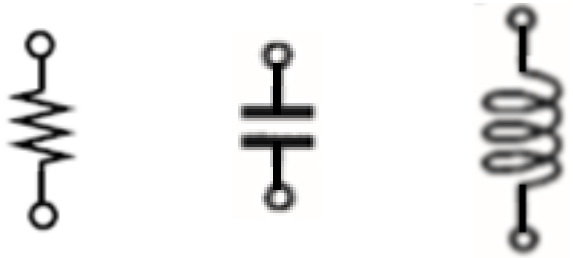
MOSFET BJT Diode



VE 311

Passive Components

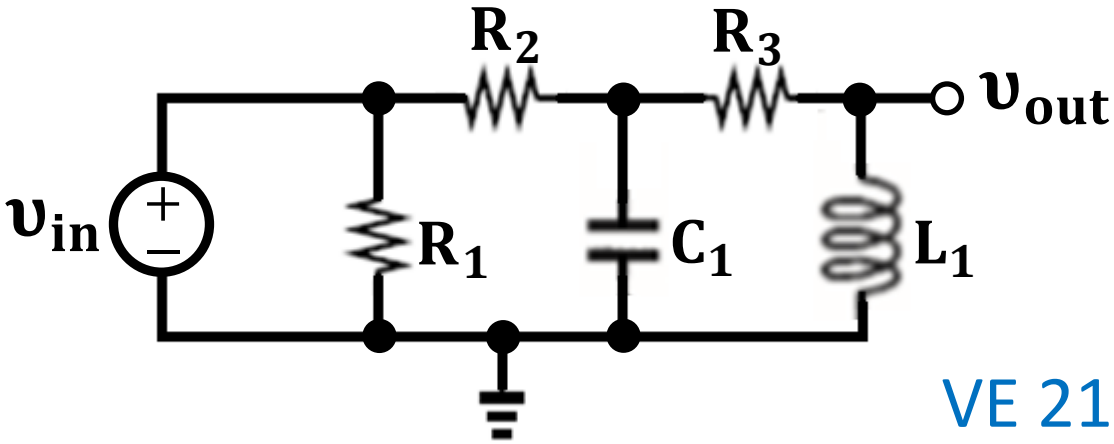
Resistor Capacitor Inductor



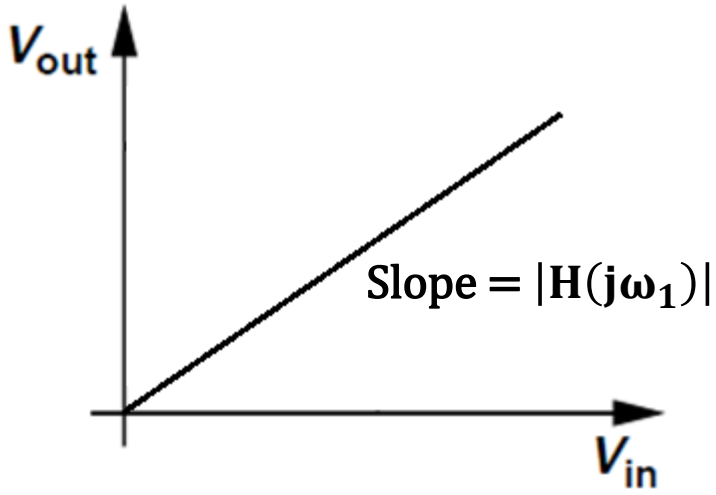
VE 215

Linear vs Nonlinear Circuit

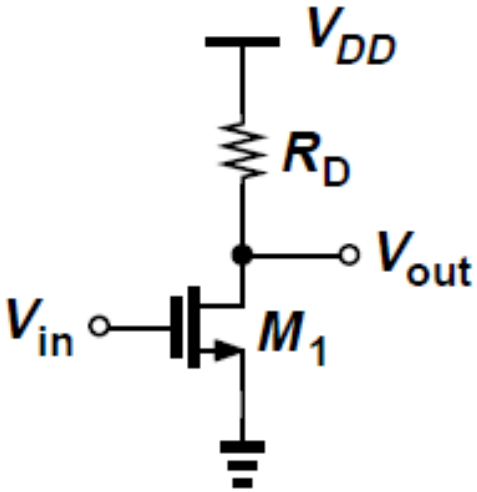
Linear Circuit



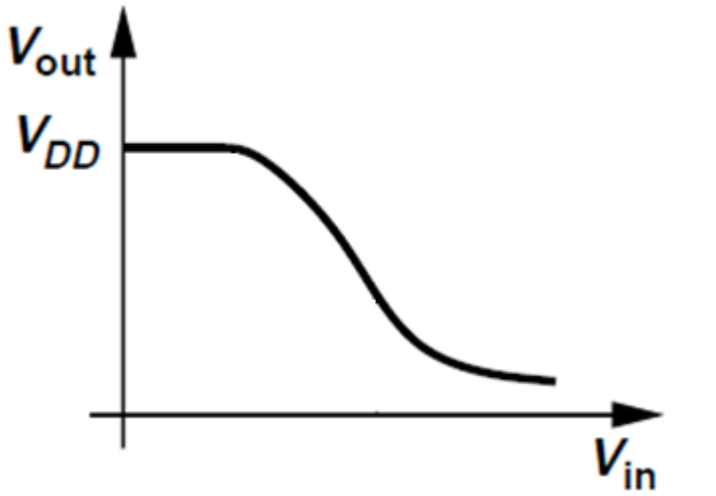
VE 215



Nonlinear Circuit

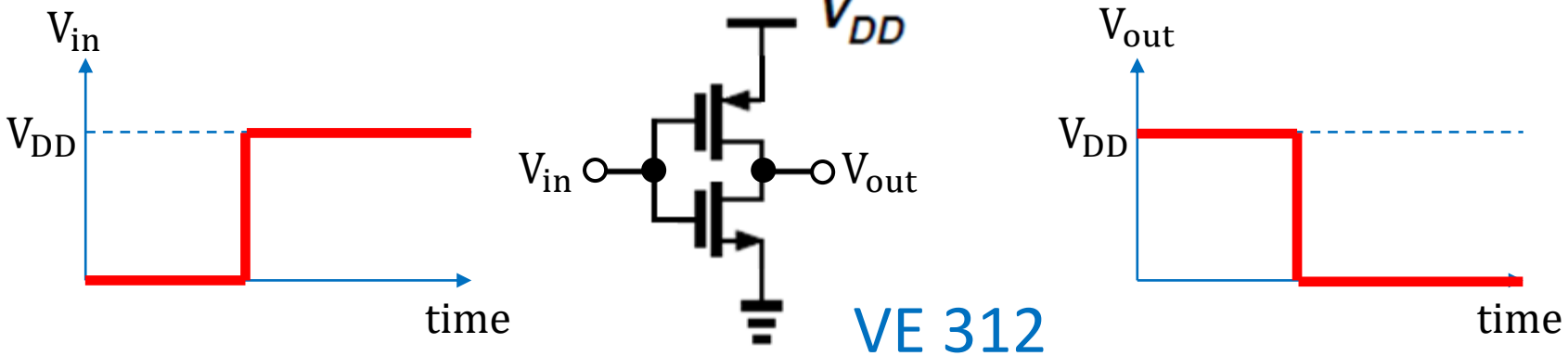


VE 311



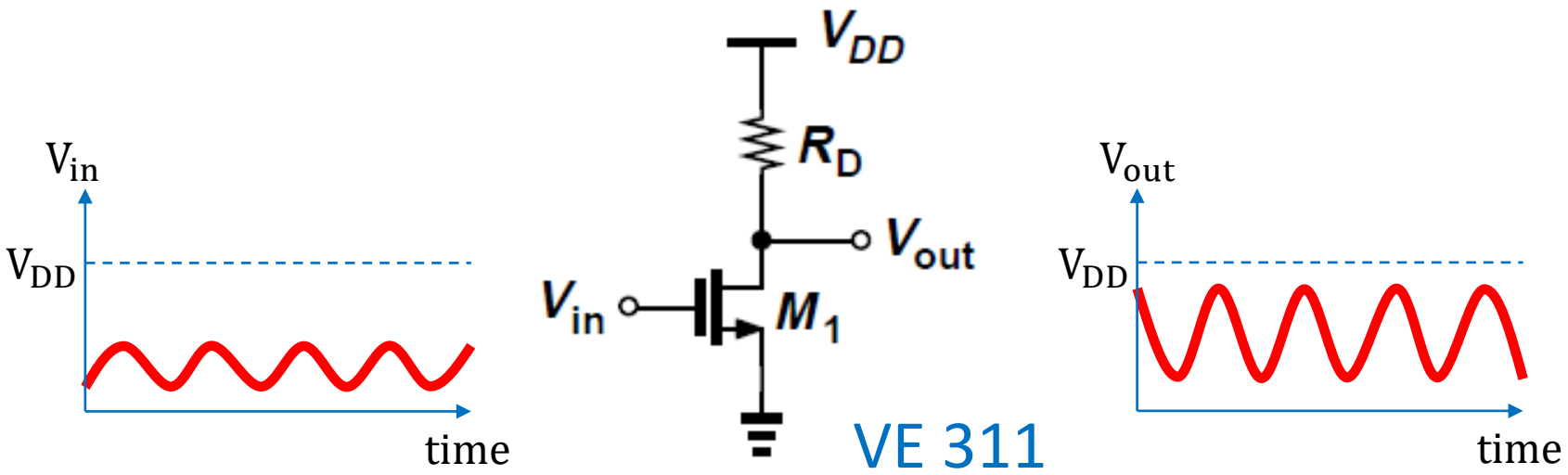
Analog vs Digital

Digital



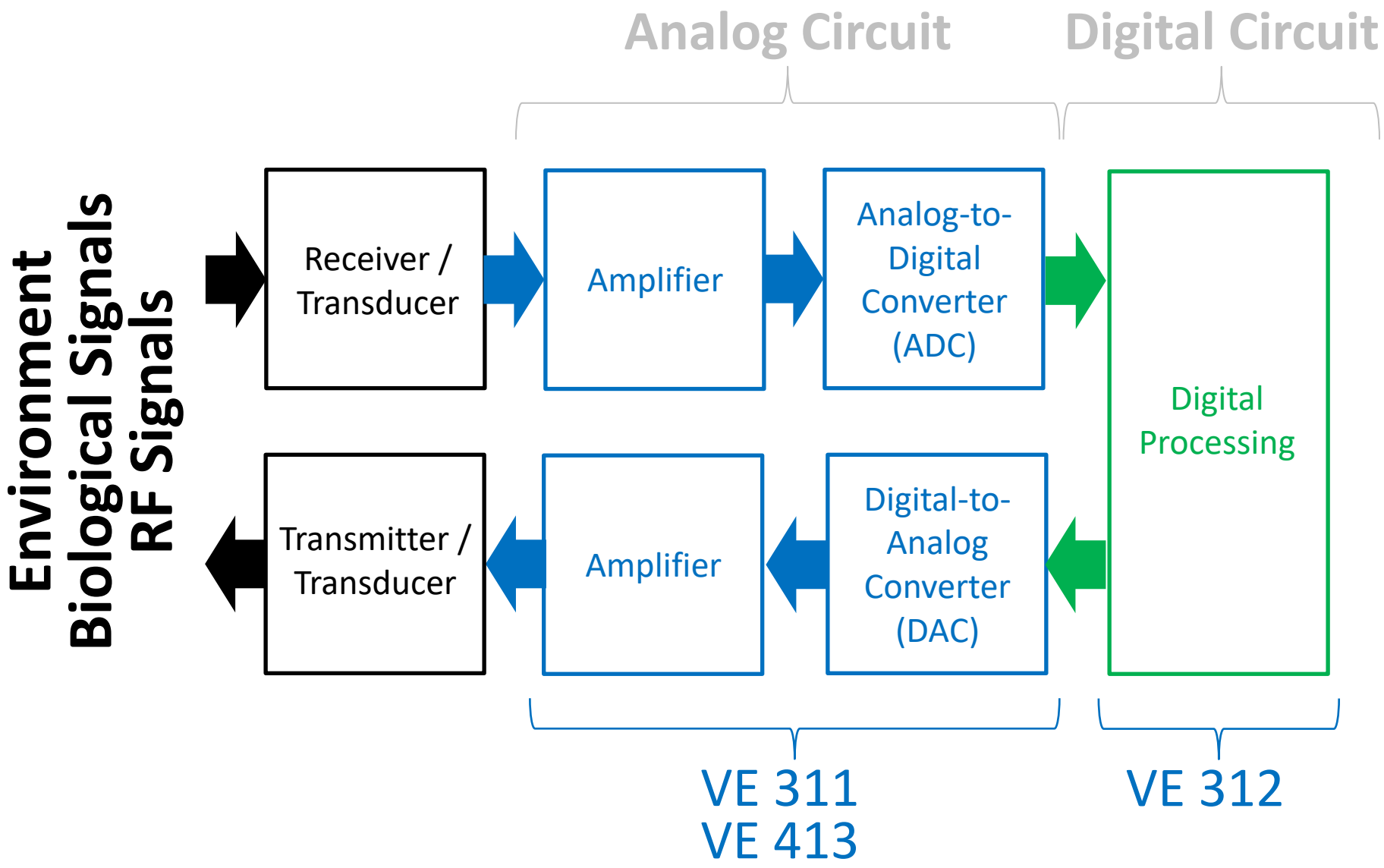
VE 312

Analog



VE 311

Analog Circuit in IC



IC Design Process

Hand calculations on paper, based on proper approximations.

Pre-simulation: Schematic design and simulation on Spice.

VE 311

Post-simulation: Layout drawing, simulation and design rule check on Cadence.

Tapeout: Layout design sent to IC manufacturers.

- Experience is the most important factor here.
- Design challenges include **transistor imperfections**, **declining supply voltages**, **power consumption**, **circuit complexity**, and **PVT (process-voltage-temperature) variations**.