HW5 Report

Q1.

Verilog Code:

```
23  module HW6(clk,S,L,SI,D,Q);
24  input clk,S,L,SI;
25  input [3:0]D;
26  output [3:0]Q;
27  reg [3:0]Q;
28  always @(posedge ~clk)begin
29      if(S) begin
30          Q[2:0]<=Q[3:1];
31          Q[3]<=SI;
32      end
33      else if (L)Q<=D;
34      /*if(!S&&L) Q<=D;
35      else if (S)begin
36          Q[2:0]<=Q[3:1];
37          Q[3]<=SI;
38          end
39      */
40      else Q<=Q;
41      end
42  endmodule
```

Stimulation Result: