VE370 HW4

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1. no

2. no

3. Without improvement

400+100+30+120+200+350+100 = 1300 ps

With improvement

1300+300 = 1600 ps

4. J format and I format

5. 200+20+90+90 = 400 ps

6. 200+20+90+250+15 = 575 ps

7. sw needs shorter time than lw

For Beq, 200+20+90+90+10 = 410 ps

So clock cycle time should at least be 575 ps.

12 add a bne/beq mux and connect with zero from ALU through an or gate, then connect it to branch

13 The control will go through jump as well as write data, and add a mux to connect PC+4 with the write register

14 add a mux before PC and connect it with register

. We can use a bunch of instructions which will call all blocks.

```
Start: add $s1, $0, $0
       sw $s0, 0($s1)
       addi $s0, $0, 1
       lw $s0, 0($s1)
       beq $s0, 0, start
       addi $s0, $0, 1
        j start
```

Yes, above test can do all because they use every block and none of them can be stuck at 0 or 1

. It is a sw instruction so signextend is 1 and shift left 2 is 0

1. 0010