VE370 HW6 Pan Chongdan

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1. LW R2, 0(R1) ①
   AND R1, R2, R1 ②
   LW 23, 0(R2) ③
   LW R1, 0(R1) ④
   SW R1, 0(R1) ⑤

Signal: ① MEM Hazard for ②
① MEM Hazard for ③
④ MEM Hazard for ⑤

2. Need IF/ID rs, rt, rd, ID/EX Rt, ID/EX MemRead, EX/MEM RegWrite
MEM/WB RegWrite
We need to stall the cycle due to no forwarding

3. For BEQ R2, R0, Label, there'll be branch hazard because the value in R2 hasn't been updated. For SW R2, 0(R5) there'll be Data Hazard because R2 hasn't been updated from last OR instruction

4. If it's in MEM stage:

LW	IF	ID	EX	MEM	WB						
BEQ		IF	ID	EX	MEM	WB					
OR						IF	ID	EX	MEM	WB	
SW							IF	ID	EX	MEM	WB

It needs 11 cycles totally

If it's in ID stage, it needs 9 cycles totally

$1 - \frac{9}{11} \times 100\% = 18\%$

5. $2 \times 0.25 \times 0.55 = 0.275$

6. Both 50%

7. 0

8. ID.Flush=0 EX.Flush=1 through flushing

9. If previous instruction needs to handle an expection, the stored data can be used to restart

10. Both of these instructions will be flushed and it will excute SLT R5, R15, R4