Ve270 Introduction to Logic Design

Homework 7

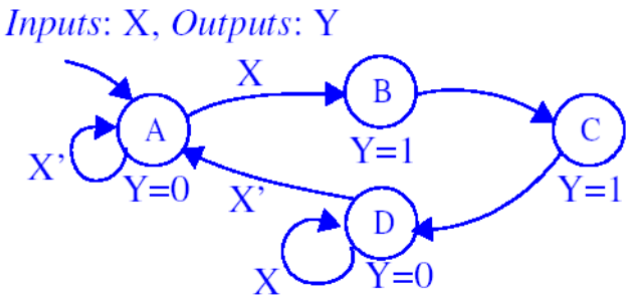
Assigned: July 5, 2018

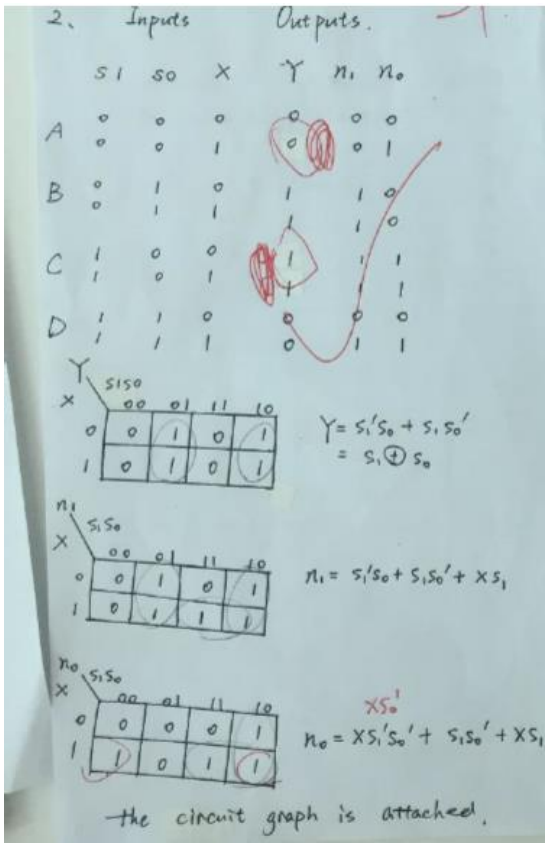
Due: July 12, 2018, 2:00pm.

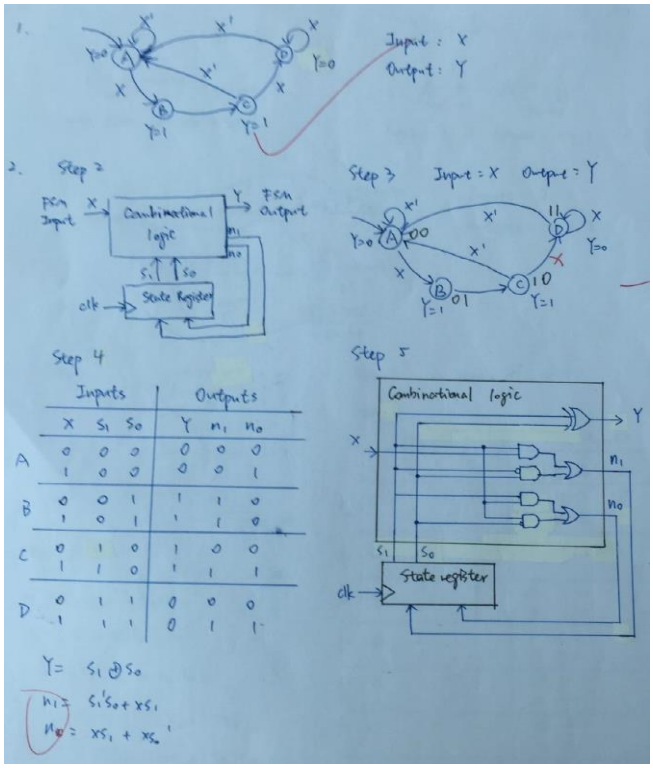
The homework should be submitted in hard copies.

1. Problem 3.24. (10 points)
2. Implement a circuit for the FSM designed in Problem 3.24. (15 points)

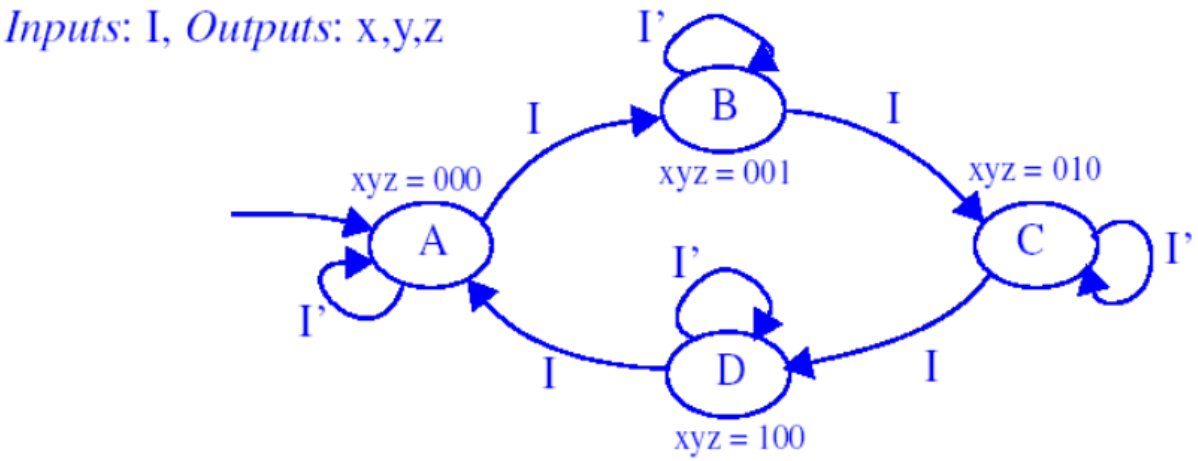
Two ways to solve the problem:



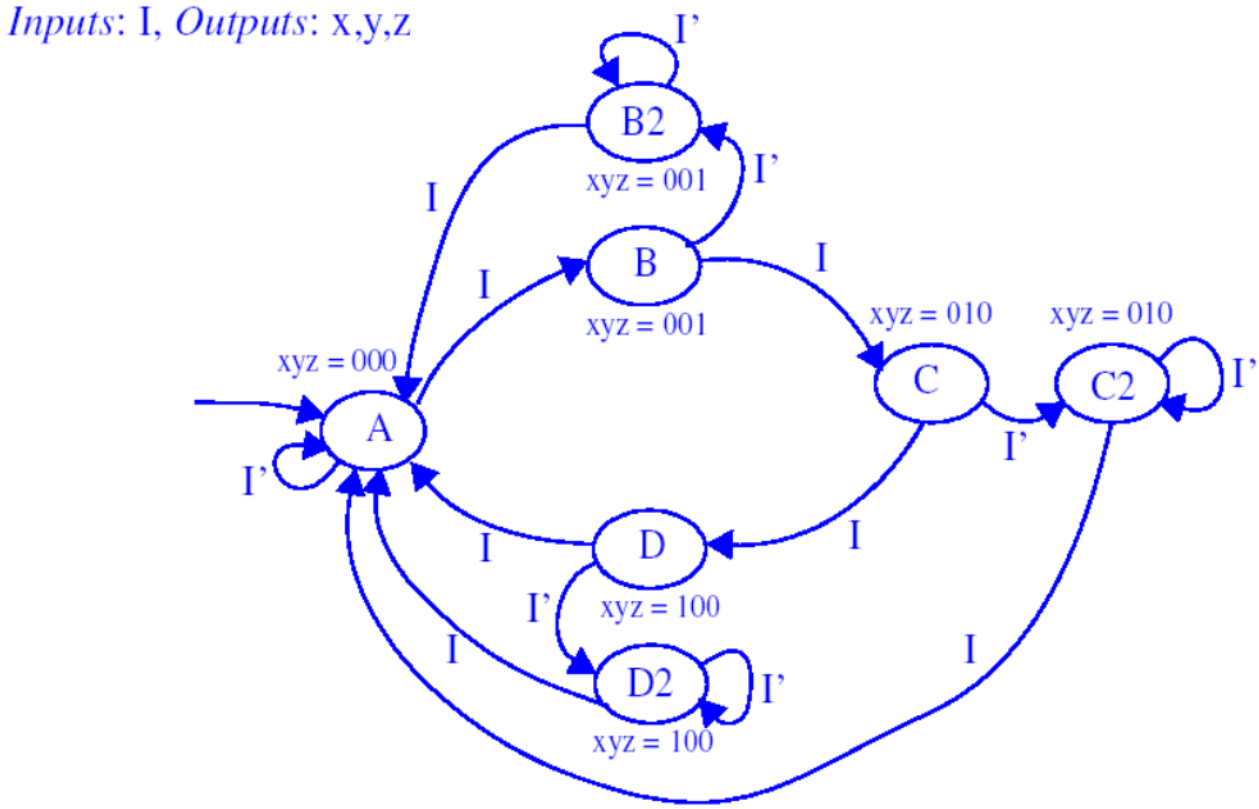




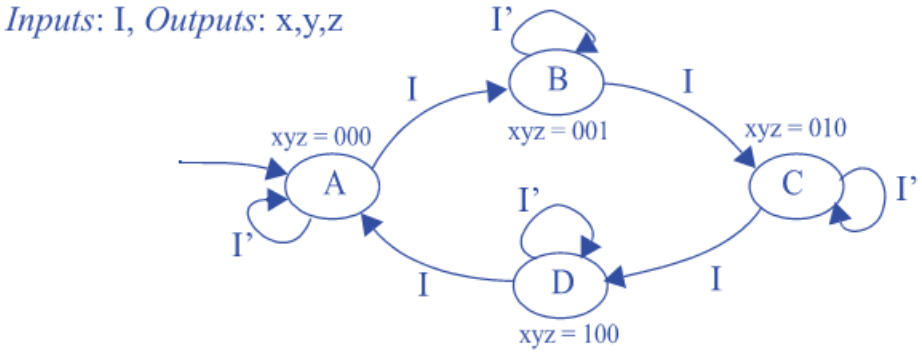
3. Problem 3.25 (10 points)



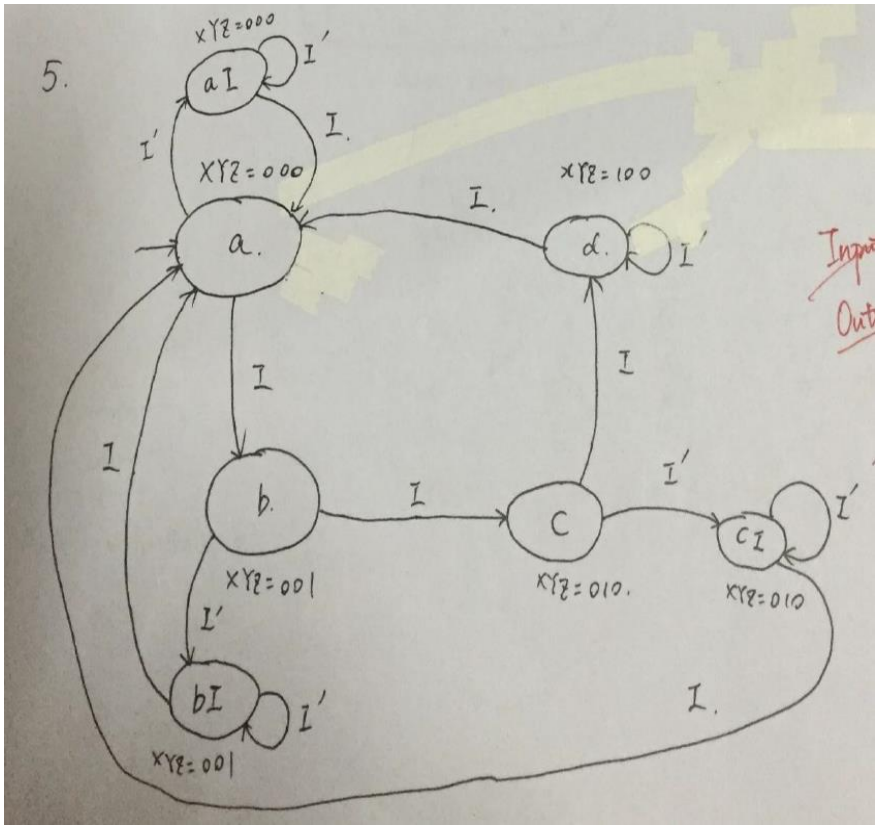
4. Problem 3.26. (10 Points)



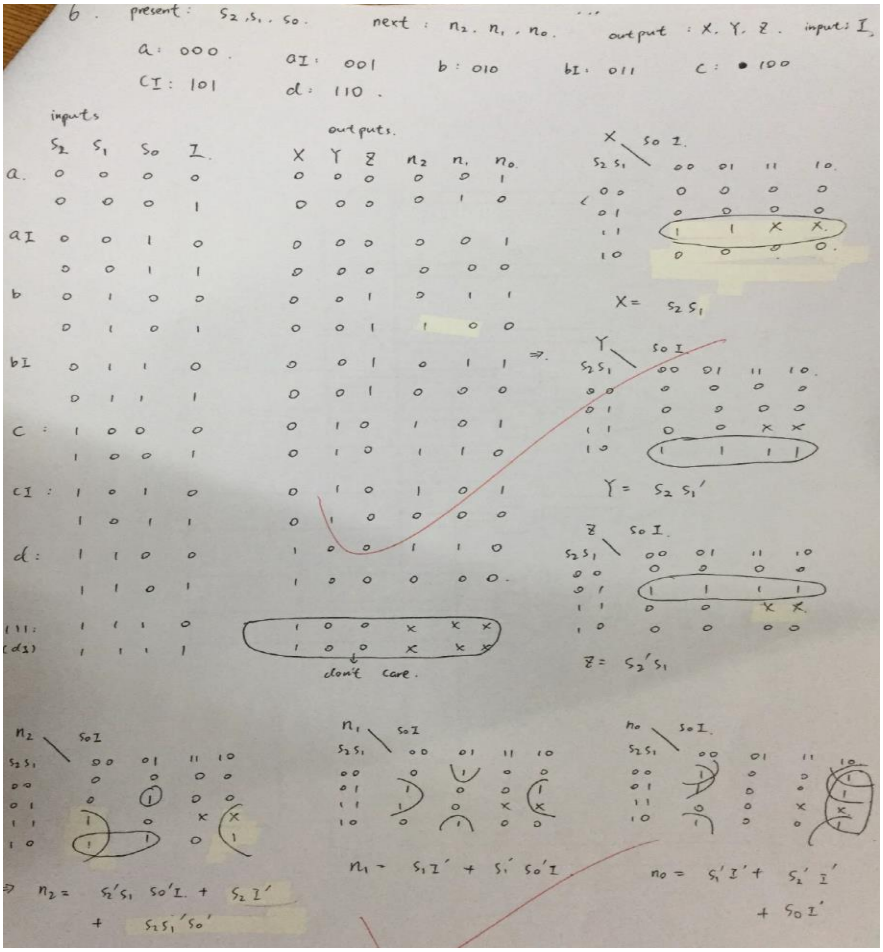
Or

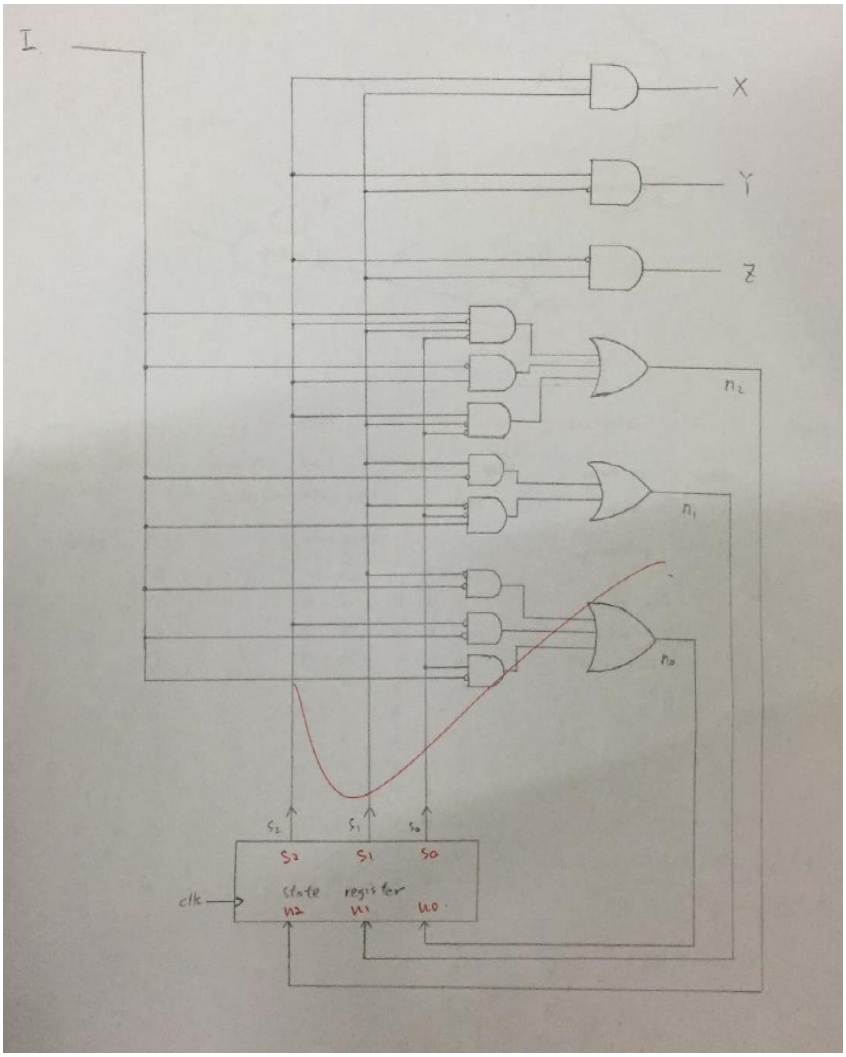


5. Problem 3.27. (10 Points)



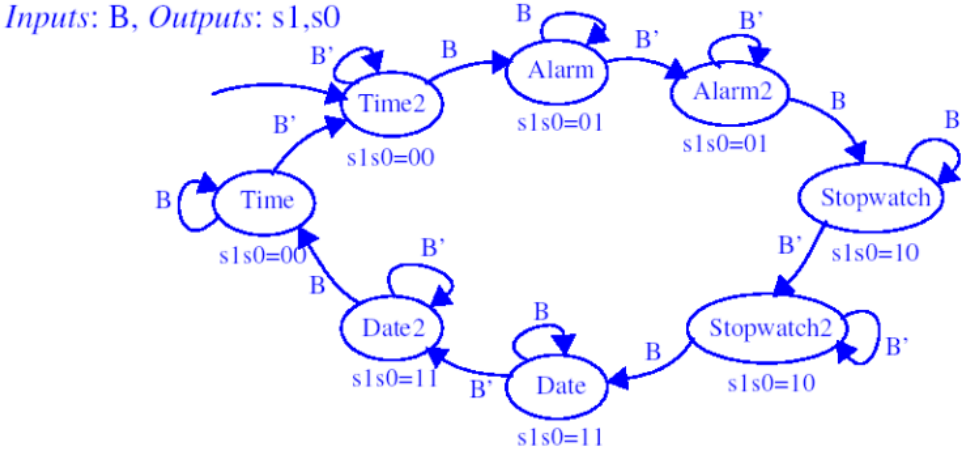
6. Implement a circuit for the FSM designed in Problem 3.27. (15 points)


b. present: S_2, S_1, S_0. next: n_2, n_1, n_0. output: X, Y, Z. input: I.
a: 000
aI: 001
b: 010
bI: 011
c: 100
cI: 101
d: 110.
inputs
outputs.
don't care.
$X = S_2 S_1$
$Y = S_2 S_1'$
$Z = S_2' S_1$
$n_2 = S_2' S_1 S_0' I + S_2 I' + S_2 S_1' S_0'$
$n_1 = S_1 I' + S_1' S_0' I$
$n_0 = S_1' I' + S_2' I' + S_0 I'$



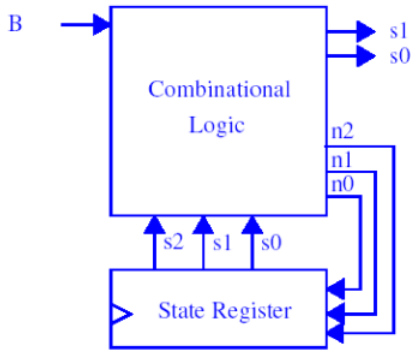
7. Problem 3.28, show design steps, equations, and draw schematics. (20 points)

Step 1 - Capture the FSM



The FSM was created during Exercise 3.27.

Step 2 - Create the architecture



Step 3 - Encode the states

A straightforward encoding is Time2=000, Alarm=001, Alarm2=010, Stop-watch=011, Stopwatch2=100, Date=101, Date2=110, Time=111.

Step 4 - Create the state table

Inputs				Outputs				
s2	s1	s0	B	n2	n1	n0	s1	s0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0	1
0	0	1	1	0	0	1	0	1
0	1	0	0	0	1	0	0	1
0	1	0	1	0	1	1	0	1
0	1	1	0	1	0	0	1	0
0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1	0
1	0	1	0	1	0	1	1	1
1	0	1	1	1	1	0	1	1
1	1	0	0	1	1	0	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0

Step 5 - Implement the combinational logic

n2 = s2's1s0B' + s2s1' + s2s0' + s2B

n1 = s1s0' + s1B + s2s0B + s2's1's0B'

n0 = s0'B + s2'B + s1B + s2s1's0B'

s1 = s2s0' + s2s1' + s2's1s0

s0 = s1 XOR s0

8. Problem 3.42 (10 points)