VE370 HW8

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1. Assume it's a 4 two-word-block cache

The memory access sequence: 0 16 0

Change it to 4-way set associative, it will reduce miss rate but diminish improvement

2. request type —write→ is it hit —Yes→ write data to cache

is it hit —Yes→ write data to memory → Done

3. Assume there are I instructions and Bandwidth is B, then the total cycles are $\frac{64}{B}$. The data cache penalty for reading is $13\times0.25\times0.02\times(1+\frac{64}{B})I$, similarly, for writing it's $13\times0.1\times0.02\times(1+\frac{64}{B})I$ and I penalty is $0.003\times(\frac{64}{B}+1)$

$$\therefore I+I\times[1.3\times0.02\times(0.25+0.1)+0.003]\times(\frac{64}{B}+1)\leq 2I$$

$$B\geq 0.784 \text{ (Bytes)}$$

4. $\frac{C1}{C2}=\frac{90}{66}=\frac{15}{11}$

5. For P1: Miss cycles $= IC\times0.36\times0.08\times\frac{70}{0.66}=3.05\,IC$

$CPI=4.05$

For P2: Similarly $CPI=1+0.36\times0.06\times\frac{70}{0.9}=2.68$

$\therefore$ P1 is faster

6. AMAT = 0.66 + 0.08 × (0.95 × 70 + 5.62) = 6.43 (s)

7. CPI = 1 + 0.36 × 0.08 × (5.62 + 0.95 × 70) ÷ 66 = 4.14

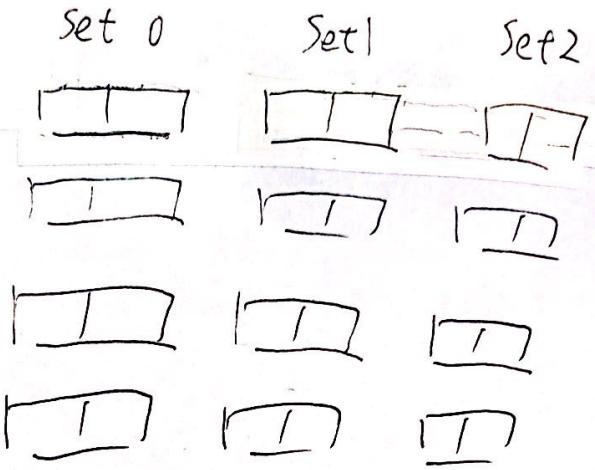
8. P2 is faster

$2.68 = 1 + 0.36 \times M \times (5.62 + 0.95 \times 70) \div 0.66$

$M = 4.3\%$

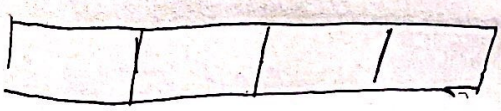
9.

Block Address Cache Index Hit/Miss



10.

11.



12. (1) CPI = 1.5 + 0.07 × 100 × 2 = 15.5

Doubled: CPI = 1.5 + 14 × 2 = 29.5 In half CPI = 15 + 14 ÷ 2 = 8.5

(2) CPI = 1.5 + 0.07 × 12 + 0.035 × 100 × 200 = 15 + 2.84 + 7 = 9.34

Doubled: 16.84 In half: 5.84

(3) CPI = 1.5 + 0.07 × 28 + 0.015 × 200 × 2 = 6.46

Doubled: 9.46 In half 4.96