JOINT INSTITUTE
交大密西根学院

Ve 270 Introduction to Logic Design

Lab 7
Design of a Digital Device

UM-SJTU Joint Institute
Shanghai Jiao Tong University
July 2018

1. Objective

To design a digital system that

- Rolls your SJTU student ID across the four SSDs on the FPGA board when the system starts, then
- Adds two 4-bit 2's complement numbers and displays the decimal results with the SSDs on the FPGA board.

2. Requirement

Part 1. Character Rolling

The first part of this lab is to roll the student ID of one of the lab partners through the four SSDs from left to right, or right to left, or back and forth. The rolling should start as soon as the device starts functioning or controlled by a switch. The rolling speed is up to the designers, but should be reasonable so people are comfortable to see each character. Other than the student ID, you may choose to display anything or any pattern you want. Be creative!

The student ID is required to roll through the SSDs for only once. But you may choose to roll it multiple times or any time activated by the control switch. As soon as the rolling is done or disabled by the control switch, the system should enter the normal operation mode – calculator.

Part 2. Simple Calculator

The calculator adds two 4-bit 2's complement numbers, and outputs one 4-bit 2's complement number which should be interpreted as a signed decimal number and displayed using one (for positive results) or two (for negative results) SSDs. The "–" sign must be displayed using one SSD for negative numbers. The calculator must also detect if there is any overflow in the results and indicate the overflowed results with an LED.

The two 4-bit operands of the calculator must be entered using the same four switches. Thus the operands have to be entered in turn, one after another. A push button must be used to function as the "enter" or "equal" key of the calculator. After the first number is formed using the four switches, the decimal equivalent should be displayed on the SSDs as soon as the "equal" button is pressed. After the second number is formed using the same four switches, the decimal result should be displayed on the SSDs as soon as the "equal" button is pressed. When the "equal" button is pushed multiple times, the calculator shall keep adding the second number to the results each time the button is pressed. The changing results should be updated on the SSDs accordingly. The following table simulates an example.

Four Switches	Equal Button	SSD	Overflow
1000	push	-8	0
0011	push	-5	0
No change	push	-2	0
No change	push	1	0
No change	push	4	0
No change	push	7	0
No change	push	-6	1
No change	push	-3	0

The above paragraphs describe the requirements for the device. Feel free to add more features and functions to the device.

NOTE: your design must be modeled with Verilog HDL.

3. Simulation, Synthesis, and FPGA Implementation

Simulate your circuit if necessary. It is a good idea to verify the functionality of all sub-circuits before you integrate them all together. Synthesize and implement your design on the Basys 3 FPGA board.

4. Deliverable

This is a 2-week lab. The full score for this lab is 300 points.

1) Demonstrate your circuits to the TAs before your lab session ends.
2) Upload source files on Canvas by **10pm, August 4, 2018**.
3) Upload peer evaluation report on Canvas by **10pm, August 4, 2018**.

Peer evaluation form:

Name	Percentage of contribution (sum to 100%)	Responsibilities
(yourself)		
(your lab partner)		