JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

Homework 10

Assigned: July 26, 2018

Due: August 2, 2018, 2:00pm.

The homework should be submitted in hard copies.

1. Problem 5.19 (30 points)

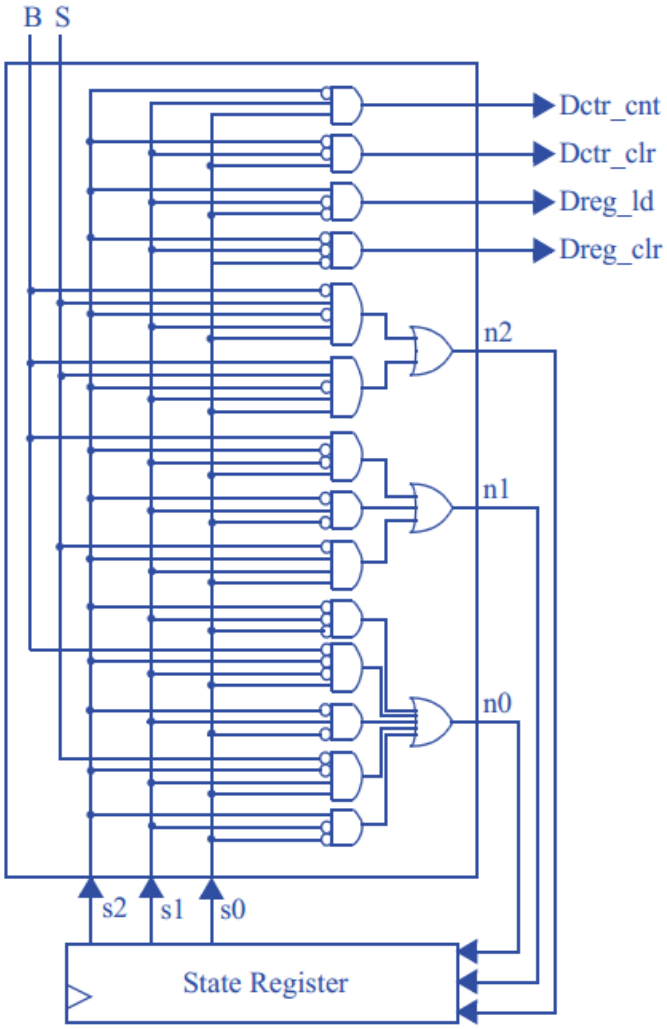
5.19 Using a timer, design a system with single-bit inputs U and D corresponding to two buttons, and a 16-bit output Q which is initially 0. Pressing the button for U causes Q to increment, while D causes a decrement; pressing both buttons causes Q to stay the same. If a single button is held down, Q should then continue to increment or decrement at a rate of once per second as long as the button is held. Assume the buttons are already debounced. Assume Q simply rolls over if its upper or lower value is reached.

2. Problem 5.26 (10+5+5 points)

(a)

Inputs					Outputs							
s2	s1	s0	B	S	n2	n1	n0	L	Dreg_clr	Dreg_ld	Dctr_clr	Dctr_cnt
0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	1	0	0	1	0	1	0	0	0
0	0	0	1	0	0	0	1	0	1	0	0	0
0	0	0	1	1	0	0	1	0	1	0	0	0
0	0	1	0	0	0	0	1	0	0	0	1	0
0	0	1	0	1	0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	0	0	0	0	1	0
0	0	1	1	1	0	1	0	0	0	0	1	0
0	1	0	0	0	0	1	1	1	0	0	0	0
0	1	0	0	1	0	1	1	1	0	0	0	0
0	1	0	1	0	0	1	1	1	0	0	0	0
0	1	0	1	1	0	1	1	1	0	0	0	0
0	1	1	0	0	0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	0	0	0	0	0	1
0	1	1	1	0	0	1	1	0	0	0	0	1
0	1	1	1	1	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	0	0	1	0	0
1	0	0	0	1	0	0	1	0	0	1	0	0
1	0	0	1	0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	0	1	0	0	1	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0

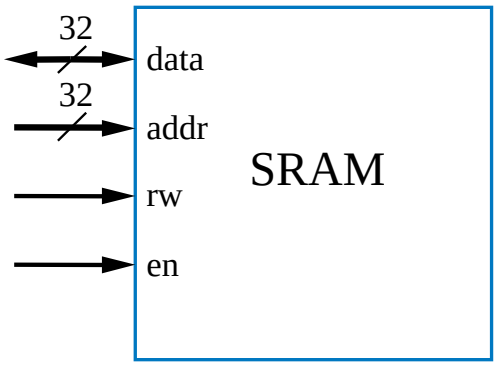
n2 = s1's1s0B'S + s2's1s0BS
n1 = s2's1's0B + s2's1s0' + s2's1s0S'
n0 = s2's1's0' + s2's1's0B' + s2's1s0' + s2's1s0S' + s2s1's0'
Dreg_clr = s2's1's0'
Dreg_ld = s2s1's0'
Dctr_clr = s2's1's0
Dctr_ctr = s2's1s0



(b) The controller features two levels of gates, resulting in a delay of 4ns. Therefore the critical path is within the up-counter, or 5ns.

(c) With a critical path of 5ns, the maximum clock frequency is 1,000,000,000/5 = 200MHz.

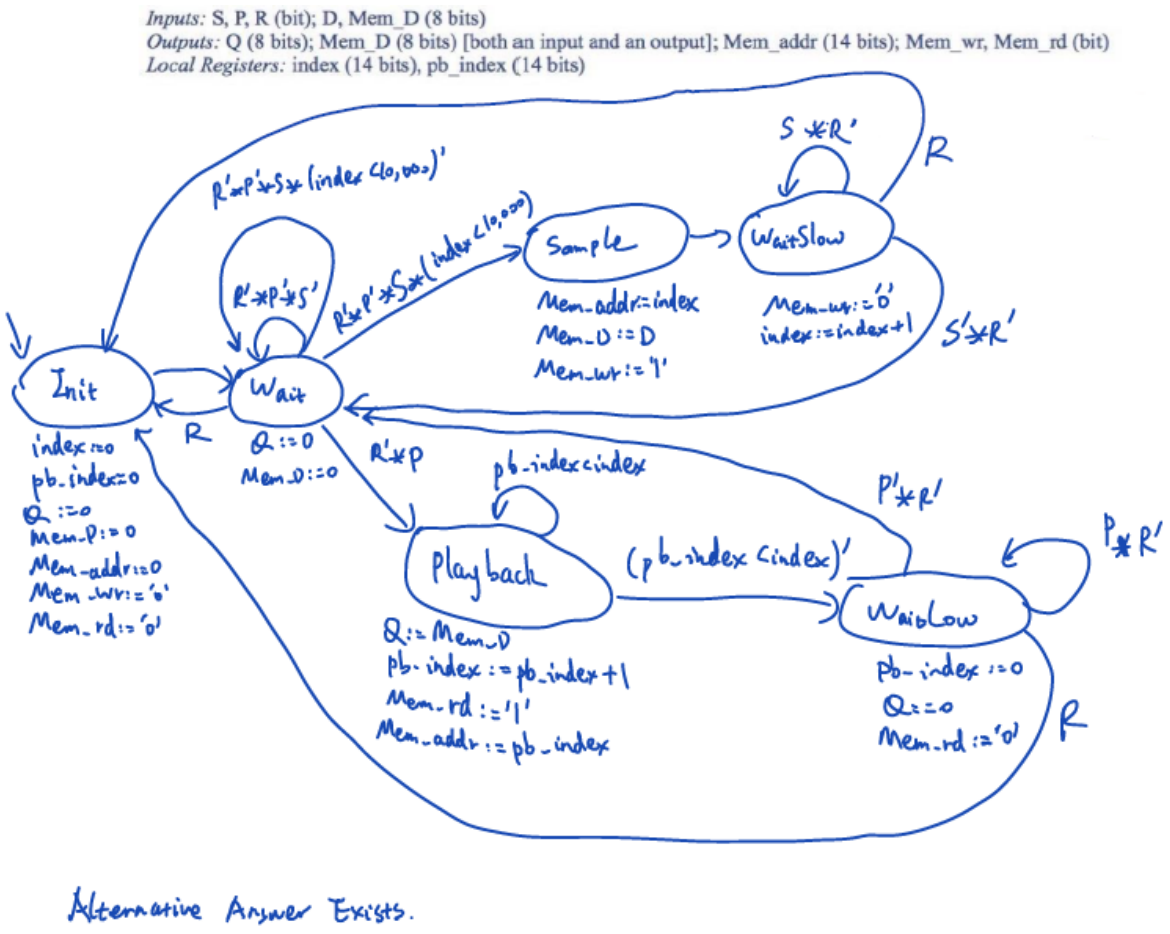
3. Given an SRAM block,



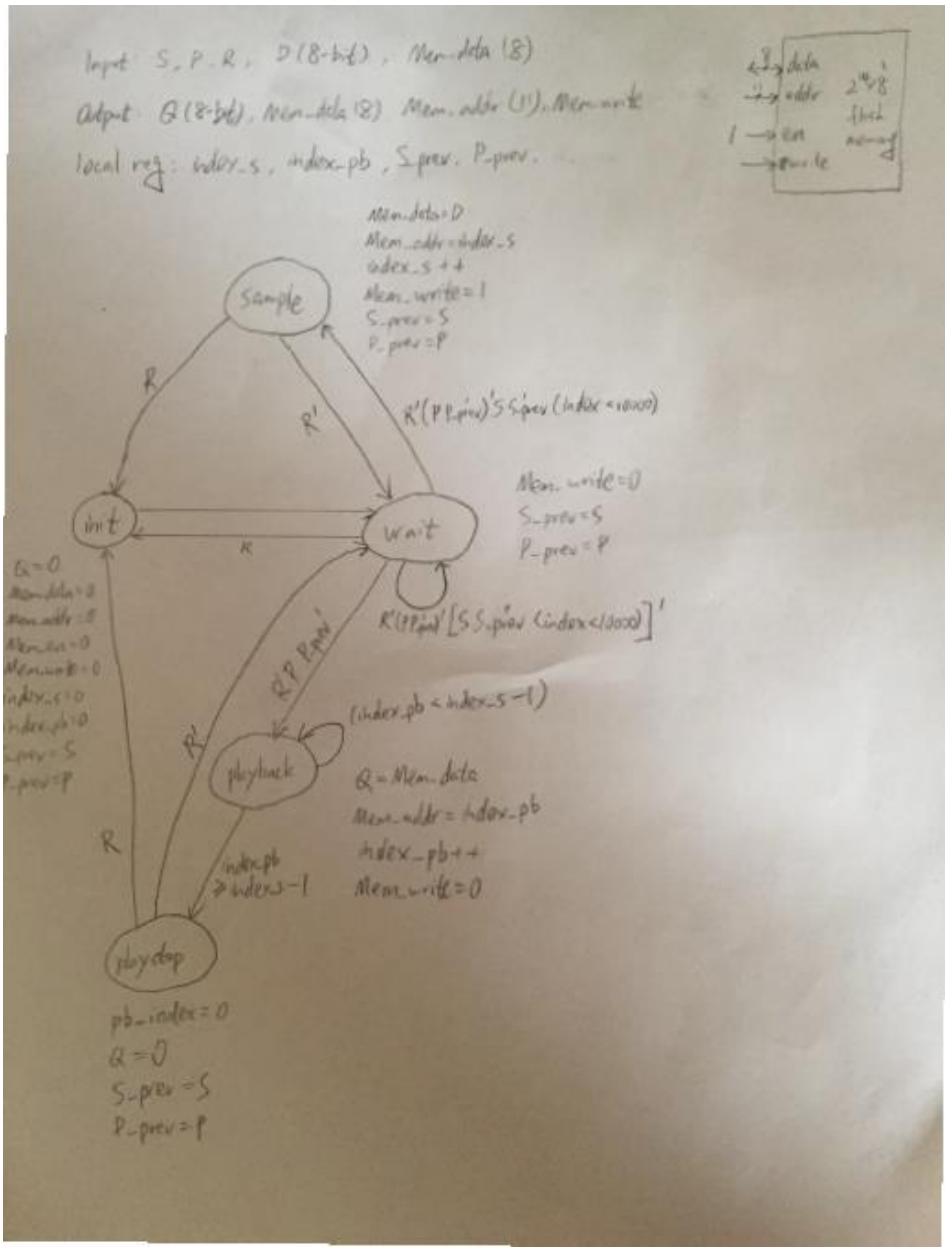
If the memory is byte addressable (each byte has an address), how many **bits** in maximum can the SRAM block have? (10 points)

$$2^{32} bytes * 8\text{bits/byte} = 2^{35} bits$$

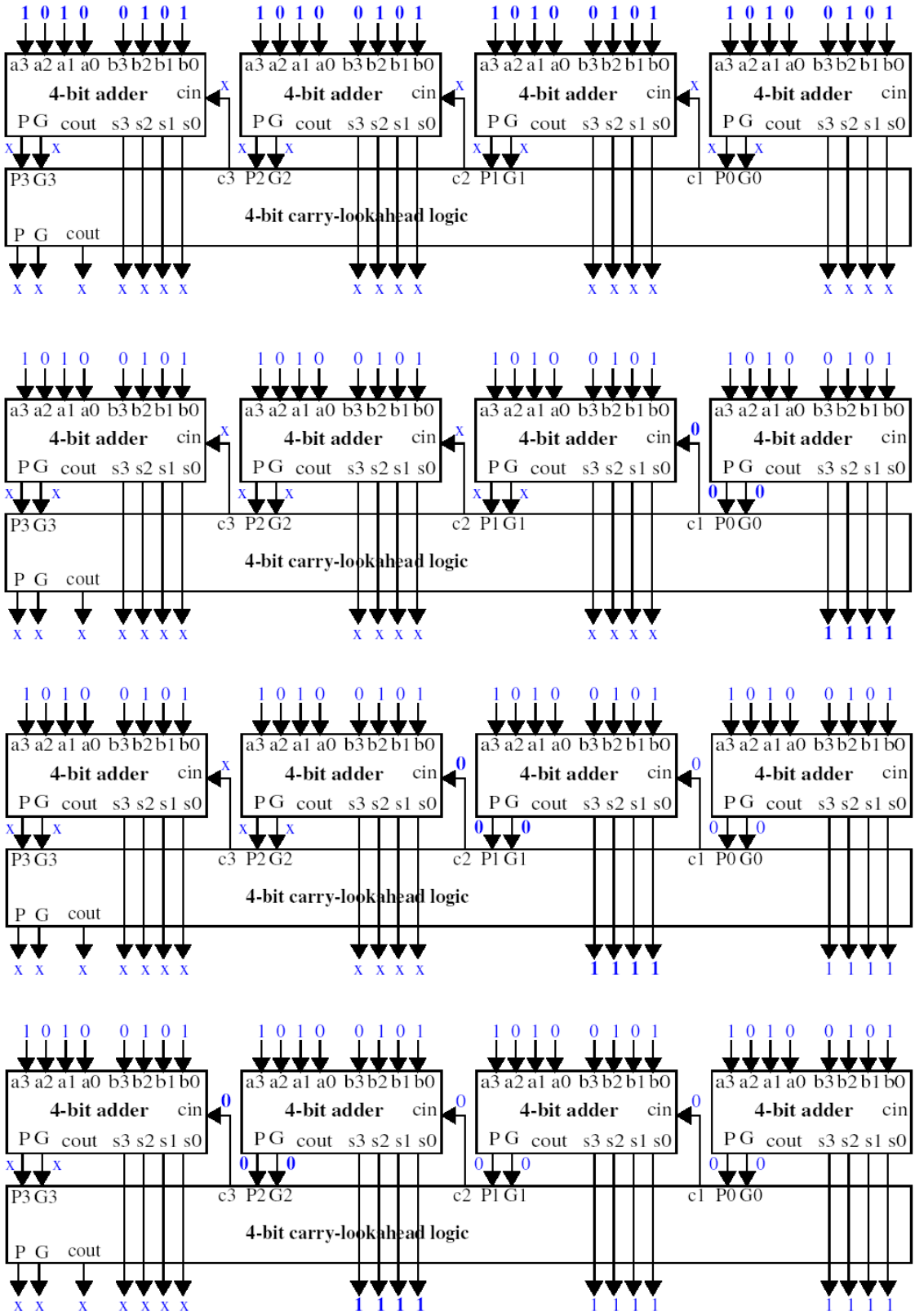
4. Problem 5.43 (30 points)

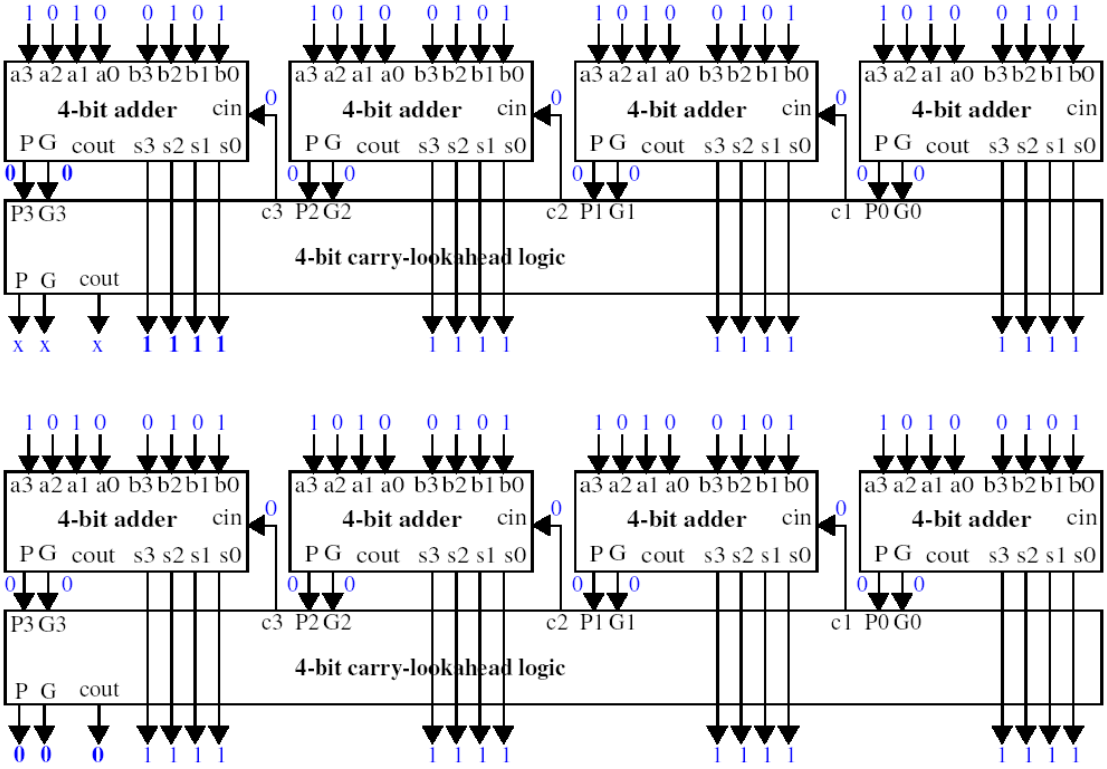


Alternative Answer Exists.



5. Problem 6.27 (10 points)


4-bit adder
4-bit carry-lookahead logic


4-bit adder
a3 a2 a1 a0 b3 b2 b1 b0
cin
P G cout s3 s2 s1 s0
4-bit carry-lookahead logic
P3 G3
c3 P2 G2
c2 P1 G1
c1 P0 G0
P G cout