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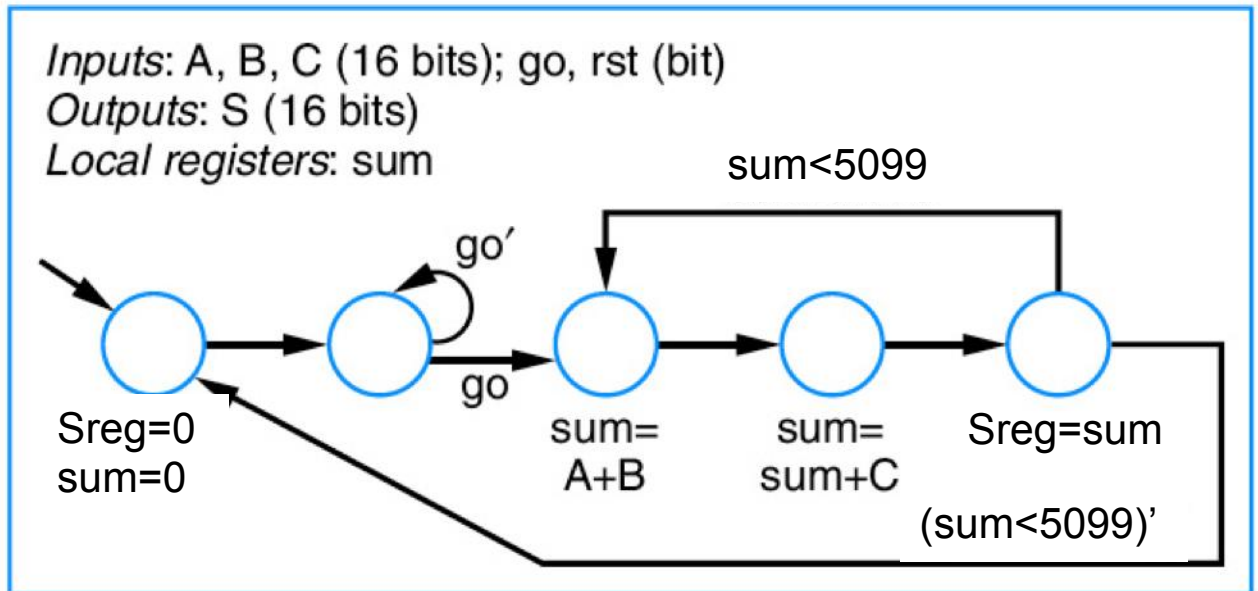


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Ve270 Introduction to Logic Design

Homework 9

1. Problem 5.7. (15 points)





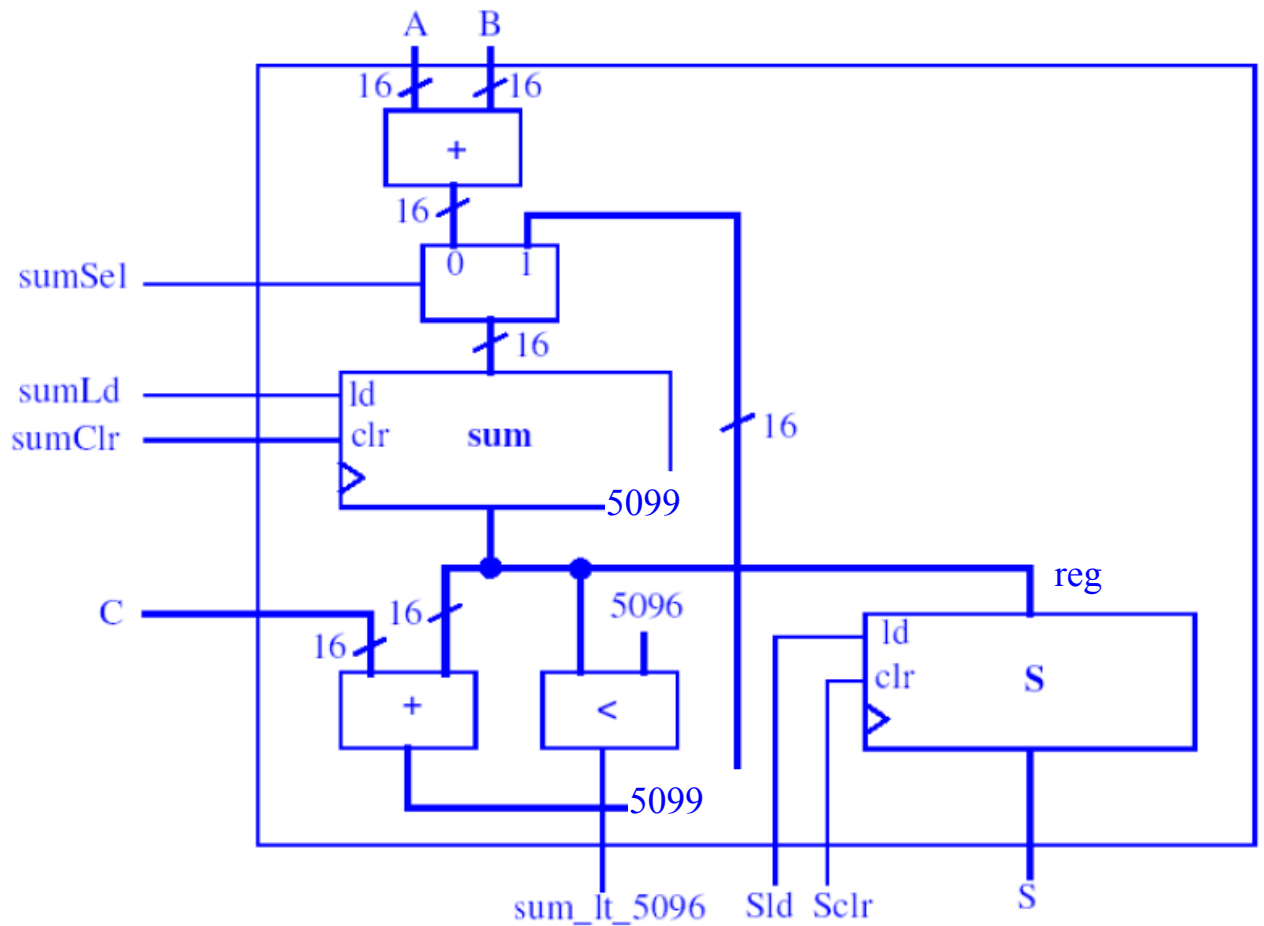
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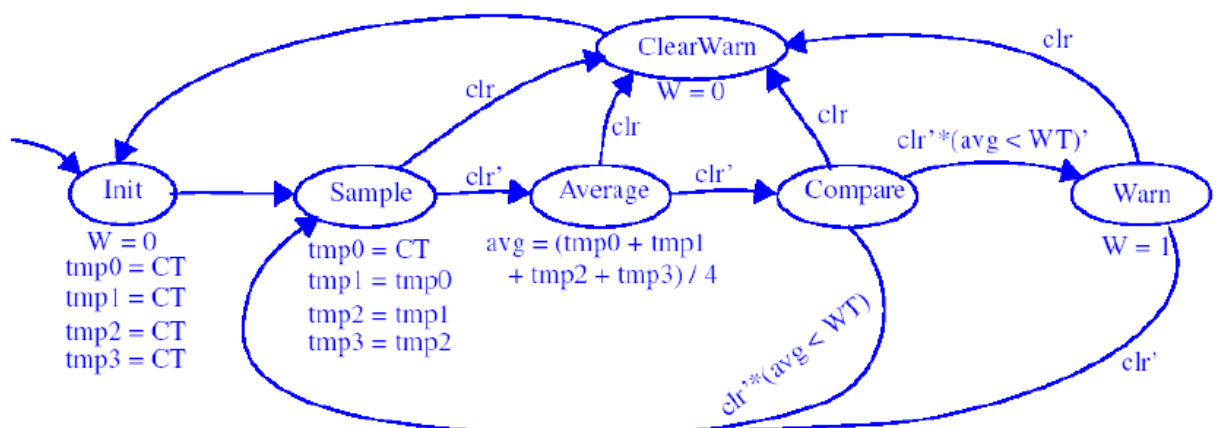
2. Problem 5.14. (15 points)

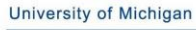
Step 1 - Capture a high-level state machine

Inputs: CT, WT (32 bits); clr (bit)

Outputs: W (bit)

Local Registers: tmp0, tmp1, tmp2, tmp3, avg (32 bits)





The diagram illustrates the proposed architecture for calculating the average of four inputs. It features four input registers (tmp3_ld, tmp2_ld, tmp1_ld, tmp0_ld) and a constant input CT. The inputs are processed through a series of adders and shifters to produce the final output avg_lt_WT. The architecture includes a feedback loop from the output back to the input, and a final comparison block.



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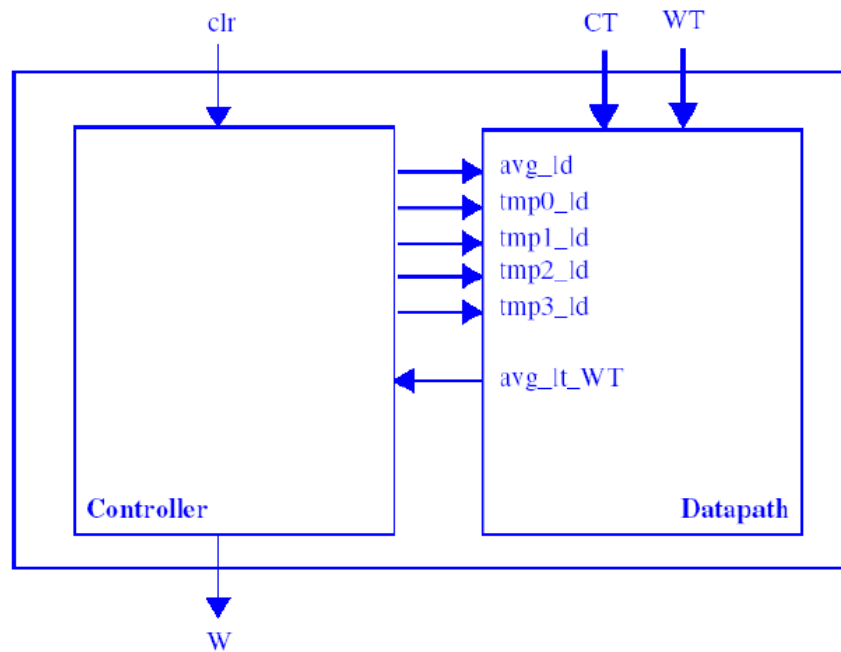
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Step 3 - Connect the datapath to a controller

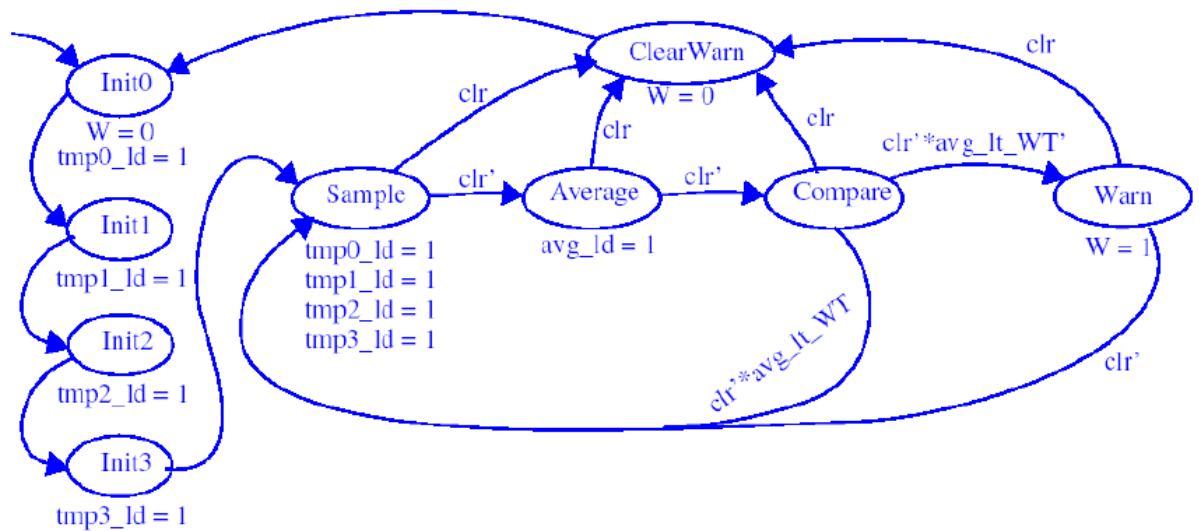


Step 4 - Derive the controller's FSM

Inputs: CT, WT (32 bits); clr (bit)

Outputs: W (bit)

Local Registers: tmp0, tmp1, tmp2, tmp3, avg (32 bits)





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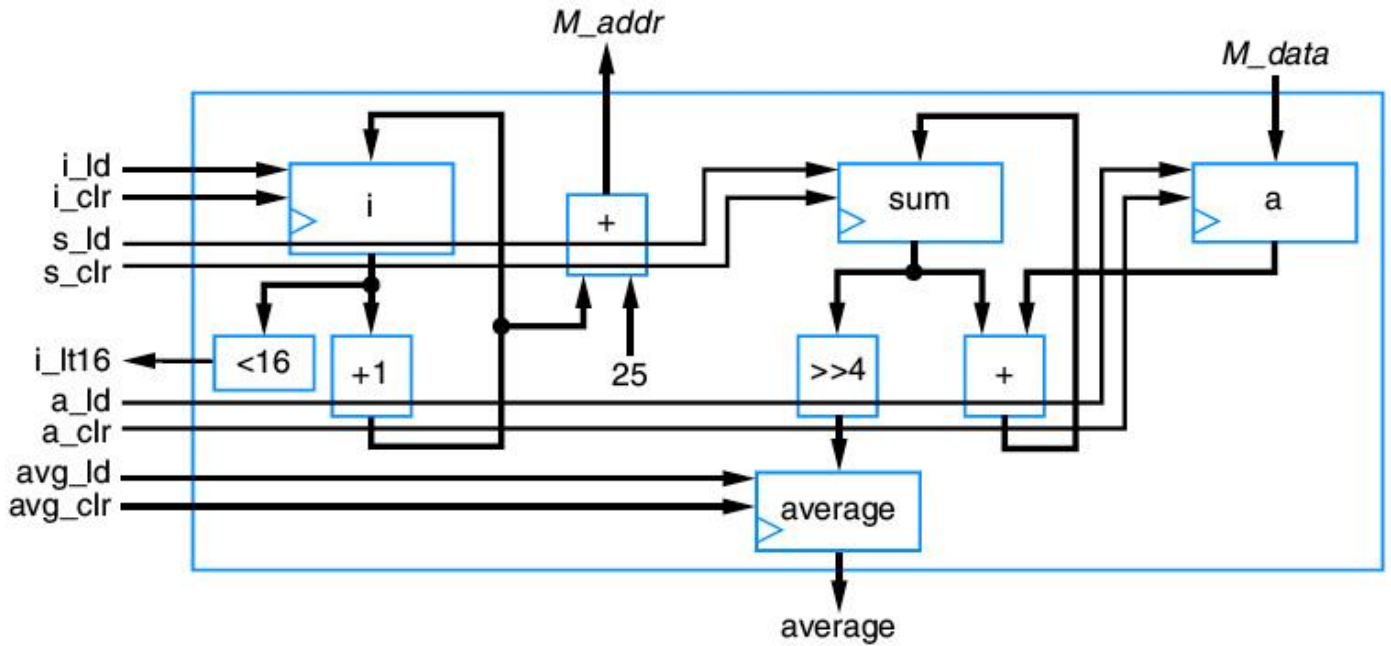
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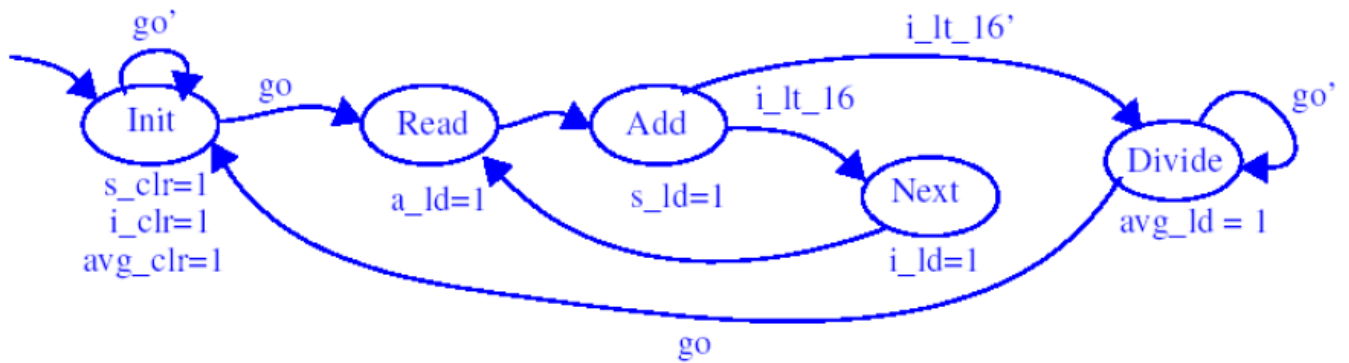
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3. Problem 5.16 (35 points)



Inputs: go , i_lt_16 (bit)

Outputs: s_clr , i_clr , avg_clr , s_ld , i_ld , a_ld (bit)





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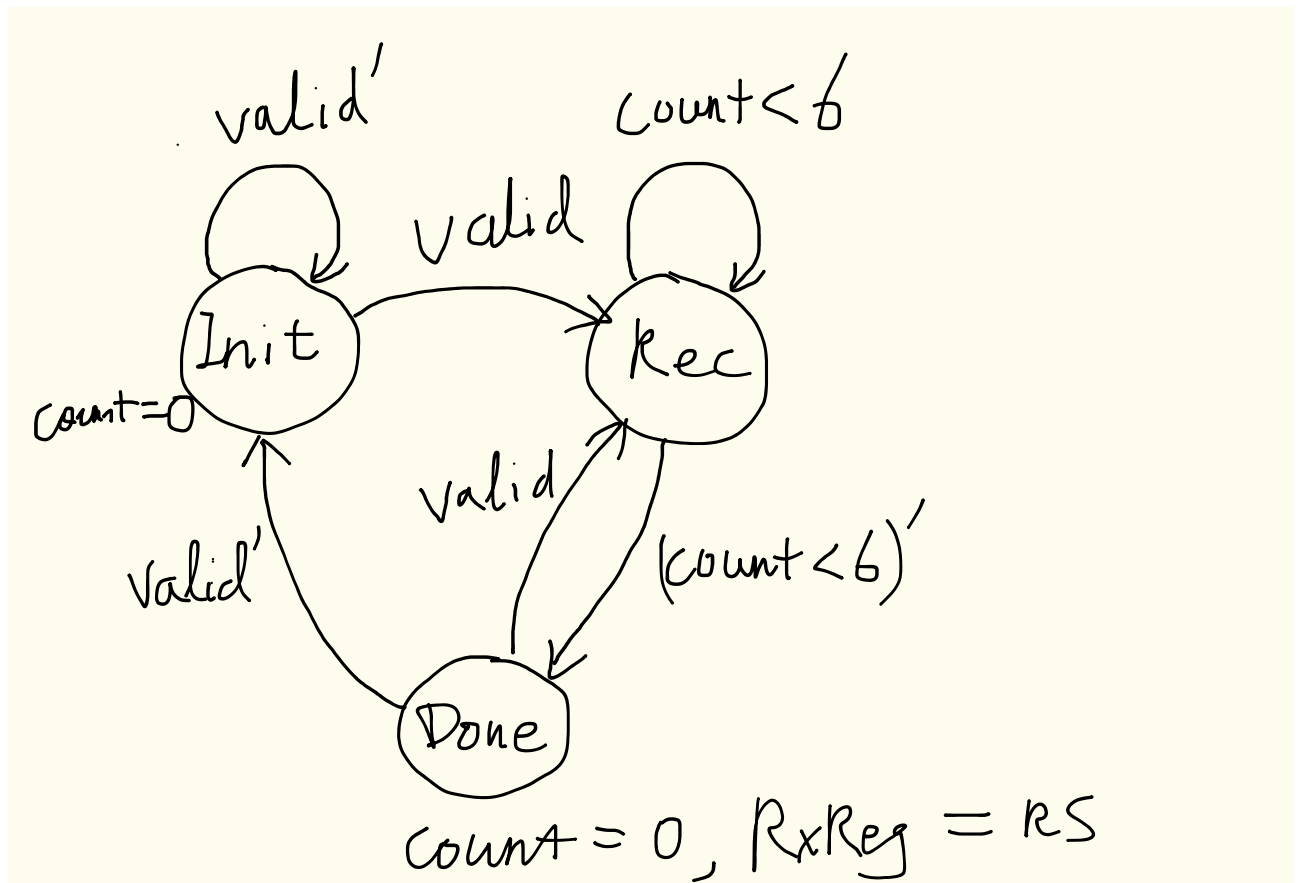
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4. Design a circuit called **Receiver** that receives two single bit signals, **Valid** and **Data_in**, from another device called **Transmitter**. The **Valid** signal sent from the **Transmitter** will be a 1-clock cycle pulse. After the **Receiver** receives the **Valid** pulse, it will start receiving 8 bits through port **Data_in**, bit by bit. After the 8 bit information is received, it should be copied into an 8-bit register called **RxReg**.

step 1:





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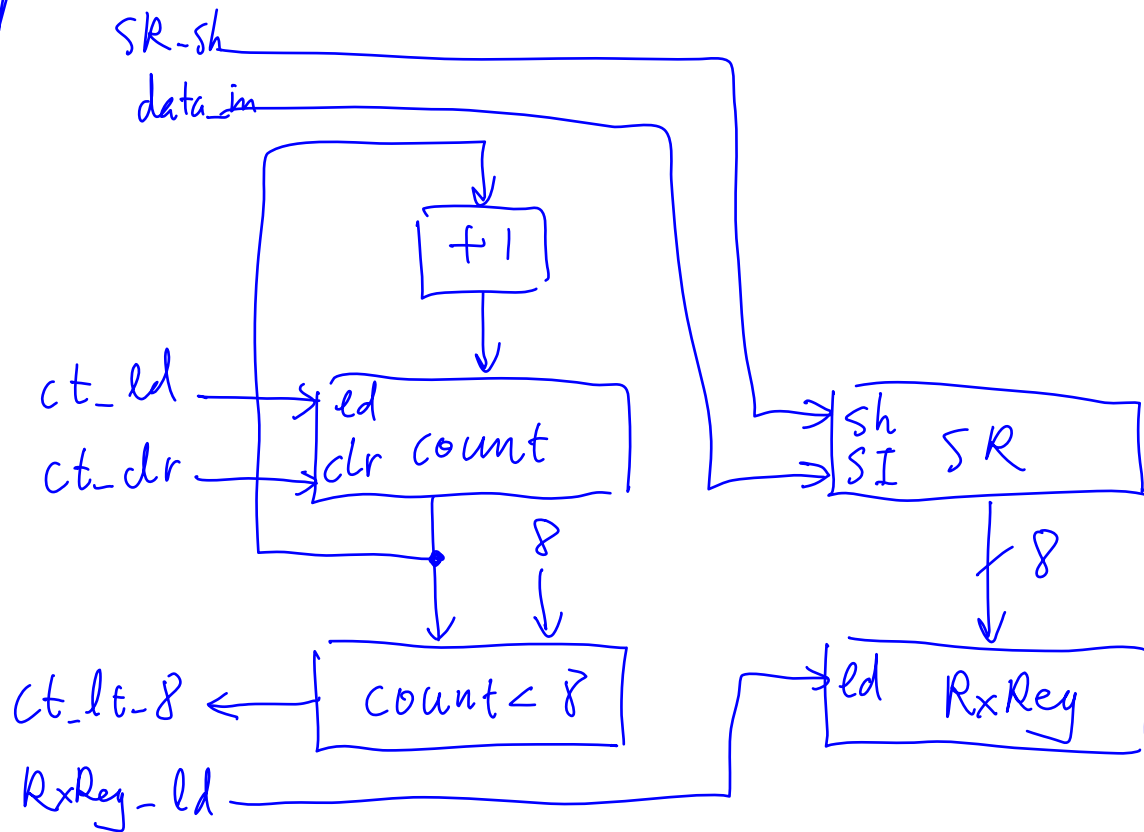
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step 2:





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