VE 320 Summer 2019

Introduction to Semiconductor Devices

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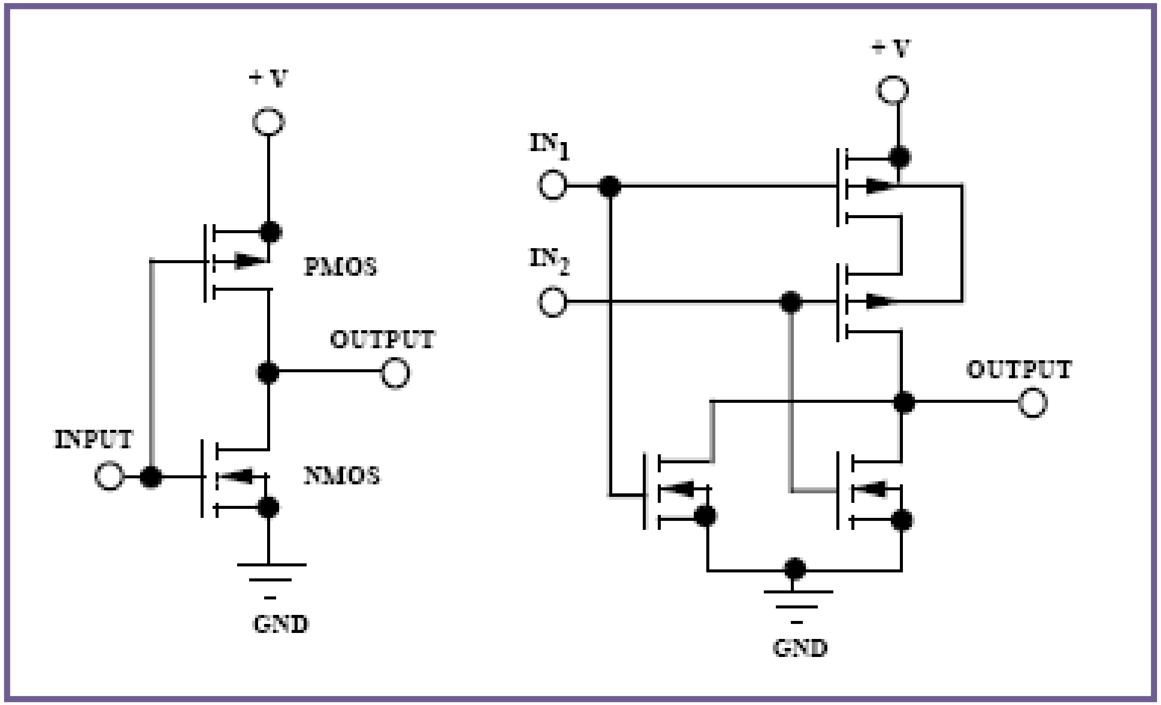
Supplementary note on the brief introduction to the fabrication process of modern integrated circuits

IC Processing

Introduction

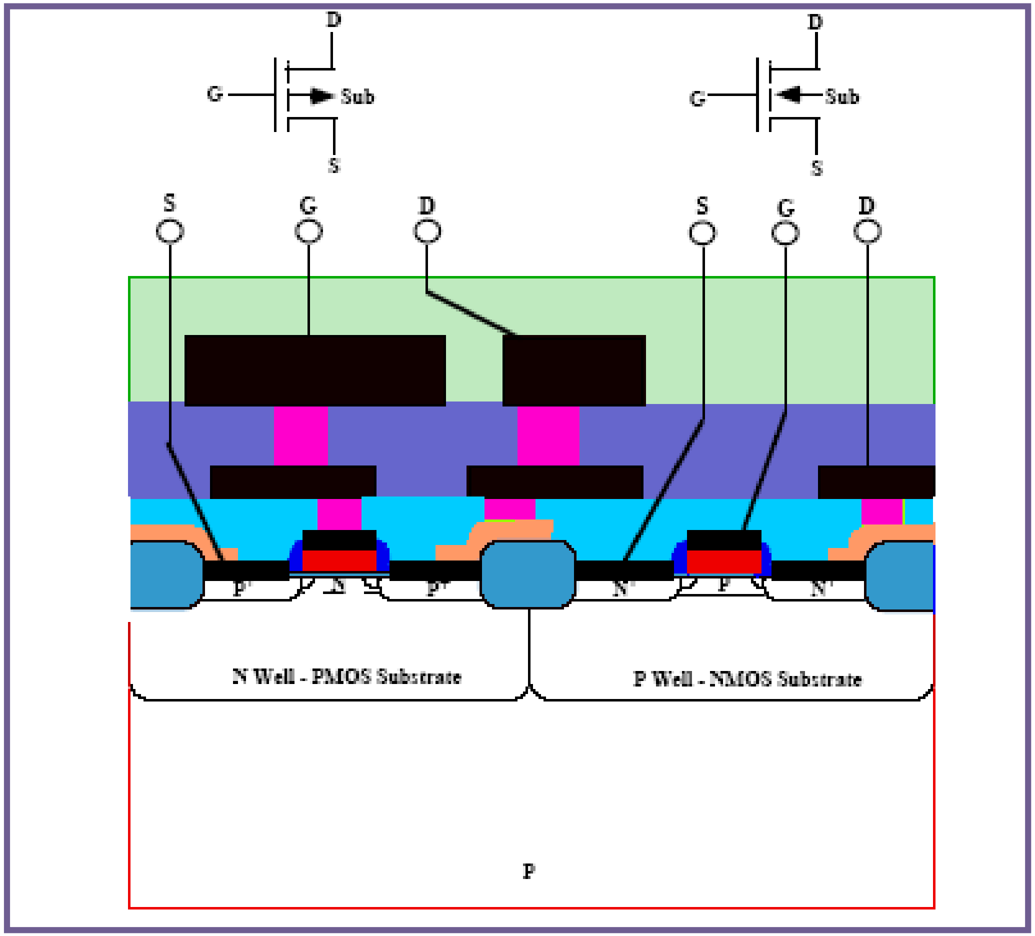
- Transistors: *As you may be used to seeing them*


+V
PMOS
OUTPUT
INPUT
NMOS
GND
+V
IN1
IN2
OUTPUT
GND

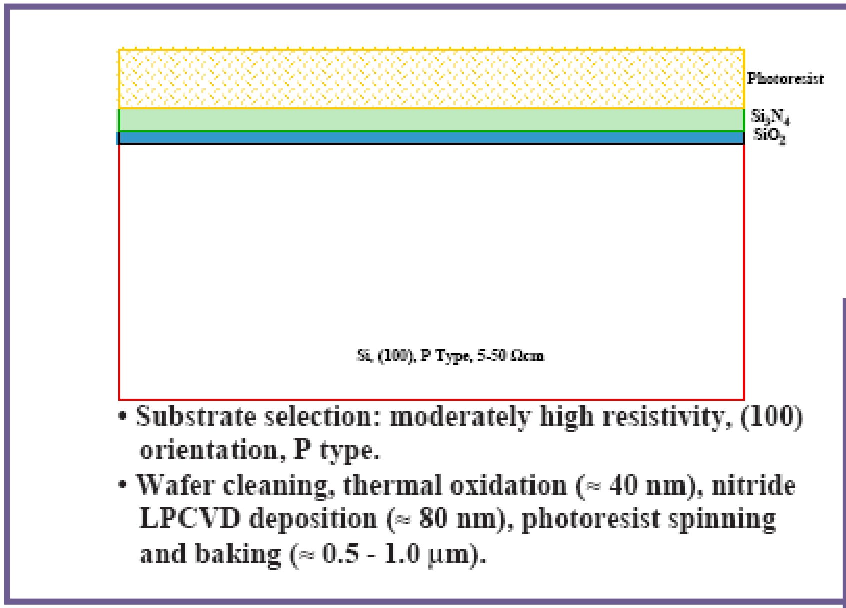
IC Processing

Introduction

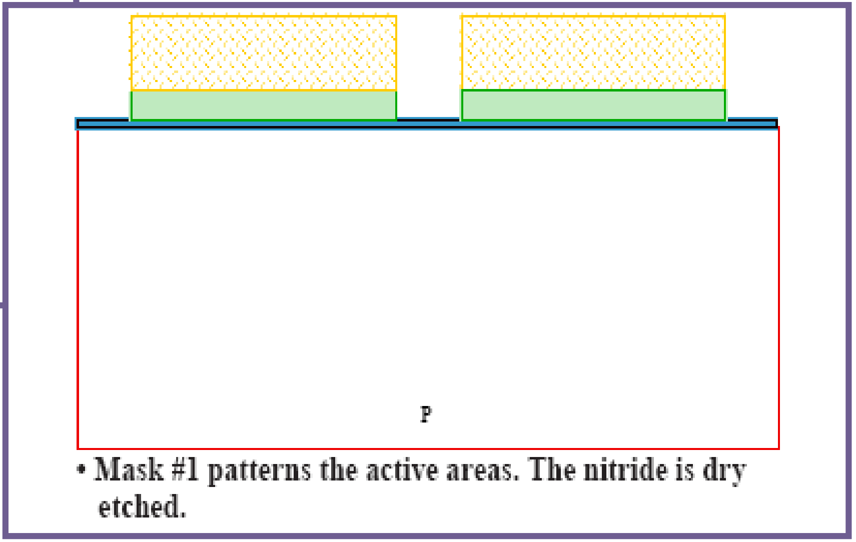
- Transistors: *As we will view them*


D
G
Sub
S
D
G
Sub
S
S
G
D
S
G
D
P+
N
P+
N+
P
N+
N Well - PMOS Substrate
P Well - NMOS Substrate
P

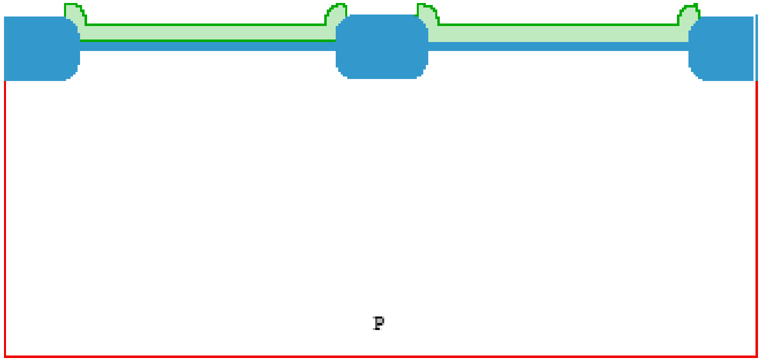
The process sequence to fabricate the transistors shown previously, as shown using cross-sections



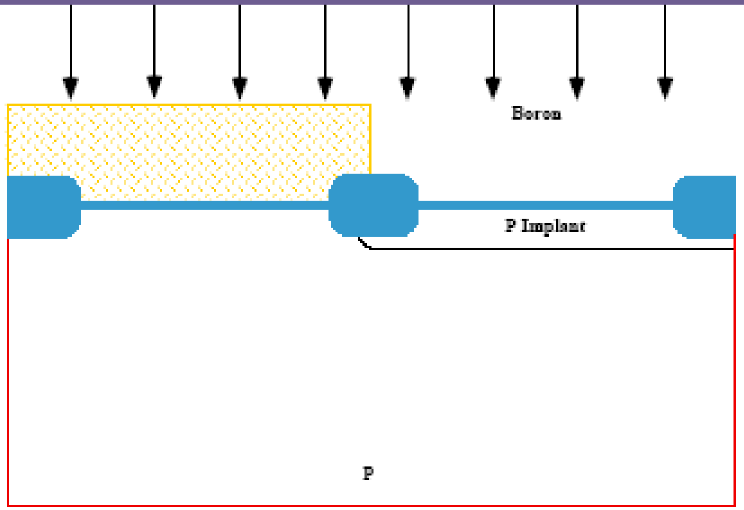
- Substrate selection: moderately high resistivity, (100) orientation, P type.
- Wafer cleaning, thermal oxidation (≈ 40 nm), nitride LPCVD deposition (≈ 80 nm), photoresist spinning and baking (≈ 0.5 - 1.0 µm).



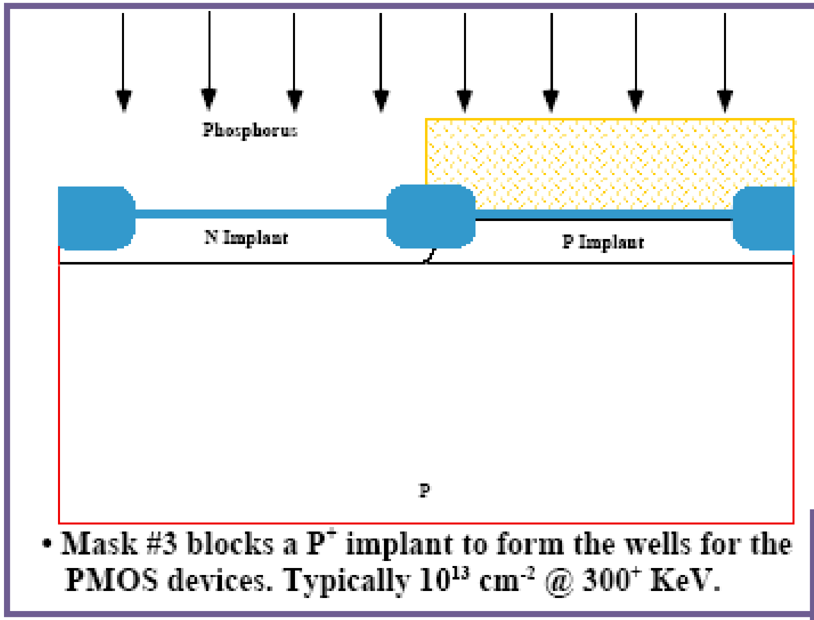
- Mask #1 patterns the active areas. The nitride is dry etched.



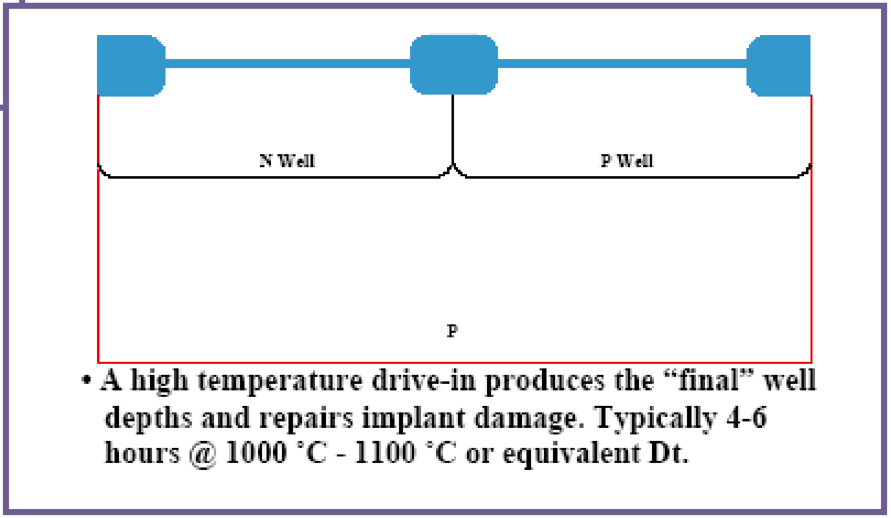
- Field oxide is grown using a LOCOS process. Typically 90 min @ 1000 °C in H_2O grows ≈ 0.5 μm.



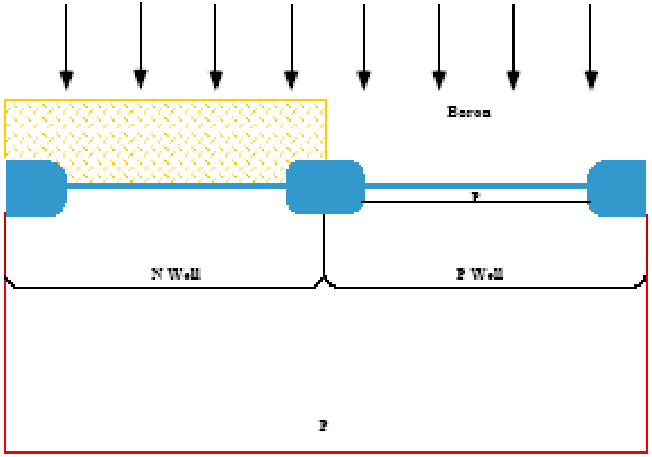
- Mask #2 blocks a B^+ implant to form the wells for the NMOS devices. Typically 10^{13} cm^{-2} @ 150-200 KeV.


Phosphorus
N Implant
P Implant
P

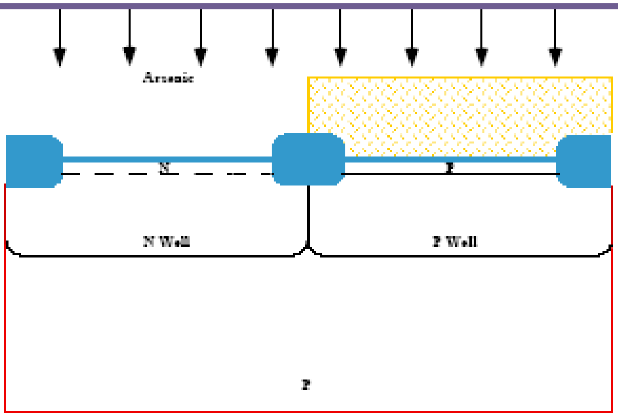
- Mask #3 blocks a P^+ implant to form the wells for the PMOS devices. Typically 10^{13} cm^{-2} @ 300^+ KeV.


N Well
P Well
P

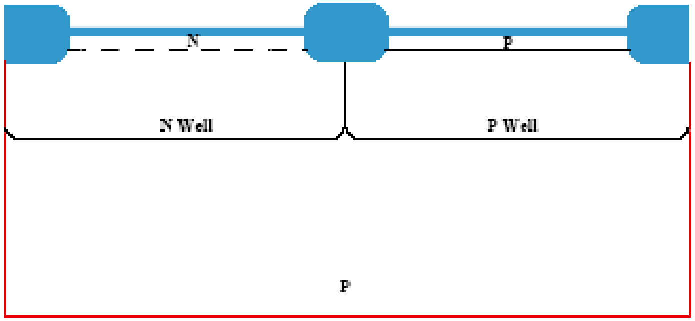
- A high temperature drive-in produces the “final” well depths and repairs implant damage. Typically 4-6 hours @ 1000 °C - 1100 °C or equivalent Dt.


Boron
P
N Well
P Well
P

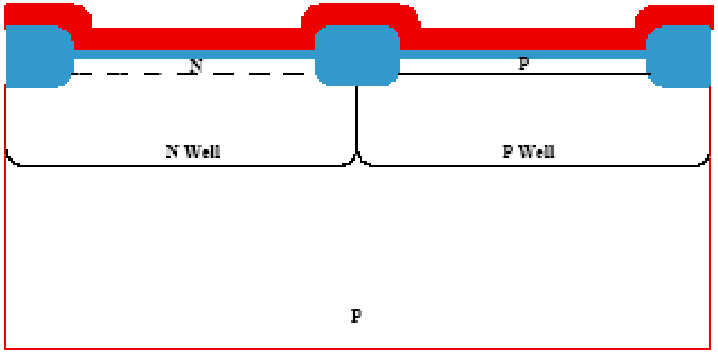
- Mask #4 is used to mask the PMOS devices. A V_{TH} adjust implant is done on the NMOS devices, typically a 1-5 x 10^{12} cm^{-2} B^+ implant @ 50 - 75 KeV.


Arsenic
N
P
N Well
P Well
P

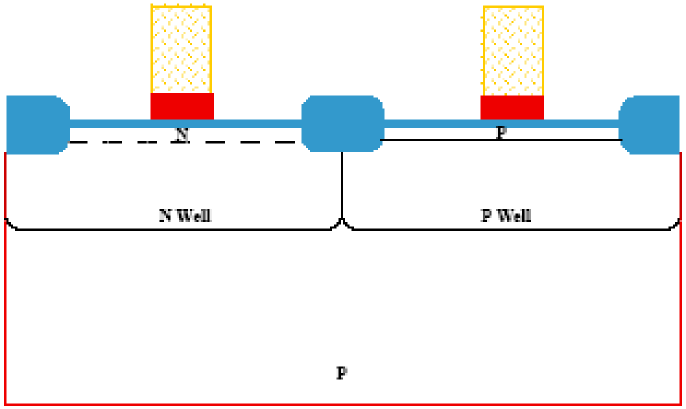
- Mask #5 is used to mask the NMOS devices. A V_{TH} adjust implant is done on the PMOS devices, typically 1-5 x 10^{12} cm^{-2} As^+ implant @ 75 - 100 KeV.


N
P
N Well
P Well
P

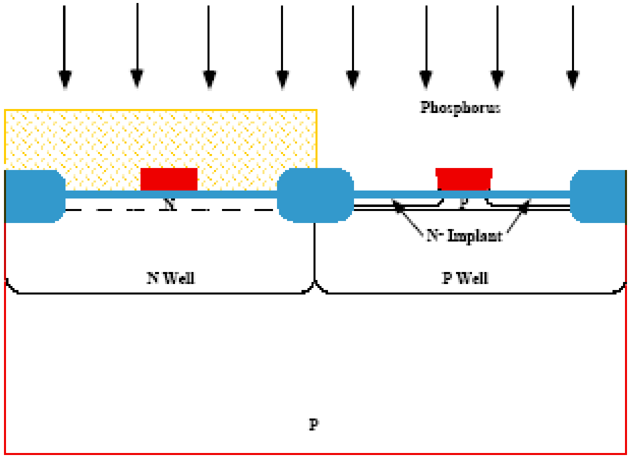
- The thin oxide over the active regions is stripped and a new gate oxide grown, typically 3 - 5 nm, which could be grown in 0.5 - 1 hrs @ 800 °C in O_2.


N
P
N Well
P Well
P

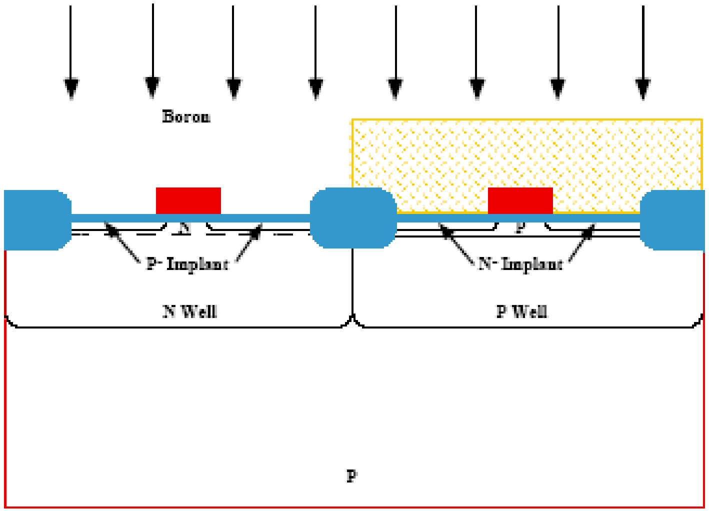
- Polysilicon is deposited by LPCVD (≈ 0.5 µm). An unmasked P^+ or As^+ implant dopes the poly (typically 5×10^{15} cm^{-2}).


N
P
N Well
P Well
P

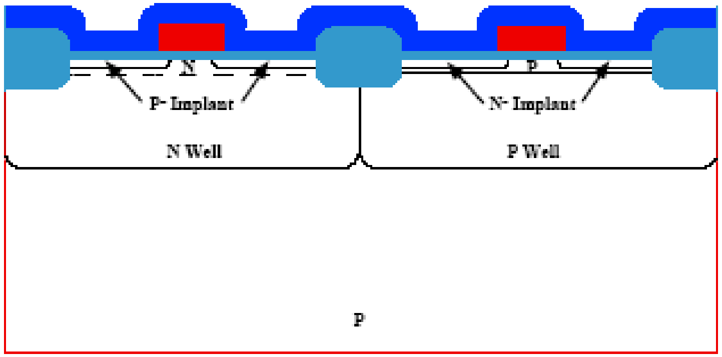
- Mask #6 is used to protect the MOS gates. The poly is plasma etched using an anisotropic etch.


Phosphorus
N
P
N- Implant
N Well
P Well
P

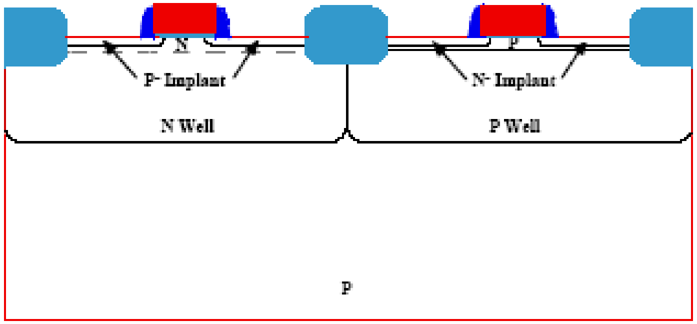
- Mask #7 protects the PMOS devices. A P^+ implant forms the LDD regions in the NMOS devices (typically 5×10^{13} cm^{-2} @ 50 KeV).


Boron
N
P
P- Implant
N- Implant
N Well
P Well
P

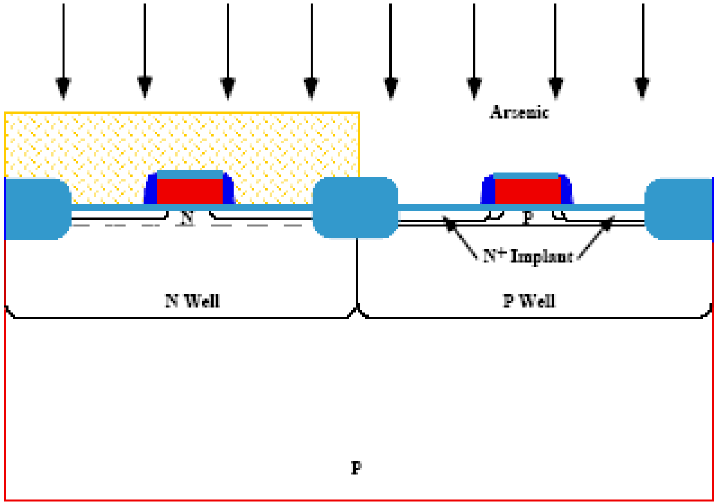
- Mask #8 protects the NMOS devices. A B^+ implant forms the LDD regions in the PMOS devices (typically 5 x 10^{13} cm^{-2} @ 50 KeV).


N
P
P- Implant
N- Implant
N Well
P Well
P

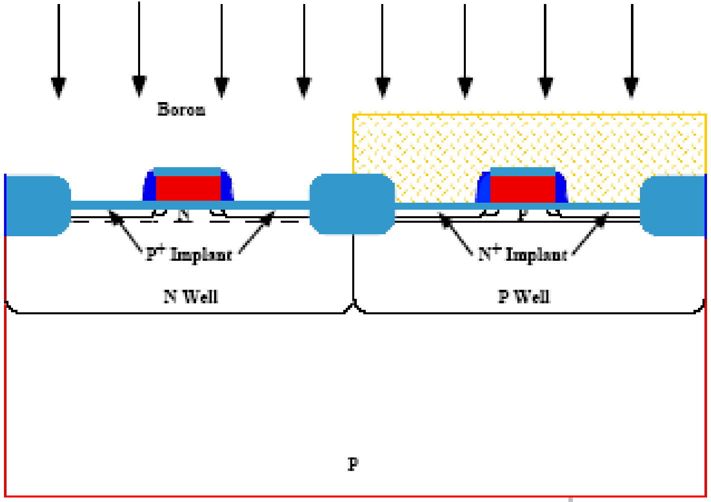
- Conformal layer of SiO_2 is deposited (typically 0.5 μm).


N
P
P- Implant
N- Implant
N Well
P Well
P

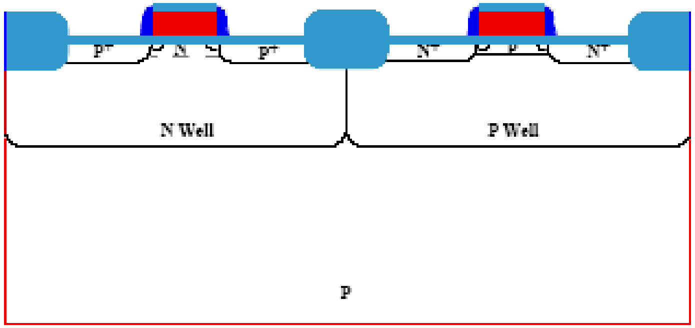
- Anisotropic etching leaves “sidewall spacers” along the edges of the poly gates.


Arsenic
N
P
N+ Implant
N Well
P Well
P

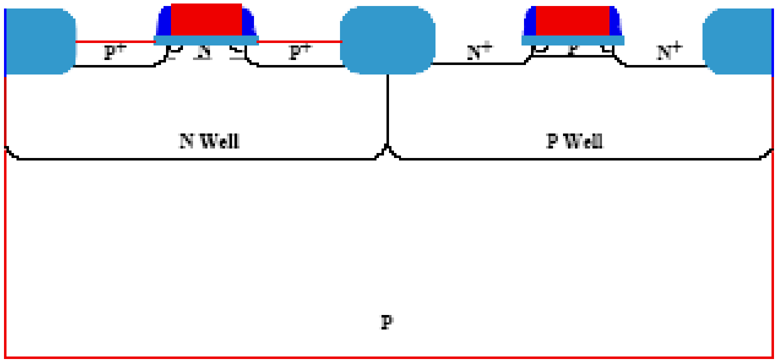
- Mask #9 protects the PMOS devices, An As$^+$ implant forms the NMOS source and drain regions (typically 2-4 x 10^{15} cm^{-2} @ 75 KeV).


Boron
N
P
P+ Implant
N+ Implant
N Well
P Well
P

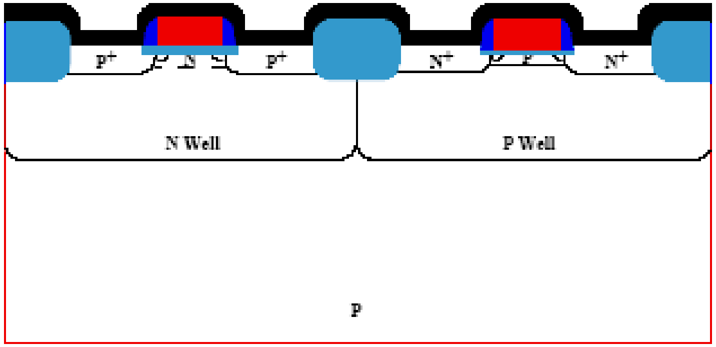
- Mask #10 protects the NMOS devices, A B^+ implant forms the PMOS source and drain regions (typically 1-3 x 10^{15} cm^{-2} @ 50 KeV).


P+
N
P+
N+
P
N+
N Well
P Well
P

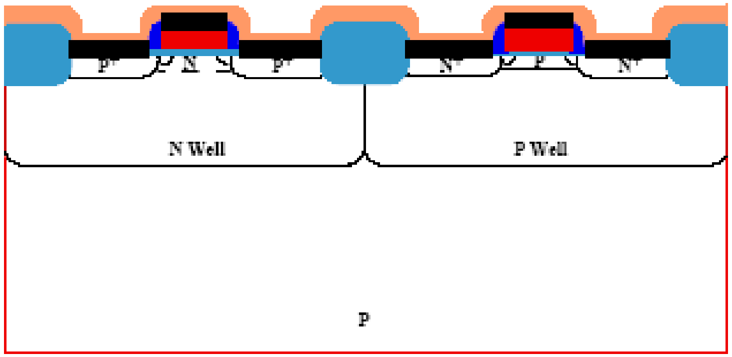
- A final high temperature anneal drives-in the junctions and repairs implant damage (typically 30 min @ 900 °C or 1 min RTA @ 1000 °C).


P+
N
P+
N+
P
N+
N Well
P Well
P

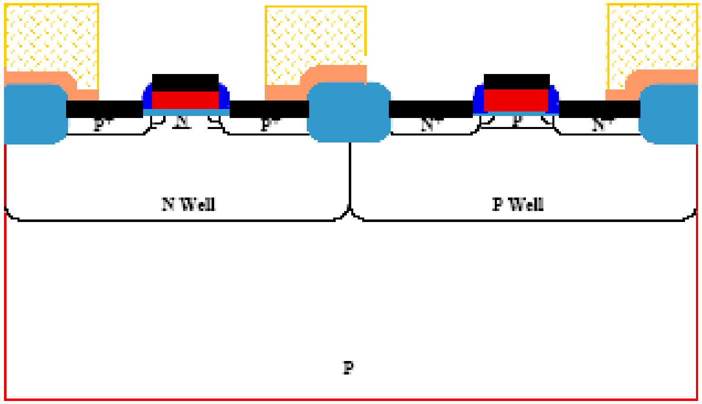
- An unmasked oxide etch allows contacts to Si and poly regions.


P+
N
P+
N+
P
N+
N Well
P Well
P

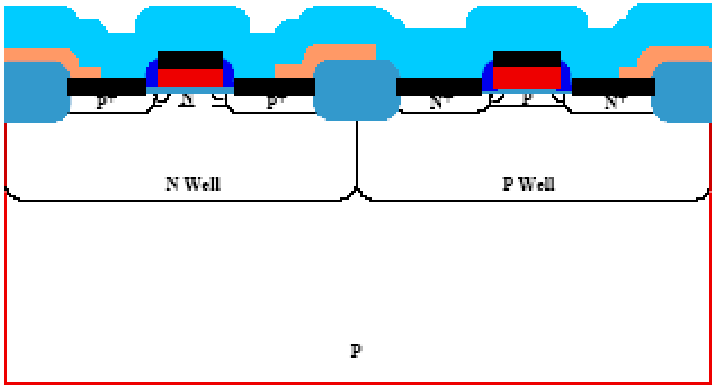
- Ti is deposited by sputtering (typically 100 nm).


P+
N
P+
N+
P
N+
N Well
P Well
P

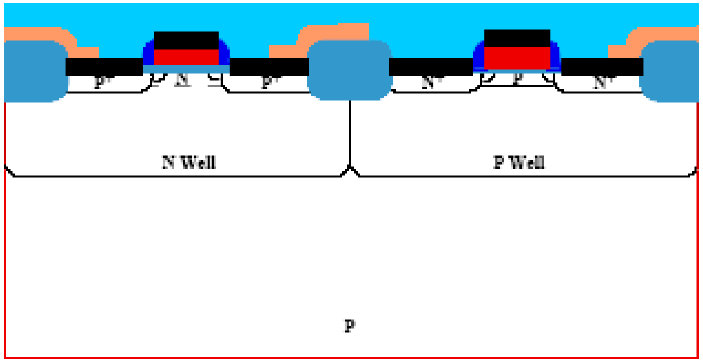
- The Ti is reacted in an N_2 ambient, forming $TiSi_2$ and TiN (typically 1 min @ 600 °C).


P+
N
P+
N+
P
N+
N Well
P Well
P

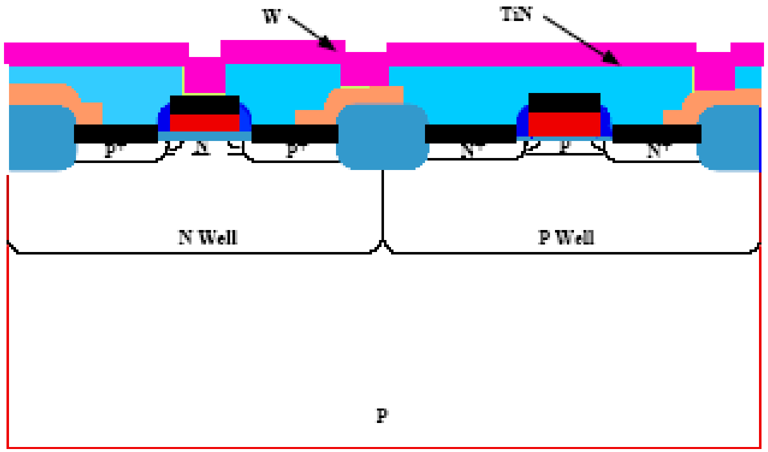
- Mask #11 is used to etch the TiN, forming local interconnects.


P+
N
P+
N+
P
N+
N Well
P Well
P

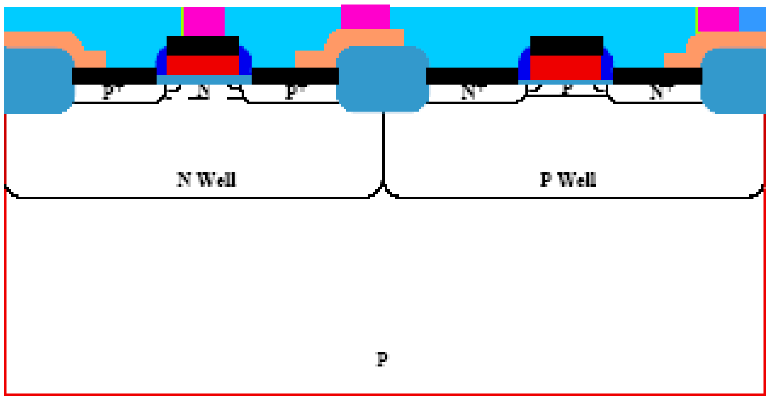
- A conformal layer of SiO_2 is deposited by LPCVD (typically 1 µm).


P+
N
P+
N+
P
N+
N Well
P Well
P

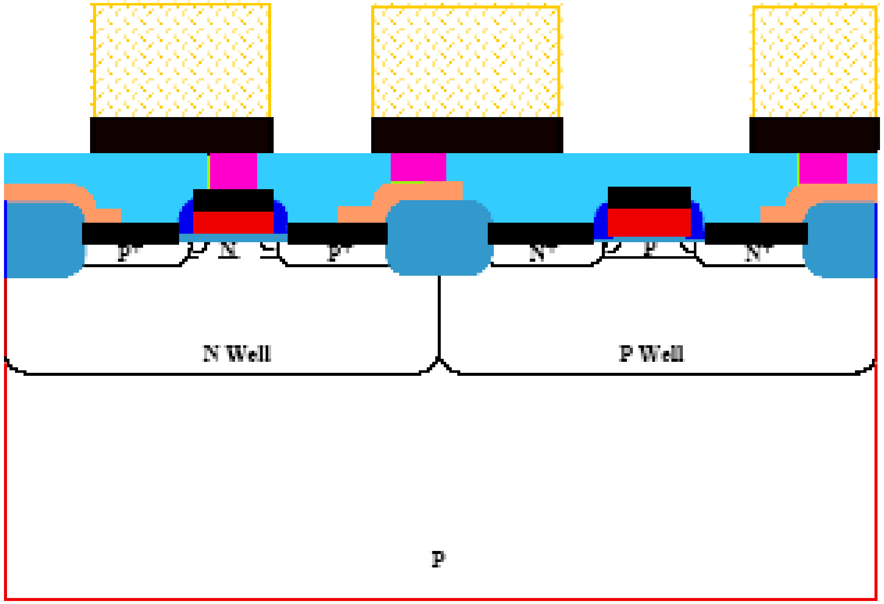
- CMP is used to planarize the wafer surface.


W
TiN
P+
N
P+
N+
P
N+
N Well
P Well
P

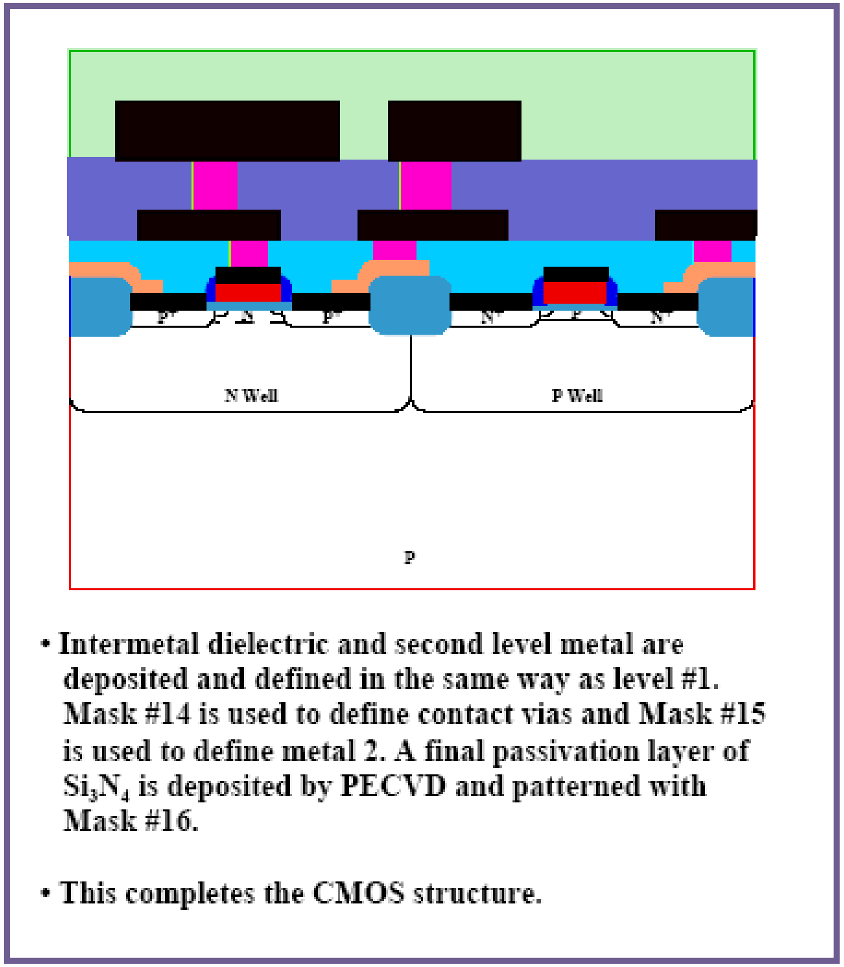
- A thin TiN barrier layer is deposited by sputtering (typically a few tens of nm), followed by W CVD deposition.


P+
N
P+
N+
P
N+
N Well
P Well
P

- CMP is used to planarize the wafer surface, completing the damascene process.


P+
N
P+
N+
P
N+
N Well
P Well
P

- Al is deposited on the wafer by sputtering. Mask #13 is used to pattern the Al and plasma etching is used to etch it.

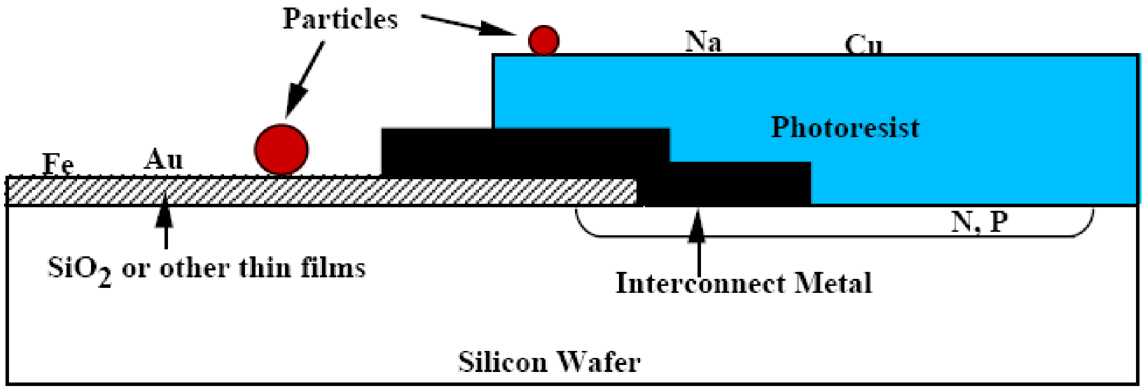


- Intermetal dielectric and second level metal are deposited and defined in the same way as level #1. Mask #14 is used to define contact vias and Mask #15 is used to define metal 2. A final passivation layer of Si_3N_4 is deposited by PECVD and patterned with Mask #16.

- This completes the CMOS structure.

Cleanroom fabrication

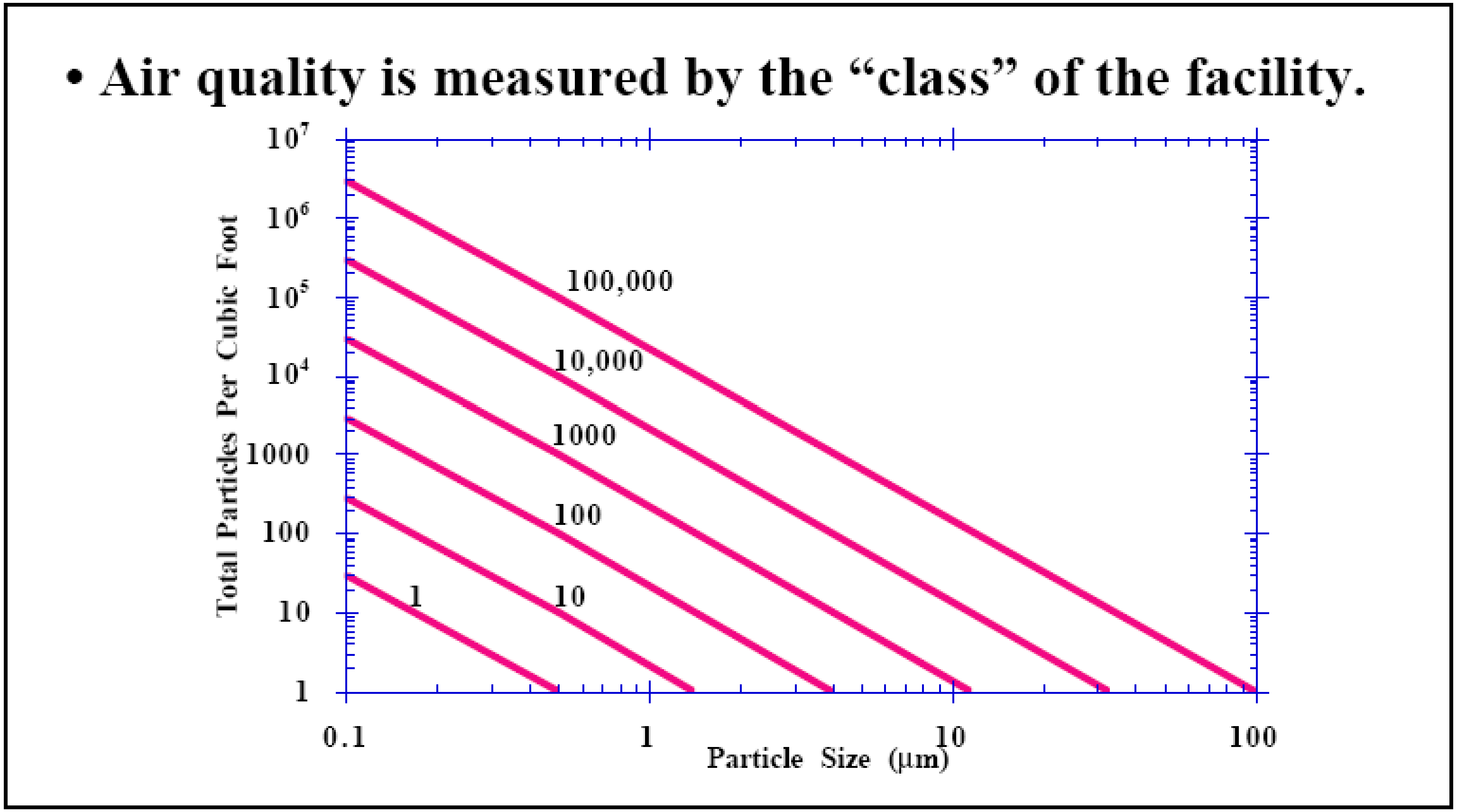
- Multi-faceted Approach:
  1. Use of clean rooms
  2. Rigid cleaning procedures
  3. Tight equipment usage protocols
  4. Gettering
- Types of Common Contaminants


Particles
Na
Cu
Photoresist
Fe
Au
N, P
SiO$_2$ or other thin films
Interconnect Metal
Silicon Wafer

- Contaminants may consist of particles, organic films (photoresist), heavy metals or alkali ions.

- Why such a big deal?
  1. Contaminants can affect fabrication yield
     - Particulates
     - Film residues
  2. Contaminants can affect device performance
     - Ionic contaminants
     - Metallic contaminants

- Level 1 Contamination Control: Cleanrooms



- Air quality is measured by the "class" of the facility.

- Cleanrooms maintain an environment that minimizes problems associated with particulates by doing the following:
  - Use of filtered air by way of HEPA (High Efficiency Particulate Air) filtering
  - Particulate control inside the facility (use of “Bunny Suits”)
  - Filtration of liquids and gases
  - Maintain strict usage protocols
    - i.e., rules for items entering facility

(Photo courtesy of Stanford Nanofabrication Facility.)

- Why such a big issue?
  - ~ 75% of yield loss in IC manufacturing is due to particulate contamination
  - Particles that are 0.1 to 0.3 μm in diameter are most problematic
    - They are large relative to critical device dimensions
    - Small particles coagulate into big ones, which precipitate into bigger ones

Si growth

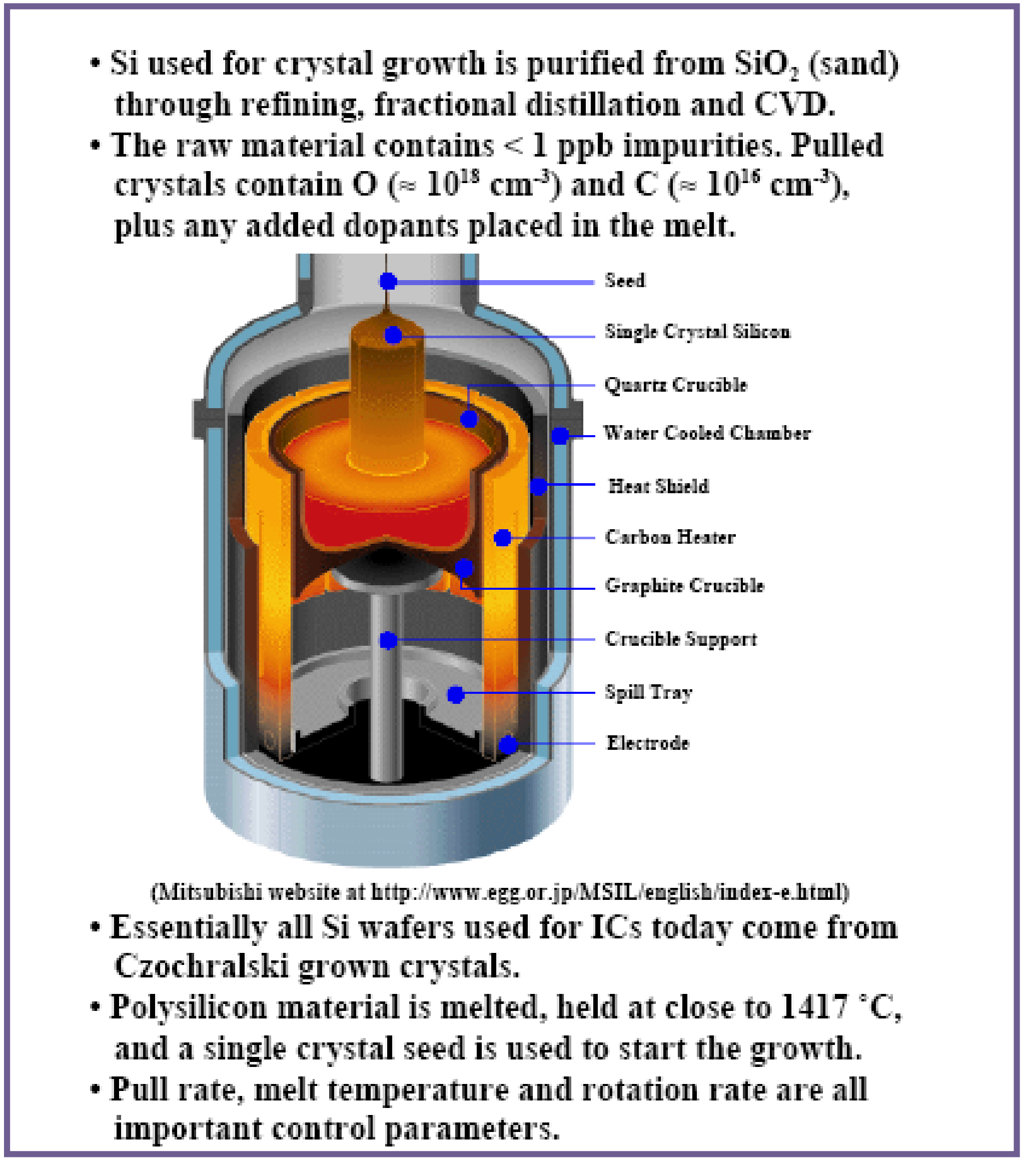
- Fabrication of Si wafers (sand to wafer!):
  - Start with quartzite (sand)
  - Step 1: Convert to metallurgical grade silicon (MGS)
    - Reaction: $SiO_2 + 2C \rightarrow Si + 2CO$
      1. Quartzite and carbon reacted at 2000C in electric arc furnace
      2. SiC is formed and reacts with SiO_2 to form SiO (gas) and Si (liquid). MGS is 98% pure
  - Step 2: Fractional Distillation
    - $MGS + HCl \rightarrow SiHCl_3$ (gas)
      1. Reaction executed at 300C, then product cooled to RT
    - Liquid $SiHCl_3$ is vaporized and distilled to remove impurities

- Step 3: Conversion to electronic grade silicon (EGS)
  - Purified $SiHCl_3$ reacted to form polysilicon
  - Reaction: $2SiHCl_3 + 2H_2 \rightarrow 2Si + 6HCl$
  - Thin polysilicon rod used as nucleation source
  - Product: Polysilicon ingot with purity in ppb level (10^{13}atoms/cm^3)
    - Size: several meters in length, several 100 mm in diam.
- Step 4: Conversion of EGS to single crystal boule
  - Czochralski Method (CZ)
  - Float Zone Method (FZ)

- *Czochralski Method:*
  1. *Most popular method*
  2. *Prone to contamination*
     - *Oxygen*
     - *Carbon*
  3. *Can be used to make very large ingots*

Process details

- uses resistive heating
- melt held in crucible
- seed dipped into melt
- seed extracted under controlled conditions



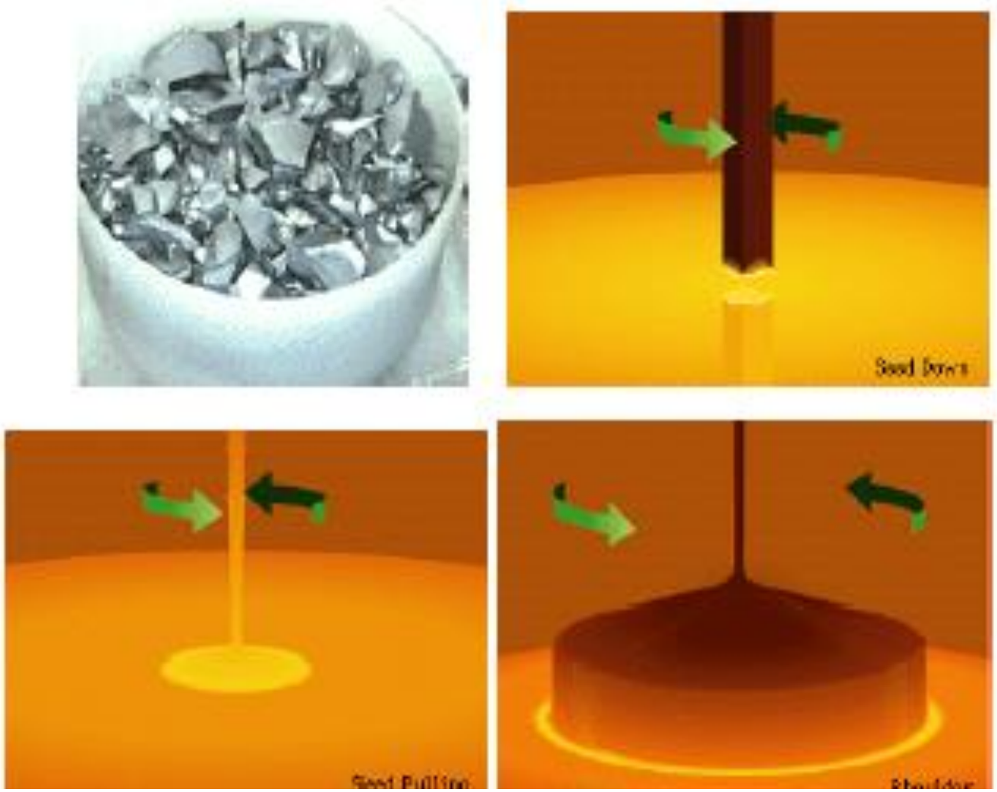
- **Si used for crystal growth is purified from SiO_2 (sand) through refining, fractional distillation and CVD.**
- **The raw material contains < 1 ppb impurities. Pulled crystals contain O (≈ 10^{18} cm^{-3}) and C (≈ 10^{16} cm^{-3}), plus any added dopants placed in the melt.**

Seed
Single Crystal Silicon
Quartz Crucible
Water Cooled Chamber
Heat Shield
Carbon Heater
Graphite Crucible
Crucible Support
Spill Tray
Electrode

(Mitsubishi website at http://www.egg.or.jp/MSIL/english/index-e.html)

- **Essentially all Si wafers used for ICs today come from Czochralski grown crystals.**
- **Polysilicon material is melted, held at close to 1417 °C, and a single crystal seed is used to start the growth.**
- **Pull rate, melt temperature and rotation rate are all important control parameters.**

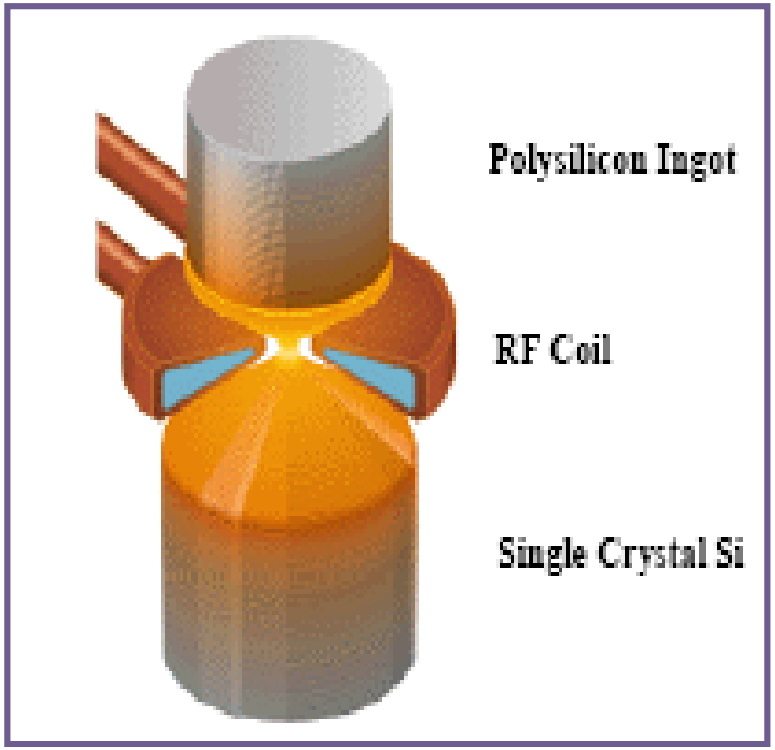
- *CZ simulations showing the melt, seed and boule*


Seed Down
Seed Pulling
Shoulder

- ***Float Zone Method***
- *Less popular than CZ*
- *Non contact*
  - *results in higher purity*
- *Scale-up is challenging*
  - *Boules generally smaller*

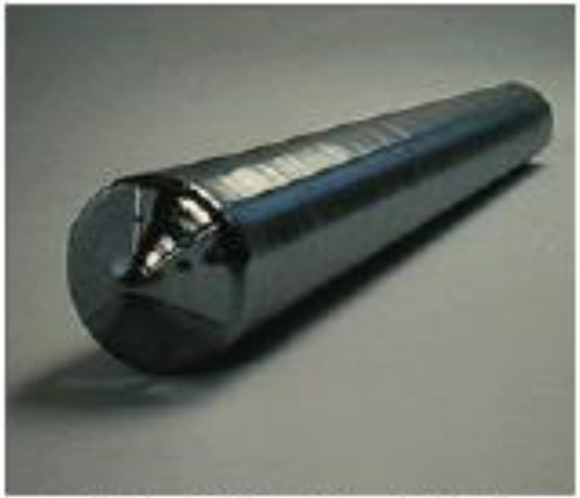
Process details

- Uses rf induction heating
- Single crystal seed clamped at one end of polysilicon rod
- Melt suspended by surface tension and levitation
- Heated zone moved along the rod


Polysilicon Ingot
RF Coil
Single Crystal Si

- *Boules to wafers: Careful low-tech processing*

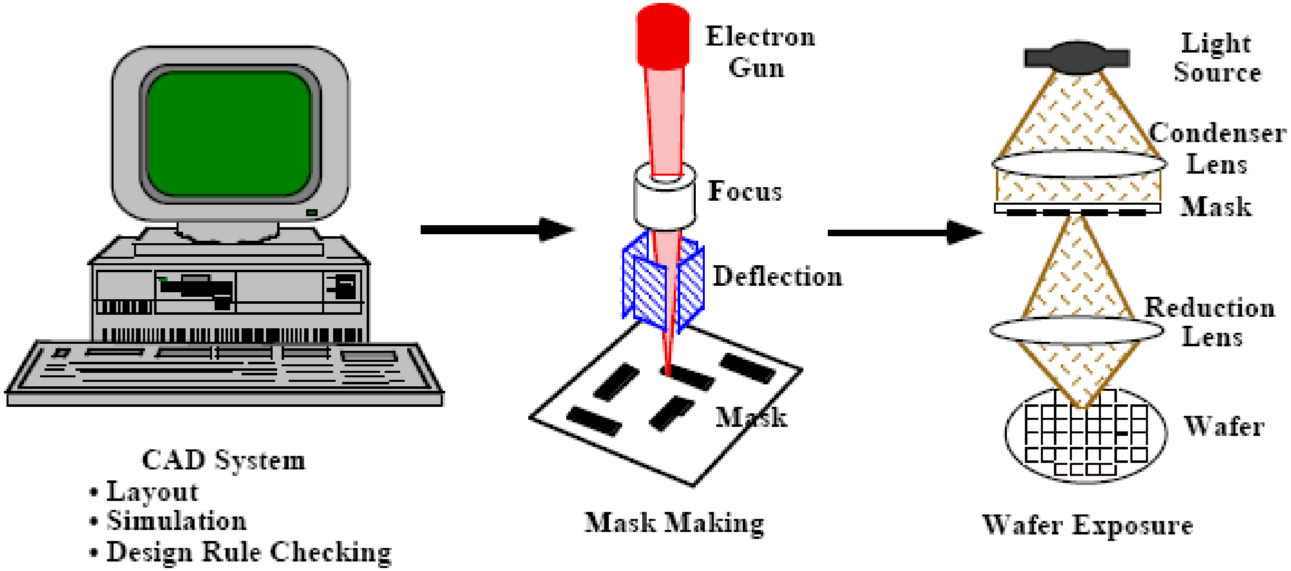
- *Boule shaped to uniform diameter by mechanical machining*
- *Wafer “flats” cut into boule*
  - used to identify crystal type and orient wafers during processing
- *Boule sawed into wafers*
  - Proper orientation required
  - 50% of ingot lost
- *Wafers mechanically lapped*
  - Al_2O_3 and glycerine slurry to remove 50 microns
- Edges of wafers rounded (champfering)
- Wafers etched in HNO_3/HF solution
- Wafers polished by CMP
  - Use silica/NaOH slurry



Lithography

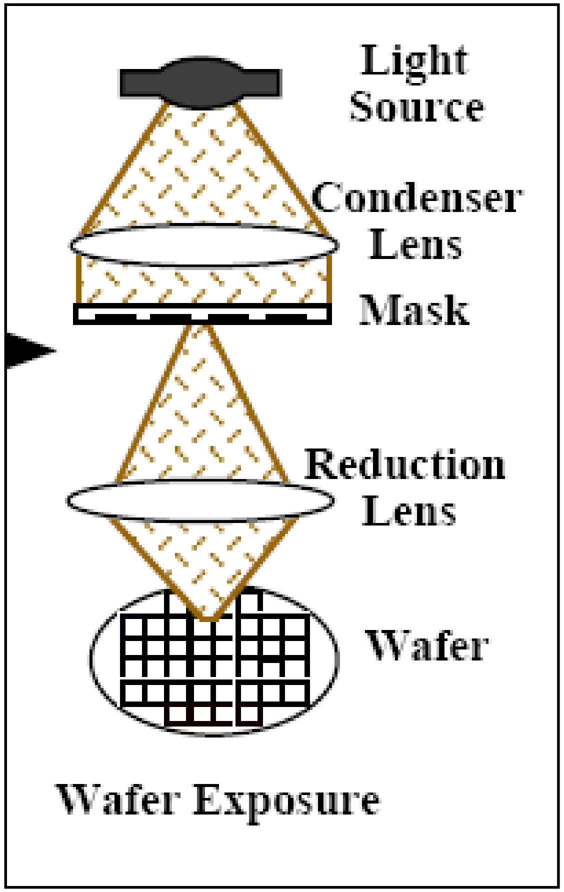
- Lithography is arguably the single most important processing step:
  - 0.7X reduction in size every 3 years
  - Placement accuracy: 1/3 of feature size
  - Involves 35% of manufacturing costs

- The basics of Patterning:
  - The basic process consists of mask design, mask fabrication and wafer printing

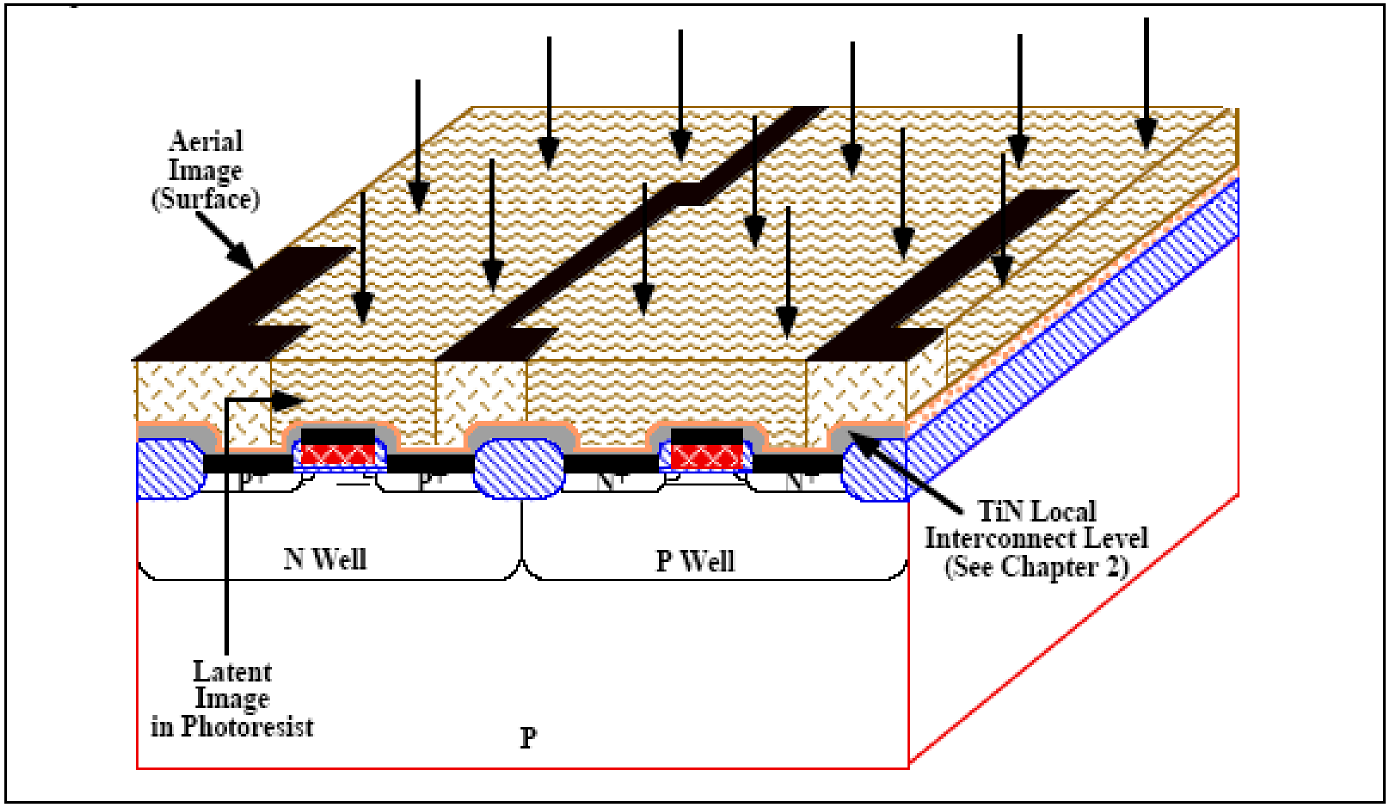

Electron Gun
Focus
Deflection
Mask
Light Source
Condenser Lens
Mask
Reduction Lens
Wafer
CAD System
• Layout
• Simulation
• Design Rule Checking
Mask Making
Wafer Exposure

- The Three Components of Wafer Printing
  - The light source
  - The wafer exposure system
  - The resist

- Each component is critical to achieving the desired results:
  - Minimum feature size
  - Maximum feature density


Light Source
Condenser Lens
Mask
Reduction Lens
Wafer
Wafer Exposure

- Aerial view of the wafer printing (exposure) process


Aerial Image (Surface)
Latent Image in Photoresist
P+
P+
N+
N+
N Well
P Well
P
TiN Local Interconnect Level (See Chapter 2)

The latent image in the resist is a 3D replica of the 2D image on the mask
It is produced by chemical processing

- The Exposure System: The Light Source
  - Basic considerations
    - Smaller features require shorter wavelengths
    - Intensity is also important
    - Bottom line: short wavelength, high intensity sources needed:
      - Hg arc lamps are most common source
        - Discharge created in a Hg-vapor filled tube (kV)
        - Hg gas is ionized and thus energized
        - Photons emitted when energized Hg atoms drop back to lower energy level

The Exposure System: The Light Source (continued)

- Photon emission is quantized since energy levels are discrete
- Strong emission from Hg is in the UV range
- The two most common are:

  436 nm (g-line) → micron resolution

  365 nm (i-line) → submicron (0.35μm)

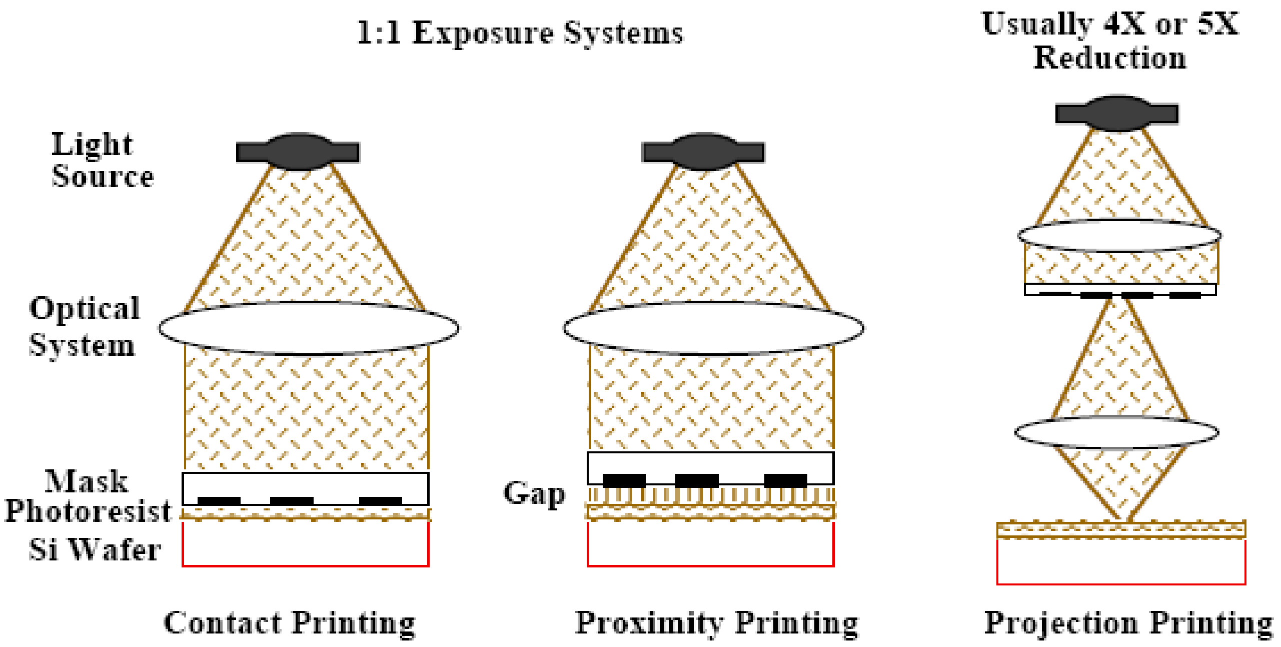
- Smaller features require deep UV radiation
  - Achieved using eximer lasers

    KrF (248 nm) → 0.25μm to 0.18 μm

    ArF (193nm) → 0.10 μm (projected)

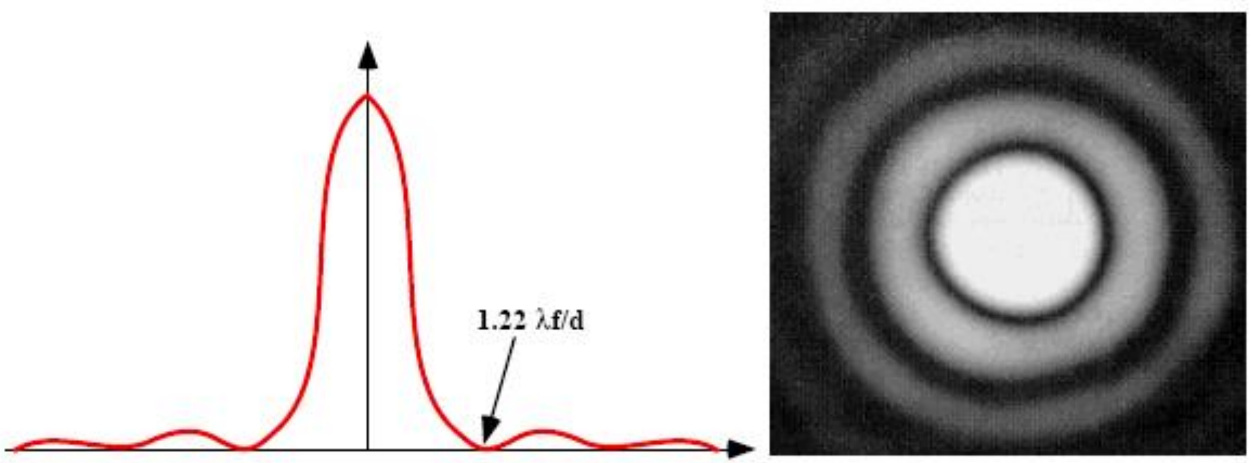
$$\mathrm{Kr} + \mathrm{NF}_3 \xrightarrow[\text{energy}]{} \mathrm{KrF} \rightarrow \text{photon emission}$$

- Exposure Systems


1:1 Exposure Systems
Usually 4X or 5X Reduction
Light Source
Optical System
Mask
Photoresist
Si Wafer
Gap
Contact Printing
Proximity Printing
Projection Printing

Projection printing is dominant today. The most common tool is called a *stepper.* They typically resolve features of about 0.25μm over an area of several cm^2. Throughput: 25 to 50 wafers/hr. Cost: up to $10M each.

- Diffraction from a small circular aperture
  - Diameter of central maximum = 1.22λf/d where f = image length, d = focusing lens diam.



(Photo courtesy of J. Goodman, reprinted with permission of McGraw Hill.)

- **Note that a point image is formed only if $\lambda \to 0$, $f \to 0$ or $d \to \infty$.**

- By definition, the numerical aperture mathematically is:

$$\boxed{\mathrm{NA} \equiv n \sin\alpha}$$

- therefore:

$$\boxed{\therefore R = \frac{0.61\,\lambda}{\mathrm{NA}} = k_1 \frac{\lambda}{\mathrm{NA}}}$$

  - Where k_1 is a unitless parameter related to the exposure tool and resist properties and ranges between 0.6 and 0.8
  - So to increase resolution, decrease wavelength or increase numerical aperture (bigger lenses)

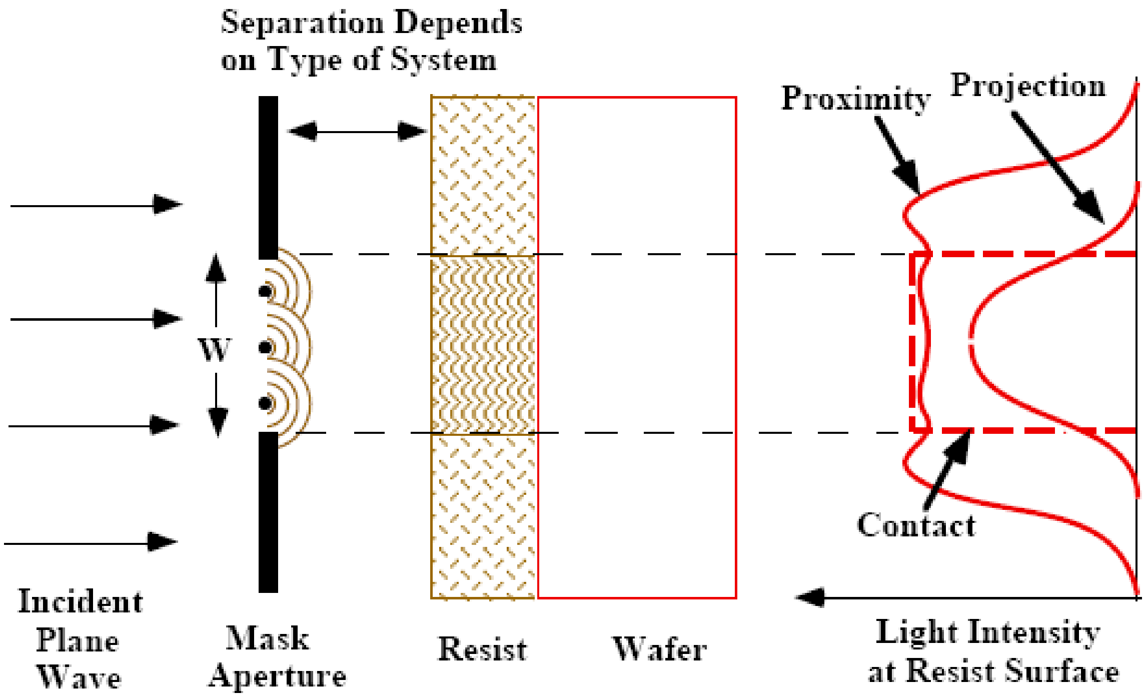
- The Big Trade-off
  - To increase NA with bigger lenses leads to a decrease in the depth of focus:

$$\mathrm{DOF} = \pm\frac{\lambda}{2(\mathrm{NA})^2} = \pm k_2 \frac{\lambda}{(\mathrm{NA})^2}$$

- where k_2 is experimentally determined

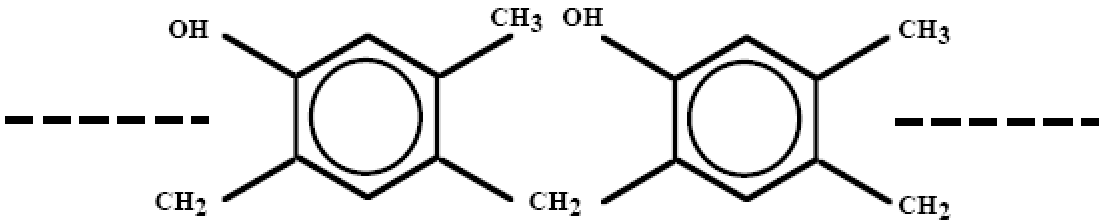
Thus a 248nm (KrF) exposure system with a NA = 0.6 would have a resolution of ≈ 0.3 µm (k_1 = 0.75) and a DOF of ≈ ± 0.35 µm (k_2 = 0.5).

- Summary of Wafer Printing Systems

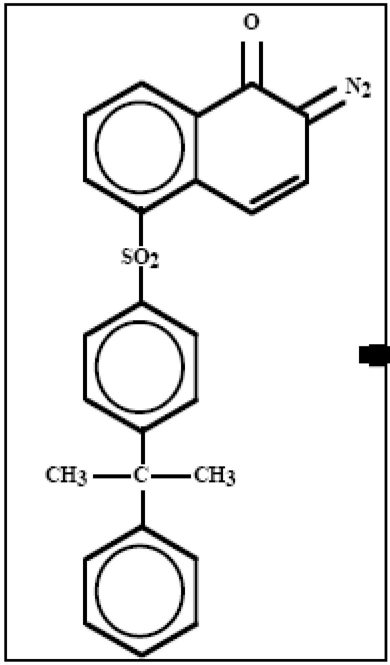

Separation Depends on Type of System
Proximity
Projection
W
Contact
Incident Plane Wave
Mask Aperture
Resist
Wafer
Light Intensity at Resist Surface

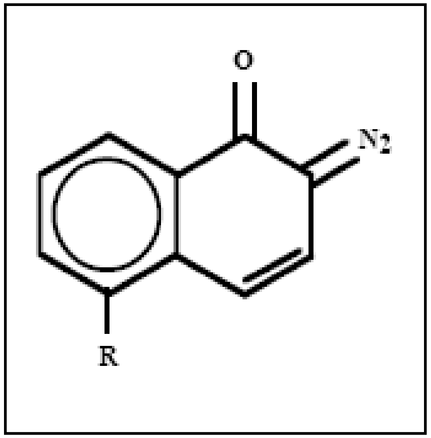
- i-line/g-line Photoresist (PR)
  - Component structure
    - resin *(Novolac)*
      - Inactive component that provides overall structure
    - Photo-active Compound *(PAC)*
      - Chemical that gives PR chemical sensitivity to light
    - Solvent
      - Makes PR a viscous liquid to enable spin casting of thin films
  - After post-exposure bake, the chemical composition is 1:1 resin to PAC

- i-line/g-line PR
  - Resin
    - Called novolac
    - Chemical name: diazonaphthoquinone ***(DNQ)***
    - Polymer consisting of hydrocarbon rings each with two methyl groups and one OH group attached, as shown below


OH
CH3
OH
CH3
CH2
CH2
CH2

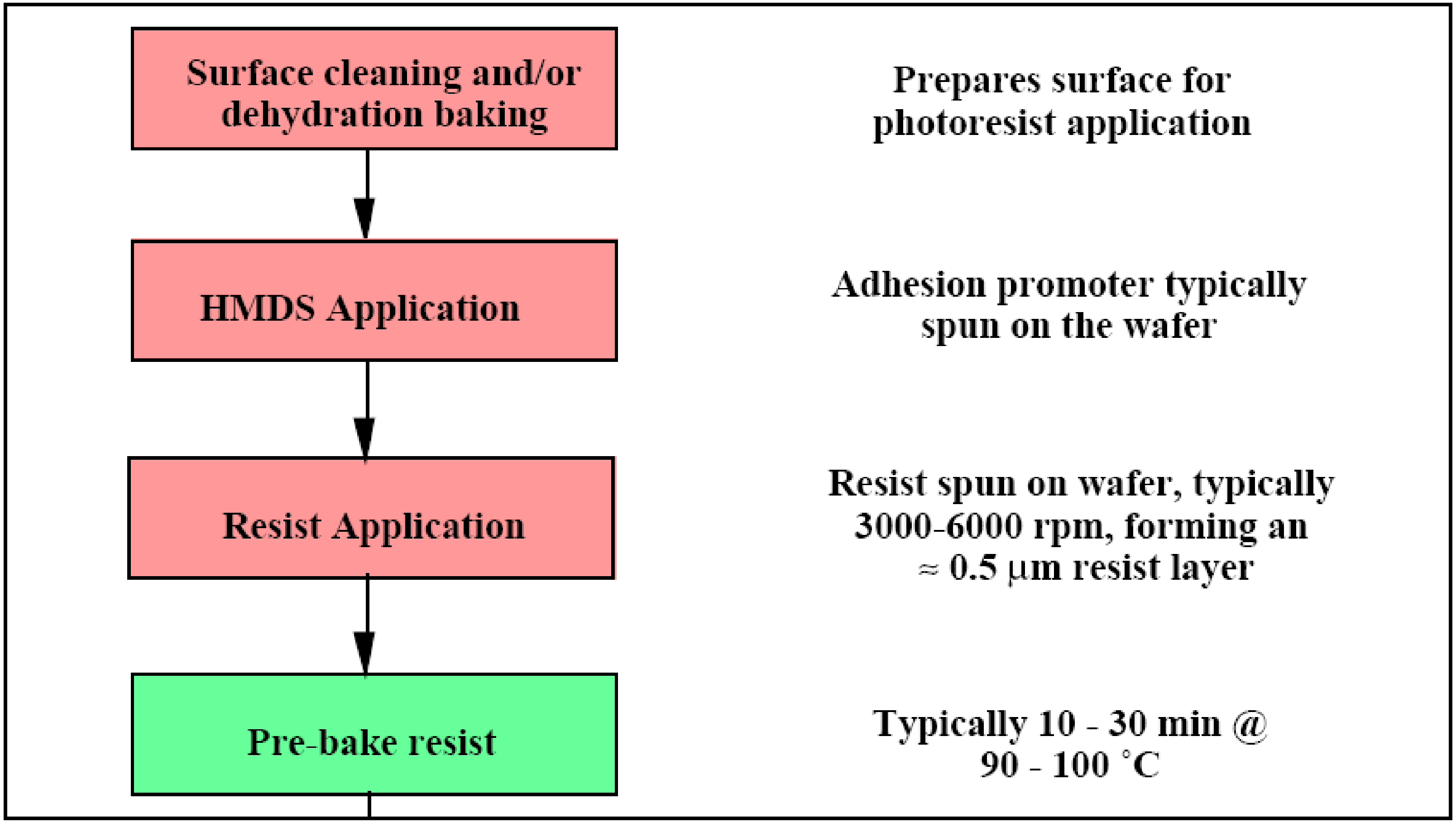
- i-line/g-line PR
  - PAC’s
    - Chemical name: diazoquinone
    - Consists of the structure shown on the left. The photo-active component is that above the SO_2 molecule
    - The figure on the right shows the shorthand notation for a PAC, highlighting the photo-active component





The dissolution rate of unexposed PAC is about 1 to 2 nm/s, thus inhibiting the dissolution of resist material in the developer.

- PR Processing Steps



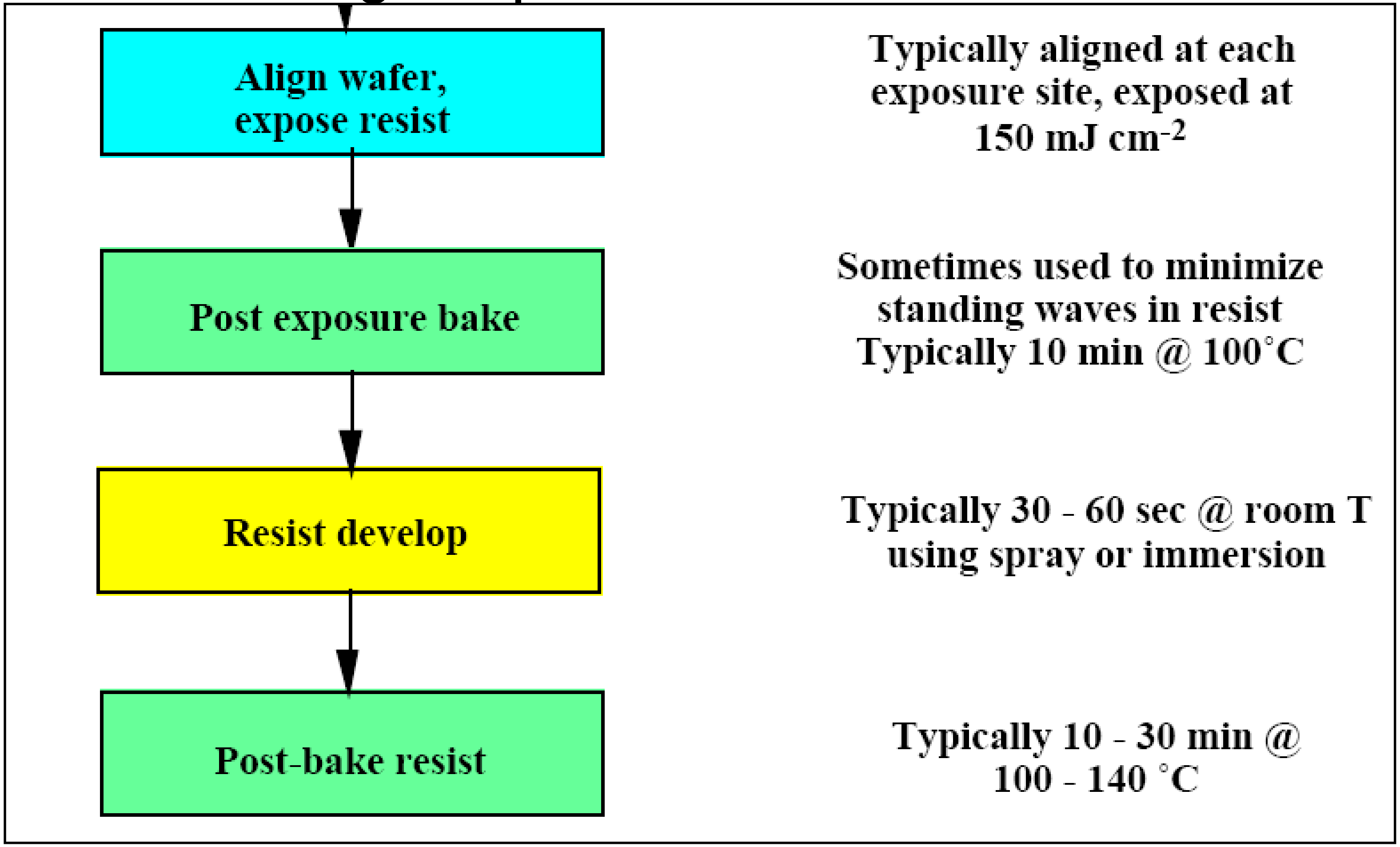
Surface cleaning and/or dehydration baking: Prepares surface for photoresist application

HMDS Application: Adhesion promoter typically spun on the wafer

Resist Application: Resist spun on wafer, typically 3000-6000 rpm, forming an ≈ 0.5 μm resist layer

Pre-bake resist: Typically 10 - 30 min @ 90 - 100 °C

- PR Processing Steps



Align wafer, expose resist

Typically aligned at each exposure site, exposed at 150 mJ cm^{-2}

Post exposure bake

Sometimes used to minimize standing waves in resist
Typically 10 min @ 100°C

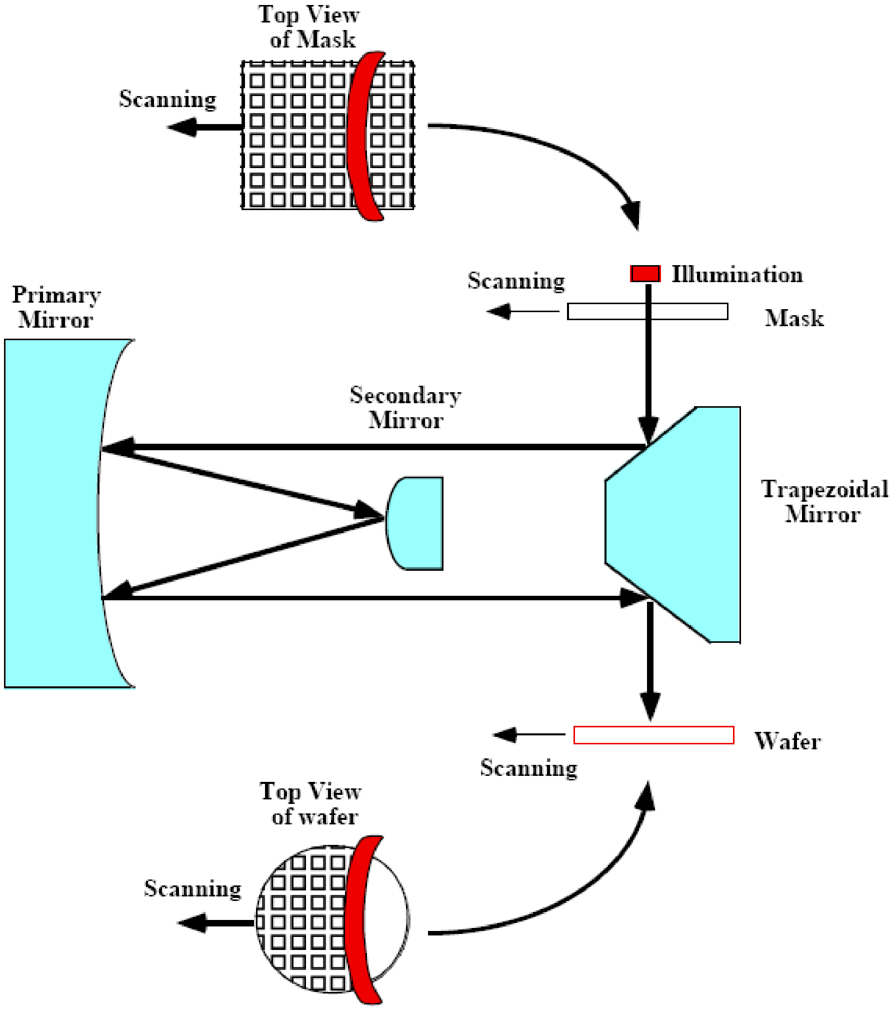
Resist develop

Typically 30 - 60 sec @ room T using spray or immersion

Post-bake resist

Typically 10 - 30 min @ 100 - 140 °C

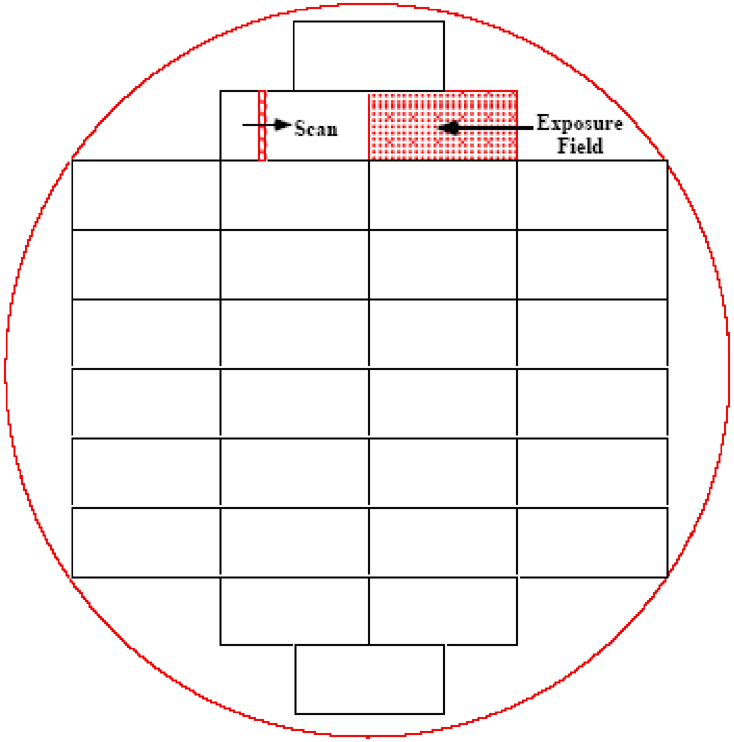
- Modern Exposure Systems
  - Use optics to reduce feature size by up to 5X


Top View of Mask
Scanning
Scanning
Illumination
Mask
Primary Mirror
Secondary Mirror
Trapezoidal Mirror
Wafer
Scanning
Top View of wafer
Scanning

- Modern Exposure Systems
  - Called “steppers” due to the way that they operate

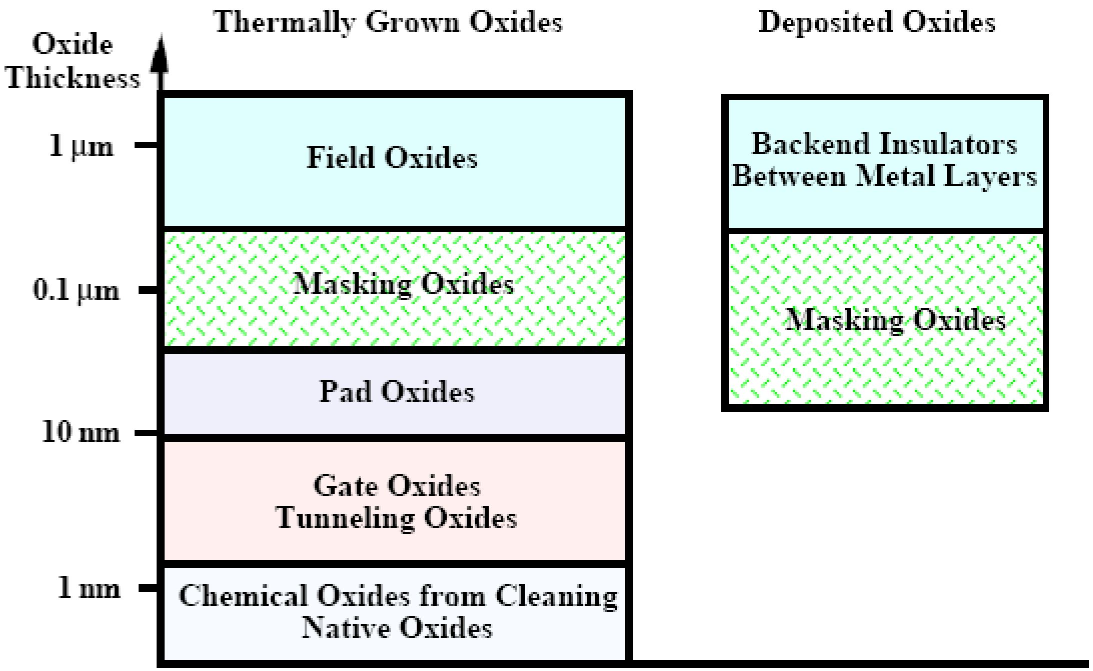
Features of a commercial stepper

1. Reduced optical window thus enabling increased performance
2. Performance specs of Canon stepper
   - 0.25 micron features
   - 8 inch wafers
   - 80 wafers/hr
   - Alignment precision +/- 70 nm
   - KrF illumination source (248 nm)
   - NA of 0.63
   - Field size: 25 x 33 mm



Thermal oxidation

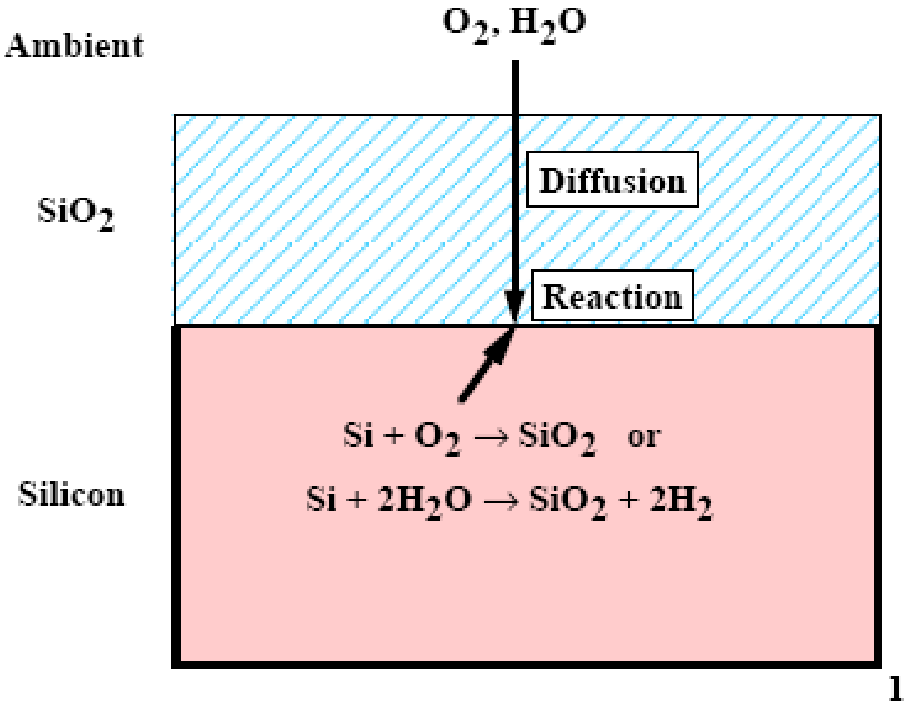
- Introduction
  - Heavy dependence on SiO_2 in Si IC devices


Thermally Grown Oxides
Deposited Oxides
Oxide Thickness
1 µm
0.1 µm
10 nm
1 nm
Field Oxides
Masking Oxides
Pad Oxides
Gate Oxides
Tunneling Oxides
Chemical Oxides from Cleaning
Native Oxides
Backend Insulators
Between Metal Layers
Masking Oxides

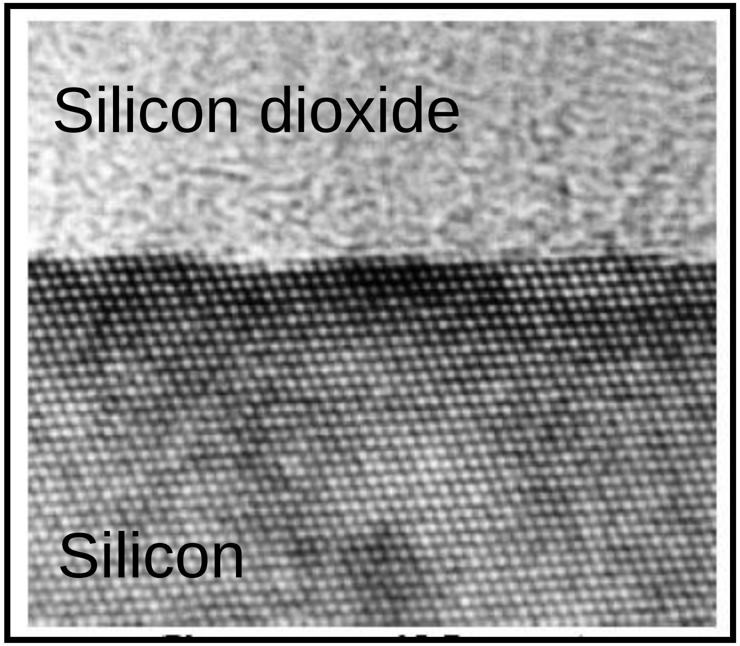
- Types of SiO_2
  - Quartz (crystalline)
  - Thermally grown (amorphous)
  - Deposited (amorphous, lower density)
    - CVD
    - PVD
    - Spin-on Glass
- Thermal oxides dominate in Si IC technology

- Why such a heavy dependence on thermal SiO_2?
  - Processing perspective
    - Can be grown directly on Si surfaces
    - Selective etching to both PR and Si
    - Good masking material for dopants (low diffusivities)
  - Materials perspective
    - Excellent insulator: $\rho > 10^{16}$ Ωcm, $E_g > 9$ eV
    - High breakdown field: 10^7 V/cm
    - Excellent passivation layer
    - Stable properties
    - *Well formed Si/SiO_2 interface*

- The Basics of Si Thermal Oxidation
  - It involves the following:
    - An oxidant
    - Temperature
    - Diffusion
    - Chemical reaction

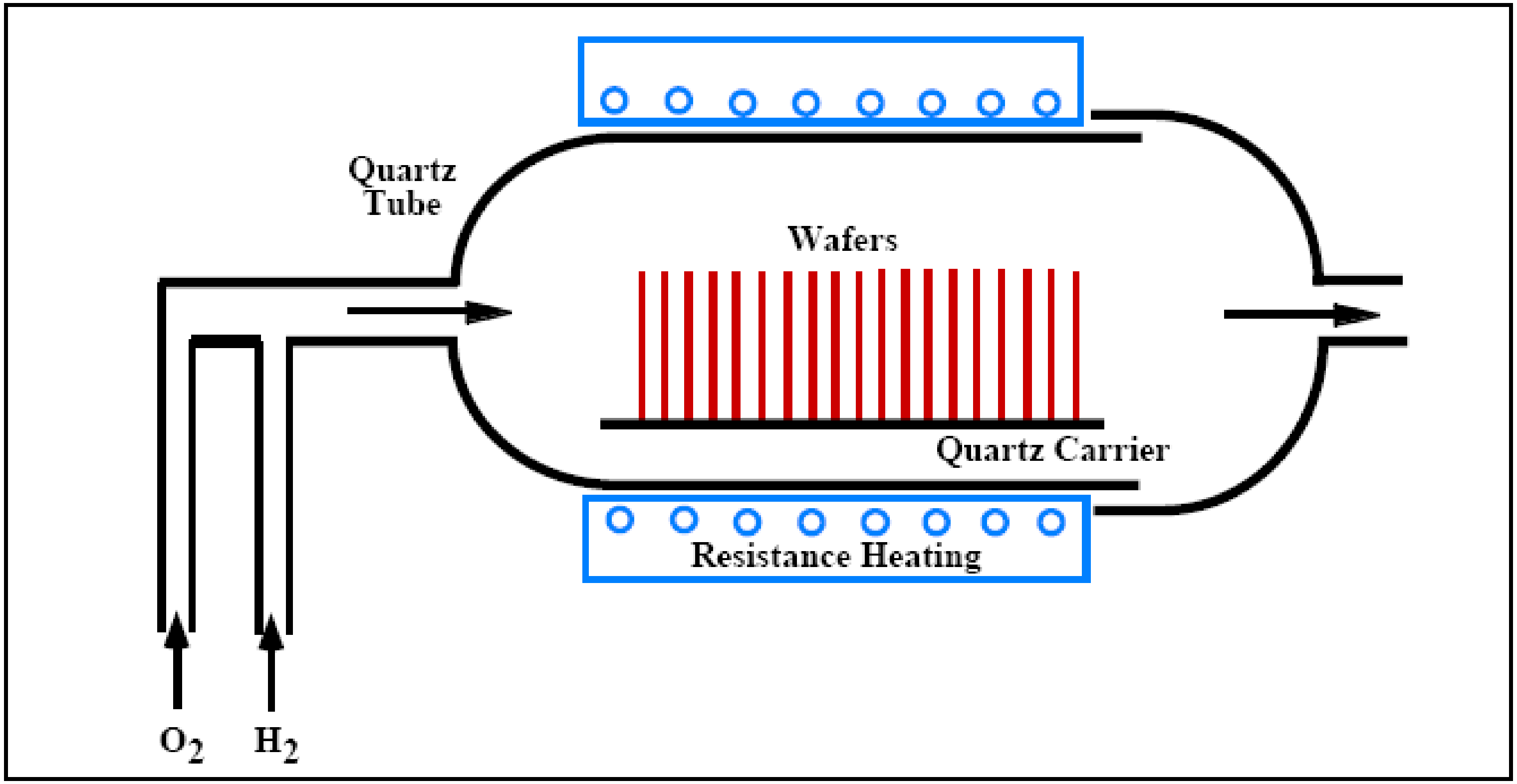

Ambient
O_2, H_2O
SiO_2
Diffusion
Reaction
Silicon
$Si + O_2 \rightarrow SiO_2$ or
$Si + 2H_2O \rightarrow SiO_2 + 2H_2$
1

- The oxide interface
  - The interface is very smooth.
  - The transition between the amorphous oxide and the crystalline Si is very abrupt.
  - These attributes make this Insulator/SC combo the best from a defect perspective



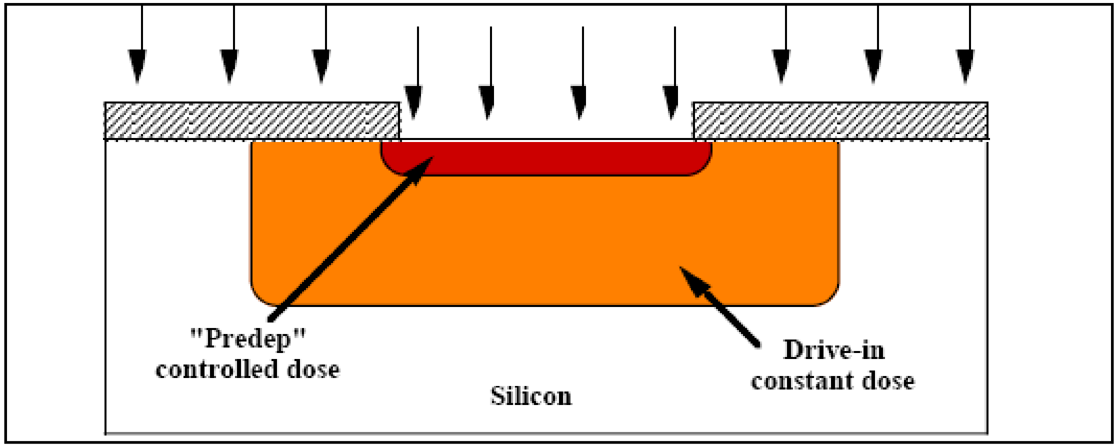
- Thermal Oxidation Processes
  - Two types
    - Dry → use O_2 only (higher quality)
    - Wet → use O_2 and H_2 (faster rate)
  - Temperatures
    - 600 to 1200ºC
    - Native oxide forms at room temperature
    - Growth rate is temp sensitive
      - 2X increase from 1000ºC to 1100ºC for wet oxidation
  - Pressure
    - Typically at atmospheric pressure
    - Higher Pressures → increased growth rate

- Typical Oxidation Furnace

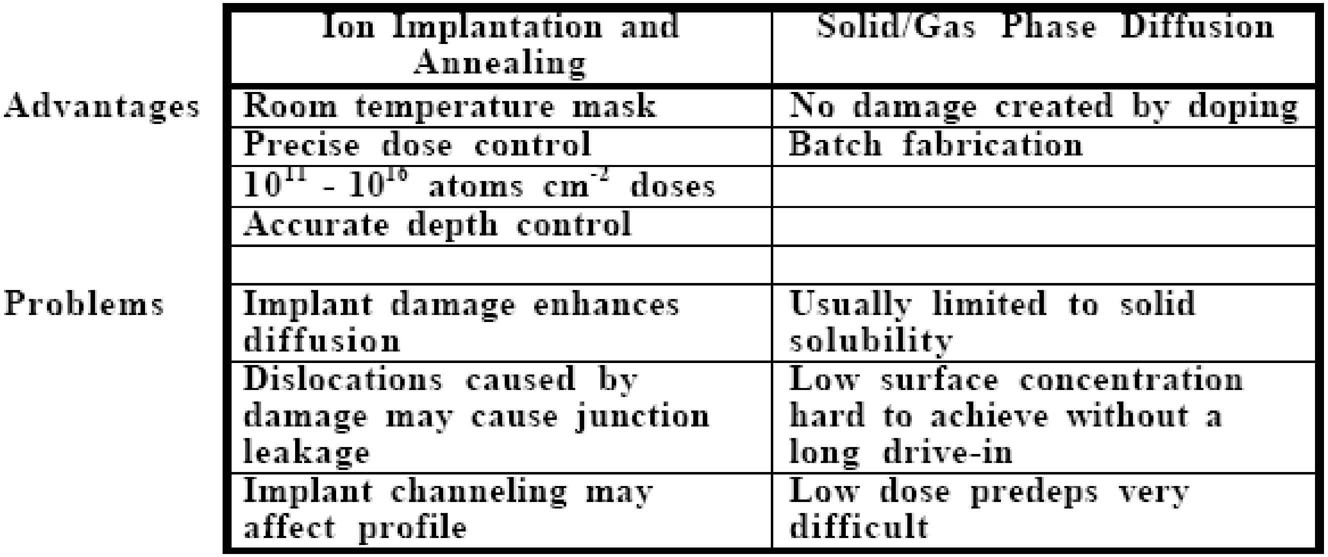

Quartz Tube
Wafers
Quartz Carrier
Resistance Heating
O_2
H_2

Diffusion

- Diffusion Basics
  - The redistribution of dopants from regions of high concentration to regions of low concentration
  - Exponential dependence on temperature
- Two-step Process
  - Pre-deposition: Introduce dopant to the surface of substrate
  - Drive-in: Redistribute dopant to the desired depth.


"Predep"
controlled dose
Drive-in
constant dose
Silicon

- Methods
  - Ion-implantation
  - Gaseous and solid source



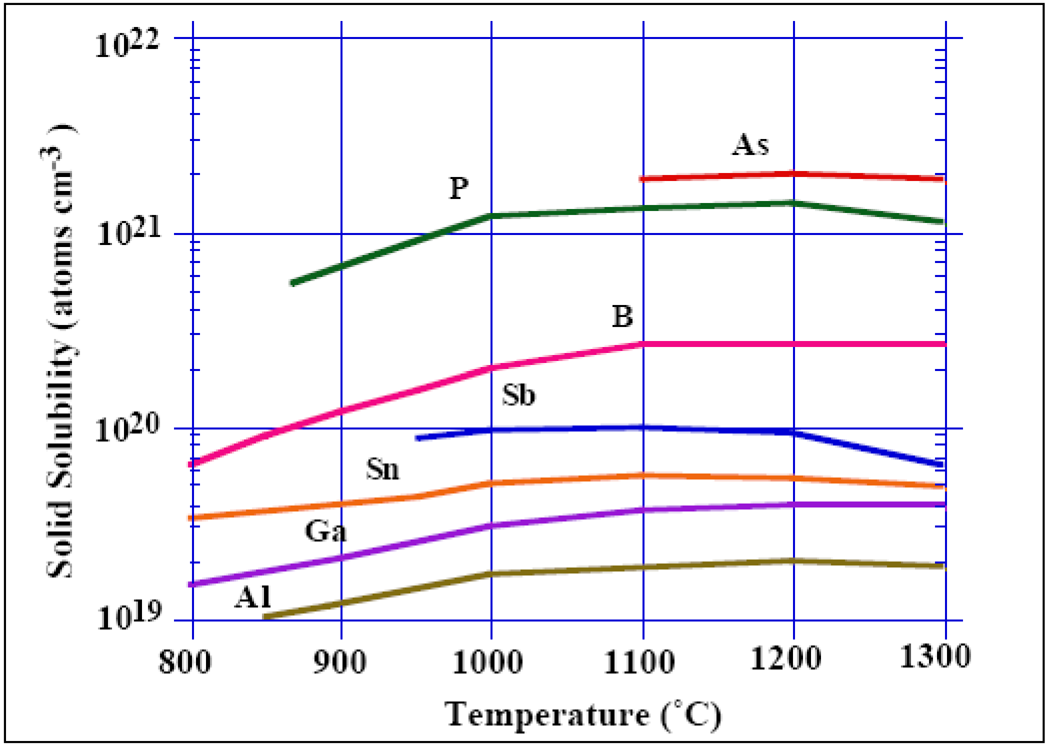
	Ion Implantation and Annealing	Solid/Gas Phase Diffusion
Advantages	Room temperature mask	No damage created by doping
	Precise dose control	Batch fabrication
	10^{11} - 10^{16} atoms cm^{-2} doses	
	Accurate depth control	
Problems	Implant damage enhances diffusion	Usually limited to solid solubility
	Dislocations caused by damage may cause junction leakage	Low surface concentration hard to achieve without a long drive-in
	Implant channeling may affect profile	Low dose predeps very difficult

- Solid Solubility
  - Definition: The maximum concentration of impurities in a substance without precipitating into another phase

It is temperature dependent

Notice As, P, B

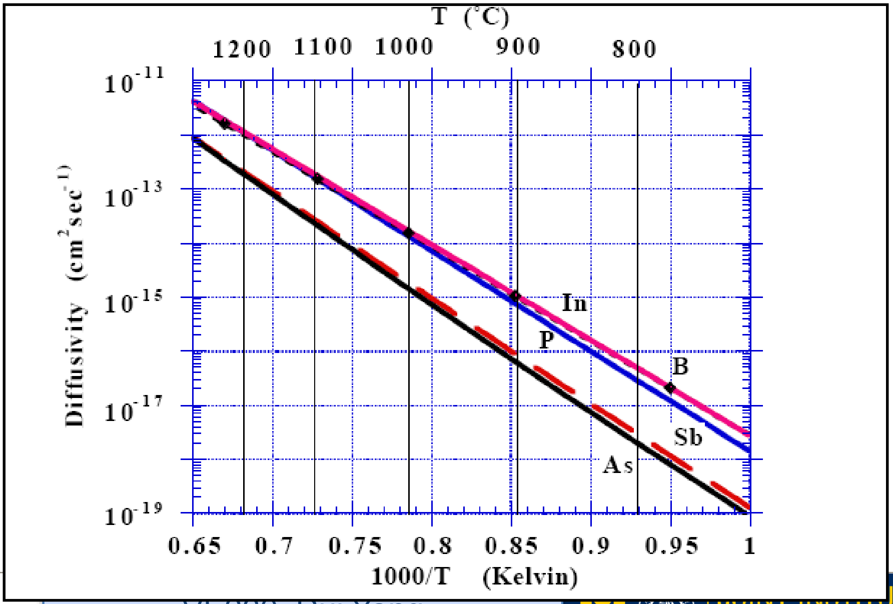
Electrical solubility can be different than solid solubility (smaller)



- Diffusivity
  - It is material and temperature dependent (not a

	Si	B	In	As	Sb	P	Units
D^0	560	1.0	1.2	9.17	4.58	4.70	$cm^2\ sec^{-1}$
E_A	4.76	3.5	3.5	3.99	3.88	3.68	eV

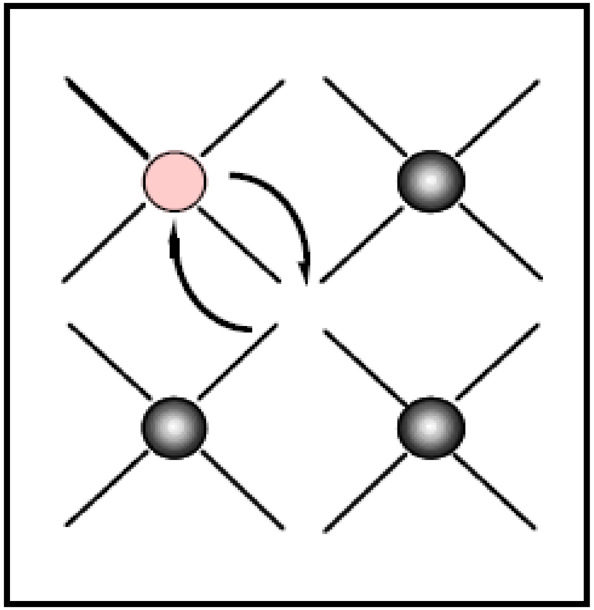
$$\boxed{D = D^0 \exp\left(\frac{-E_A}{kT}\right)}$$



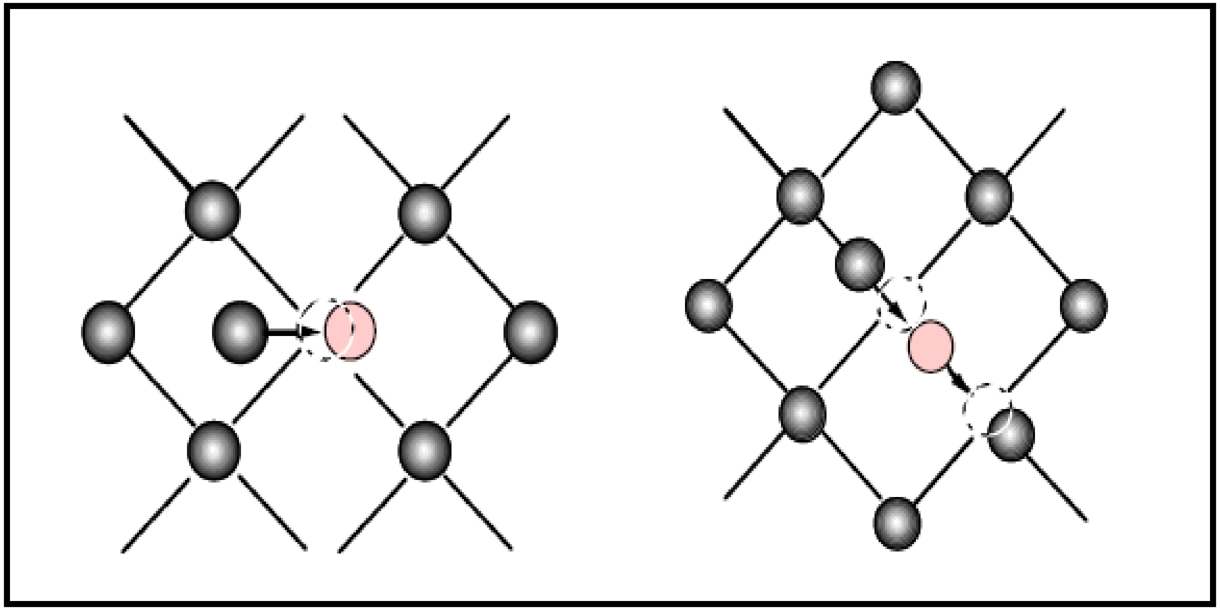
- Diffusion Processing Techniques
  - General Description
    - Requires high temp to be efficient (800 to 1100ºC)
  - Methods
    - Furnace
      - Batch Technique
      - Long processing times
      - Slow temperature ramps (5 to 100C/min)
      - Long temperature stabilization times
      - Excellent temperature control
    - Rapid Thermal Annealing
      - Single wafer systems
      - Short processing times
      - Fast temperature ramps (100C/sec)
      - Temperature control challenging

- Diffusion at the Atomic Scale
  - It relates to defects

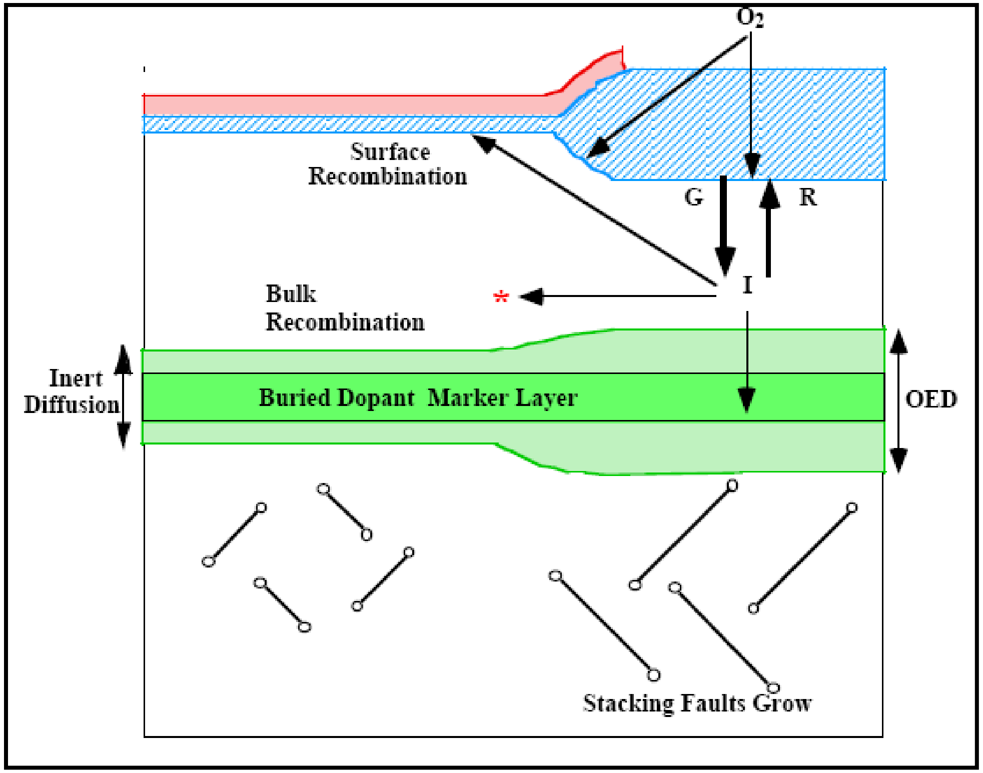
Vacancy Assisted



Interstitial Assisted – Kick out



- Defects and Processing
  - Oxidation → I
  - Nitridation → V

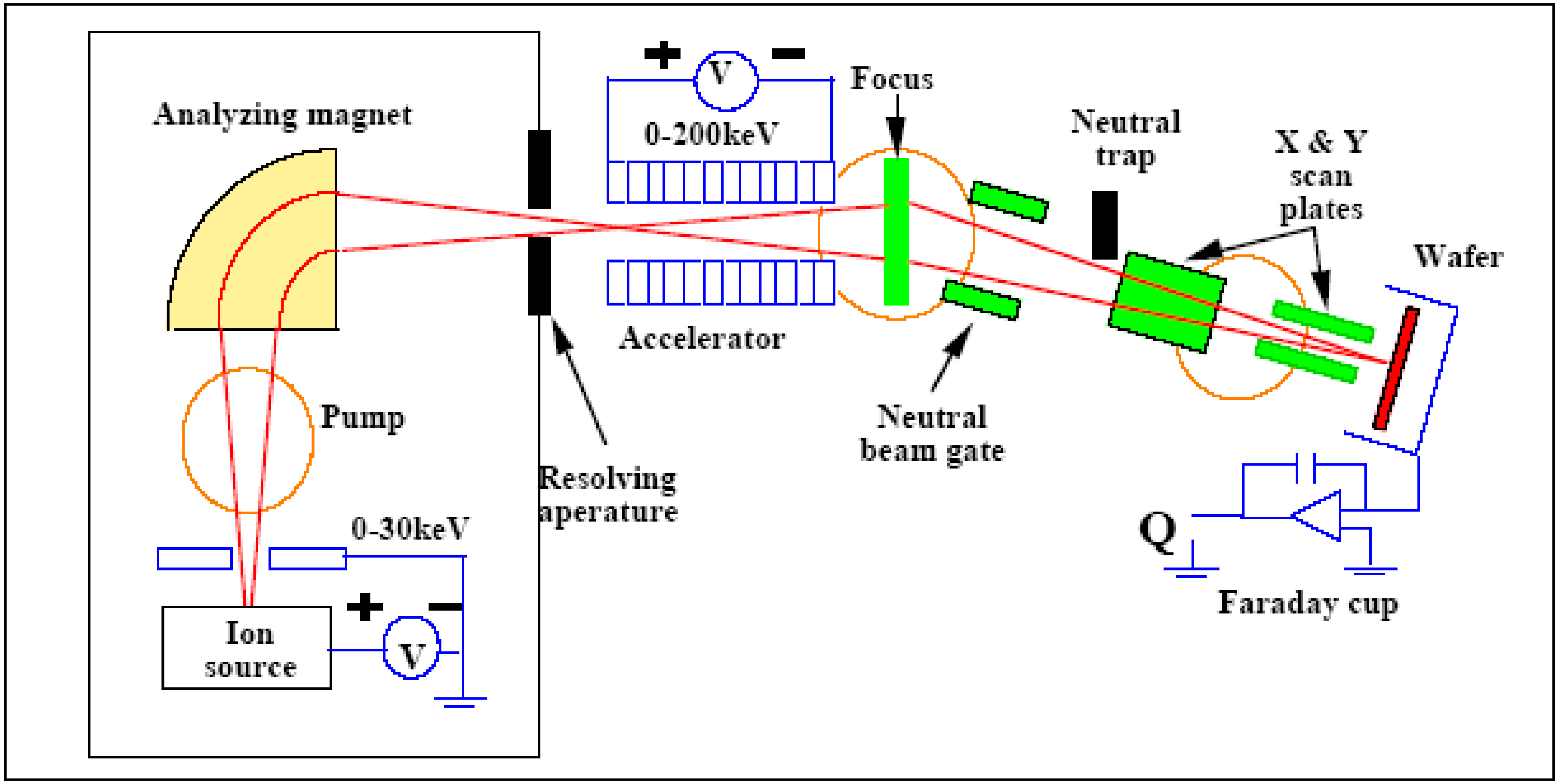


O_2
Surface Recombination
G
R
I
Bulk Recombination
*
Inert Diffusion
Buried Dopant Marker Layer
OED
Stacking Faults Grow

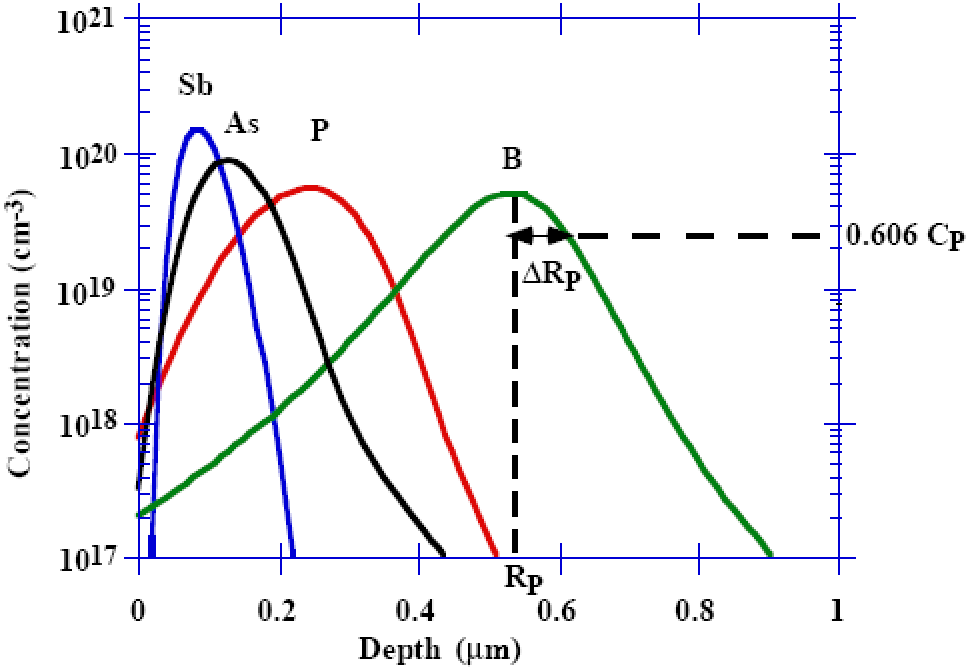
  - Oxygen enhanced diffusion
  - Oxygen retarded diffusion

Ion implantation

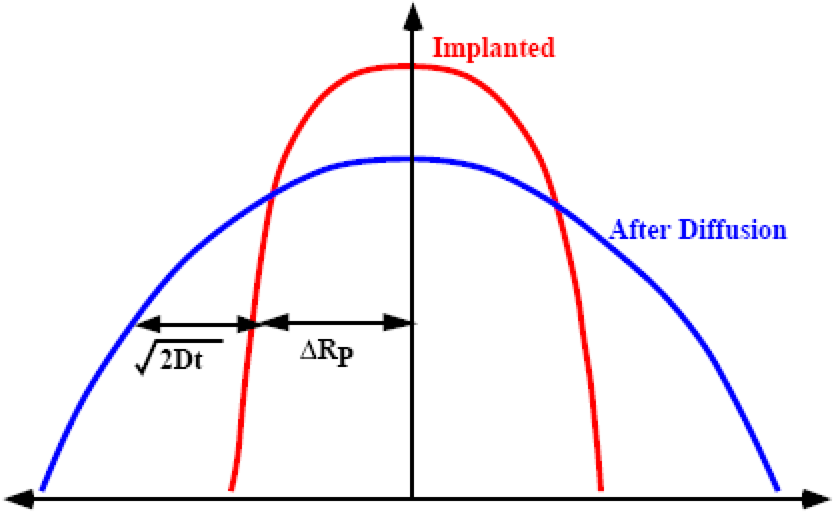
- Ion Implantation Equipment


Analyzing magnet
+ V −
0-200keV
Focus
Neutral trap
X & Y scan plates
Wafer
Accelerator
Pump
Neutral beam gate
Resolving aperature
0-30keV
Q
Faraday cup
Ion source
+ V −

- Implant Profiles

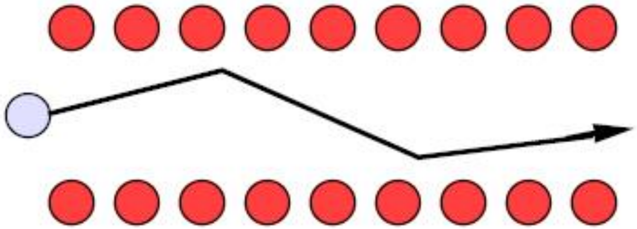


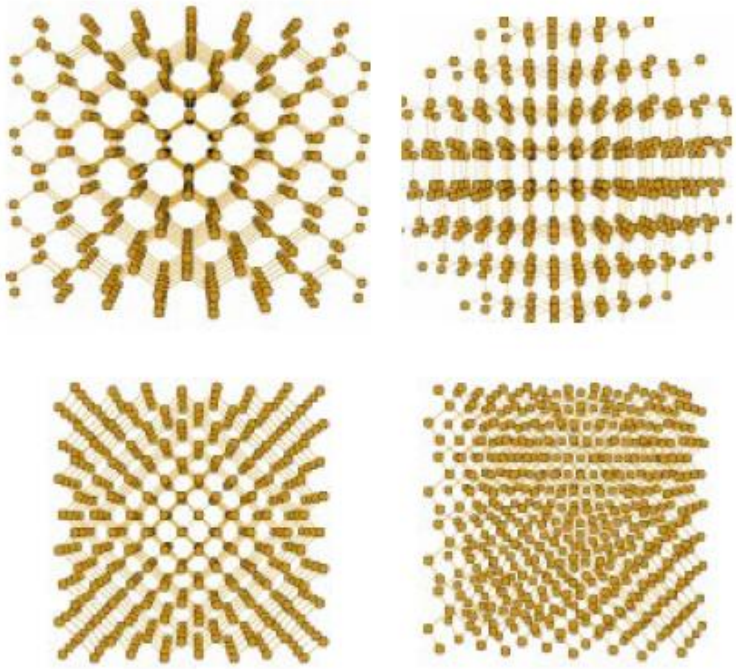
- Implantation and Annealing



$$C(x,t)=\frac{Q}{\sqrt{2\pi\left(\Delta R_P^2+2Dt\right)}}\exp\left(-\frac{\left(x-R_P\right)^2}{2\left(\Delta R_P^2+2Dt\right)}\right)$$

- Channeling
  - Effect related to ions moving thru a lattice
  - Results in deeper penetration of ions than would otherwise be predicted
  - Mitigation:
    - Tilt substrate (~ 7º)
    - Use amorphous overcoat (SiO_2)





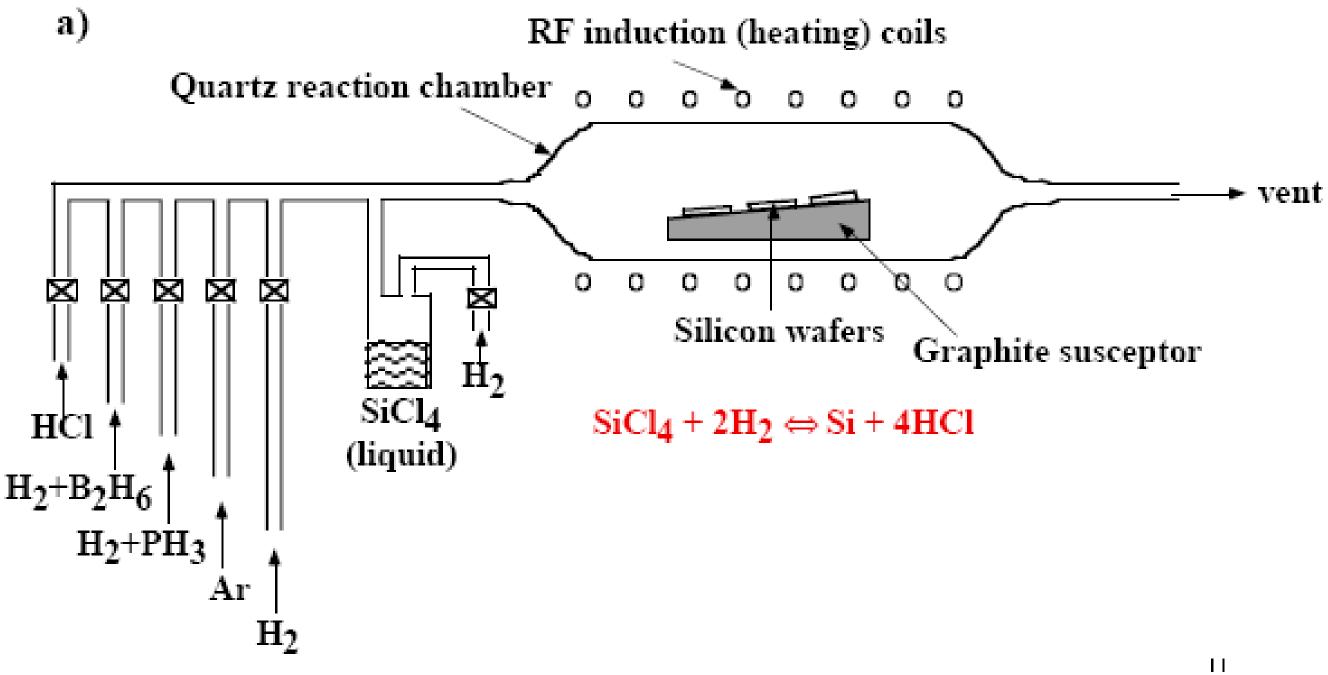
- Annealing
  - Goals
    - Remove primary implant damage
    - Activate dopants (substitutional sites)
    - Restore crystal structure of lattice
    - Restore carrier mobilities
    - Minimize dopant redistribution
  - Temperature regimes
    - Low temp (400ºC)
      - Vacancy complexes in bulk dissociate and annihilate interstitials

  - All vacancies are consumed, excess interstitials remain
  - These interstitials condense to form rod-like clusters, especially at temps above 400C.
  - These clusters lie on {311} planes forming ribbon-like planar defects
- Annealing above 900C causes dissociation of these defects, but only if below a critical threshold damage level.
  - Above this value, the defects actually grow to form dislocation loops (called secondary defects)
  - These can be thermally stable
  - Most likely to occur during high dose implanting
  - Most commonly found at boundary between amorphous and SC layer
  - Commonly called “End-of-Range” defects
  - Annealing these defects out results in the formation of interstitials

Thin film growth

- Deposition Categories
  - Chemical Vapor Deposition
    - APCVD, LPCVD, PECVD
  - Physical Vapor Deposition
    - Evaporation, sputtering
  - Spin Casting
    - viscous fluids
  - Dip coating
    - monolayers

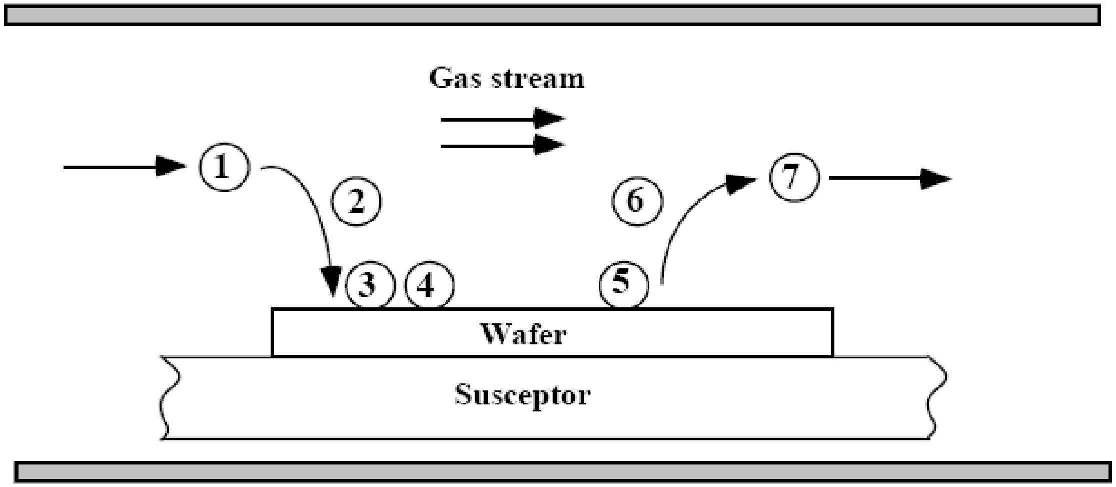
- Atmospheric Pressure Chemical Vapor Deposition
  - Typical System Setup


a)
RF induction (heating) coils
Quartz reaction chamber
vent
Silicon wafers
Graphite susceptor
HCl
H_2+B_2H_6
H_2+PH_3
Ar
H_2
$SiCl_4$
(liquid)
H_2

$$SiCl_4 + 2H_2 \Leftrightarrow Si + 4HCl$$

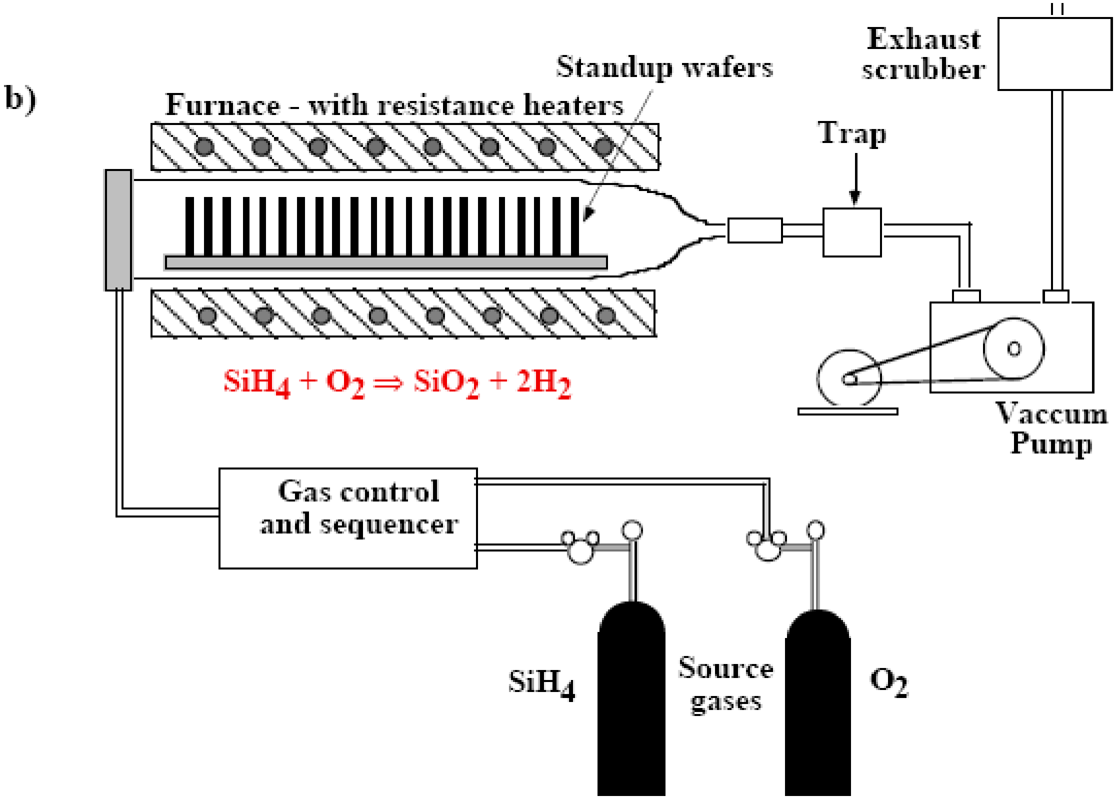
- APCVD
  - General Process
    - Transport of reactants through the main gas flow to the deposition region
    - Diffusion through the boundary layer to substrate surface
    - Absorption of reactants on substrate surface
    - Execution of surface reactions
      - Dissociation of reactants, surface migration, reactions
    - Desorption of byproducts
    - Transport of byproducts through boundary layer
    - Transport of byproducts through main gas flow

- General Process (continued)


Gas stream
①
②
③
④
⑤
⑥
⑦
Wafer
Susceptor

  - The process can be described in terms of fluxes
  - Deal-Grove applies and can be used to determine deposition rates

- Low Pressure Chemical Vapor Deposition Setup
  - Typical System Setup

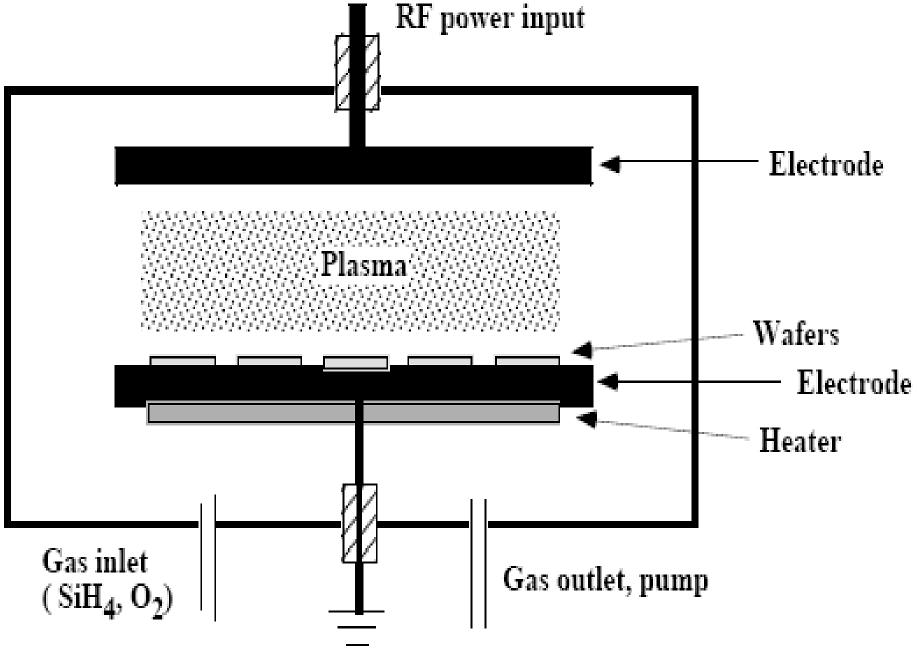

b)
Furnace - with resistance heaters
Standup wafers
Exhaust scrubber
Trap
Vaccum Pump
Gas control and sequencer
SiH4
Source gases
O2

$SiH_4 + O_2 \Rightarrow SiO_2 + 2H_2$

- Why LPCVD?
  - APCVD operates in mass transport limited regime
    - Requires control of geometry to ensure uniformity
  - Could switch to surface reaction regime by lowering temperature
    - Deposition rate goes down
    - Film quality suffers at the lower temps
  - Lowering pressure addresses these issues
    - Increases diffusion
    - Extends reaction rate regime to higher temps

- Plasma Enhanced Chemical Vapor Deposition

1. Low pressures: 50 mTorr to 5 Torr
2. 13.56 MHz
3. High field
4. High energy electrons strike gas molecules and ionize them. Low pressures insure high collision energies

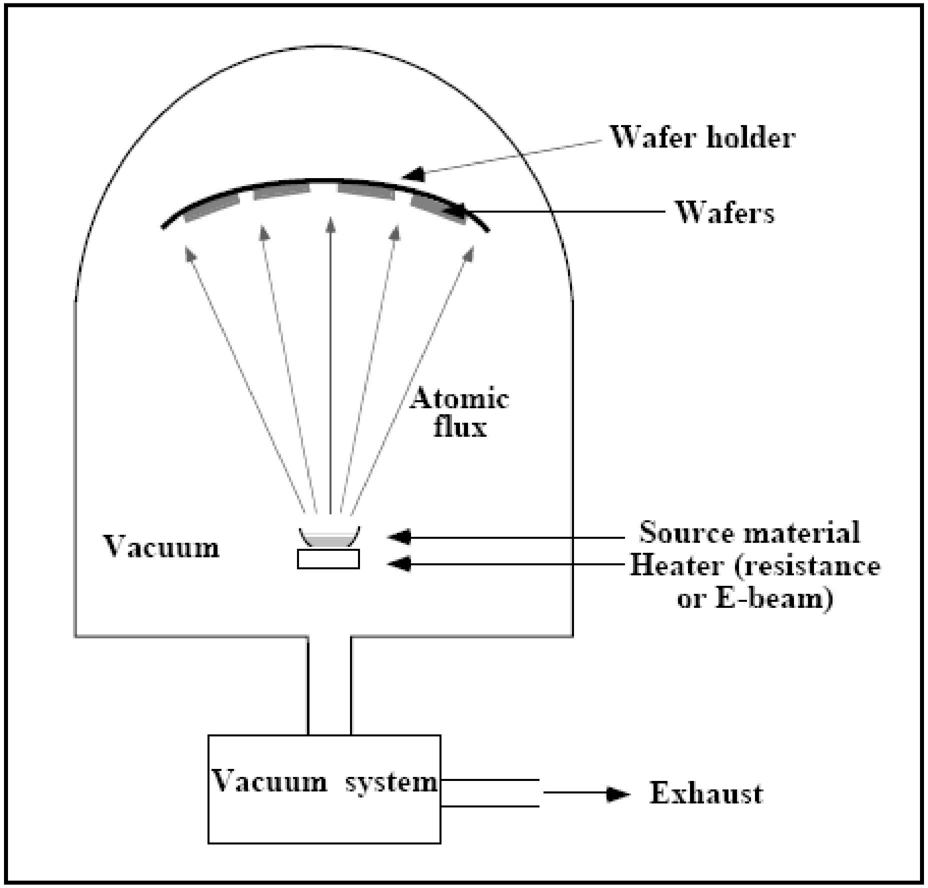

RF power input
Electrode
Plasma
Wafers
Electrode
Heater
Gas inlet
(SiH_4, O_2)
Gas outlet, pump

- PECVD
  - Much like LPCVD but uses a plasma discharge as a source of energy
    - Results in lowering of substrate temperature
  - What is a plasma?
    - An energetic gaseous collection of electrons charged molecules, neutral molecules, neutral and charged molecular fragments of energetically excited molecules and free radicals
    - Free radicals → electrically neutral species that have incomplete chemical bonds

- Physical Vapor Deposition (PVD)
  - Relies on physical processes to produce reactants
    - Evaporation
    - Sputtering
  - Requires long mean free path to insure the following:
    - Reactions don’t occur in gas phase
    - Physical processes have maximum available energy
    - Reactants have maximum energy when adsorbed on surface.
  - Generally lower temperature process than CVD
  - Popular for metals

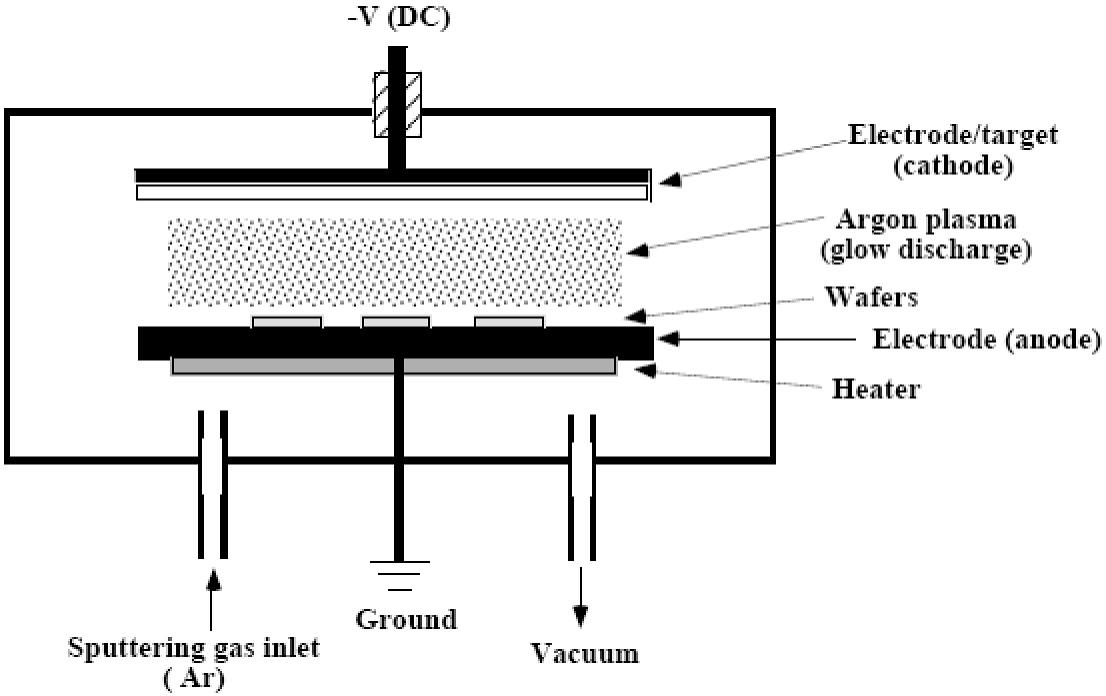
- Evaporation
  - Source material heated in vacuum
    - Resistance heating
      - Heats entire source
    - Electron beam heater
      - Higher temperatures
      - Localized heating (near source surface)
      - Produces x-rays
    - Vacuum assures the following:
      - High purity (many metals are reactive with oxygen)
      - Long mean free path (reactants have straight line path from source to target

- Evaporation
  - System Schematic

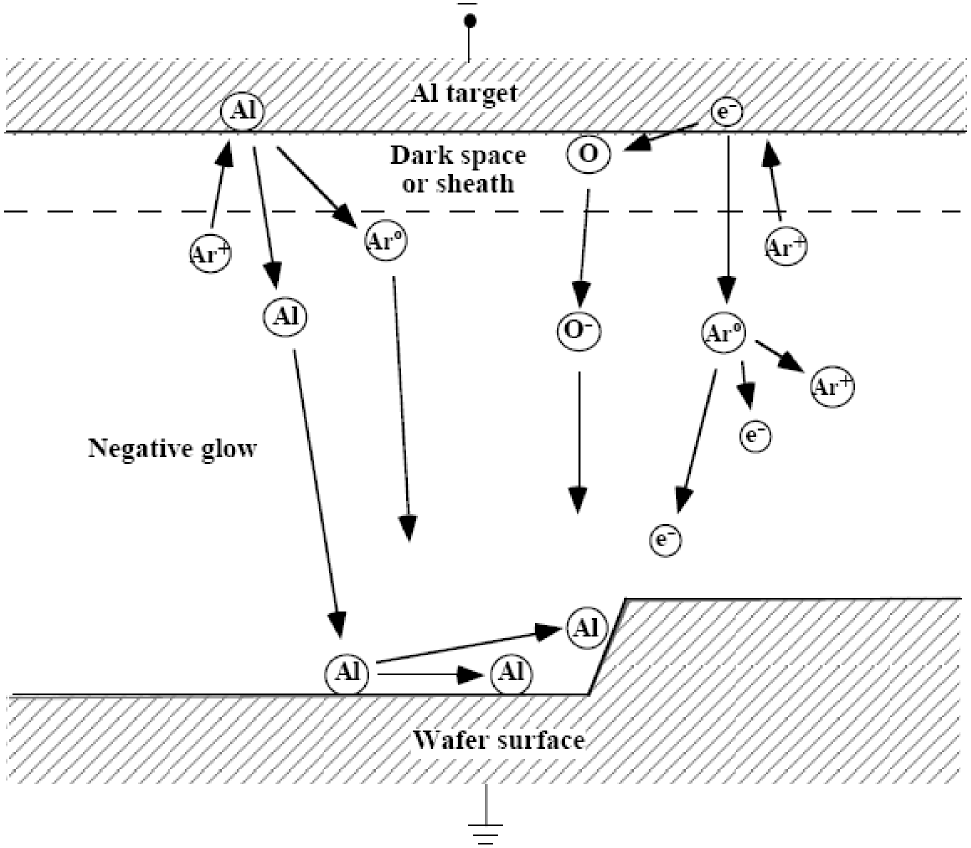

Wafer holder
Wafers
Atomic flux
Vacuum
Source material
Heater (resistance or E-beam)
Vacuum system
Exhaust

- Sputtering
  - Uses plasma to generate energetic ions that bombard a target to liberate reactants that are used to form a film
  - Two types
    - DC Sputtering → conductive targets
    - RF Sputtering → insulating targets
  - Uses vacuum, but usually higher pressures than evaporation (10 to 1000 mTorr)

- Sputtering
  - General System Schematic

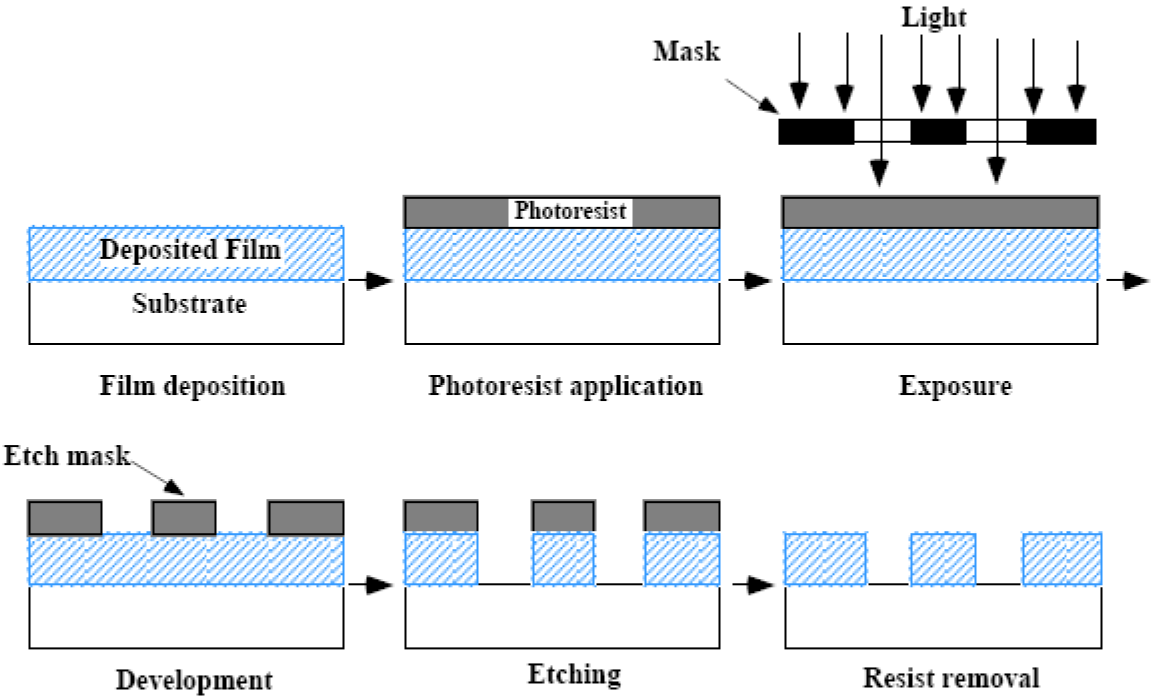

-V (DC)
Electrode/target (cathode)
Argon plasma (glow discharge)
Wafers
Electrode (anode)
Heater
Sputtering gas inlet (Ar)
Ground
Vacuum

- Sputtering: General Processes

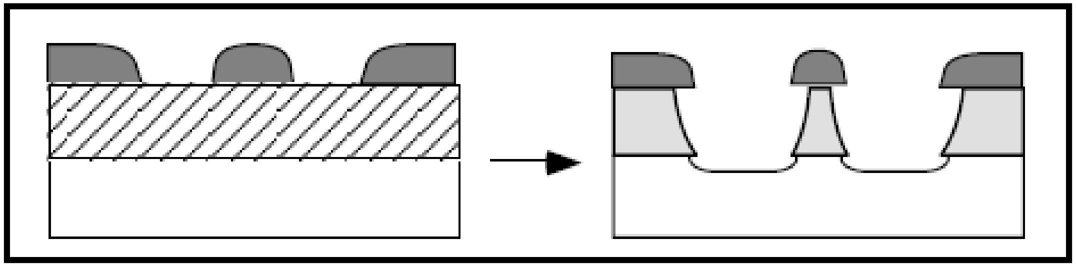

Al target
Al
e-
O
Dark space
or sheath
Ar+
Ar°
Ar+
Al
O-
Ar°
Ar+
e-
e-
Negative glow
Al
Al
Al
Wafer surface

Etching

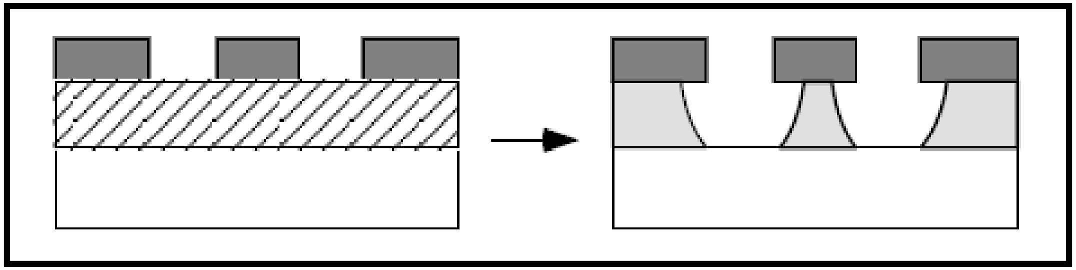
- Main Use – To create structures in substrate or thin film


Light
Mask
Deposited Film
Substrate
Photoresist
Film deposition
Photoresist application
Exposure
Etch mask
Development
Etching
Resist removal

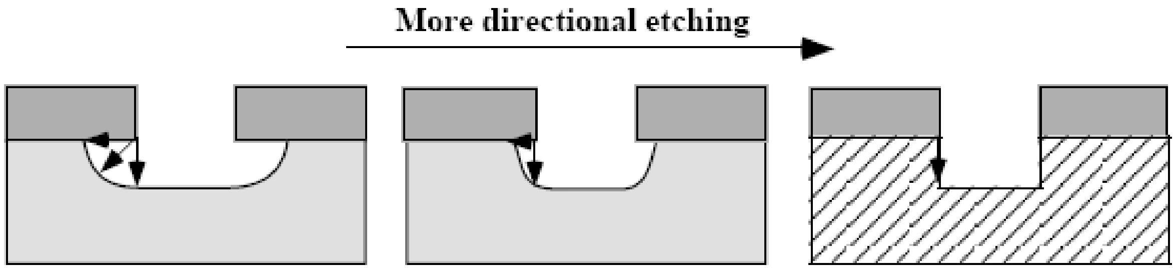
- Issues
  - Selectivity
    - Driven by chemistry



  - Directionality
    - Driven by physics



- Isotropy
  - A measure of etch directionality

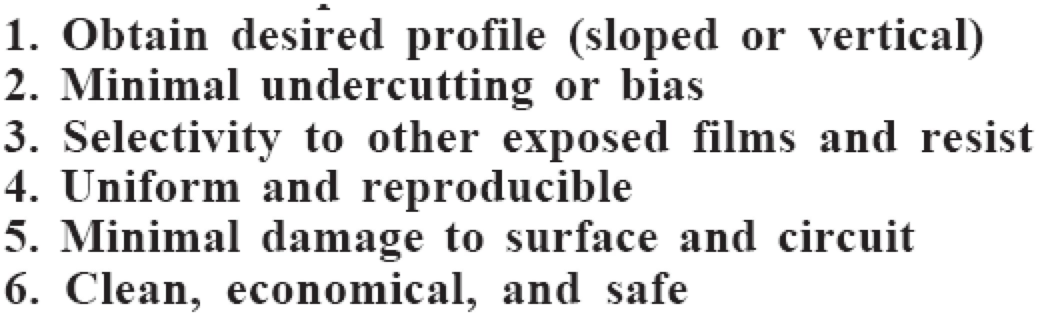


a) isotropic

b) anisotropic

c) completely anisotropic

- General Requirements



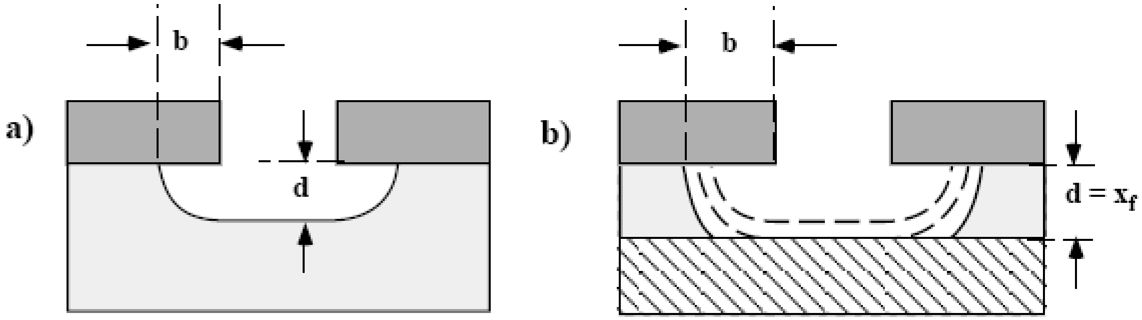
1. Obtain desired profile (sloped or vertical)
2. Minimal undercutting or bias
3. Selectivity to other exposed films and resist
4. Uniform and reproducible
5. Minimal damage to surface and circuit
6. Clean, economical, and safe

- Wet Chemical Etching
  - Immersion into aqueous solutions
  - Characteristics
    - Isotropic
    - Highly selective
  - Examples
    - SiO_2
    - Si

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2$$

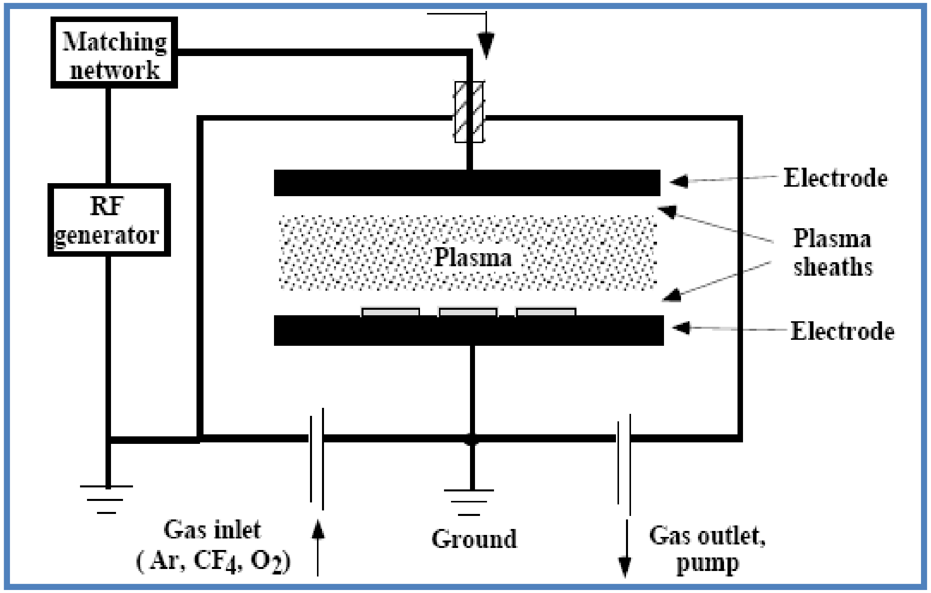
- Wet Chemical Etching
  - Undercutting
    - Due to isotropic nature of etch
    - Can be quantified in terms of anisotropy

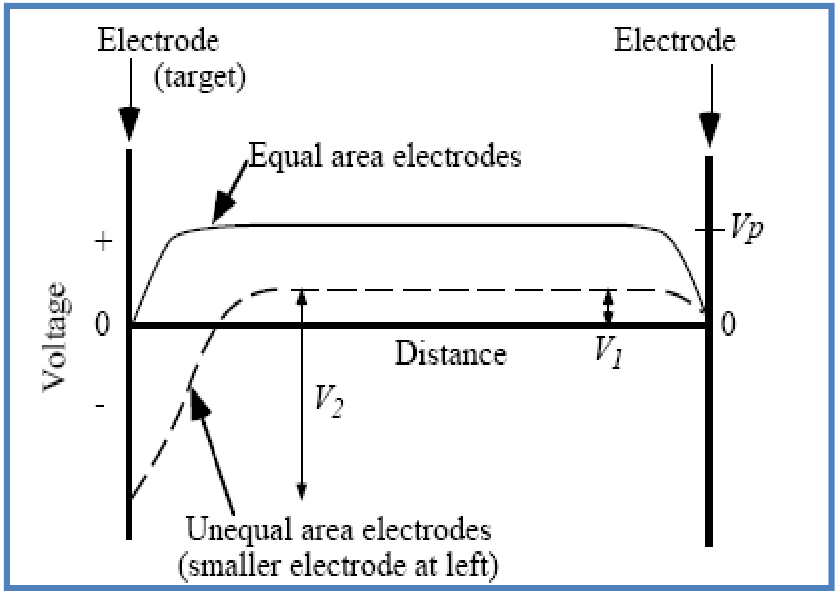


$$A_f = 1 - \frac{r_{lat}}{r_{ver}} = 1 - \frac{b}{d}$$

- Dry Etching
  - Addresses key issues related to patterning of small features on complex substrates
    - High anisotropy
    - High selectivity
    - High etch rate
  - Uses plasmas as an alternative to dry etching

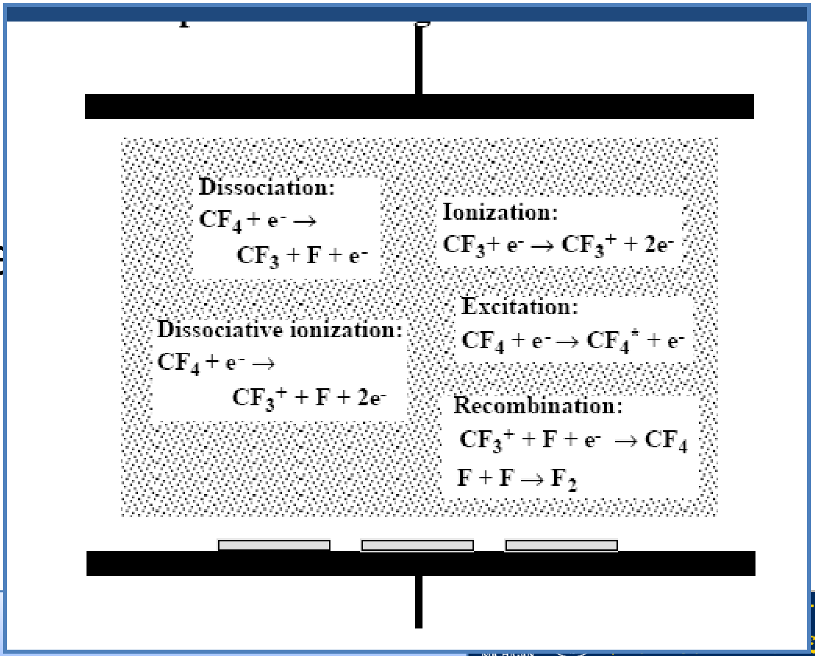
- Dry etching
  - Looks a lot like sputtering!
  - Use reactive gases that attack substrate
  - Configured to suppress sputtering


Matching network
RF generator
Plasma
Electrode
Plasma sheaths
Electrode
Gas inlet (Ar, CF4, O2)
Ground
Gas outlet, pump

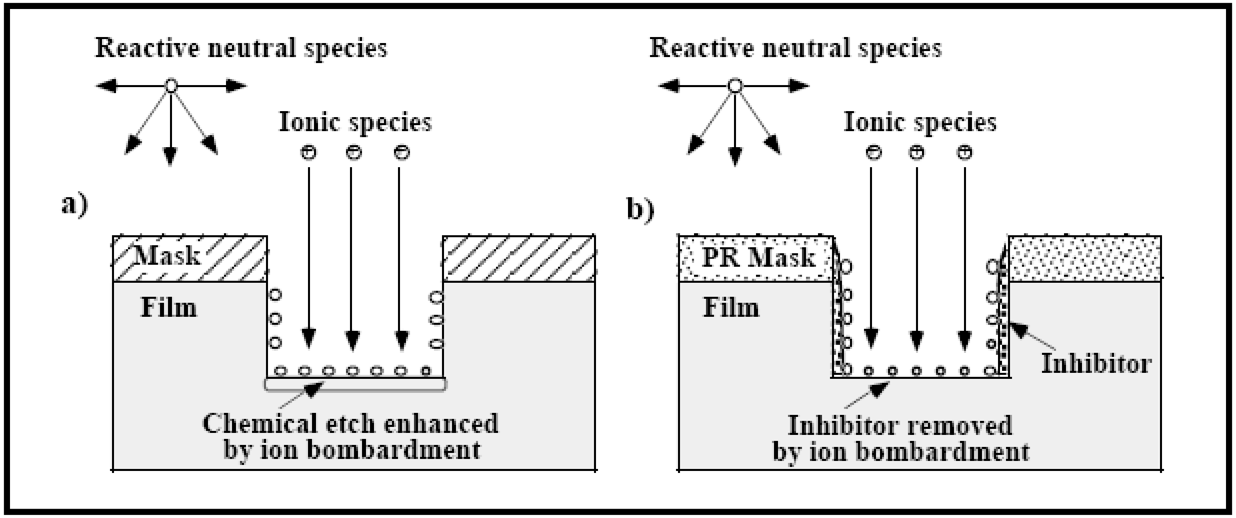


- Dry Etching
  - General process description
    - V_P is positive to equalize ion and electron fluxes
    - Electrode are of unequal size to enhance field density
    - Reactive gases
      - For Si and Si-derivatives, gaseous halides are used as reactive gases (CF_4, SF_6, HBr, Cl_2, etc)
      - Additives such as O_2, Ar, He sometimes used
      - O_2 alone used to etch carbon-based films (i.e., PR)

- Dry Etching
  - Two species involved in etching (reactive neutrals and ions)
    - Density of neutrals = $10^{15}/cm^3$ (10% free radicals)
    - Density of charged particles = 10^8 to 10^{12} $/cm^3$
  - In general, power related to plasma density
  - Mechanisms
    - Chemical
      - Isotropic, selective
    - Physical
      - Anisotropic, less selective
    - Ion enhanced
      - Anisotropic, selective

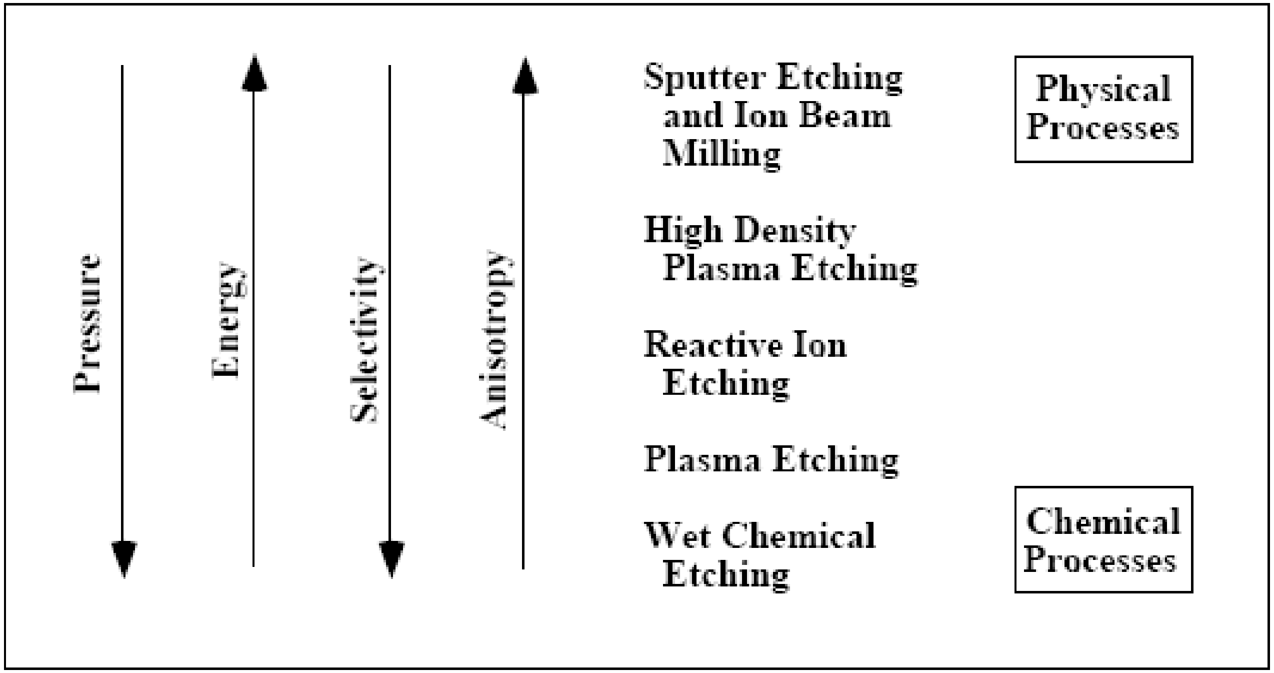

Dissociation:
$CF_4 + e^- \rightarrow CF_3 + F + e^-$
Ionization:
$CF_3 + e^- \rightarrow CF_3^+ + 2e^-$
Excitation:
$CF_4 + e^- \rightarrow CF_4^* + e^-$
Dissociative ionization:
$CF_4 + e^- \rightarrow CF_3^+ + F + 2e^-$
Recombination:
$CF_3^+ + F + e^- \rightarrow CF_4$
$F + F \rightarrow F_2$

- Dry Etching
  - Ion enhanced etching
    - Characteristics
      - Anisotropic (due to ion flux)
      - Selective (due to chemical etch component)
      - High etch rate (due to combination)
    - Proposed mechanisms

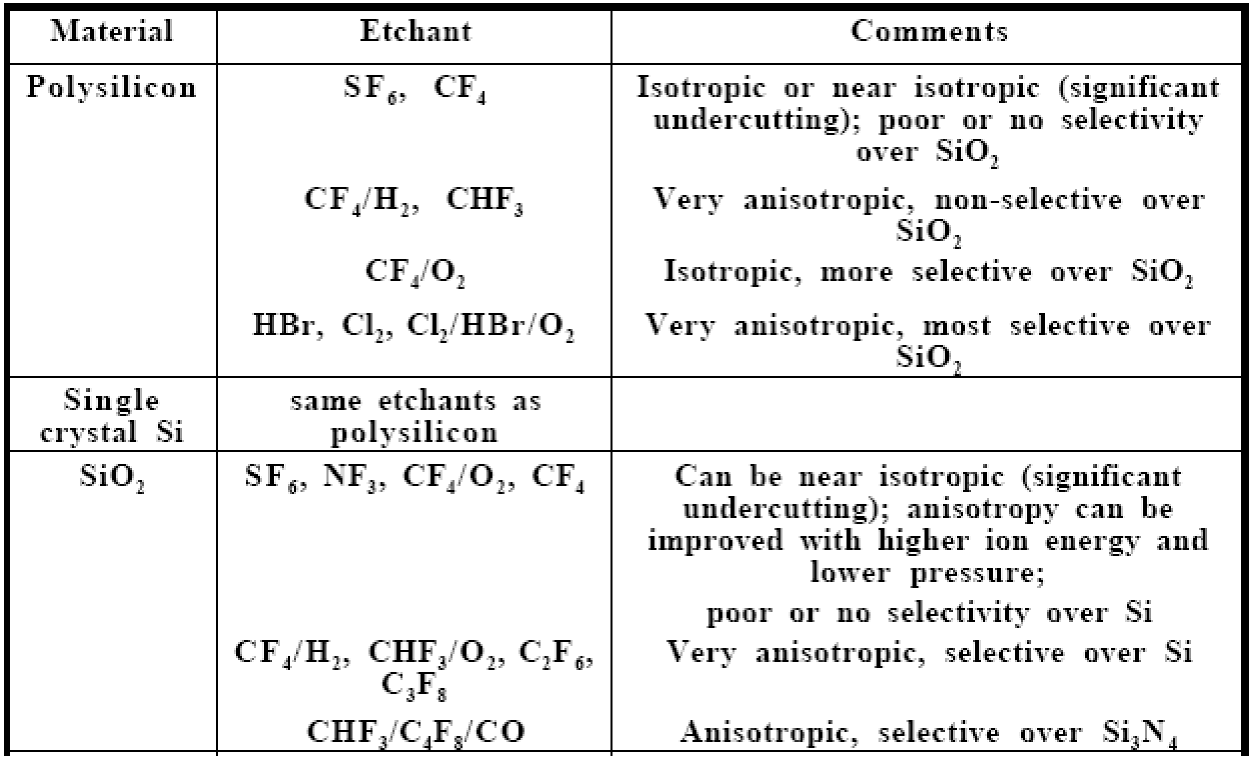

Reactive neutral species
Ionic species
a)
Mask
Film
Chemical etch enhanced by ion bombardment
Reactive neutral species
Ionic species
b)
PR Mask
Film
Inhibitor
Inhibitor removed by ion bombardment

- Dry Etching
  - Etching tools
    - Parallel Plate Etcher
      - Can operate in two modes
        - Plasma Mode
        - Reactive Ion Etching Mode
      - Plasma Mode
        - Electrodes are of the same size or substrate electrode is larger
        - Leads to moderate sheath voltages (1 to 100 eV), thus ion energy is modest → etching mostly chemical
      - RIE Mode
        - Wafers sit on smaller electrode
        - Large ion component with significant energy (100 to 700 eV)
        - Lower pressures than plasma etching (mTorr versus Torr)

- Summary of Etch Process Characteristics


Pressure
Energy
Selectivity
Anisotropy
Sputter Etching and Ion Beam Milling
High Density Plasma Etching
Reactive Ion Etching
Plasma Etching
Wet Chemical Etching
Physical Processes
Chemical Processes

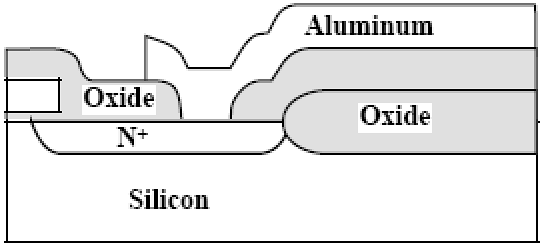
- Actual Etch Processes
  - Si, SiO_2

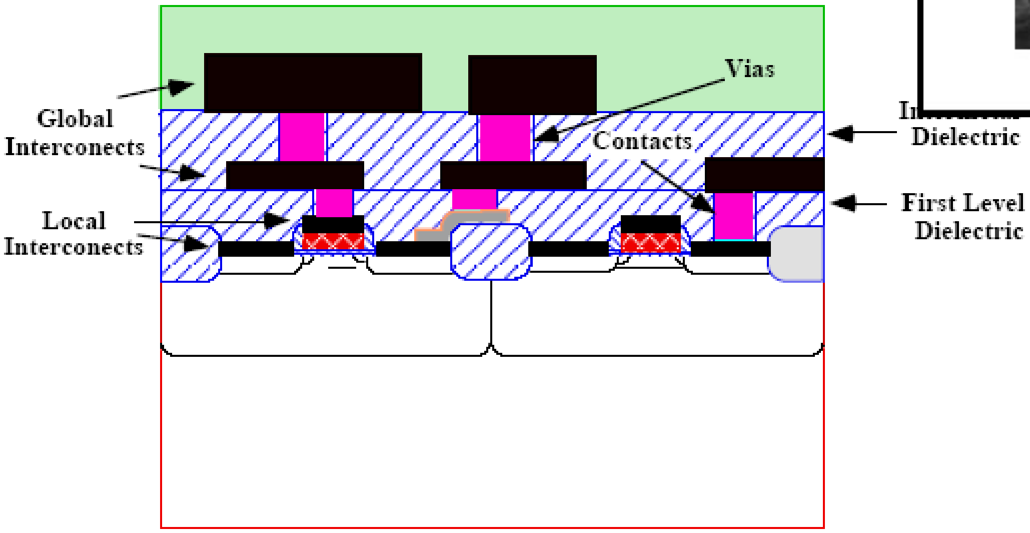


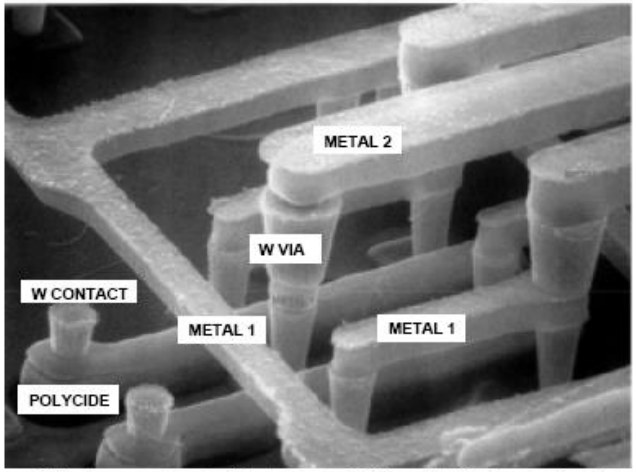
Material	Etchant	Comments
Polysilicon	SF_6, CF_4	Isotropic or near isotropic (significant undercutting); poor or no selectivity over SiO_2
	CF_4/H_2, CHF_3	Very anisotropic, non-selective over SiO_2
	CF_4/O_2	Isotropic, more selective over SiO_2
	HBr, Cl_2, $Cl_2/HBr/O_2$	Very anisotropic, most selective over SiO_2
Single crystal Si	same etchants as polysilicon	
SiO_2	SF_6, NF_3, CF_4/O_2, CF_4	Can be near isotropic (significant undercutting); anisotropy can be improved with higher ion energy and lower pressure; poor or no selectivity over Si
	CF_4/H_2, CHF_3/O_2, C_2F_6, C_3F_8	Very anisotropic, selective over Si
	$CHF_3/C_4F_8/CO$	Anisotropic, selective over Si_3N_4

Back end processing

- Metal interconnects


Aluminum
Oxide
Oxide
N+
Silicon


Vias
Global
Interconnects
Contacts
Local
Interconnects
In
Dielectric
First Level
Dielectric


METAL 2
W VIA
W CONTACT
METAL 1
METAL 1
POLYCIDE

(Photo courtest of Integrated Circuit Engineering.)