



HW7

5.2.1-3

Exercise 5.2

In this exercise we look at memory locality properties of matrix computation. The following code is written in C, where elements within the same row are stored contiguously.

a.	<pre>for (I=0; I<8000; I++) for (J=0; J<8; J++) A[I][J]=B[J][0]+A[J][I];</pre>
b.	<pre>for (J=0; J<8; J++) for (I=0; I<8000; I++) A[I][J]=B[J][0]+A[J][I];</pre>

5.2.1 [5] <5.1> How many 32-bit integers can be stored in a 16-byte cache line?

5.2.2 [5] <5.1> References to which variables exhibit temporal locality?

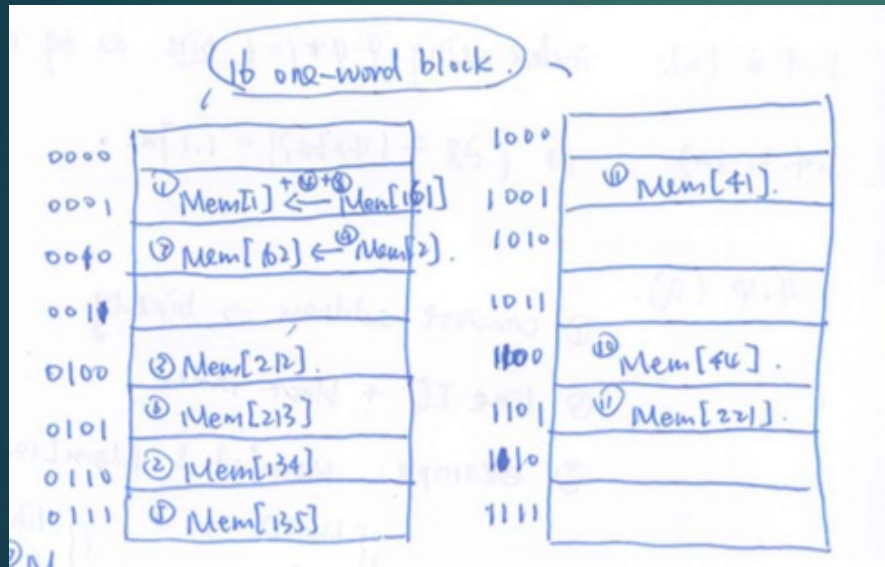
5.2.3 [5] <5.1> References to which variables exhibit spatial locality?

4 integers

temporal: (a) I, J (b) I, J, B[J][0]

Spatial: (a) A[I][J] (b) A[J][I]

5.3.1-4



Exercise 5.3

Caches are important to providing a high performance memory hierarchy to processors. Below is a list of 32-bit memory address references, given as word addresses.

a.	1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221
b.	6, 214, 175, 214, 6, 84, 65, 174, 64, 105, 85, 215

5.3.1 [10] <5.2> For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

5.3.2 [10] <5.2> For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of eight blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

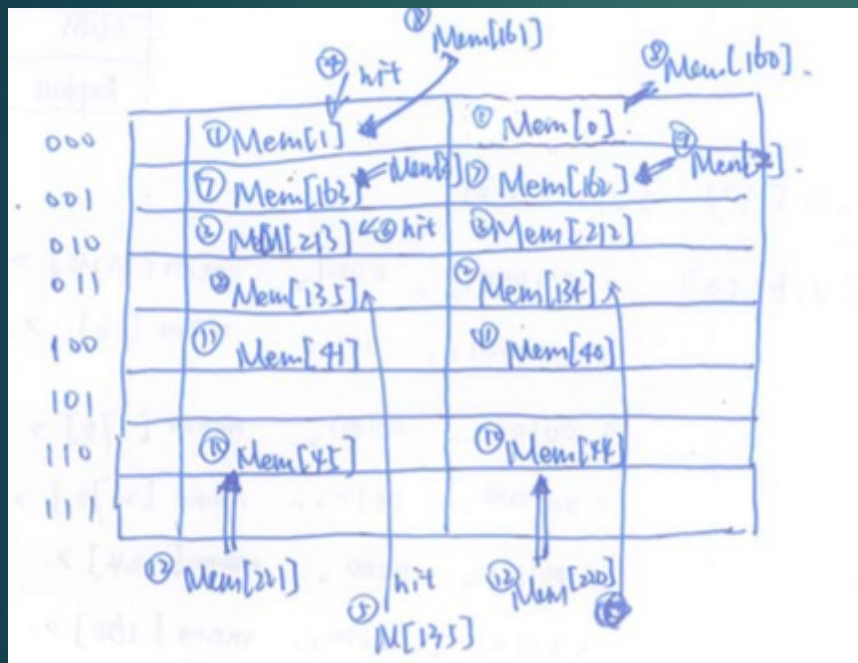
5.3.3 [20] <5.2, 5.3> You are asked to optimize a cache design for the given references. There are three direct-mapped cache designs possible, all with a total of eight words of data: C1 has one-word blocks, C2 has two-word blocks, and C3 has four-word blocks. In terms of miss rate, which cache design is the best? If the miss stall time is 25 cycles, and C1 has an access time of 2 cycles, C2 takes 3 cycles, and C3 takes 5 cycles, which is the best cache design?

There are many different design parameters that are important in cache design. The overall miss rate and the access time of the cache are the most important.

5.3.1

a.	Binary address: $1_2, 10000110_2, 11010100_2, 1_2, 10000111_2, 11010101_2, 10100010_2, 10100001_2, 10_2, 101100_2, 101001_2, 11011101_2$ Tag: Binary address $\gg 4$ bits Index: Binary address mod 16 Hit/Miss: M, M, M, H, M, M, M, M, M, M, M, M
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5.3.1-4



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There are many different design parameters that are important to a cache's overall performance. The table below lists parameters that are important to a cache's overall performance.

5.3.2

- a.** Binary address: $1_2, 10000110_2, 11010100_2, 1_2, 10000111_2, 11010101_2, 10100010_2, 10100001_2, 10_2, 101100_2, 101001_2, 11011101_2$
 Tag: Binary address $\gg 3$ bits
 Index: (Binary address $\gg 1$ bit) mod 8
 Hit/Miss: M, M, M, H, H, H, M, M, M, M, M, M

5.3.1-4

C1: 1 hit, C2: 3 hits, C4: 2 hits.

C1: Stall time = $25 \times 11 + 2 \times 12 = 299$

C2: Stall time = $25 \times 9 + 3 \times 12 = 261$

C3: Stall time = $25 \times 10 + 5 \times 12 = 310$

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There are many different design parameters that are important to a cache's overall performance. The table below lists parameters for different direct-mapped cache designs.

	Cache data size	Cache block size	Cache access time
a.	64 KB	1 word	1 cycle
b.	64 KB	2 word	2 cycle

5.3.4 [15] <5.2> Calculate the total number of bits required for the cache listed in the table, assuming a 32-bit address. Given that total size, find the total size

5.3.4

There are many different design parameters that are important to a cache's overall performance. The table below lists parameters for different direct-mapped cache designs.

	Cache data size	Cache block size	Cache access time
a.	64 KB	1 word	
b.	64 KB	2 word	1 cycle
			2 cycle

5.3.4 [15] <5.2> Calculate the total number of bits required for the cache listed in the table, assuming a 32-bit address. Given that total size, find the total size

of the closest direct-mapped cache with 16-word blocks of equal size or greater. Explain why the second cache, despite its larger data size, might provide slower performance than the first cache.

5.3.4

- a.** Using equation on page 351, $n = 14$ bits, $m = 0$ (1 word per block)
 $2^{14} \times (2^0 \times 32 + (32 - 14 - 0 - 2) + 1) = 802$ Kbits
Calculating for 16 word blocks, $m = 4$, if $n = 10$ then the cache is 541 Kbits, and if $n = 11$ then the cache is 1 Mbit. Thus the cache has 128 KB of data.
The larger cache may have a longer access time, leading to lower performance.

Cache Size in Bits

- Given
 - 32-bit byte address
 - 2^n blocks in cache
 - 2^m words per block, 2^{m+2} bytes
- Size of tag field = $32 - (n + m + 2)$
 - n bits to index blocks in cache
 - m bits used to select words in a block
 - 2 bits used to select the 4 bytes in a word
 - Tag field decreases when n and m increase
- Cache size = $2^n \times (\text{block size} + \text{tag size} + \text{valid field size})$

5.4.1-3

$$1. 2^2 = 4$$

$$2. 2^6 = 64$$

$$3. 1 + (23/4/32) = 1.18$$

Exercise 5.4

For a direct-mapped cache design with 32-bit address, the following bits of the address are used to access the cache.

	Tag	Index	Offset
a.	31-10	9-4	3-0
b.	31-12	11-15	4-0

5.4.1 [5] <5.2> What is the cache line size (in words)?

5.4.2 [5] <5.2> How many entries does the cache have?

5.4.3 [5] <5.2> What is the ratio between total bits required for such a cache implementation over the data storage bits?

Starting from power on, the following byte-addressed cache references are recorded.

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
---------	---	---	----	-----	-----	-----	------	----	-----	------	-----	------

5.4.4 [10] <5.2> How many blocks are replaced?

5.4.5 [10] <5.2> What is the hit ratio?

5.4.4-6

Starting from power on, the following byte-addressed cache references are recorded.

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
---------	---	---	----	-----	-----	-----	------	----	-----	------	-----	------

5.4.4 [10] <5.2> How many blocks are replaced?

5.4.5 [10] <5.2> What is the hit ratio?

5.4.6 [20] <5.2> List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.

5.4.4 3

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Line ID	0	0	1	8	14	10	0	1	8	1	11	8
Hit/miss	M	H	M	M	M	M	M	H	H	M	M	M
Replace	N	N	N	N	N	N	Y	N	N	Y	N	Y

5.4.5 0.25

5.4.6 <Index, tag, data>:

<000001₂, 0001₂, mem[1024]>
 <000001₂, 0011₂, mem[16]> 3088
 <001011₂, 0000₂, mem[176]>
 <001000₂, 0010₂, mem[2176]>
 <001110₂, 0000₂, mem[224]>
 <001010₂, 0000₂, mem[160]>

5.6.1-2

Exercise 5.6

Media applications that play audio or video files are part of a class of workloads called “streaming” workloads; i.e., they bring in large amounts of data but do not reuse much of it. Consider a video streaming workload that accesses a 512 KB working set sequentially with the following address stream:

0, 4, 8, 12, 16, 20, 24, 28, 32, ...

5.6.1 [5] <5.5, 5.3> Assume a 64 KB direct-mapped cache with a 32-byte line. What is the miss rate for the address stream above. How is this miss rate sensitive to the size of the cache or the working set? How would you categorize the misses this workload is experiencing, based on the 3C model.

5.6.2 [5] <5.5, 5.1> Recompute the miss rate when the cache line size is 16 bytes, 64 bytes, and 128 bytes? What kind of locality is this workload exploiting?

5.6.1

12.5% miss rate. The miss rate doesn't change with cache size or working set. These are cold misses.

5.6.2

25%, 6.25% and 3.125% miss rates for 16-byte, 64-byte and 128-byte blocks. Spatial locality.