VE370 HW5

PanChongdan

516370910124

1. SW instruction in IF/ID, Rb, Rib value in ID/EX, Rib, control, ALU in EX/MEM, control, ALU, RegDst in MEM/WB and PC+4 Rb, Rib control signals

2. Rb, Rib, IF/ID, ID/EX, EX/MEM are needed and MEM/WB is also read

3. In EX, it calculate the address of 100(Rb), calculate PC

   In MEM, it write data into it, calculate PCrc

4.

	CC1	CC2	CC3	CC4	CC5	CC6
LW R2, 0(R1)	WB					
LW R2, 16(R2)	DM	WB				
SLT R1, R2, R4	EX	DM	WB			
BEQ R1, R9, LOOP	ID	EX	DM	WB		
ADD R1, R2 R1	IF	ID	EX	DM	WB	
LW R2, 0(R1)		IF	ID	EX	DM	WB
LW R2, 16(R2)			IF	ID	EX	DM
SLT R1, R2, R4				IF	ID	EX
BEQ R1, R9, LOOP					IF	ID
ADD R1, R2, R1						IF

5. $\frac{2}{5} \approx 40\%$

6. BEQ R1, R9, Loop instruction, PC+4

7. 30%

8. ALUSrc=1 RegDst=0 ALUOP=00 MemWrite=0 MemRead=1 Branch=0
   MemtoReg=1 RegWrite=1

9. 0 If it's generated in EX stage, then EX/MEM register can be smaller but EX stage will be longer

10. Read after Write I1~I2, I3, I4 ($1) I2-I4($2)
    Write after Read I1~I2($2) I1~I3($1)
    Write after Write I1~I3($1)

11. With forwarding I2~I4($2) I3~I4($1) Without forwarding: I1-I2 I3($1) I2-I4 $2) I3-I4($1)

12. $1=0 $2=0, $3=31

13.
```
add $1, $2, $1        NOP
NOP                   NOP
NOP                   or $3, $1, $2
Lw $2, 0($1)
Lw $1, 4($1)
```