JOINT INSTITUTE
交大密西根学院

Ve270 Introduction to Logic Design

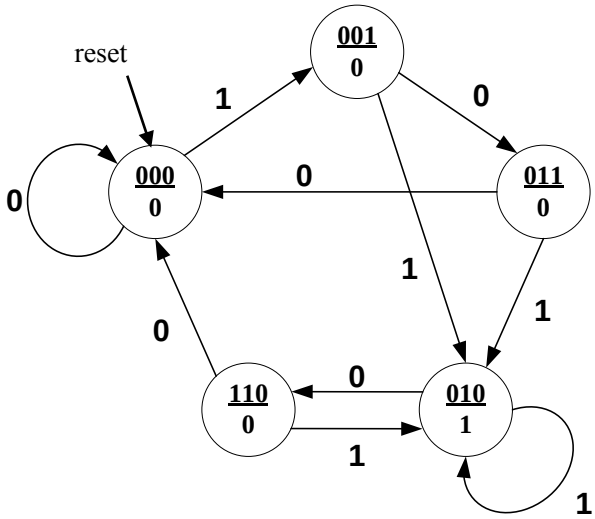
Homework 8

Assigned: July 12, 2018

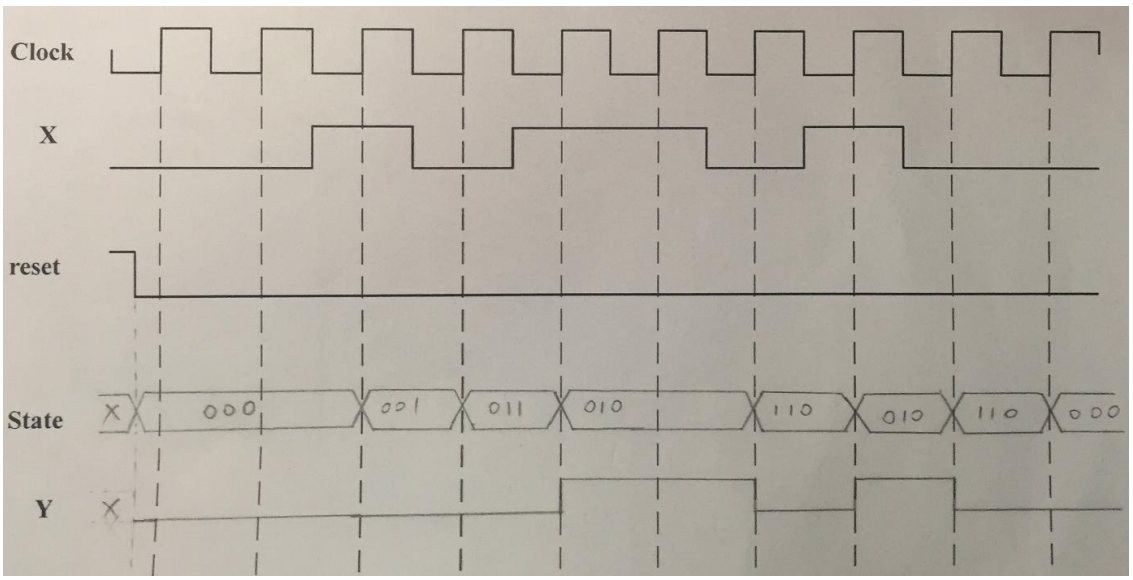
Due: July 19, 2018, 2:00pm.

The homework should be submitted in hard copies.

1. Design a finite state machine described by the following state diagram using D type flip flops. The state machine has one input X and one output Y. (30 Points)



(a). Create a state table and find equations for the next state and FSM outputs.
(b). Complete the timing diagrams of states and output **Y** according to the given inputs.
(c). Is the FSM self-starting? If not, make it a self-starting FSM.



1 (a). state table:

In	present state			next state			out
X	P_2	P_1	P_0	n_2	n_1	n_0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	0
0	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1
0	1	1	0	0	0	0	0
	X				X		
1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	1	0	1
1	1	1	0	0	1	0	0
	X				X		

n_2 \ P_1P_0 / XP_2

XP_2 \ P_1P_0	00	01	11	10
00	0	0	0	1
01	X	X	X	0
11	X	X	X	0
10	0	0	0	0

$\Rightarrow n_2 = X'P_2'P_1P_0'$

n_1 \ P_1P_0 / XP_2

XP_2 \ P_1P_0	00	01	11	10
00	0	1	0	1
01	X	X	X	0
11	X	X	X	1
10	0	1	1	1

$\Rightarrow n_1 = P_1'P_0 + XP_1 + P_2'P_1P_0'$

Y \ P_1P_0 / XP_2

XP_2 \ P_1P_0	00	01	11	10
00	0	0	0	1
01	X	X	X	0
11	X	X	X	0
10	0	0	0	1

$\Rightarrow Y = P_2'P_1P_0'$

n_0 \ P_1P_0 / XP_2

XP_2 \ P_1P_0	00	01	11	10
00	0	1	0	0
01	X	X	X	0
11	X	X	X	0
10	1	0	0	0

$\Rightarrow n_0 = XP_1'P_0' + X'P_1'P_0$

$= P_1'(XP_0' + X'P_0) = P_1'(X \oplus P_0)$

so $n_2 = X'P_2'P_1P_0'$

$n_1 = P_1'P_0 + XP_1 + P_2'P_1P_0'$

$n_0 = P_1'(X \oplus P_0)$

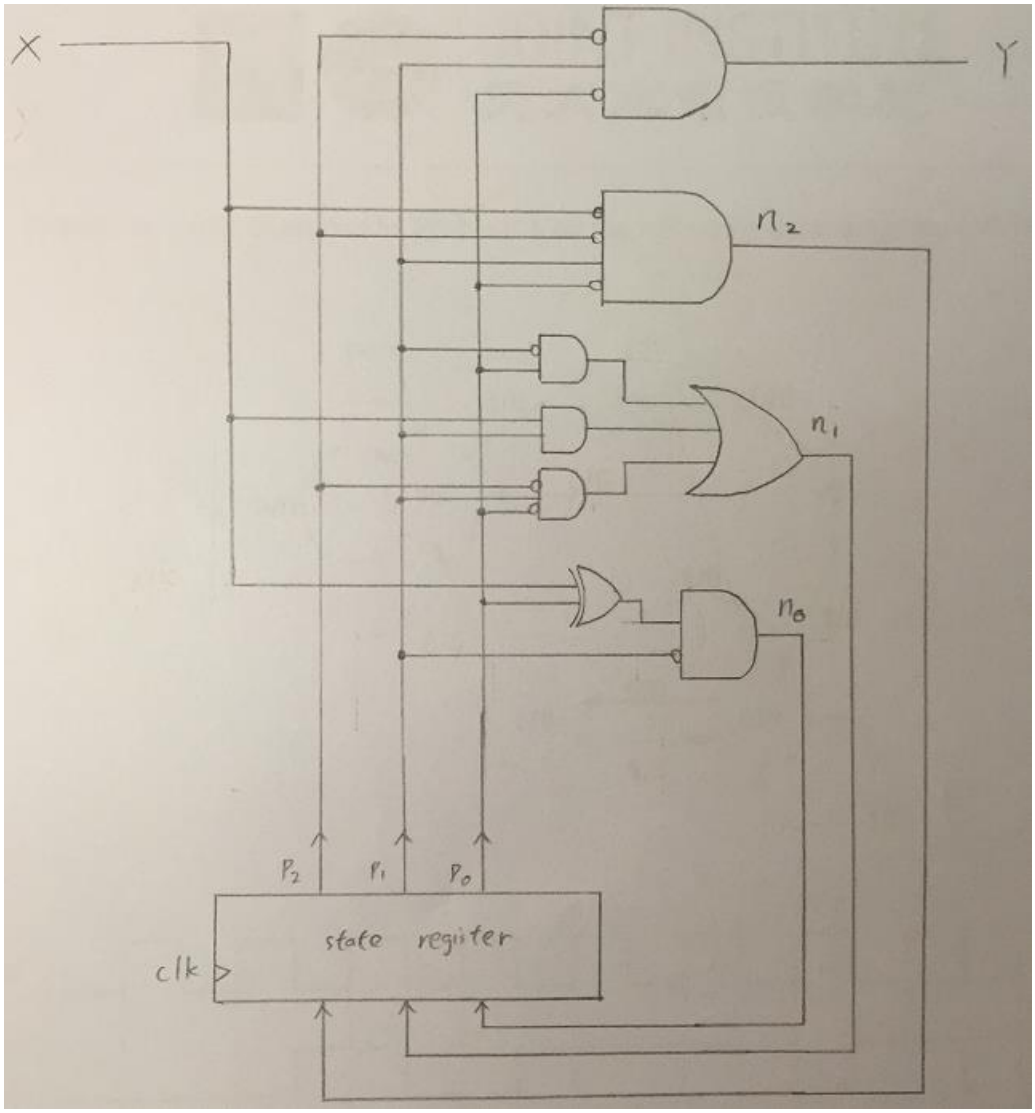
$Y = P_2'P_1P_0'$

(c). we write out the x part.

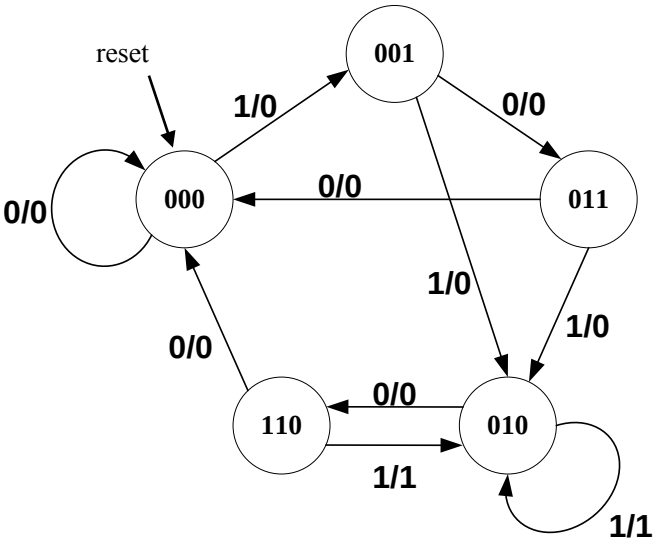
X	P_2	P_1	P_0	n_2	n_1	n_0	Y	
0	1	0	0	0	0	0	0	✓
0	1	0	1	0	1	1	0	✓
0	1	1	1	0	0	1	0	✓
1	1	0	0	0	0	1	0	✓
1	1	0	1	0	1	0	0	✓
1	1	1	1	0	1	0	0	✓

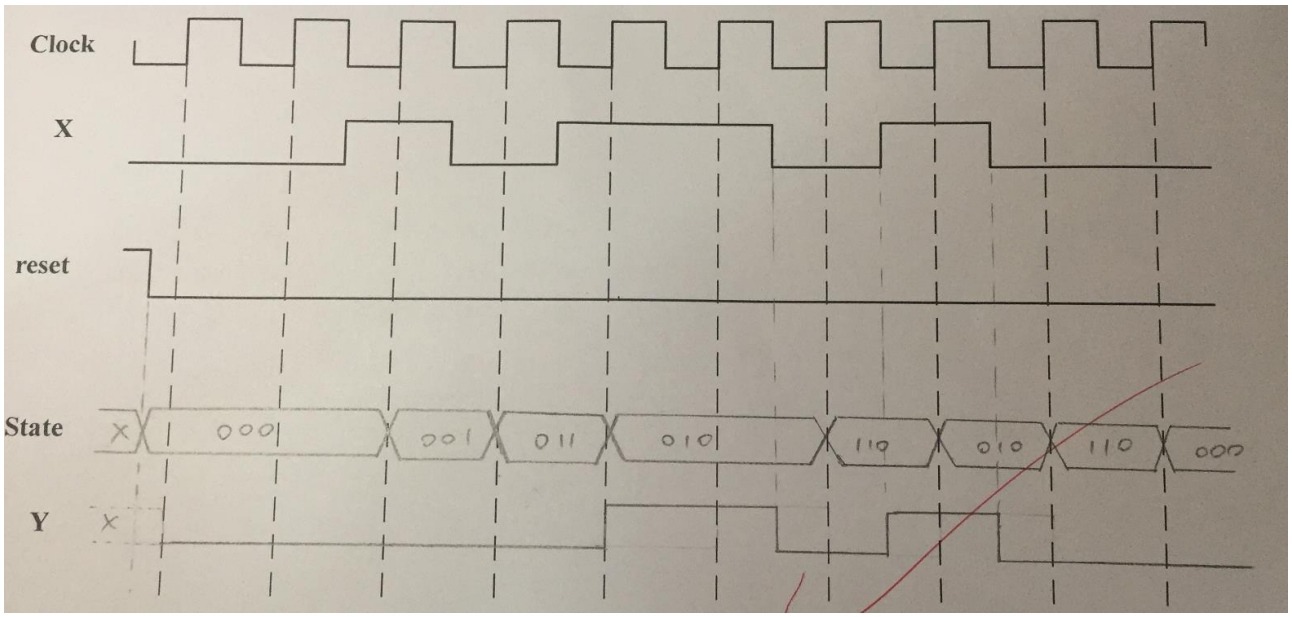
so all the next state is in the 000, 001, 010, 011, 110

so it is a self-starting FSM


X
Y
n_2
n_1
n_0
P_2
P_1
P_0
state register
clk

2. Repeat the same questions as Problem 1 on the following state diagram. (30 Points)





2(a). state table:

In.	Present state			next state			Out
X	P_2	P_1	P_0	n_2	n_1	n_0	Y
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	0
0	0	1	1	0	0	0	0
0	0	1	0	1	1	0	0
0	1	1	0	0	0	0	0
1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	1	0	1
1	1	1	0	0	1	0	1

we can the n_2, n_1, n_0 is the same as the n_2, n_1, n_0 in Q1.

$\Rightarrow n_2 = x' P_2' P_1 P_0'$

$n_1 = P_1' P_0 + x P_1 + P_2' P_1 P_0'$

$n_0 = P_1' (x \oplus P_0')$

Y \ P_1P_2	00	01	11	10
x P_2				
0	0	0	0	0
1	x	x	x	1

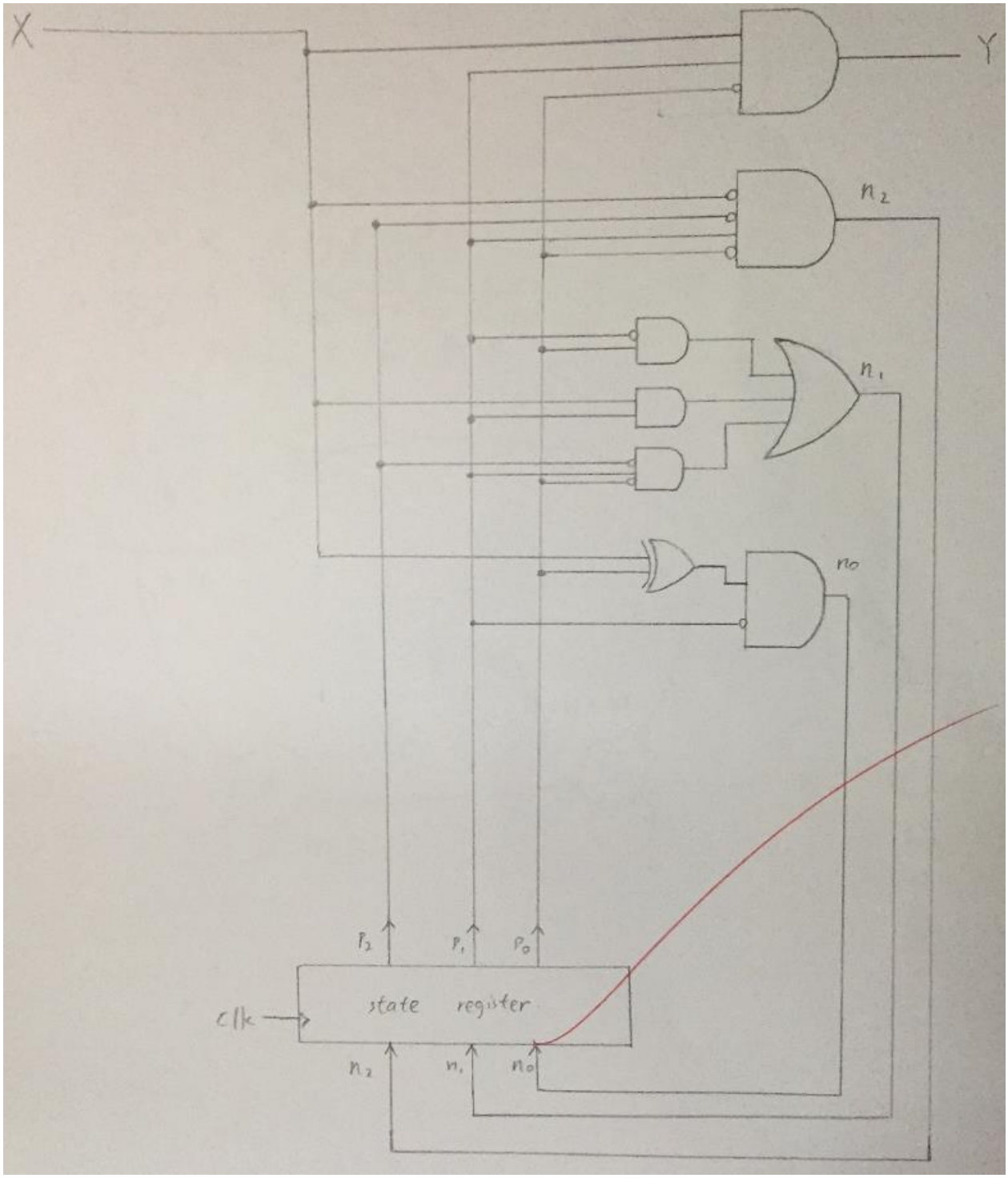
$\Rightarrow Y = x P_1 P_0'$

(c). the X part:

x	P_2	P_1	P_0	n_2	n_1	n_0	
0	0	0	0	0	0	0	✓
0	1	0	1	0	1	0	✓
0	1	1	1	0	0	1	✓
1	1	0	0	0	0	1	✓
1	1	0	1	0	1	0	✓
1	1	1	1	0	1	0	✓

all the next state is in 000, 001, 010, 011, 110.

so it is a self-starting FSM


X
Y
n_2
n_1
n_0
P_2
P_1
P_0
clk
state register
n_2
n_1
n_0

3. Problem 6.17, using implication table method (20 Points)

Reduce the number of states for the FSM in Figure 6.92 by using an implication table.

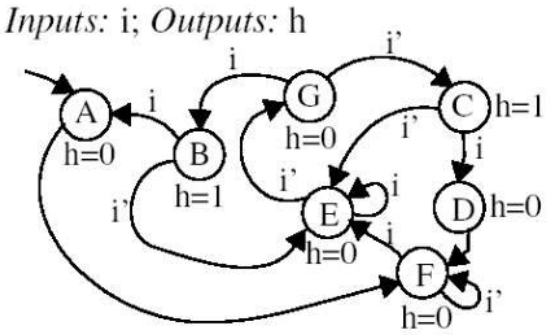
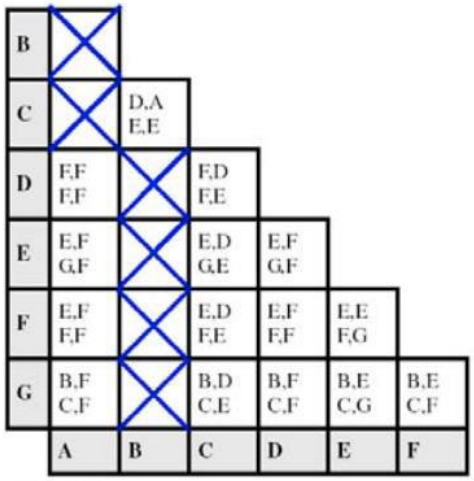
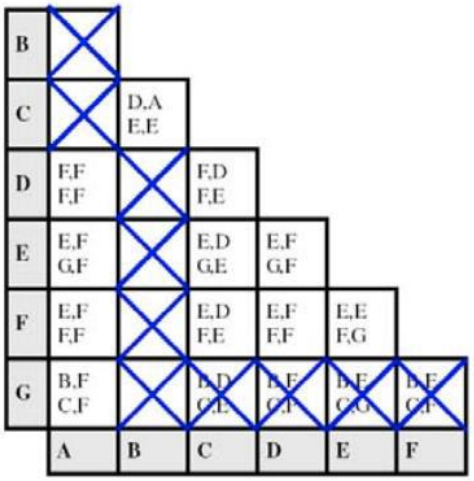


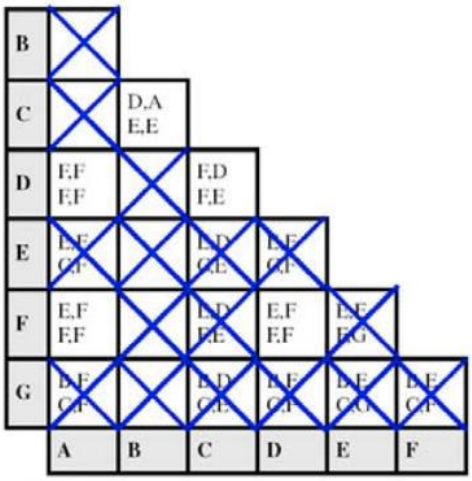
Figure 6.92: FSM example.



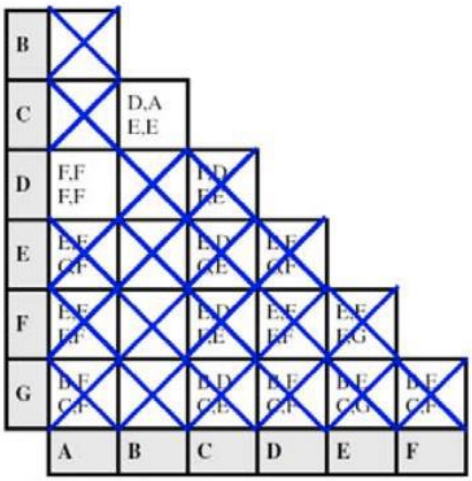
First Pass



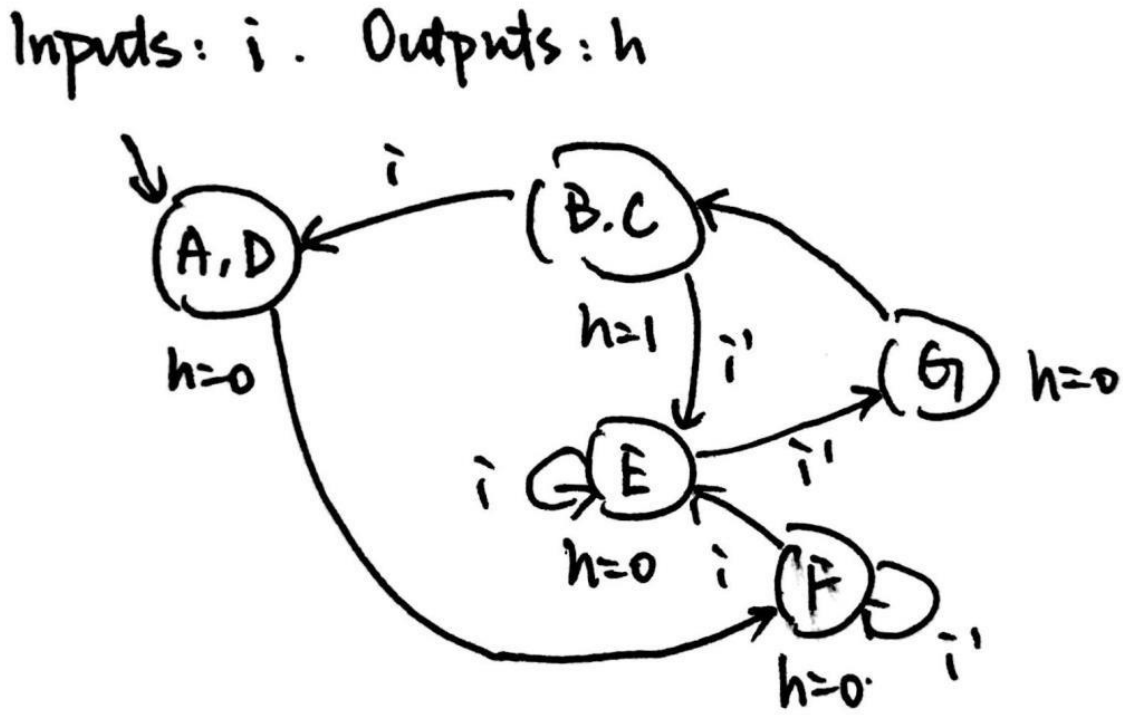
Second Pass



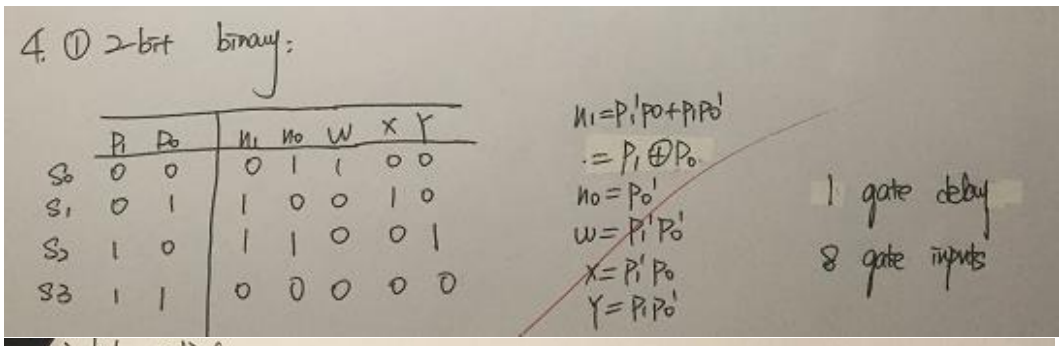
Third Pass

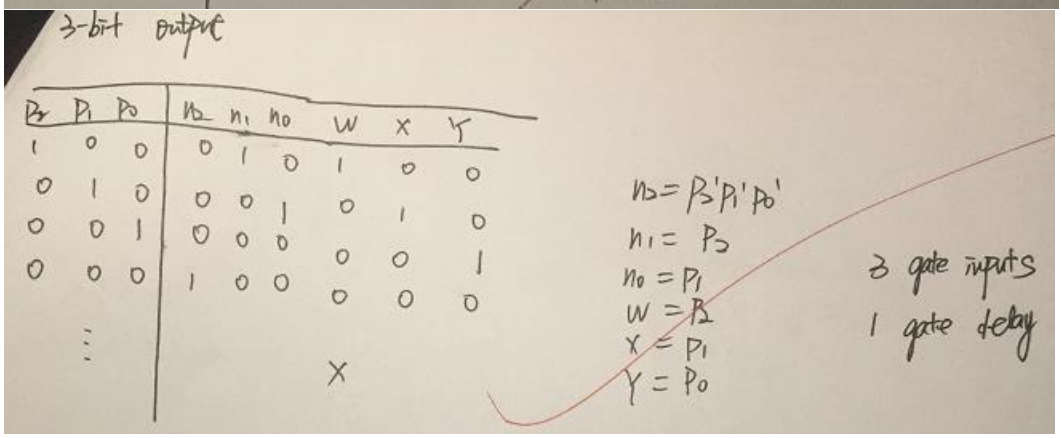


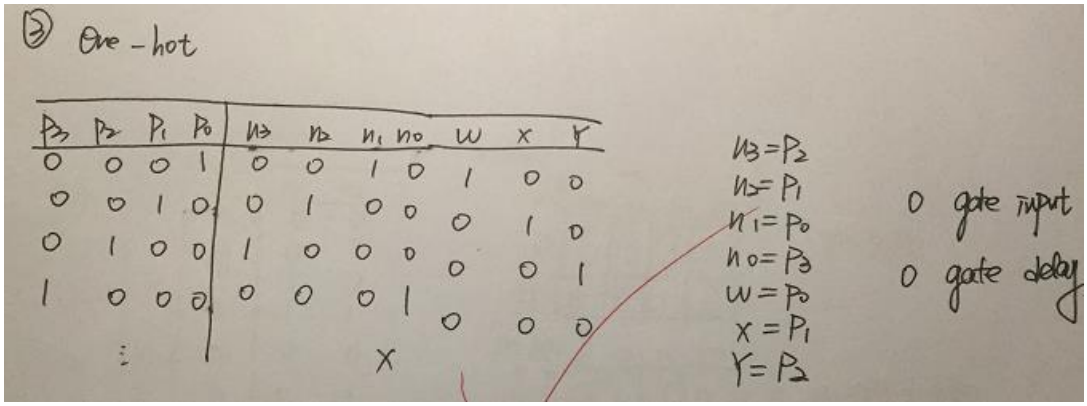
Fourth and Final Pass



4. Problem 6.18 (assuming the next state of S3 is S0) (20 Points)






③ One-hot
P3 P2 P1 P0 n3 n2 n1 n0 W X Y
0 0 0 1 0 0 1 0 1 0 0
0 0 1 0 0 1 0 0 0 1 0
0 1 0 0 1 0 0 0 0 0 1
1 0 0 0 0 0 0 1 0 0 0
X
n3=P2
n2=P1
n1=P0
n0=P3
W=P0
X=P1
Y=P2
0 gate input
0 gate delay