5.10.1 a) 4kB page, 12-bit page offset, 15-12b virtual page number

4669 = 0x1 23D Page fault, disk ⇒ physical page 13(D), ⇒ TLB slot 3

2227 = 0x08B3 TLB Miss, ⇒ TLB slot 0

13916 = 0x365C TLB Hit (slot 2)

34587 = 0x871B Page fault, disk ⇒ physical page 14(E), ⇒ TLB slot 1

48870 = 0xBEE6 TLB Miss, 12 ⇒ TLB slot 3

12608 = 0x3140 TLB Hit (slot 2)

49225 = 0xC049 Page fault, disk ⇒ physical page 15(F) ⇒ TLB slot 0

TLB:

V	Tag	PPN
1	C	15(F)
1	8	14(E)
1	3	6
1	B	12

PT:

#	V	PPN
0	1	5
1	1	D
2	0	disk
3	1	6
4	1	9
5	1	11
6	0	disk
7	1	4
8	0→1	disk→E
9	0	disk
A	1	03
B	1	12
C	1	F
:		
:		
:		

2. a) 16 KB page, 14-bit page offset, 15-14b virtual page number

virtual addr	virtual number	
0x123D	0	TLB miss, PP 5 ⇒ TLB slot 3
0x08B3	0	TLB Hit slot 3
0x365C	0	TLB Hit slot 3
0x871B	1	Page fault, disk ⇒ PP 13 (D) ⇒ TLB slot 0
0xBEE6	10 = 2	Page fault, disk ⇒ PP 14 (E) ⇒ TLB slot 1
0x3140	0	TLB Hit slot 3
0xC049	11 = 3	TLB Hit slot 2

TLB:

V	tag	PPN
1	1	0
1	2	1
1	3	6
1	0	5

PT:

#	V	PPN
1	0 → 1	disk → 13 (D)
2	0 → 1	disk → 14 (E)

Large Page size decreases the page fault rate generally but if the program use addresses in very sparse fashion the cost of fetching larger page from disk is high.

3. a) 2-way set associative 15-12b virtual page number, 15-13b tag, 12b set

virtual addr	VPN	tag	set	
0x123D	1	000 = 0	1	Page fault, disk ⇒ PPN 13 (D) ⇒ TLB set 1 slot 1
0x08B3	0	0	0	TLB Miss, PPN 5 ⇒ TLB set 0 slot 0
0x365C	3	001 = 1	1	TLB Miss, PPN 6 ⇒ TLB set 1 slot 0
0x871B	8	100 = 4	0	Page fault, disk ⇒ PPN 14 (E) ⇒ TLB set 0 slot 1
0xBEE6	B	101 = 5	1	TLB Miss, PPN 12 (C) ⇒ TLB set 1 slot 1
0x3140	3	001 = 1	1	TLB Hit set 1 slot 0
0xC049	C	110 = 6	0	Page fault, disk ⇒ PPN 15 (F) ⇒ TLB set 0 slot 0

TLB

	V	tag	PPN	V	tag	PPN
set 0	1	6	F	1	4	14 (E)
set 1	1	1	6	1	5	12 (C)

2 cont'me.

Direct mapped : 15-14b tag, 13-12b set

VPN	tag	set (index)	
1	0	1	Page fault, disk ⇒ PPN 13 (D) ⇒ TLB index 1
0	0	0	TLB miss, PPN 5 ⇒ TLB index 0
3	0	11=3	TLB miss, PPN 6 ⇒ TLB index 3
8	01=1	0	Page fault, disk ⇒ PPN 14 (E) ⇒ TLB index 0
B	10=2	11=3	TLB miss, PPN 12 (C) ⇒ TLB index 3
3	00=0	11=3	TLB miss, PPN 6 ⇒ TLB index 3
C	11=3	00=0	Page fault, disk ⇒ PPN 15 (F) ⇒ TLB index 0

TLB:

	V	tag	PPN
0	1	3	15(F)
1	1	0	13(D)
2	1	3	6
3	1	0	6

TLB is important to decrease the time to access memory to translate.

4 # Page offset = $\log_2$(page size)

Page number (virtual) = # addr − # page offset

Page table entries = $2^{\#\text{ page number}}$

Page table size = # page table entries × entry size

a). ~~8KB~~ $2^{32-\log_2 8K} \times 4 = 2^{21}$ bytes per App

Total = 5×2^{21} bytes

5.11.1 a) Similar to previous, # Page tabe entry = $2^{43-\log_2 4K} = 2^{31}$

Page table size = $2^{31} \times 4 = 2^{33}$ byte = 8 GB

5.11.2 a) Each page can contain 4KB/4B = 1K = 2^{10} entries as a page table. $(2^{10})^4 = 2^{40} > 2^{31}$ (4-level PT)

2 address transition is needed.

5.12.1 a) Zero hit..

Target	Hit/Miss	Set 0	Set 0	set 1	set 1
0	M	0			
2	M	0	2		
4	M	4	2		
8	M	4	8		
10	M	10	8		
12	M	10	12		
14	M	14	12		
16	M	14	16		
0	M	0	16		

5.12.2 (a) One hit.

Target	H/M	Set 0	Set 0	Set 1	Set 1
0	M	0			
2	M	0	2		
4	M	0	4		
8	M	0	8		
10	M	0	10		
12	M	0	12		
14	M	0	14		
16	M	0	16		
0	H	0	16		