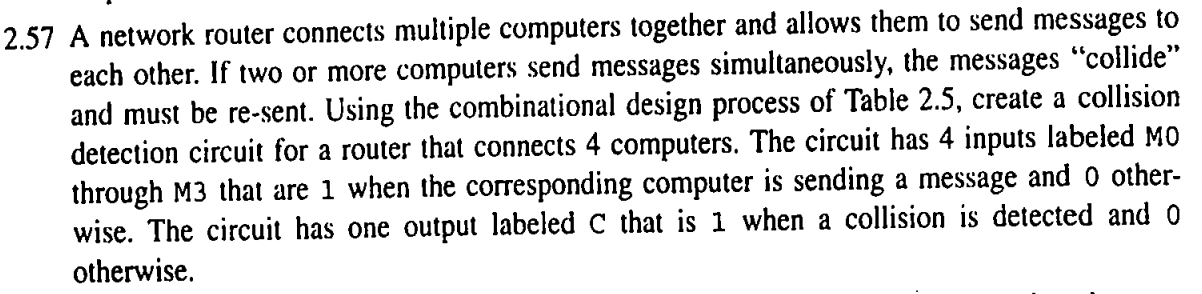
**Ve270 Introduction to Logic Design Homework 3**

**Assigned: May 31, 2018**

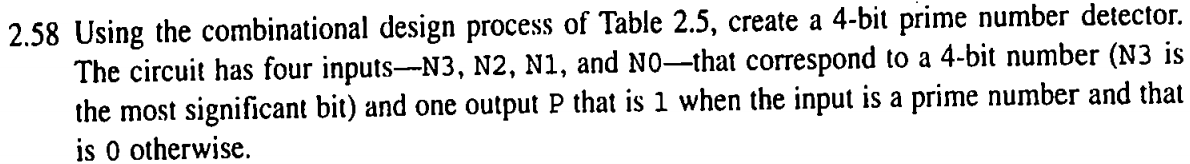
**Due: June 7, 2018, 2:00pm.**

**The homework should be submitted in hard copies.**

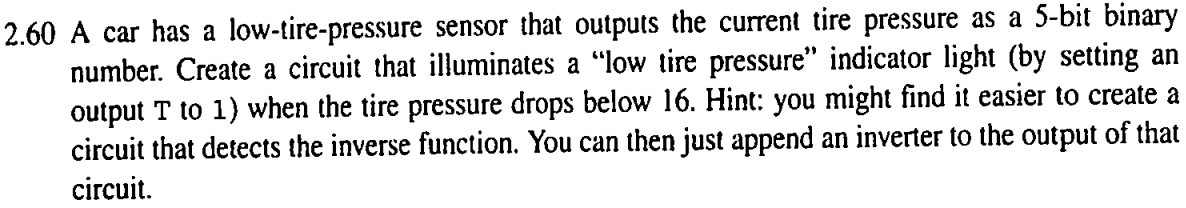
1. Problem 2.57 (15 points)



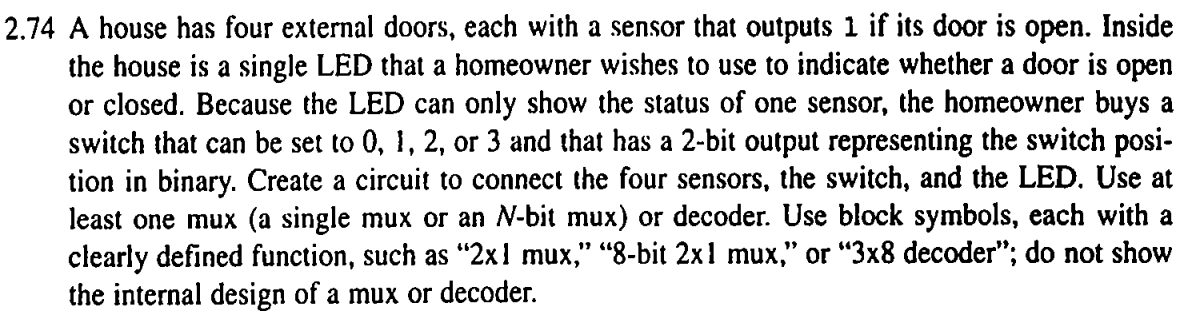
1. Problem 2.58 (15 points)



1. Problem 2.60 (15 points)



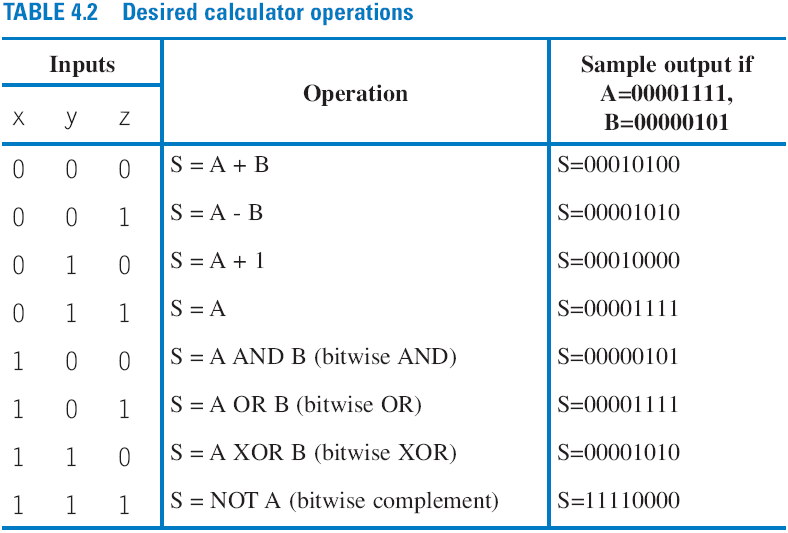
1. Problem 2.74 (15 points)



1. Show how four 2-to-1 and one 4-to-1 MUXs could be connected to form an 8-to-1 MUX. (5 points)
2. Show how to make a 4-to-1 MUX using an 8-to-1 MUX. (5 points)
3. Use one 4-to-1 MUX and one inverter to implement a digital circuit for following truth table. (5 points)

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | F |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

1. Use one 3-by-8 decoder to implement a digital circuit for above truth table. (10 points)
2. Design an 8-bit ALU described in the following functional table. Use building blocks. (10 points)



1. Highlight the critical path of the following circuit. Assume that each gate has a delay of 1 ns and each wire has a delay of 0.5 ns. (5 points)

