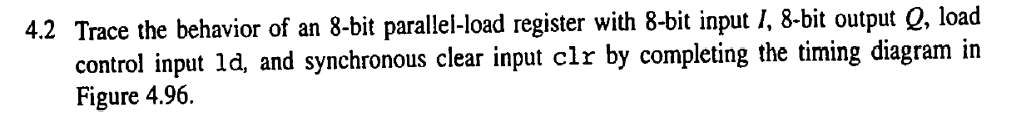
**Ve270 Introduction to Logic Design Homework 6**

**Assigned: June 28, 2018**

**Due: July 5, 2018, 2:00pm.**

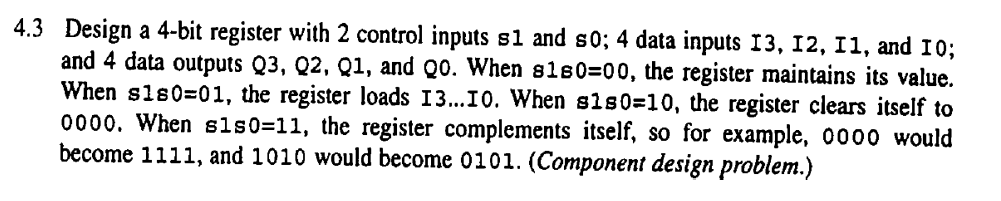
**The homework should be submitted in hard copies.**

1. Problem 4.2 (10 points)

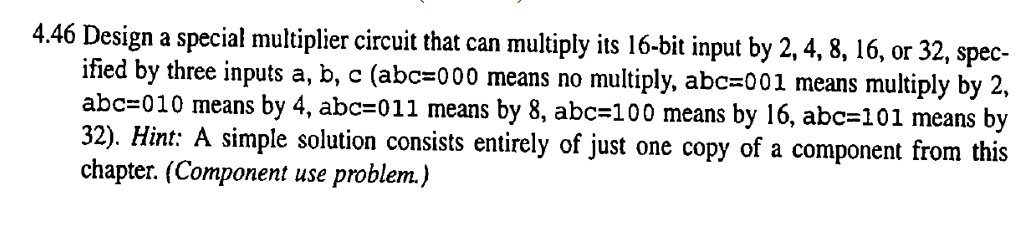




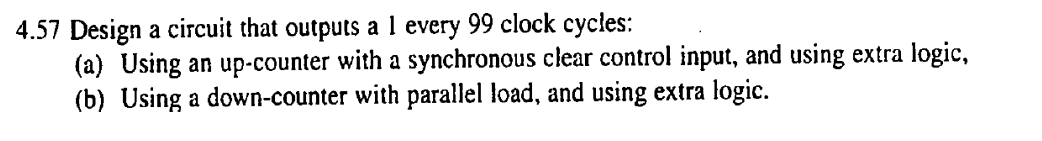
1. Problem 4.3, using components to draw schematic (20 points)



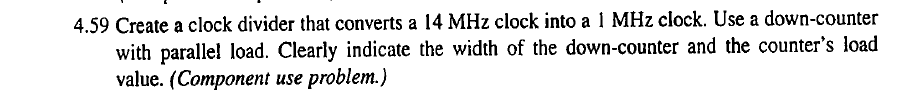
1. Problem 4.46. Draw schematic. (20 Points).



1. Problem 4.57. Draw schematic (a), (b). (20 points)



1. Problem 4.59. Draw schematic (10 Points)



1. Model a Universal Shift Register (shown below) with Verilog. Simulate your design. (20 Points)

