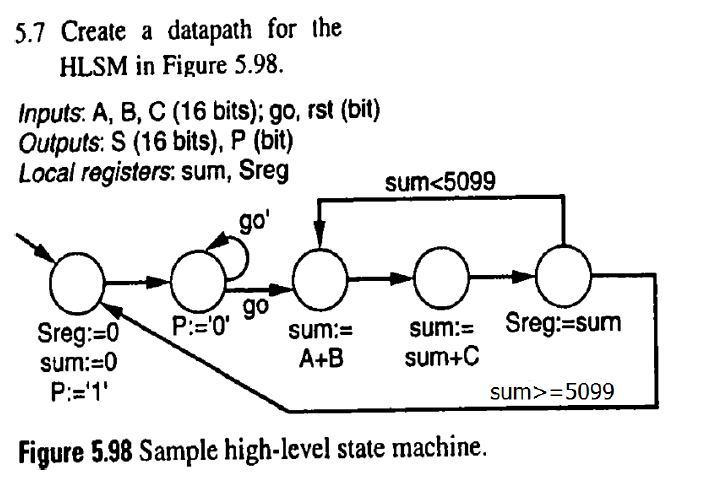
**Ve270 Introduction to Logic Design Homework 9**

**Assigned: July 19, 2018**

**Due: July 26, 2018, 2:00pm.**

**The homework should be submitted in hard copies.**

1. Problem 5.7. (15 points) **Note**: (sum < 5099) should be (sum < 5099)’



1. Problem 5.14. (15 points)



1. Problem 5.16 (35 points)

You can assume you only need to calculate the average once. (No need to return to the init state)



1. Design a circuit called ***Receiver*** that receives two single bit signals, **Valid** and **Data\_in**, from another device called ***Transmitter***. The **Valid** signal sent from the ***Transmitter*** will be a 1-clock cycle pulse. After the ***Receiver*** receives the **Valid** pulse, it will start receiving 8 bits through port **Data\_in**, bit by bit. After the 8 bits of data is received, it should be copied into an 8-bit register called **RxReg**. (35 points)

(RxReg is the only output of this HLSM)

(RxReg should save the 8-bit data until the next valid pulse)