HDMI Compliance Test Software: Measurement Report

Tektronix Enabling Innovation

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Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DPO73304S - 10.8.5 Build 4
TDSHT3 Version	5.3.6 Build 54

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	297.001
Resolution	4K30
Refresh Rate	30Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	37
Pass	31
Fail	6

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.068*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.07*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.08*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.07*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.018*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.067*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.05*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	170.09ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	112.15ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	108.64ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	114.79ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	175.63ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	113.54ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	111.51ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	112.96ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	51.08%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.3%	Pass
18	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.8213V	Pass
19	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.6587V	Fail
20	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.8439V	Pass
21	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.6664V	Fail
22	7-2 : Source Low Amplitude +(Supported Sink > 165MHz)	CK+	2.600V < VL < 2.900V;	2.8213V	Pass
23	7-2 : Source Low Amplitude +(Supported Sink > 165MHz)	D0+	2.600V < VL < 2.900V;	2.6554V	Pass
24	7-2 : Source Low Amplitude -(Supported Sink > 165MHz)	CK-	2.600V < VL < 2.900V;	2.8439V	Pass
25	7-2 : Source Low Amplitude -(Supported Sink > 165MHz)	D0-	2.600V < VL < 2.900V;	2.6664V	Pass
26	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.6573V	Fail
27	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.6982V	Fail
28	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.6631V	Fail
29	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.6702V	Fail
30	7-2 : Source Low Amplitude +(Supported Sink > 165MHz)	D1+	2.600V < VL < 2.900V;	2.6573V	Pass
31	7-2 : Source Low Amplitude +(Supported Sink > 165MHz)	D2+	2.600V < VL < 2.900V;	2.7055V	Pass
32	7-2 : Source Low Amplitude -(Supported Sink > 165MHz)	D1-	2.600V < VL < 2.900V;	2.6631V	Pass
33	7-2 : Source Low Amplitude -(Supported Sink > 165MHz)	D2-	2.600V < VL < 2.900V;	2.6664V	Pass
34	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.101*Tbit	Pass
35	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.071*Tbit	Pass
36	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.077*Tbit	Pass
37	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.059*Tbit	Pass

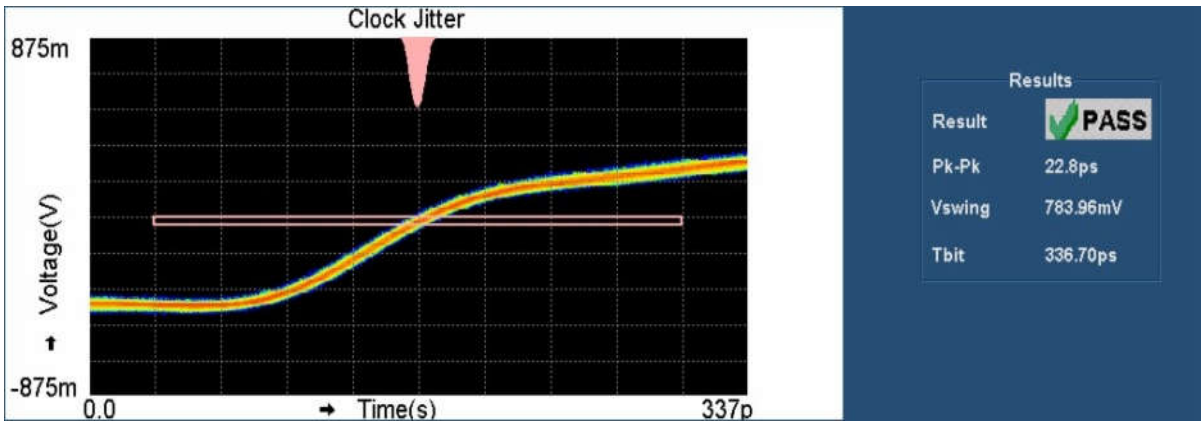
Detailed Results

7-9 : Source Clock Jitter : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.068*Tbit	336.70ps	783.96mV	0.18*Tbit	50.000M	Pass

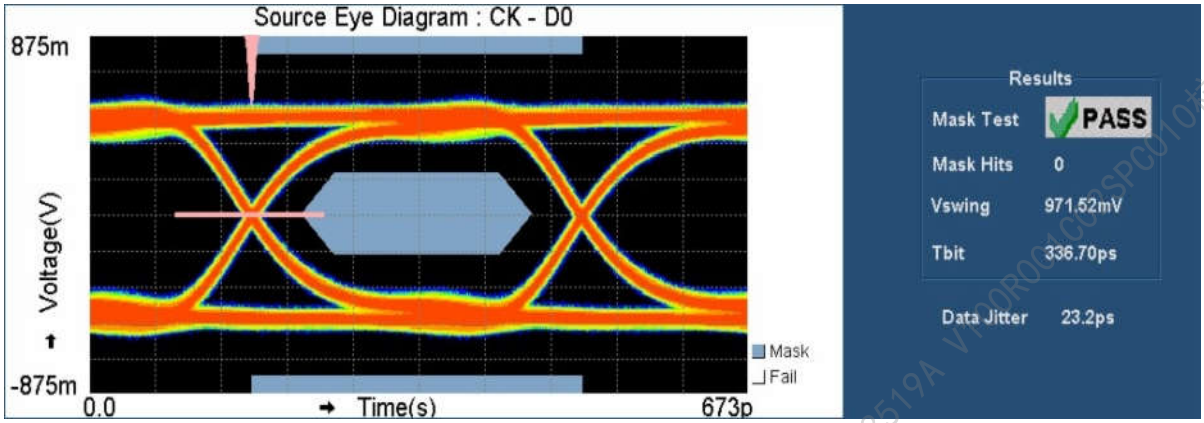
Waveform/Plot



- **7-10 : Source Eye Diagram : CK - D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.07*Tbit	336.70ps	971.52mV	231.2m*Tbit	50.000M	0	Pass

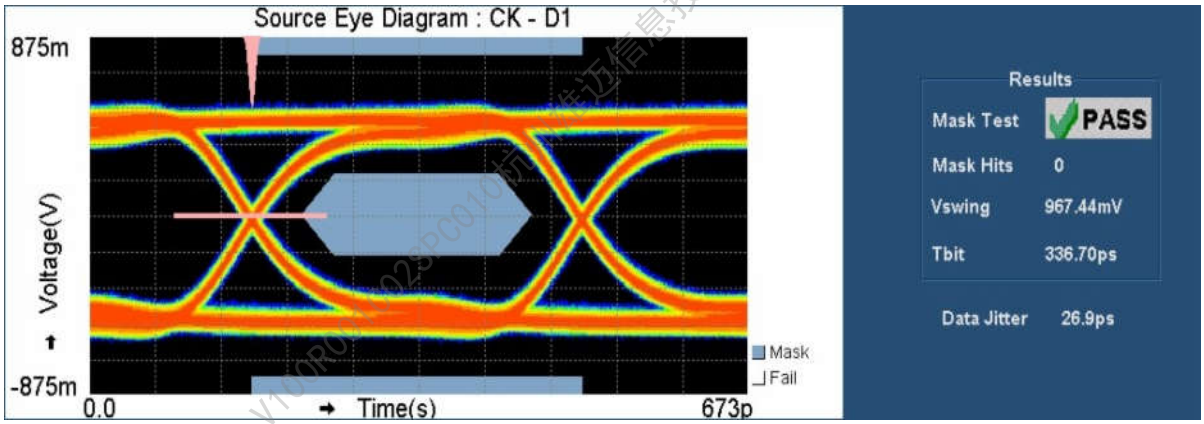
  - **Waveform/Plot**



- **7-10 : Source Eye Diagram : CK - D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.08*Tbit	336.70ps	967.44mV	220.2m*Tbit	50.000M	0	Pass

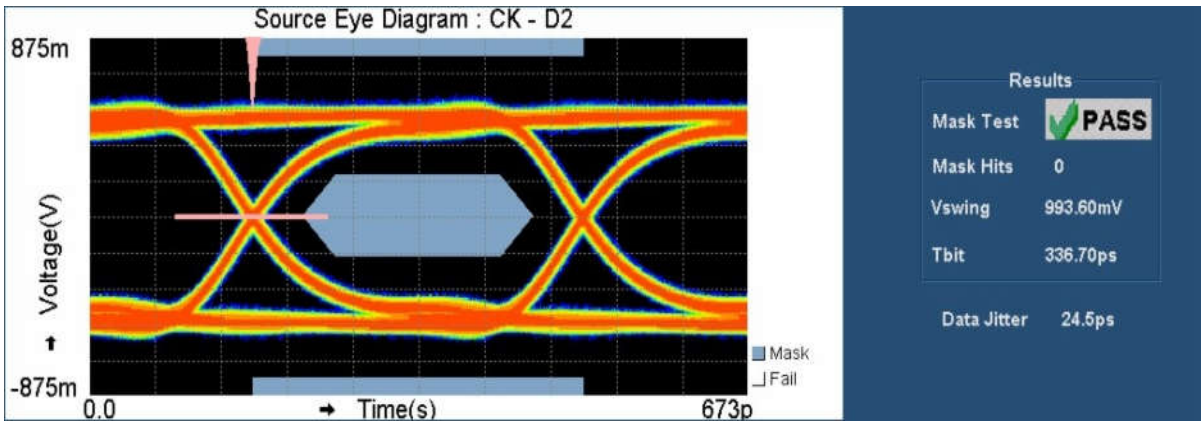
  - **Waveform/Plot**



- **7-10 : Source Eye Diagram : CK - D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask Hits	Result
Data Jitter < 0.3*Tbit;	0.07*Tbit	336.70ps	993.60mV	227.3m*Tbit	50.000M	0	Pass

  - **Waveform/Plot**



- **7-6 : Source Inter-Pair Skew : D0 - D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.018*TPixel	336.70ps	= 971.52mV, Vs = 967.44mV	57.243p	63.227p	59.719p	Pass

- **7-6 : Source Inter-Pair Skew : D1 - D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.067*TPixel	336.70ps	= 967.44mV, Vs = 993.60mV	223.31p	228.93p	226.52p	Pass

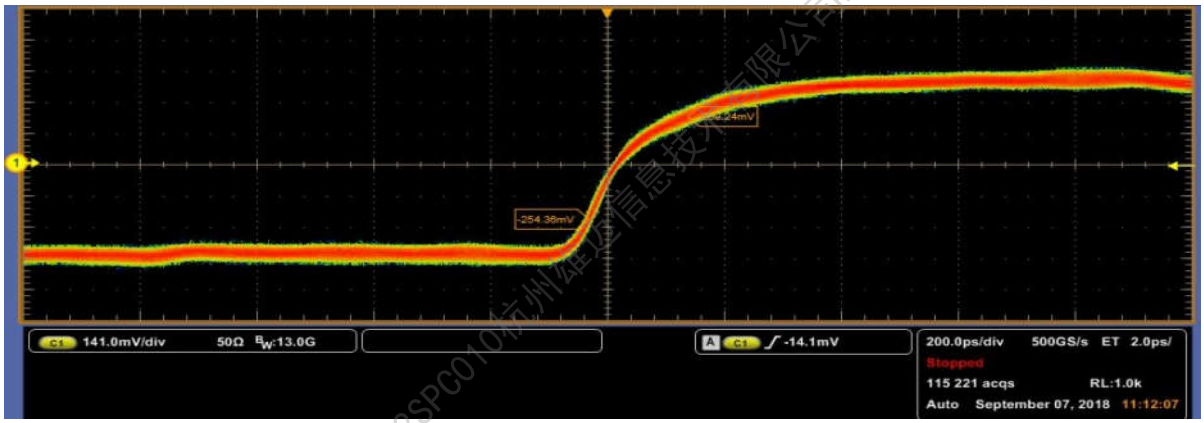
- **7-6 : Source Inter-Pair Skew : D2 - D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs(D2 - D0)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.05*TPixel	336.70ps	= 993.60mV, Vs = 971.52mV	164.24p	169.39p	166.80p	Pass

- **7-4 : Source Rise Time : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	170.09ps	336.70ps	772.68mV	95.09ps	Pass

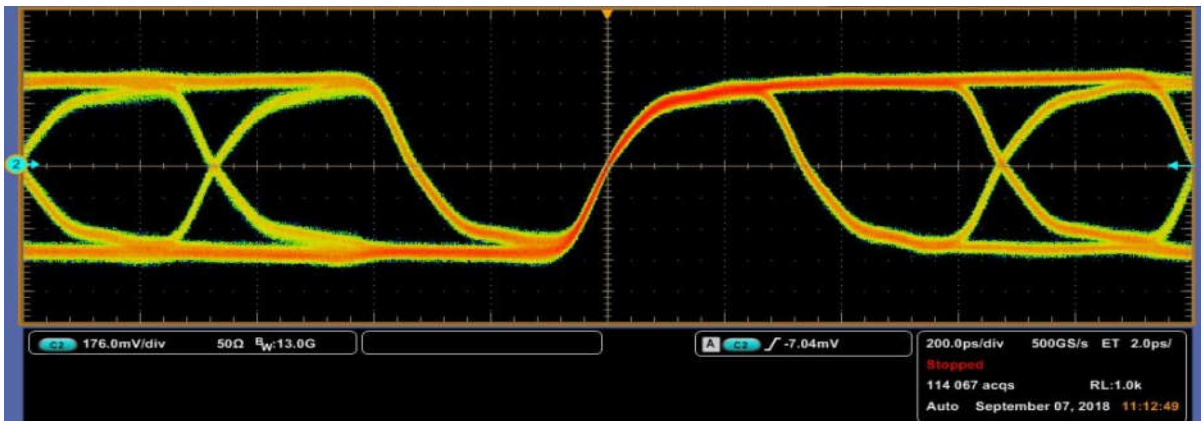
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	112.15ps	336.70ps	978.56mV	37.15ps	Pass

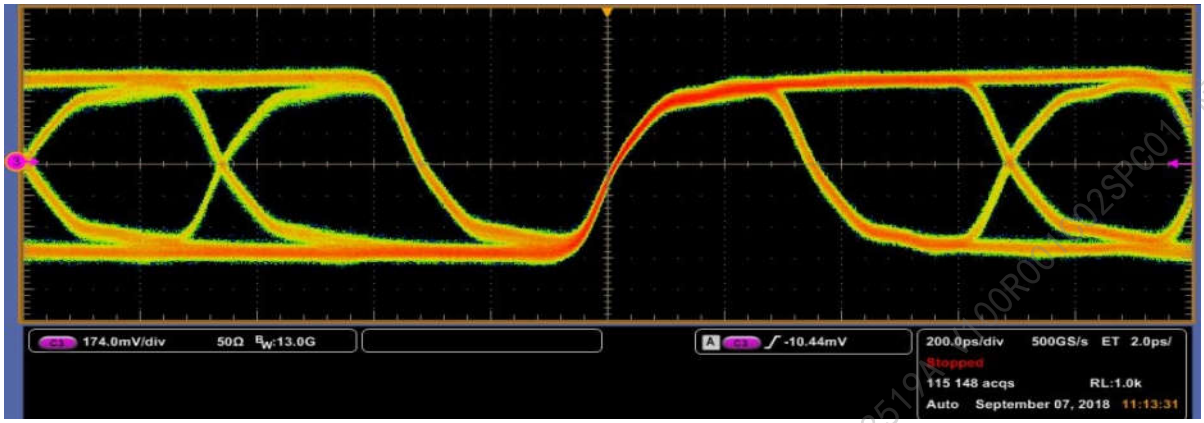
  - **Waveform/Plot**



- **7-4 : Source Rise Time : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	108.64ps	336.70ps	974.40mV	33.64ps	Pass

  - **Waveform/Plot**



- **7-4 : Source Rise Time : D2**
  - **Results**

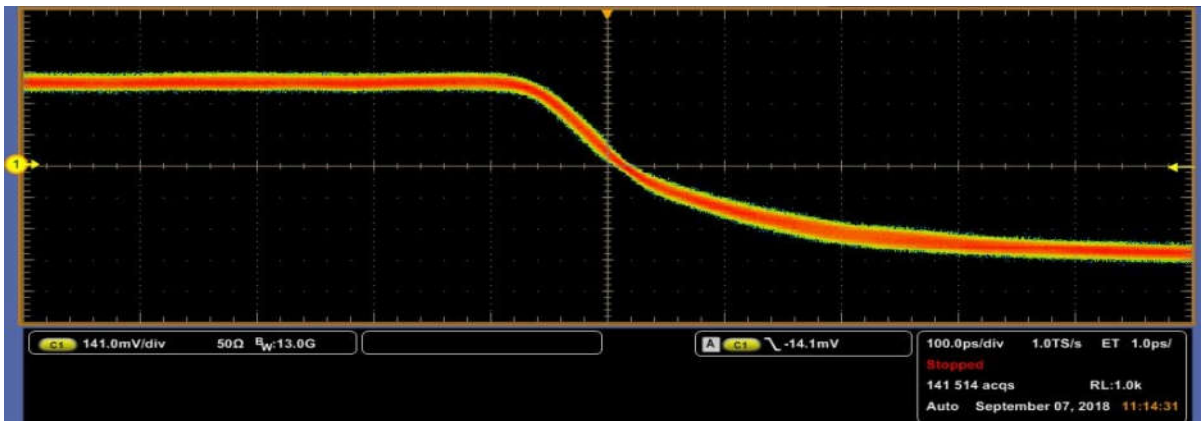
Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	114.79ps	336.70ps	986.40mV	39.79ps	Pass

  - **Waveform/Plot**

- **7-4 : Source Fall Time : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	175.63ps	336.70ps	772.68mV	100.6ps	Pass

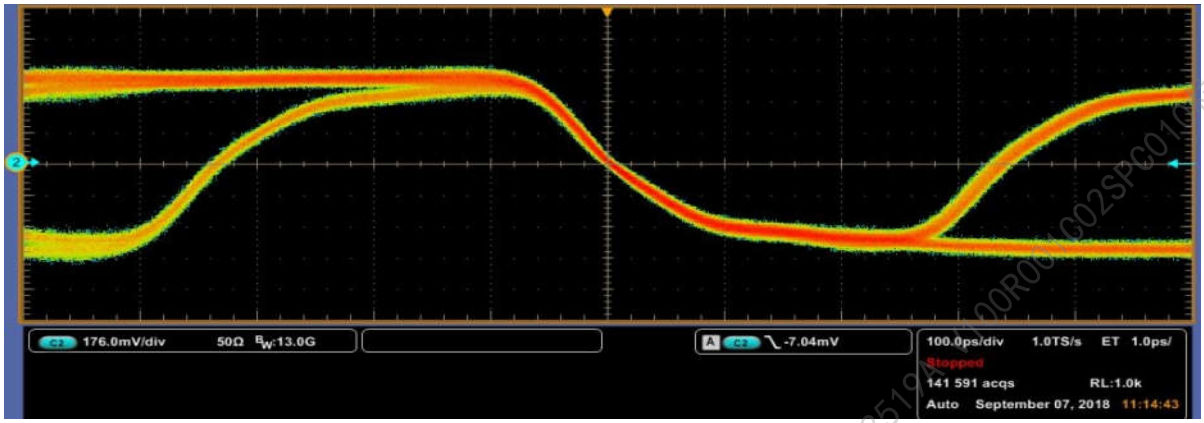
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	113.54ps	336.70ps	978.56mV	38.54ps	Pass

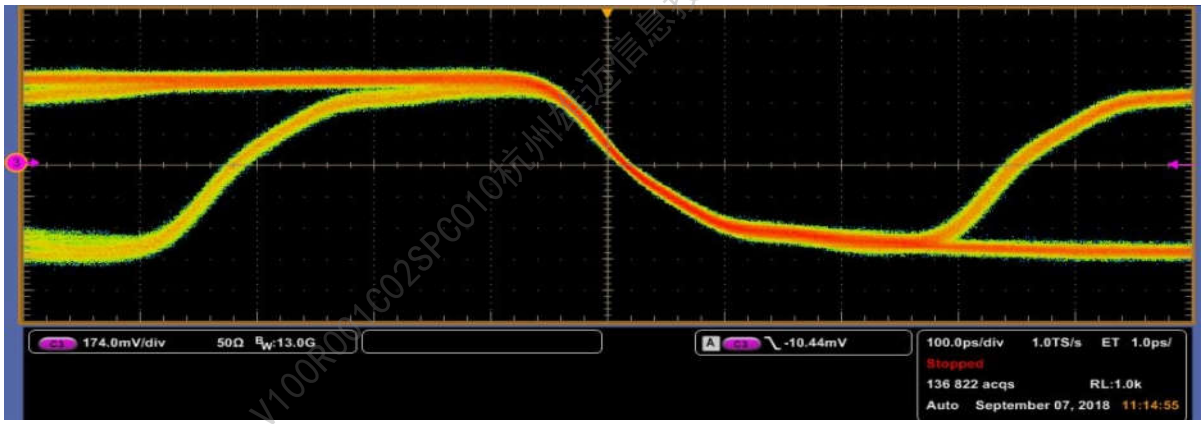
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	111.51ps	336.70ps	974.40mV	36.51ps	Pass

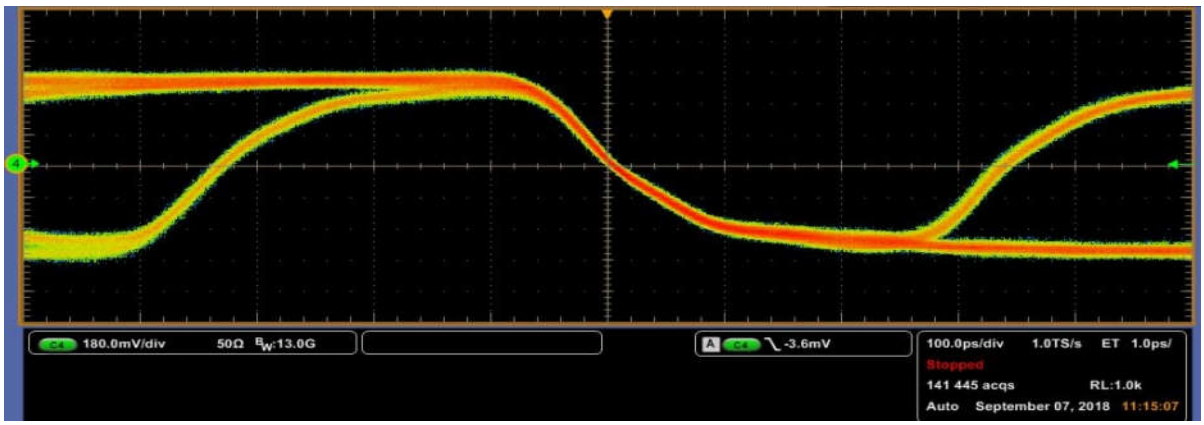
  - **Waveform/Plot**



- **7-4 : Source Fall Time : D2**
  - **Results**

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	112.96ps	336.70ps	986.40mV	37.96ps	Pass

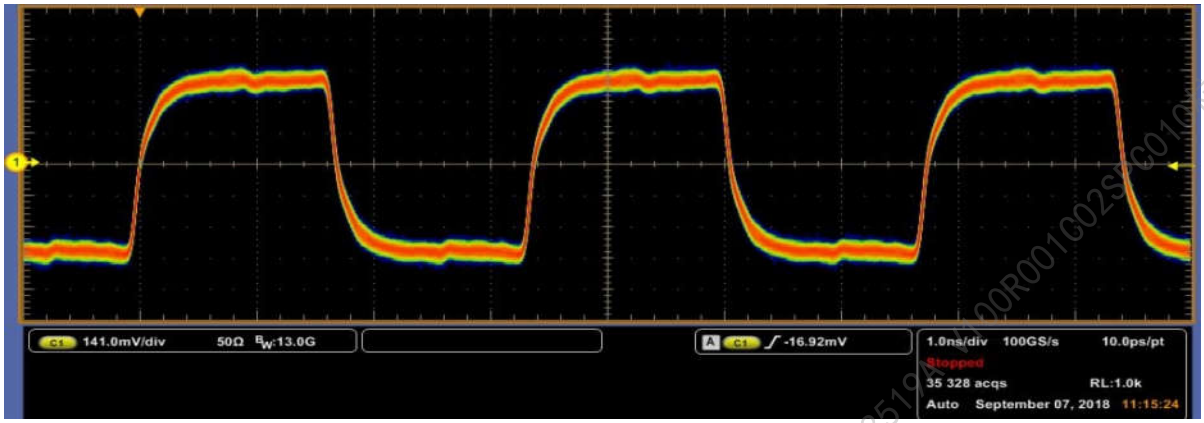
  - **Waveform/Plot**



- **7-8 : Max Duty Cycle : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	51.08%	336.70ps	8.92%	Pass

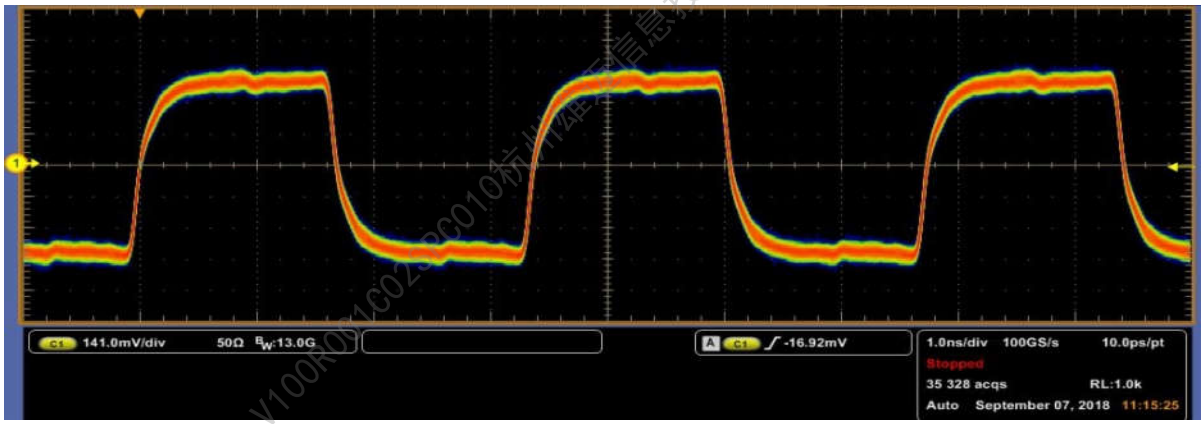
  - **Waveform/Plot**



- **7-8 : Min Duty Cycle : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.3%	336.70ps	9.3%	Pass

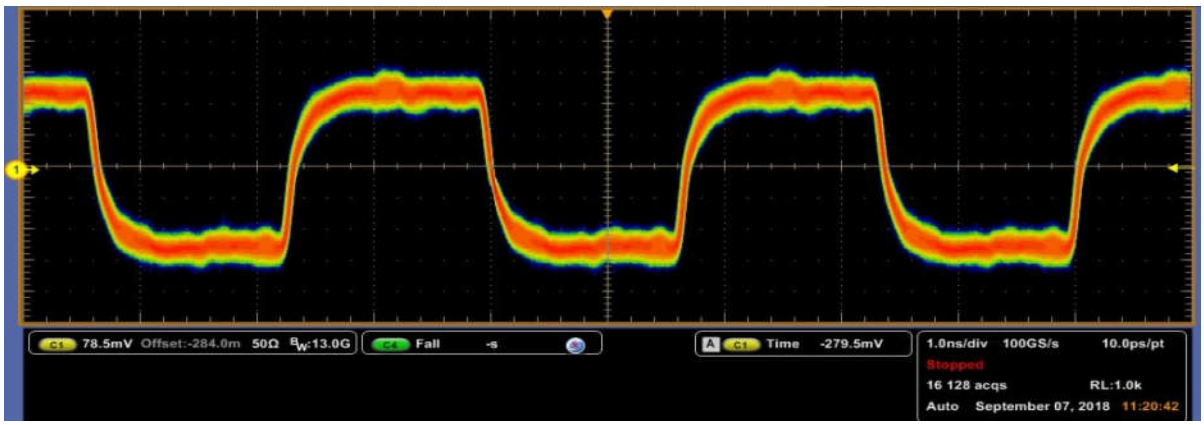
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : CK+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8213V	78.68mV	121.3mV	Pass

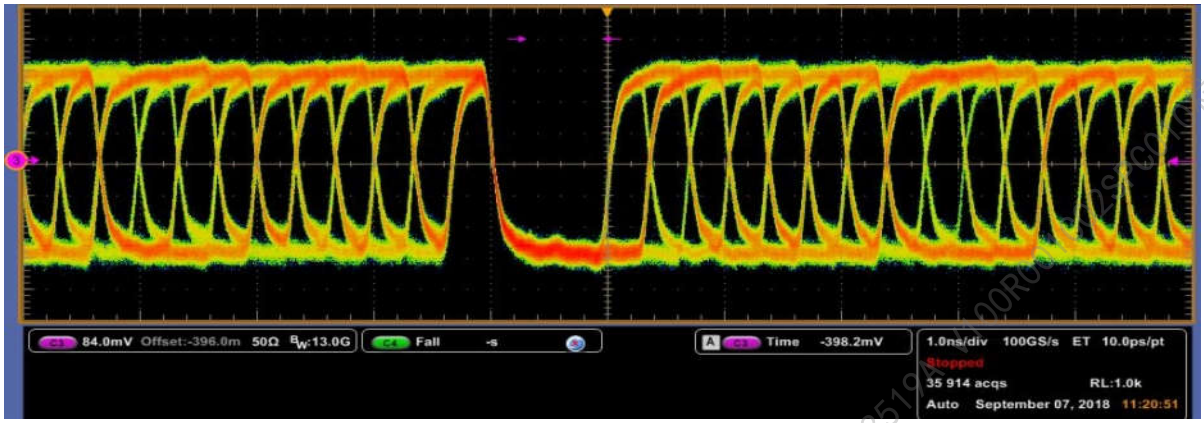
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D0+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.6587V	241.3mV	-41.28mV	Fail

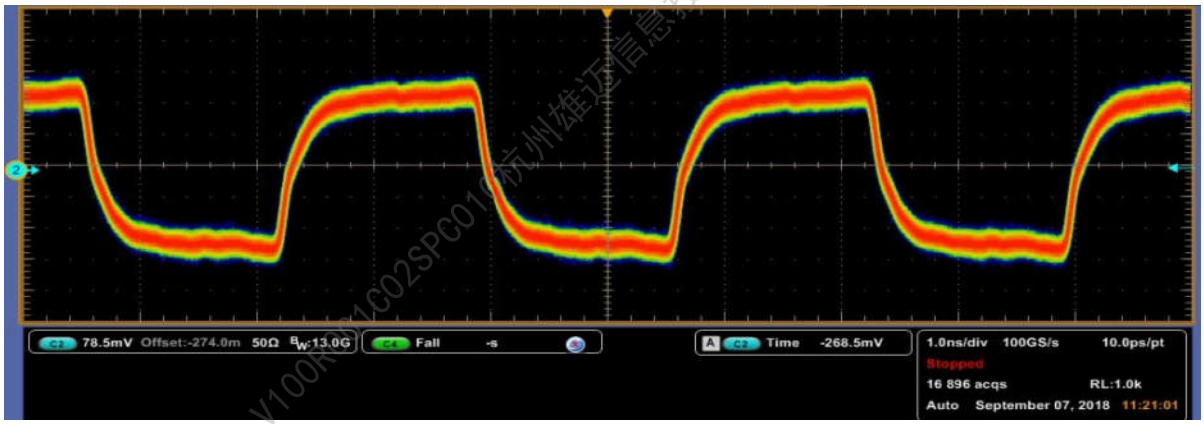
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : CK-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.8439V	56.12mV	143.9mV	Pass

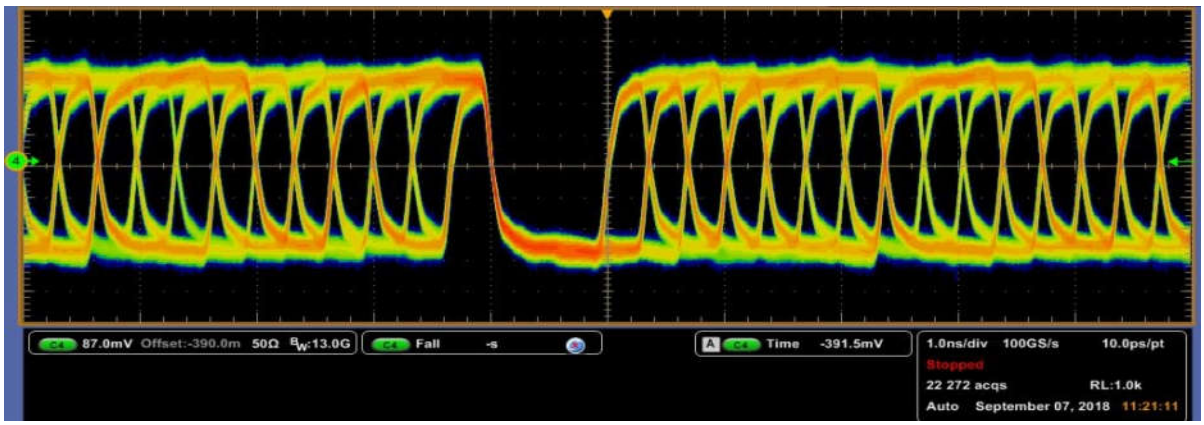
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D0-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.6664V	233.6mV	-33.60mV	Fail

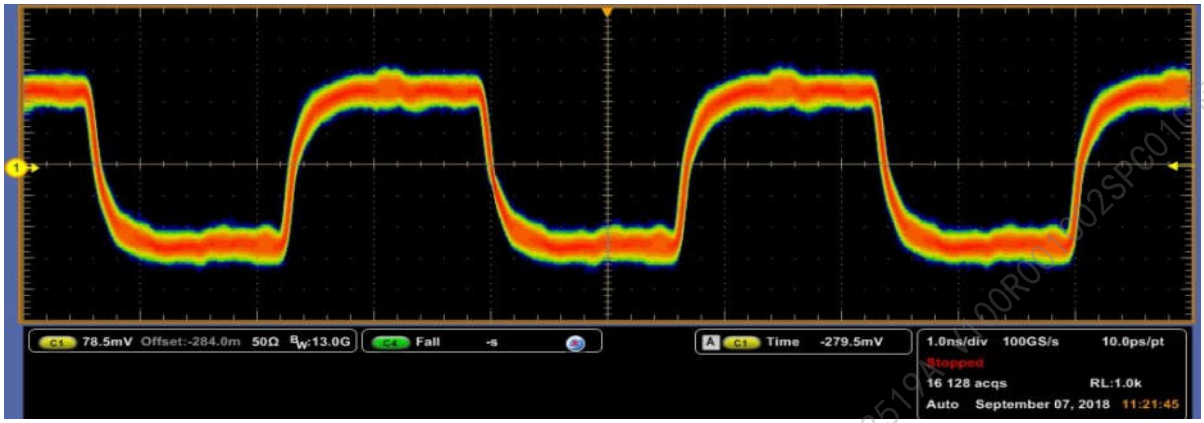
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink > 165MHz) : CK+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.8213V	78.68mV	221.3mV	Pass

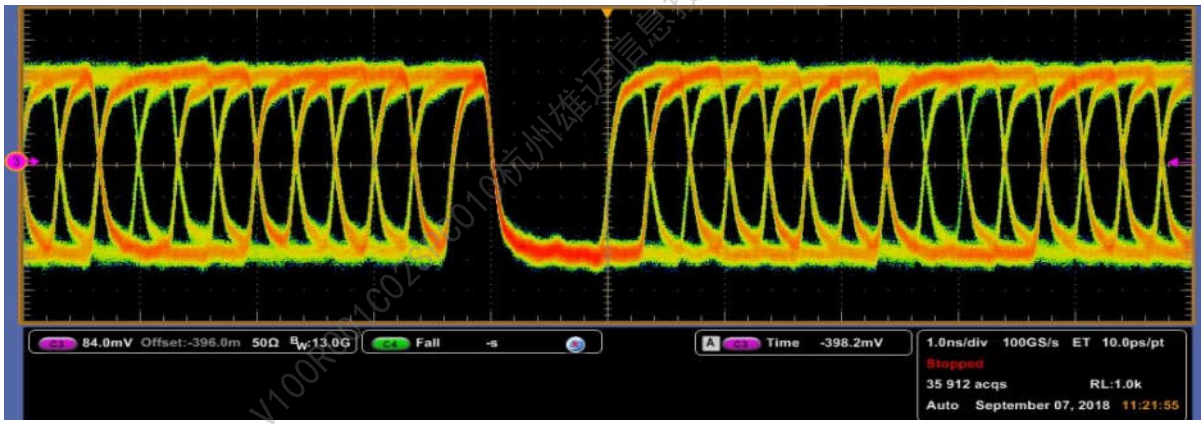
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink > 165MHz) : D0+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.6554V	244.6mV	55.36mV	Pass

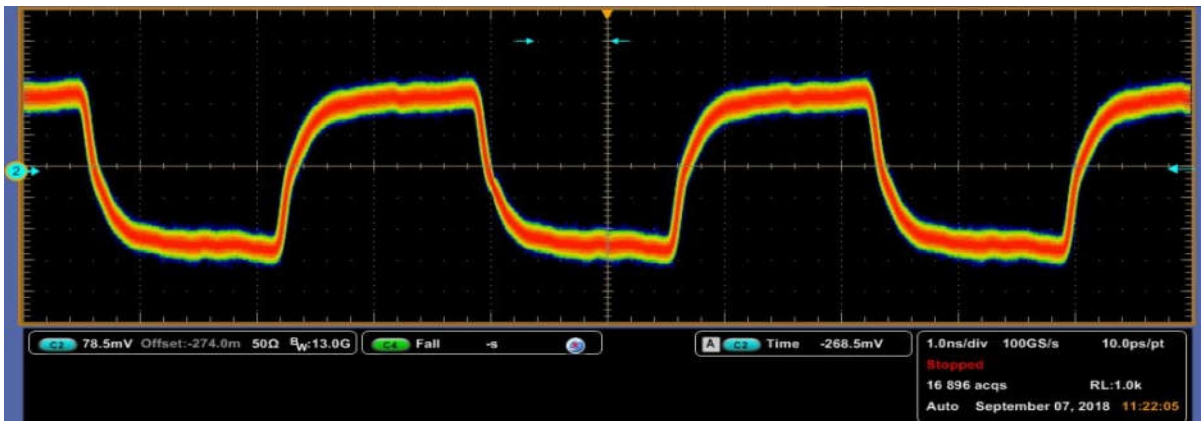
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink > 165MHz) : CK-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.8439V	56.12mV	243.9mV	Pass

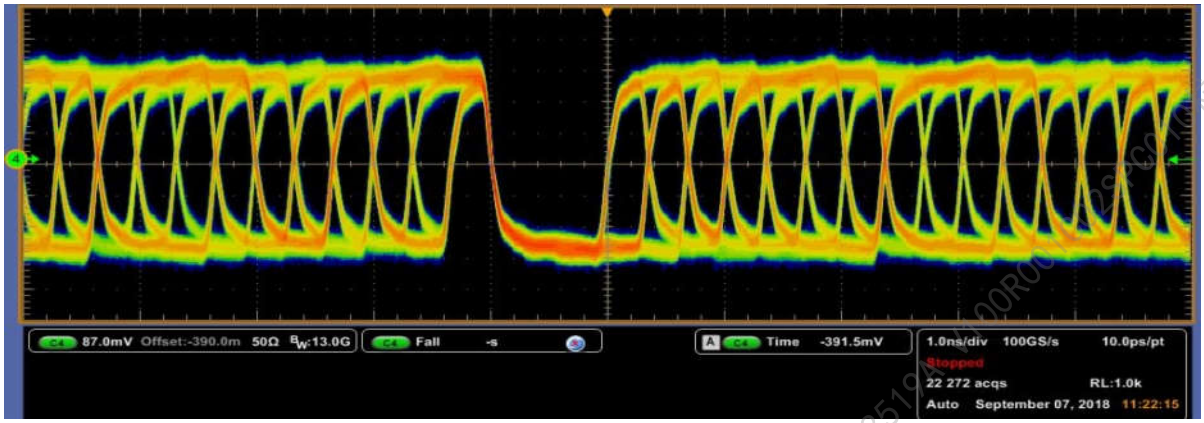
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink > 165MHz) : D0-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.6664V	233.6mV	66.40mV	Pass

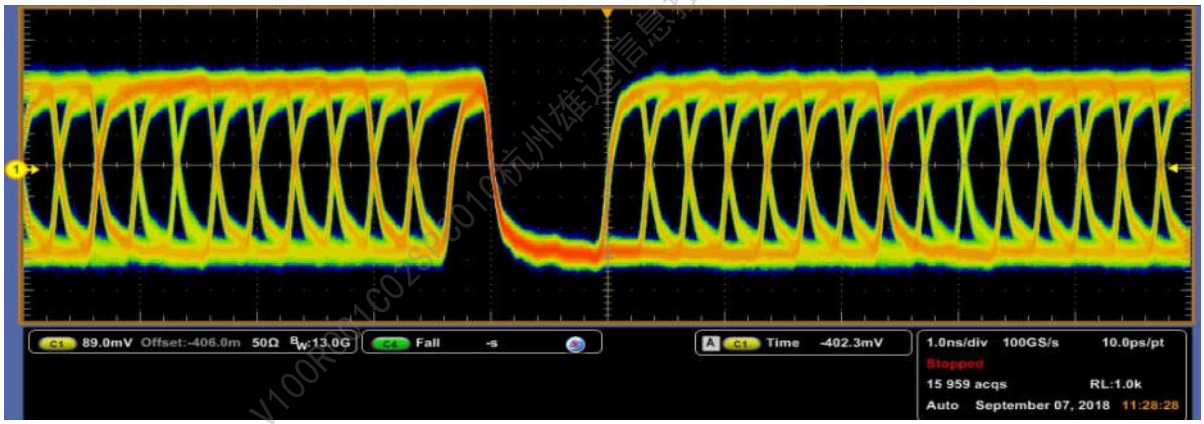
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D1+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.6573V	242.7mV	-42.74mV	Fail

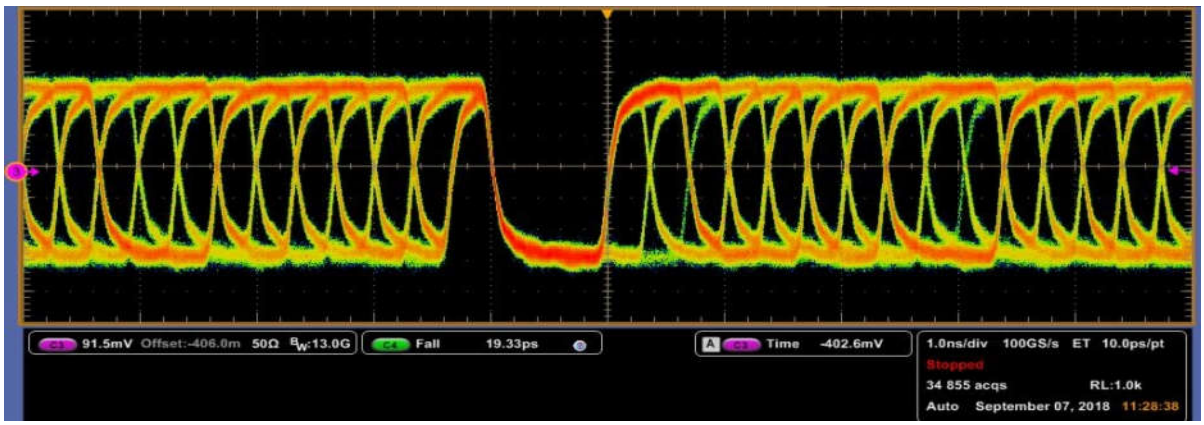
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink <= 165MHz) : D2+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.6982V	201.8mV	-1.810mV	Fail

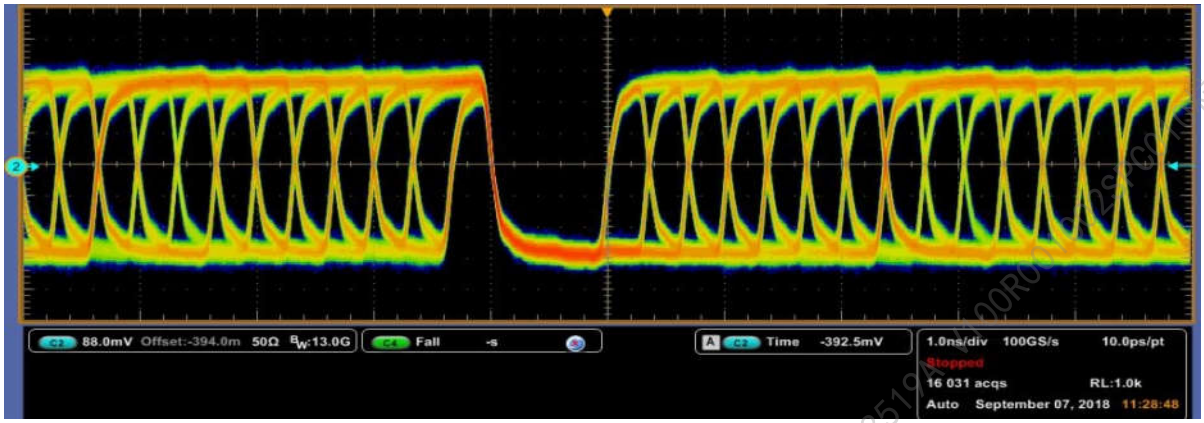
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D1-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.6631V	236.9mV	-36.88mV	Fail

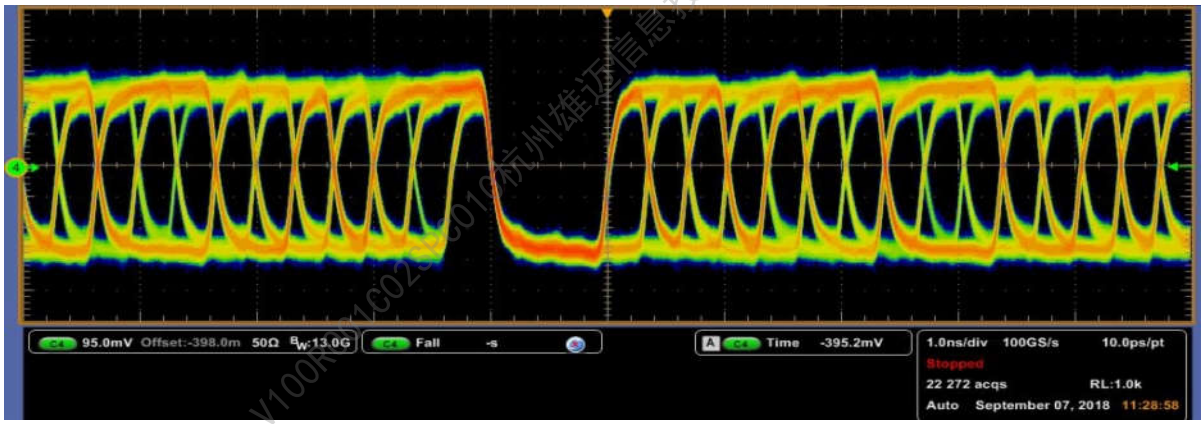
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink <= 165MHz) : D2-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.700V < VL < 2.900V;	2.6702V	229.8mV	-29.80mV	Fail

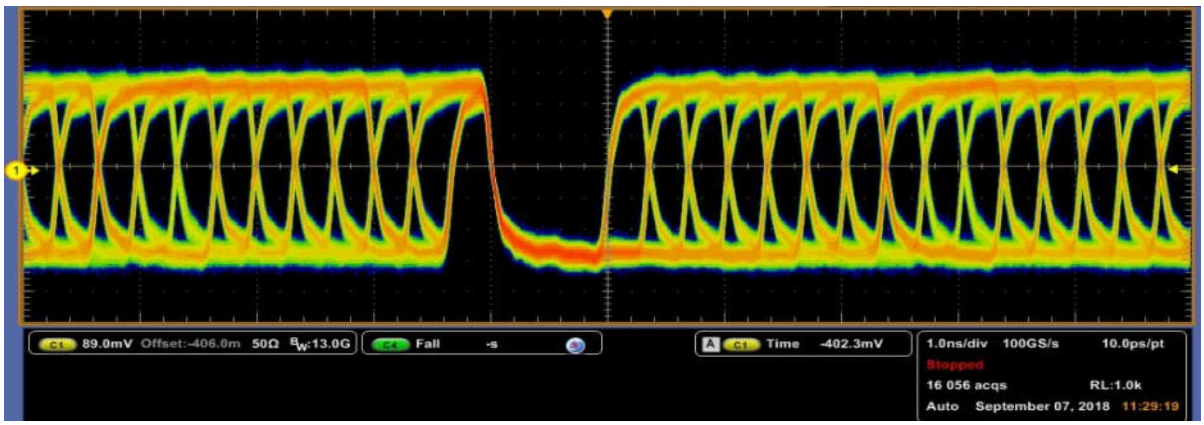
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink > 165MHz) : D1+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.6573V	242.7mV	57.26mV	Pass

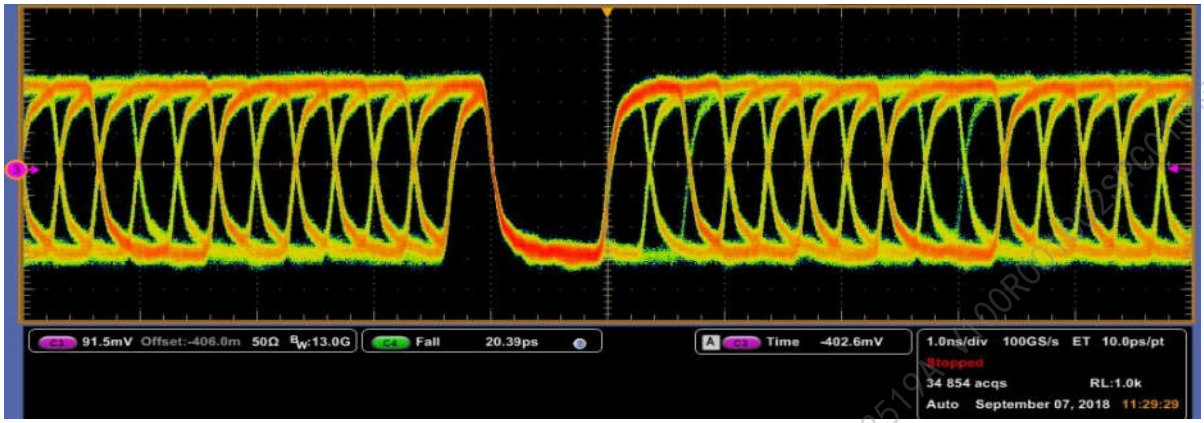
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude +(Supported Sink > 165MHz) : D2+**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.7055V	194.5mV	105.5mV	Pass

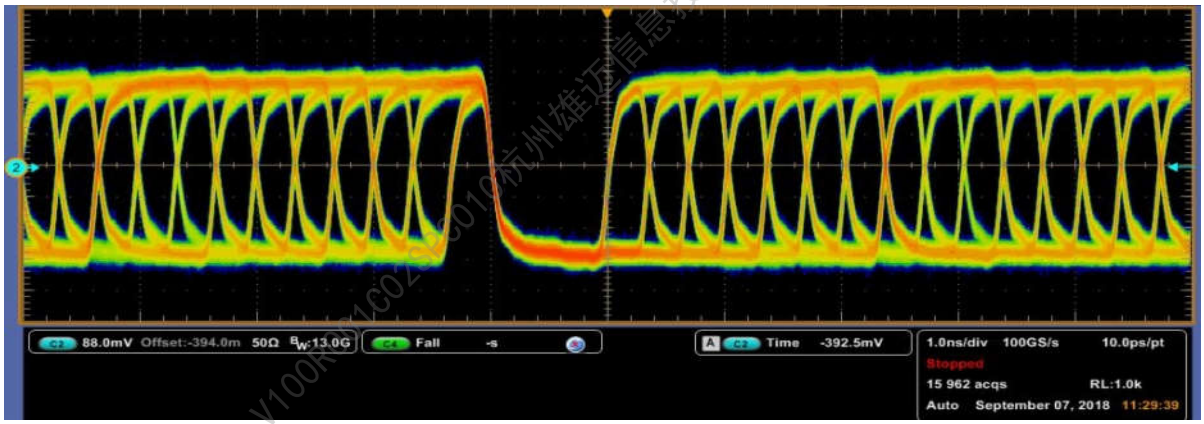
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink > 165MHz) : D1-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.6631V	236.9mV	63.12mV	Pass

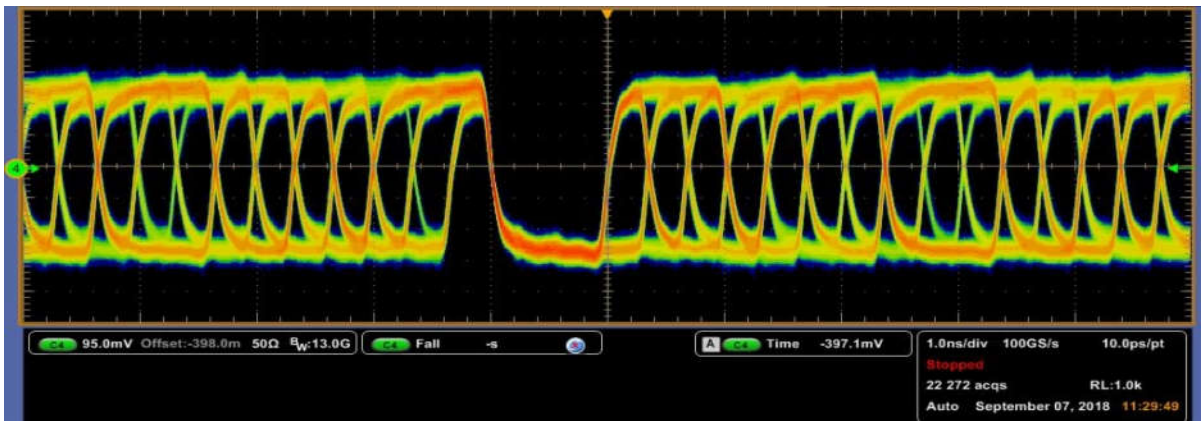
  - **Waveform/Plot**



- **7-2 : Source Low Amplitude -(Supported Sink > 165MHz) : D2-**
  - **Results**

Spec Range	Meas Value	Upper Margin	Lower Margin	Result
2.600V < VL < 2.900V;	2.6664V	233.6mV	66.40mV	Pass

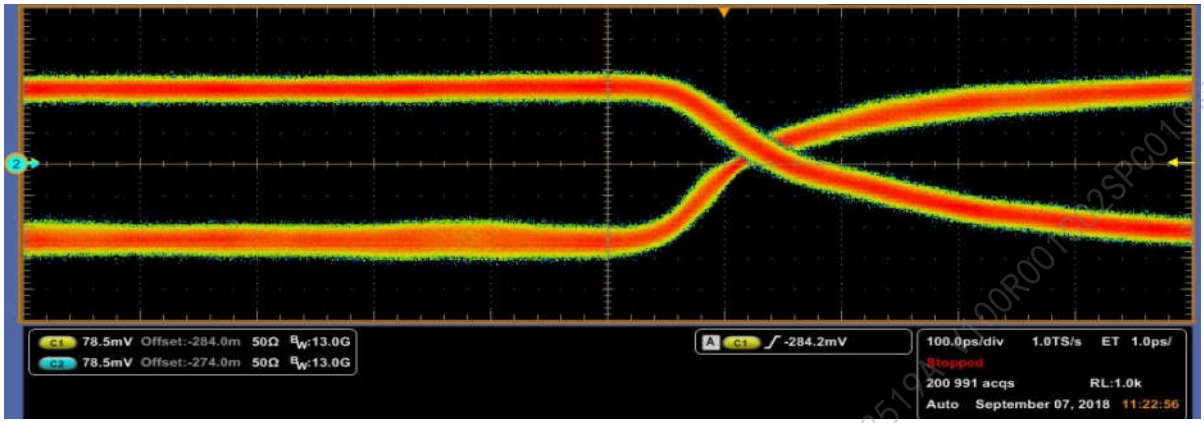
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : CK**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.101*Tbit	336.70ps	0.05*Tbit	Pass

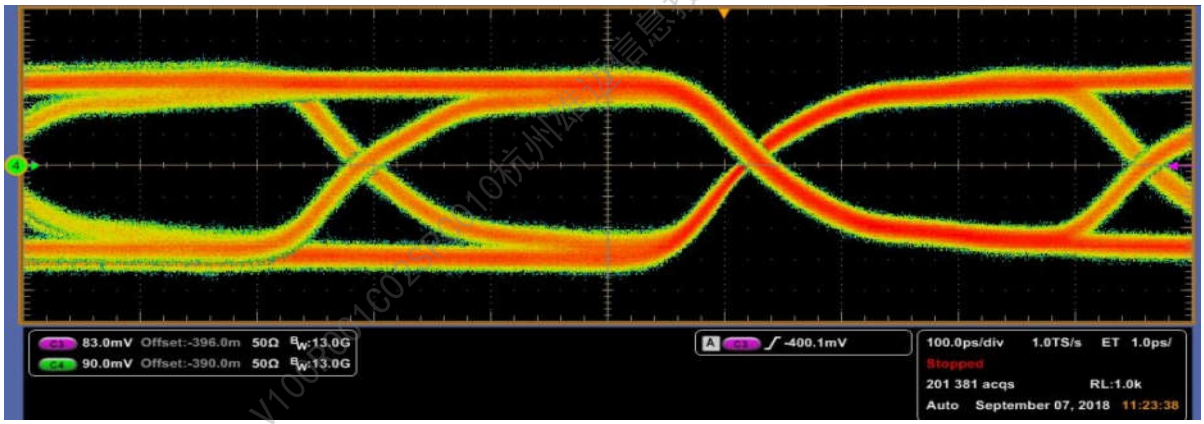
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : D0**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.071*Tbit	336.70ps	0.08*Tbit	Pass

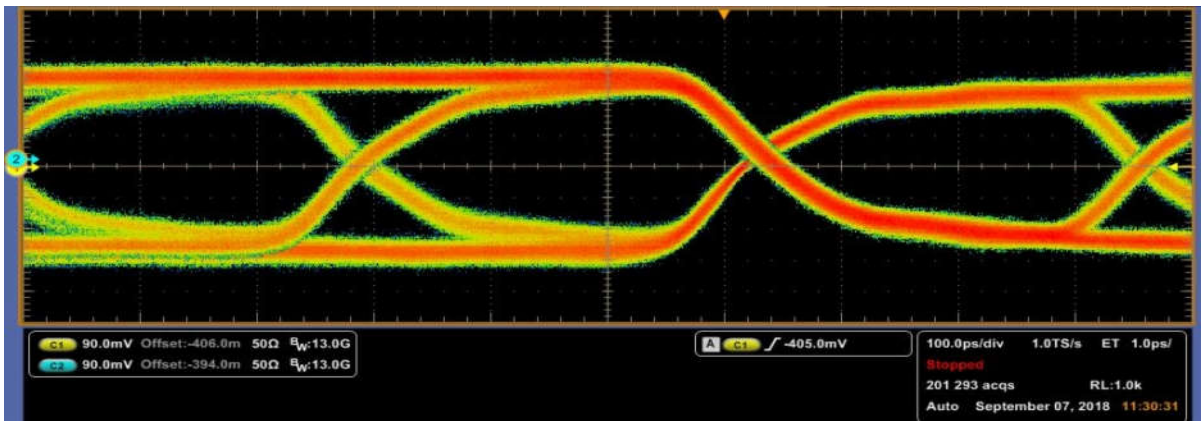
  - **Waveform/Plot**



- **7-7 : Source Intra-Pair Skew : D1**
  - **Results**

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.077*Tbit	336.70ps	0.07*Tbit	Pass

  - **Waveform/Plot**

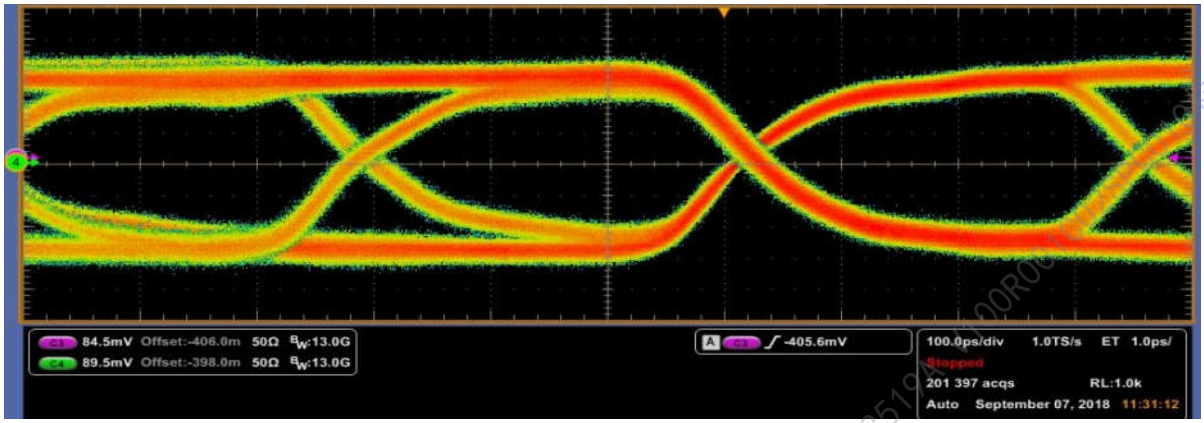


7-7 : Source Intra-Pair Skew : D2

Results

Spec Range	Meas Value	Tbit	Margin	Result
Skew < 0.15*Tbit;	0.059*Tbit	336.70ps	0.09*Tbit	Pass

Waveform/Plot



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