TekExpress HDM

Source Test Report

Setup Information			
DUT ID	DUT001	Scope Model	DPO73304SX
Date/Time	2018-09-07 15:10:43	Scope Serial Number	B320098
Device Type	HDM Physical Layer Solution	SPC, FactoryCalibration	PASS;PASS
TekExpress Version	HDM:10.1.0.40 Framework:4.2.10.28	Scope F/W Version	10.8.5 Build 4
Spec Version	CTS 2.0	DPOJET Version	10.0.5.1
Overall Compliance Mode	Yes	Ch1 Deskew Time (s)	0.000000
Execution Mode	Live	Ch2 Deskew Time (s)	0.000000
Overall Execution Time	0:55:06	Ch3 Deskew Time (s)	0.000000
Overall Test Result	Pass	Ch4 Deskew Time (s)	0.000000
		Probe1 Model	P7313SMA
		Probe1 Serial Number	B021831
		Probe2 Model	P7313SMA
		Probe2 Serial Number	B022061
		Probe3 Model	P7313SMA
		Probe3 Serial Number	B021582
		Probe4 Model	P7313SMA
		Probe4 Serial Number	B022424
DUT COMMENT:	General Comment - HDM2.0 Source		

Test Name Summary Table		
Test Name	Result	Execution Time
HF1-2- TRISE, TFALL	Pass	0:05:12
HF1-3- Inter-Pair Skew	Pass	0:07:04
HF1-5- Differential Voltage	Pass	0:02:58
HF1-6- Clock Duty Cycle and Clock Rate	Pass	0:03:07
HF1-7- Clock Jitter	Pass	0:00:59
HF1-1- VL and VSwing	Pass	0:10:44
HF1-4- Intra-Pair Skew	Pass	0:10:31
HF1-8- Data Eye Diagram	Pass	0:13:47

HF1-2- TRISE, TFALL

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	Clock Rise Time	170.2912	ps	168.3496 ps	5.94 Gbps	Pass	95.2912	75.0000	-	
Clock	Clock Fall Time	168.7065	ps	168.3496 ps	5.94 Gbps	Pass	93.7065	75.0000	-	
D0	D0 Rise Time	65.6485	ps	168.3496 ps	5.94 Gbps	Pass	23.1485	42.5000	-	
D0	D0 Fall Time	65.7442	ps	168.3496 ps	5.94 Gbps	Pass	23.2442	42.5000	-	
D1	D1 Rise Time	65.1342	ps	168.3496 ps	5.94 Gbps	Pass	22.6342	42.5000	-	
D1	D1 Fall Time	65.1725	ps	168.3496 ps	5.94 Gbps	Pass	22.6725	42.5000	-	
D2	D2 Rise Time	68.1270	ps	168.3496 ps	5.94 Gbps	Pass	25.6270	42.5000	-	
D2	D2 Fall Time	69.0679	ps	168.3496 ps	5.94 Gbps	Pass	26.5679	42.5000	-	
COMMENTS										

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HF1-3- Inter-Pair Skew

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
D0	Inter-Pair Skew: D0-D1	-0.0414	Tcharacter	168.3496 ps	5.94 Gbps	Pass	0.1586	-0.2000	0.2000	-41.3776 mTpixel
D1	Inter-Pair Skew: D1-D2	0.1372	Tcharacter	168.3496 ps	5.94 Gbps	Pass	0.0628	-0.2000	0.2000	137.1607 mTpixel
D2	Inter-Pair Skew: D0-D2	0.0958	Tcharacter	168.3496 ps	5.94 Gbps	Pass	0.1042	-0.2000	0.2000	95.7830 mTpixel
COMMENTS										

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HF1-5- Differential Voltage

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	Clock Minimum Differential Voltage	-541.2000	mV	168.3494 ps	3.71 Gbps	Pass	238.8000	-780.0000	-	
Clock	Clock Maximum Differential Voltage	495.0000	mV	168.3494 ps	3.71 Gbps	Pass	285.0000	-	780.0000	
D0	D0 Minimum Differential Voltage	-614.8800	mV	168.3494 ps	3.71 Gbps	Pass	165.1200	-780.0000	-	
D0	D0 Maximum Differential Voltage	600.2400	mV	168.3494 ps	3.71 Gbps	Pass	179.7600	-	780.0000	
D0	D0 Data Jitter	31.0301	ps	168.3494 ps	3.71 Gbps	Informative	N.A	N.A	N.A	
D0	D0 Data Jitter	0.1843	TBit	168.3494 ps	3.71 Gbps	Informative	N.A	N.A	N.A	
	D1 Minimum									

D1	Differential Voltage	-633.3600	mV	168.3494 ps	3.71 Gbps	Pass	146.6400	-780.0000	-	
D1	D1 Maximum Differential Voltage	596.9600	mV	168.3494 ps	3.71 Gbps	Pass	183.0400	-	780.0000	
D1	D1 Data Jitter	28.0582	ps	168.3494 ps	3.71 Gbps	Informative	N.A	N.A	N.A	
D1	D1 Data Jitter	0.1667	TBit	168.3494 ps	3.71 Gbps	Informative	N.A	N.A	N.A	
D2	D2 Minimum Differential Voltage	-621.6000	mV	168.3494 ps	3.71 Gbps	Pass	158.4000	-780.0000	-	
D2	D2 Maximum Differential Voltage	606.8000	mV	168.3494 ps	3.71 Gbps	Pass	173.2000	-	780.0000	
D2	D2 Data Jitter	29.0103	ps	168.3494 ps	3.71 Gbps	Informative	N.A	N.A	N.A	
D2	D2 Data Jitter	0.1723	TBit	168.3494 ps	3.71 Gbps	Informative	N.A	N.A	N.A	
COMMENTS										

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HF1-6- Clock Duty Cycle and Clock Rate

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	Maximum Duty Cycle	50.38	%	168.3496 ps	5.94 Gbps	Pass	-9.62	-	60.00	
Clock	Minimum Duty Cycle	49.80	%	168.3496 ps	5.94 Gbps	Pass	9.80	40.00	-	
Clock	Clock Rate	148.50	MHz	168.3496 ps	5.94 Gbps	Pass	63.50 & 1.50	85	150	
Clock	Maximum Duty Cycle	50.40	%	168.3494 ps	3.71 Gbps	Pass	-9.60	-	60.00	
Clock	Minimum Duty Cycle	49.78	%	168.3494 ps	3.71 Gbps	Pass	9.78	40.00	-	
Clock	Clock Rate	148.50	MHz	168.3494 ps	3.71 Gbps	Pass	63.50 & 1.50	85	150	
COMMENTS										

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HF1-7- Clock Jitter

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	TMDS Clock Jitter at TP2	26.6755	ps	168.3496 ps	5.94 Gbps	Pass	-23.8294	-	50.5049	
Clock	TMDS Clock Jitter at TP2	0.1585	TBit	168.3496 ps	5.94 Gbps	Pass	-0.1415	-	0.3000	
Clock	TMDS VSwing at TP1	727.2917	mV	168.3496 ps	5.94 Gbps	Pass	327.29 & 472.71	400.00	1200.00	
COMMENTS										

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HF1-1- VL and VSwing

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
Clock	TMDS VLow for Clock+	2.7833	V	168.3494 ps	3.71 Gbps	Pass	0.4833 & 0.3167	2.3	3.1	
Clock	TMDS VLow for Clock-	2.7850	V	168.3494 ps	3.71 Gbps	Pass	0.4850 & 0.3150	2.3	3.1	
Clock	VSwing for Clock+	433.6356	mV	168.3494 ps	3.71 Gbps	Pass	233.6356 & 166.3644	200	600	
Clock	VSwing for Clock-	446.0851	mV	168.3494 ps	3.71 Gbps	Pass	246.0851 & 153.9149	200	600	
D0	TMDS VLow for D0+	2.4466	V	168.3494 ps	3.71 Gbps	Pass	0.1466 & 0.4534	2.3	2.9	
D0	TMDS VLow for D0-	2.4567	V	168.3494 ps	3.71 Gbps	Pass	0.1567 & 0.4433	2.3	2.9	
D0	VSwing for D0+	487.5363	mV	168.3494 ps	3.71 Gbps	Pass	87.5363 & 112.4637	400	600	
D0	VSwing for D0-	487.2680	mV	168.3494 ps	3.71 Gbps	Pass	87.2680 & 112.7320	400	600	
D1	TMDS VLow for D1+	2.4462	V	168.3494 ps	3.71 Gbps	Pass	0.1462 & 0.4538	2.3	2.9	
D1	TMDS VLow for D1-	2.4491	V	168.3494 ps	3.71 Gbps	Pass	0.1491 & 0.4509	2.3	2.9	
D1	VSwing for D1+	477.3746	mV	168.3494 ps	3.71 Gbps	Pass	77.3746 & 122.6254	400	600	
D1	VSwing for D1-	490.5342	mV	168.3494 ps	3.71 Gbps	Pass	90.5342 & 109.4658	400	600	
D2	TMDS VLow for D2+	2.4311	V	168.3494 ps	3.71 Gbps	Pass	0.1311 & 0.4689	2.3	2.9	
D2	TMDS VLow for D2-	2.4368	V	168.3494 ps	3.71 Gbps	Pass	0.1368 & 0.4632	2.3	2.9	
D2	VSwing for D2+	489.9346	mV	168.3494 ps	3.71 Gbps	Pass	89.9346 & 110.0654	400	600	
D2	VSwing for D2-	505.1337	mV	168.3494 ps	3.71 Gbps	Pass	105.1337 & 94.8663	400	600	
COMMENTS										

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HF1-4- Intra-Pair Skew

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments

Clock	TMDS Intra-Pair Skew for Clock	20.8375	ps	168.3496 ps	5.94 Gbps	Pass	-4.4150	-	25.2524	
Clock	TMDS Intra-Pair Skew for Clock	0.12	TBit	168.3496 ps	5.94 Gbps	Pass	-0.03	-	0.15	
D0	TMDS Intra-Pair Skew for D0	9.7981	ps	168.3496 ps	5.94 Gbps	Pass	-15.4543	-	25.2524	
D0	TMDS Intra-Pair Skew for D0	0.06	TBit	168.3496 ps	5.94 Gbps	Pass	-0.09	-	0.15	
D1	TMDS Intra-Pair Skew for D1	13.1876	ps	168.3496 ps	5.94 Gbps	Pass	-12.0648	-	25.2524	
D1	TMDS Intra-Pair Skew for D1	0.08	TBit	168.3496 ps	5.94 Gbps	Pass	-0.07	-	0.15	
D2	TMDS Intra-Pair Skew for D2	9.3393	ps	168.3496 ps	5.94 Gbps	Pass	-15.9131	-	25.2524	
D2	TMDS Intra-Pair Skew for D2	0.06	TBit	168.3496 ps	5.94 Gbps	Pass	-0.09	-	0.15	
COMMENTS										

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HF1-8- Data Eye Diagram

Lane Name	Measurement Details	Measured Value	Units	TBit	Data Rate	Test Result	Margin	Low Limit	High Limit	Comments
D0	TMDS Data Eye Diagram Delay on Positive D0 Lane	0	Hits	168.3496 ps	5.94 Gbps	Pass	0	-	0	Data Jitter(ps) on Positive D0 Lane: 56.41
D0	TMDS Data Eye Diagram Delay on Negative D0 Lane	0	Hits	168.3496 ps	5.94 Gbps	Pass	0	-	0	Data Jitter(ps) on Negative D0 Lane: 61.37
D1	TMDS Data Eye Diagram Delay on Positive D1 Lane	0	Hits	168.3496 ps	5.94 Gbps	Pass	0	-	0	Data Jitter(ps) on Positive D1 Lane: 52.42
D1	TMDS Data Eye Diagram Delay on Negative D1 Lane	0	Hits	168.3496 ps	5.94 Gbps	Pass	0	-	0	Data Jitter(ps) on Negative D1 Lane: 56.04
D2	TMDS Data Eye Diagram Delay on Positive D2 Lane	0	Hits	168.3496 ps	5.94 Gbps	Pass	0	-	0	Data Jitter(ps) on Positive D2 Lane: 53.15
D2	TMDS Data Eye Diagram Delay on Negative D2 Lane	0	Hits	168.3496 ps	5.94 Gbps	Pass	0	-	0	Data Jitter(ps) on Negative D2 Lane: 56.51
COMMENTS										

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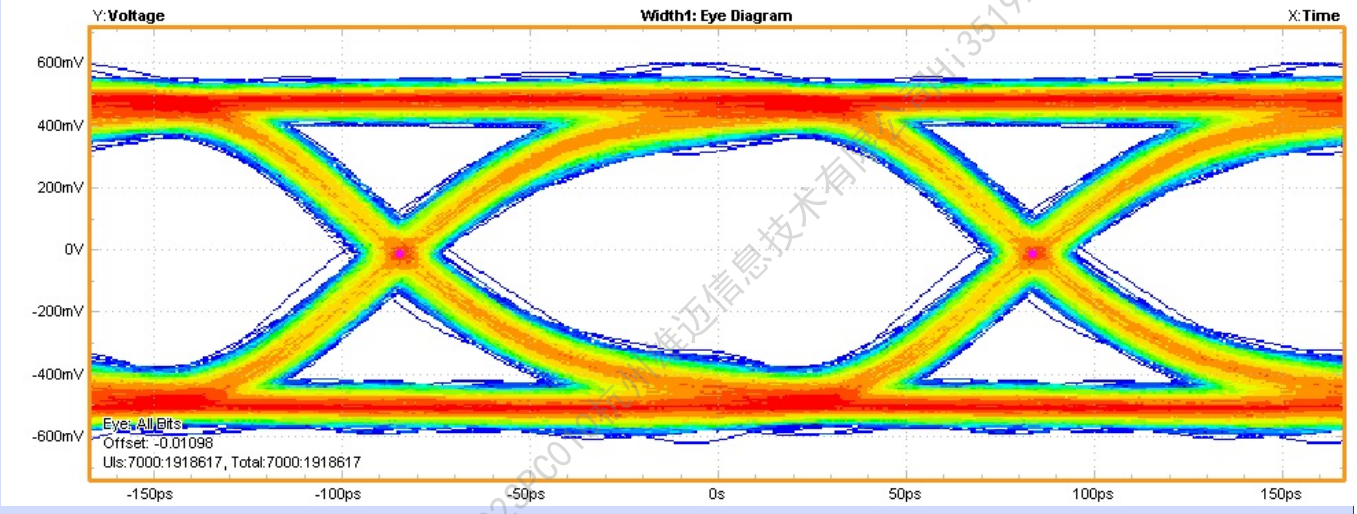
HF1-2- TRISE, TFALL

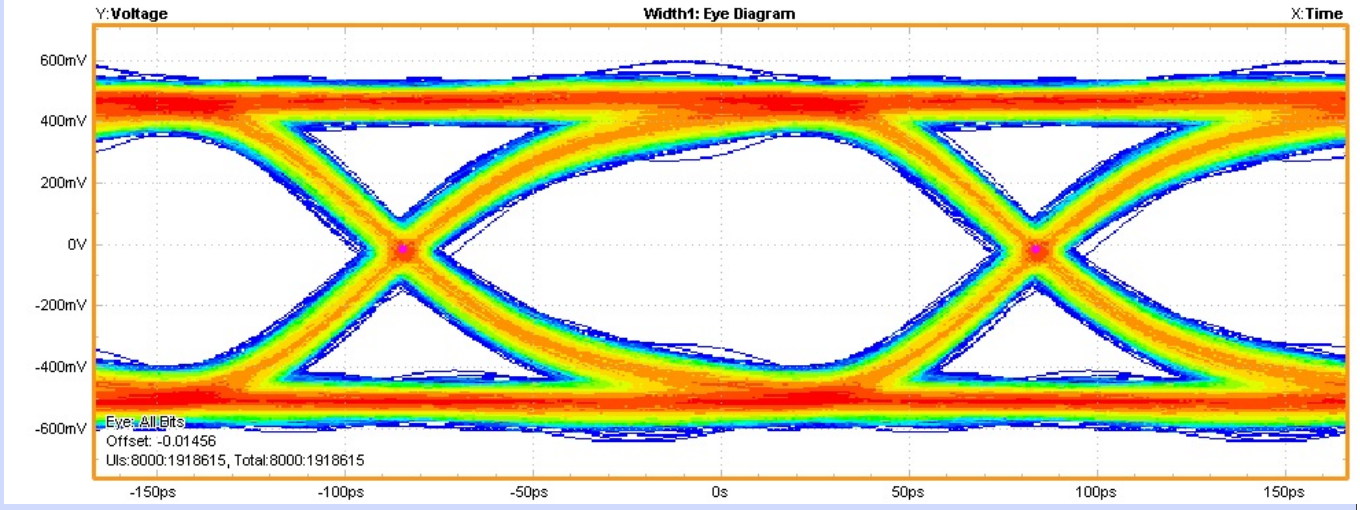
Waveform Plot for Rise Time Fall Time

HF1-5- Differential Voltage

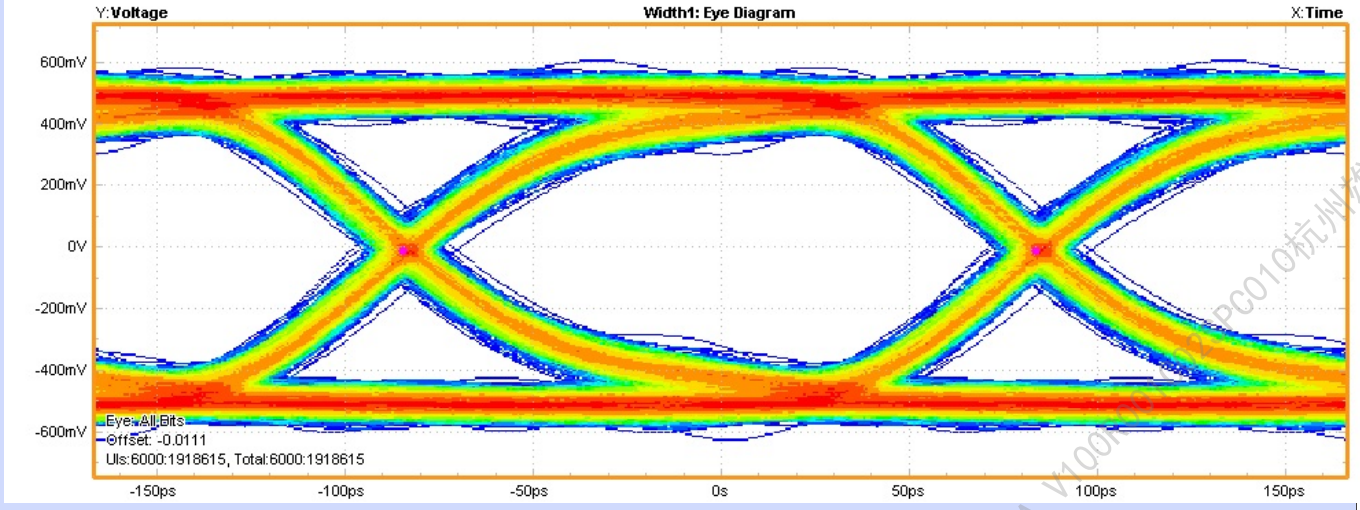
TP1 EyeDiagram- D0



TP1 EyeDiagram- D1

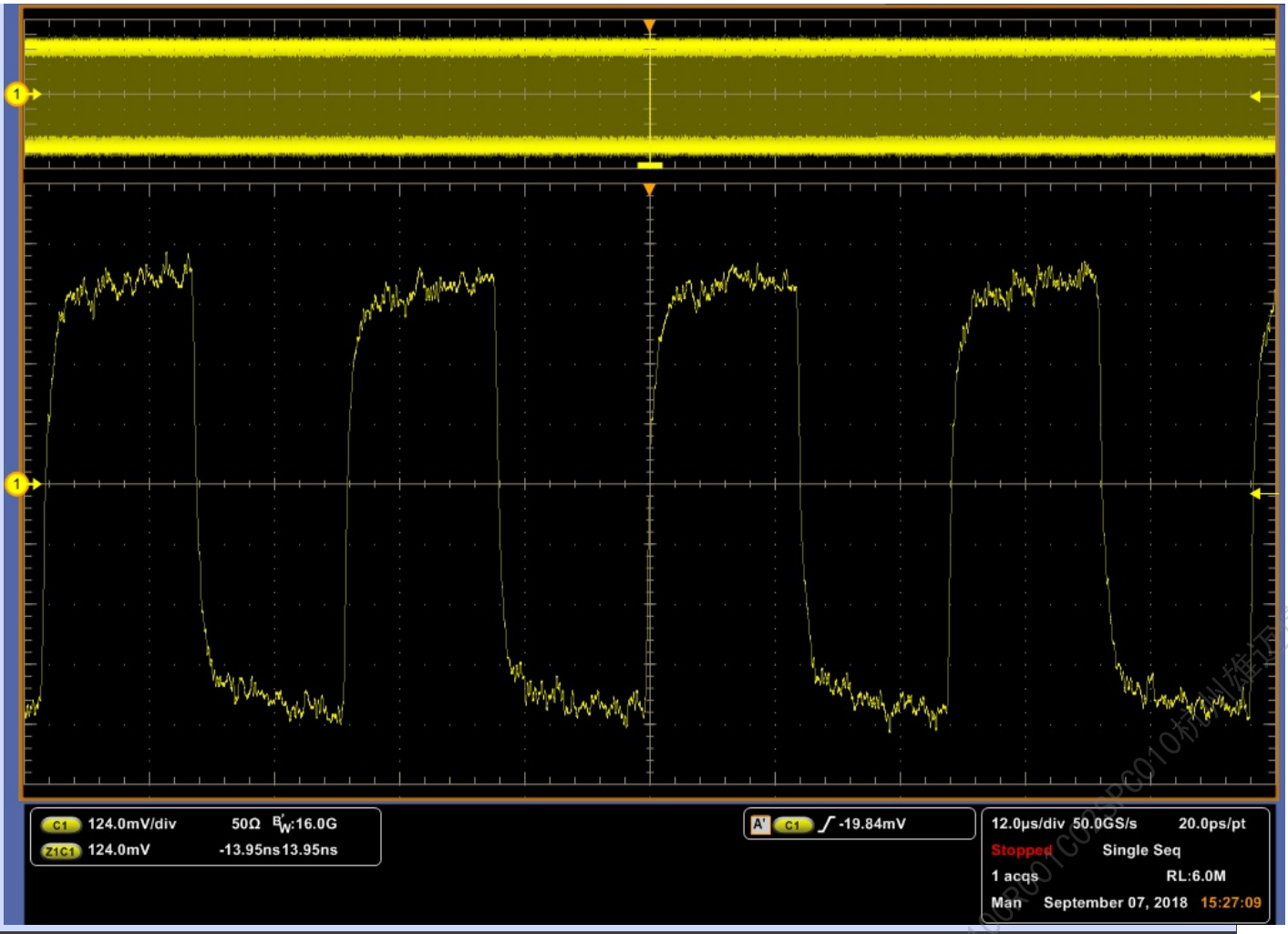


TP1 EyeDiagram- D2



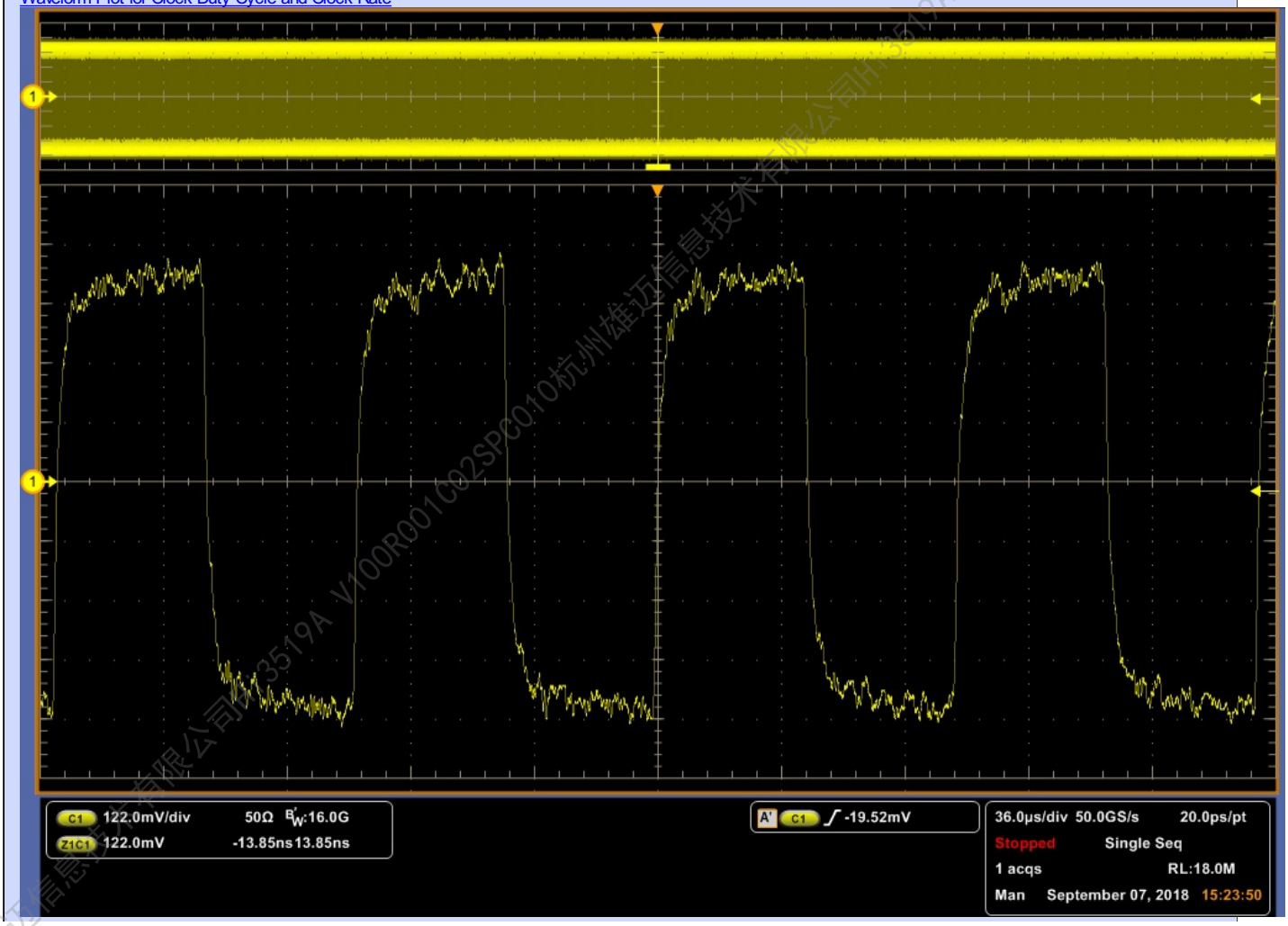
HF1-6- Clock Duty Cycle and Clock Rate

Waveform Plot for Clock Duty Cycle and Clock Rate



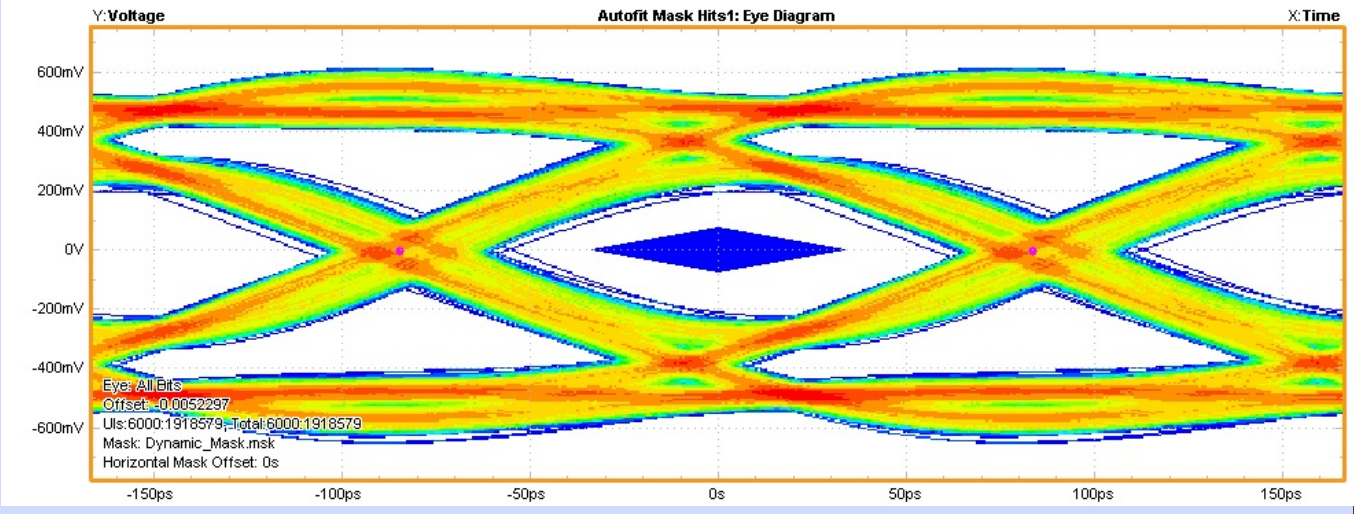
HF1-7- Clock Jitter

Waveform Plot for Clock Duty Cycle and Clock Rate

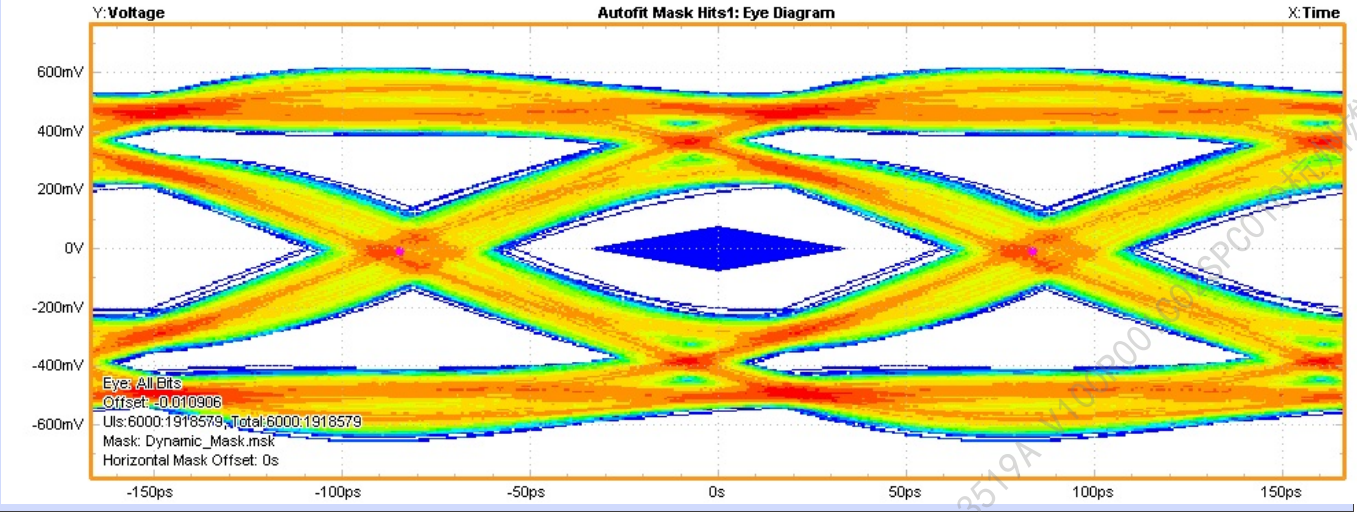


HF1-8- Data Eye Diagram

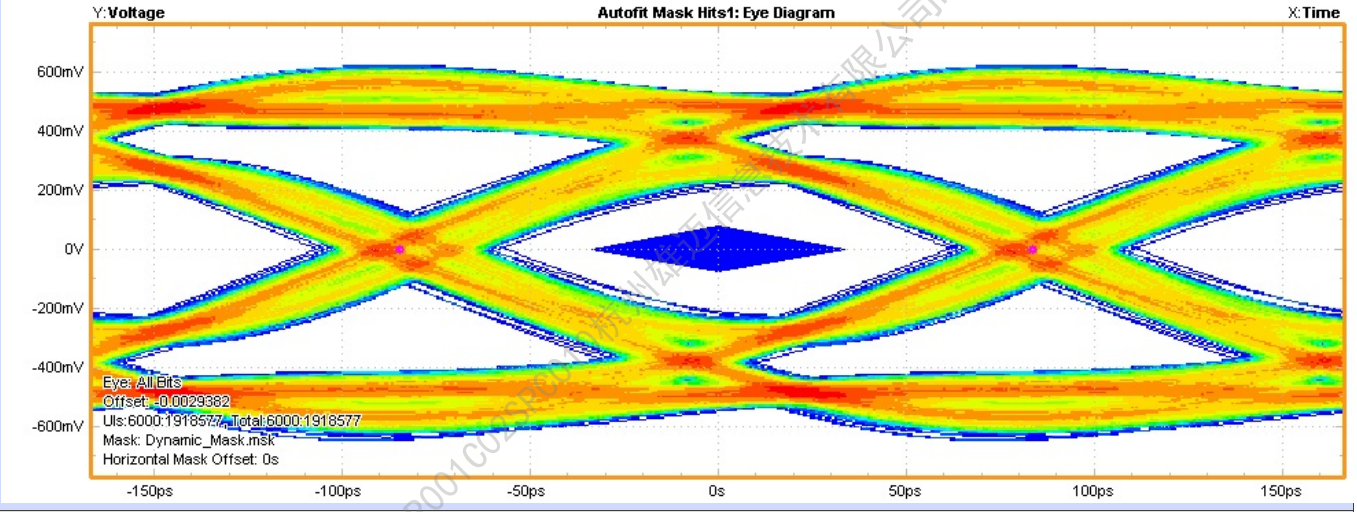
EyeDiagram D0 PositiveLane



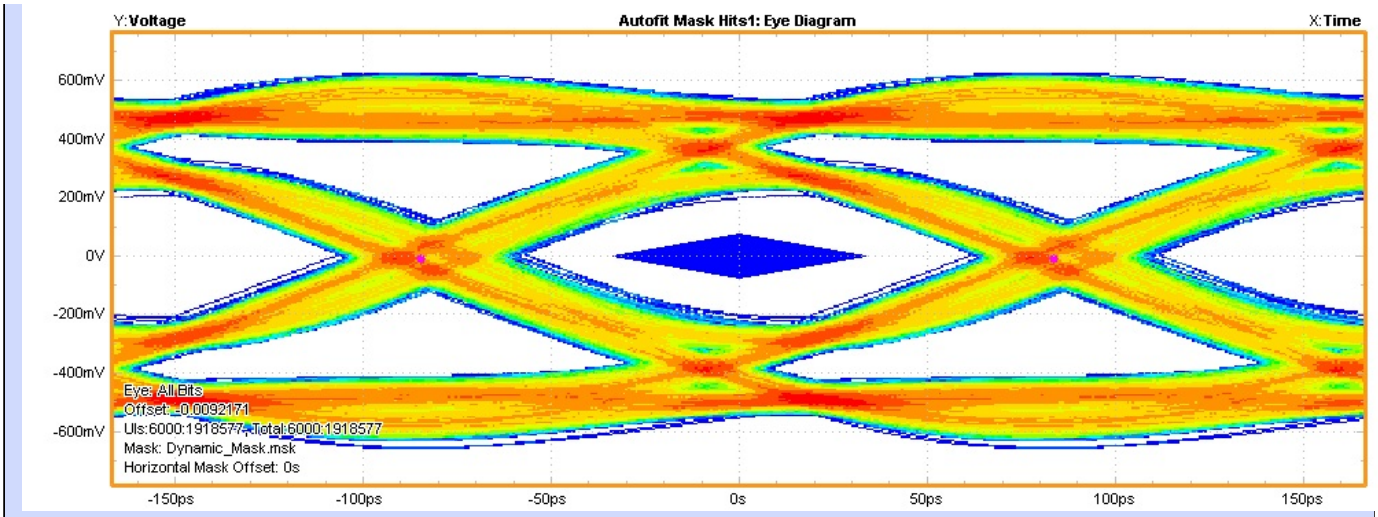
EyeDiagram D0 NegativeLane



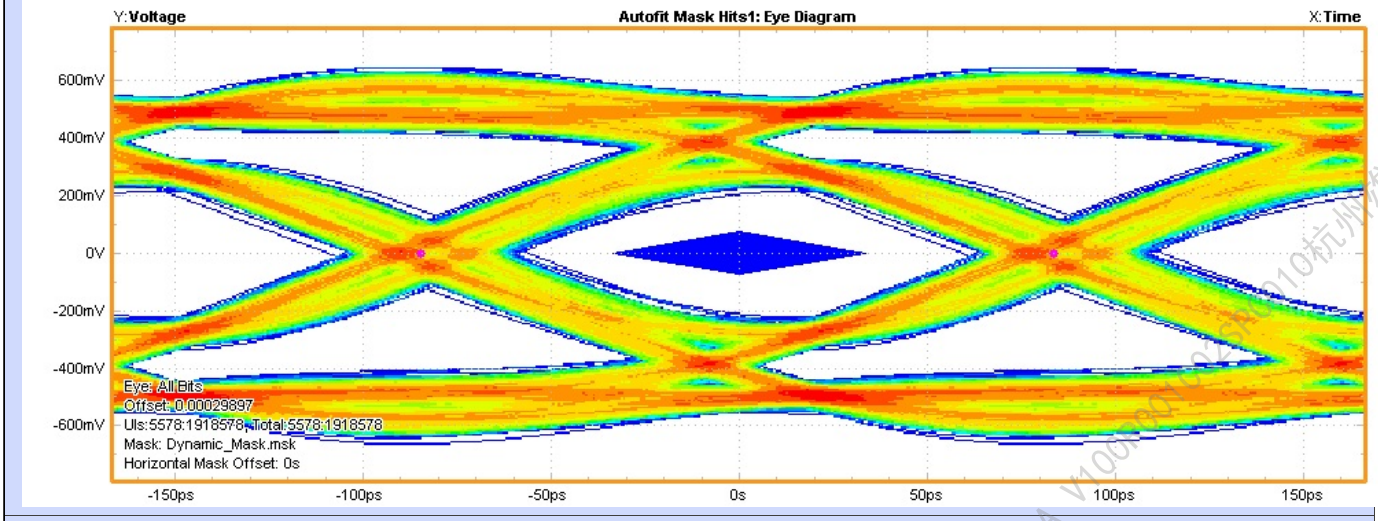
EyeDiagram D1 PositiveLane



EyeDiagram D1 NegativeLane



EyeDiagram D2 PositiveLane



EyeDiagram D2 NegativeLane