

I²CIP: Inter-Integrated Circuit Intra-networking Protocols

Design Report

Jayden Lefebvre - Founder & CEO, Lead Engineer

Northumberland County, ON, Canada

Primary Contact Email: contact@peapodtech.com

Revision 1.0

PeaPod Technologies Inc.

November 2025

Contents

1	Design Abstract	2
2	Design Description	3
2.1	Hardware Specification	4
2.2	Software Protocols	5
3	Design Operations	6
4	Design Requirements	7
5	Design Performance	8
6	Design Potential	9

1 Design Abstract

The Intra-Integrated Circuit Intra-networking Protocols (I²CIP) is a hardware design specification and communications protocols suite that enables hot-swappable, plug-and-play modular components for embedded systems. By leveraging existing I²C components and enhancing them with a bus-switching architecture and dynamic communication protocols, I²CIP allows for rapid prototyping and deployment of embedded systems with minimal configuration. Through this approach, I²CIP aims to revolutionize the way embedded systems are designed and implemented, providing a flexible and scalable solution for developers and engineers.

2 Design Description

The I²CIP technology is designed to facilitate seamless communication and interoperability between various I²C devices in a modular embedded system environment. It achieves this by defining a set of hardware and software standards that enable hot-swapping of components, dynamic routing of data, and efficient management of device resources.

2.1 Hardware Specification

- **Electrical Isolator:** Prevents ground loops and protects sensitive components (**ISO1540**).
- **Level Shifters:** Allows communication between devices operating at different voltage levels.
- **Modules:** A physical collection of one or more I²C devices connected to a common switch, including one SPRT EEPROM and the switch itself.
 - **Switching Multiplexer (MUX):** A bus-switching multiplexer (**TCA9548A**). Eight possible MUX addresses (0x70-0x77) enables the instantiation of up to 8 modules per I²C bus.
 - **SPRT EEPROM:** A non-volatile memory device (**24LC32**) located on MUX bus 0 at default address 0x50. Stores a Static Partial Routing Table (SPRT) encoding intra-network location information for all devices on one switch's subnetworks.
 - **Stuck-Bus Buffer:** A buffer that holds the I²C bus state during module hot-swapping (**TCA4307**).

2.2 Software Protocols

- **Fully-Qualified Addressing** (FQA): Enables unique identification of each device in the network. Encodes I²C bus (3 bits; MSB 0-2), module number (3 bits; MSB 3-5), multiplexer bus (3 bits; MSB 6-8), and device address (7 bits; MSB 9-15) into a single 16-bit address.
- **Quality-of-Service Protocol** (QSP): Pings devices prior to and after any transmission, including multiplexers. Ensures transmission integrity and device availability using acknowledgments and retries with timeouts. Provides error level feedback to the Dynamic Routing Protocol (DRP).
- **Bus Switching Protocol** (BSP): Multiplexer control protocol that manages switching between multiple I²C buses on a single module.
- **Device Lookup Protocol** (DLP): Enables groups of device FQAs to be looked up by ID.
- **Reverse Device Lookup Protocol** (RDLP): Enables devices' IDs to be looked up by their FQA.
- **Intra-network Discovery Protocol** (IDP): Reads SPRT EEPROMs to build two parallel working maps of the intra-network topology: a hash table for DLP and a binary tree for RDLP.
- **Dynamic Routing Protocol** (DRP): Utilizes the working maps generated by IDP and the error level feedback from QSP to inform routing decisions for data transmissions; i.e. if a module is unreachable, DRP will remove the module's devices from the working maps.

3 Design Operations

4 Design Requirements

5 Design Performance

6 Design Potential

References