# $I^2CIP$: Inter-Integrated Circuit Intra-networking Protocols

Requirements for: a Hardware Design Specification for Bus-Switched Hot-Swap Modules of $I^2C$ Targets, and; a Software Library of Intra-Network Communications Protocols for Rapid Implementation of Plug-and-Play Embedded Systems

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# 1 Introduction

## 1.1 Purpose

The purpose of this document is to two-fold:

Outline the categorical requirements (Section 2.2) of an intra-network design specification for hot-swap bus-switched modules of plug-and-play I²C devices, and a software library for communications protocols

Detail the scoped requirements (Section 1.3) for the design and protocols as-proposed by PeaPod Technologies Inc., namely **I²CIP**.

## 1.2 Design Paradigm

All Solutions provided by PeaPod Technologies are fully documented and backed by our rigorous top-down engineering-design paradigm, applied at all steps, enabling us to frame the Problem in such a way that a Solution is a provable and self-evident combination of our Services:

- **2.1 - Problem Statement**: A scoped overview of the opportunity or **Problem**. Anything not covered by this **Statement** is not considered in the execution of the project.
- **2.2 - Solution Requirements**: Categorical requirements for *any* solution to the problem, interpolated from the scope boundaries in the **Problem Statement**. If any of these are not met, the problem is not solved, providing a distinct *pass/fail threshold*, or "razor", for possible Solutions.
- **2.3 - Stakeholders and Values**: *Perspectives* in consideration (i.e. ITCGI, the client, client-of-client), along with a summarized *value proposition* for each person or group, derived from the **Problem Statement** and **Requirements**. These are the people who are and will be *directly affected* by the **Problem**, and as such their **Values** will influence the selection of factors about which we shall select the ideal **Solution**.
- **2.4 - Problem-Solving Goals**: *Conceptual* design goals (e.g. Safety, Efficiency) derived from **Requirements** and **Stakeholder Values**.

- **2.5 - Solution Objectives**: *Tactical* implementation targets derived from the **Requirements** and **Goals**.
- **2.6 - Metrics**: Granular, *quantitative* measures of design success/fit/utility/etc. derived from the **Objectives**, which are either Constrained or Graded according to the **Requirements**, **Goals**, and **Objectives**.
- **2.7 - Constraints**: *Mandatory* thresholds (i.e. true/false, pass/fail) and extrema (minima, maxima) for evaluating and disqualifying proposed solutions along Constrained **Metrics**.
- **2.8 - Criteria**: *Points-based* system for evaluating and ranking proposed solutions along Graded **Metrics**.

## 1.3 Scope and Justification

### 1.3.1 I²C Specification

From the I²C Specification Version 7 (2021, *NXP Semiconductors*): 8-bit-oriented one-ended (controller-driven) bidirectional (read & write) serial communication over a 2-wire bus (data "SDA" & clock "SCL") for integrated circuit "devices" ("targets"), including (but not limited to):

- **Remote Multi-Channel Ports**: GPIO banks, internal-clock PWM drivers, A/D and D/A converters, etc.
- **System Devices**: real-time clocks, LCD screens, etc.
- **Data Storage Devices**: EEPROM, SRAM, FRAM, etc.
- **Digital Sensors**: temperature, light, speed, pressure, etc.

The I²C Specification can be imagined as an incomplete analogue to the Internet's OSI Model, with the following layers defined:

SC1. **Physical Layer** - Compare to RJ45

   (a) **VDD & GND** - +5 VDC

   (b) **SDA & SCL** - Pull-Up Bias Resistors (10 kΩ)

SC2. **Data Link Layer** - Compare to Ethernet

   (a) **Controller** - Bus Speed Control, Start & Stop Conditions, Multi-Controller Arbitration

   (b) **Targets** - 7-bit Device Addressing, Acknowledgement ("ACK")

   (c) **Packet Structure** Read & Write Flags, 8-/16-bit Register Addressing, Byte-Stream Data

The **Network** (data routing), **Transport** (data delivery), and **Session** (transmission context) layers of the OSI model analogy are not defined by the I²C Specification. The following proposed extensions to the I²C Specification, the focus of the **I²CIP** design, are intended to fill this gap, enabling **Presentation** and **Application** layer functionality to be rapidly implemented by developers for embedded systems.

### 1.3.2 Switched-Bus Intra-Networking

Suppose an I²C target device $D$ with $N$ possible unique addresses. An I²C bus controller can communicate with $N$ uniquely-addressed instantiations of $D$ on one bus without conflict or modification to connections.

Suppose an I²C target device with $M$ possible unique addresses that acts as a multiplexer and repeater ("switch") for $B$ bitwise-enabled output busses ("subnets"). An I²C bus controller can communicate with $M \cdot B \cdot N$ independently-addressable instantiations of $D$ across $M \cdot B$ subnets by setting ONE active output bus on each of the $M$ switches (and disabling ALL on the remaining $M - 1$).

Example: For $M = 8$ switches with $B = 8$ subnets each, the total number of uniquely-addressable instantiations of $D$ on an I²CIP intra-network is $8 \cdot 8 \cdot N = 64N$, effectively enabling a 64-fold increase in independently-addressable targets of all types by a single controller.

SC3. **Network Layer** - Fully-Qualified Addressing ("FQA") - Compare to IP Addressing

SC4. **Transport Layer** - Switch & Target Ping and Target Control with Quality-of-Service 2 ("only-once" delivery) via ACK - Compare to TCP

SC5. **Session Layer** - Target Discovery & Module Configuration via Dedicated EEPROM Target

## 1.4 Definitions

A number of useful definitions have emerged from the above scoping:

1. **Switch** - An I²C target device that acts as a repeater for bitwise multiplexed output busses.
2. **Subnet** - A specific output bus of a specific switch.
3. **Intra-Network** - A general term referring to ALL routable targets (not including switches) on ALL subnets across ALL of a controller's I²C busses (in the case of multiple controller busses).
4. **Fully-Qualified Address (FQA)** - A unique intra-network routing location identifier, encoding: a specific I²C bus (in the case of multiple controller busses), and; a specific Subnet,

and; a target's address.

5. **Module** - A switch, and; a physical collection of targets located on the switch's subnets, and; a data storage target with a predetermined address with all routing information for all targets on this switch's subnets.

# 2 Framing

## 2.1 Problem Statement

## 2.2 Solution Requirements

The following are the overall challenge requirements compiled from A, B, and an excerpt from C:

R1. **Must** lorem ipsum dolor sit amet, consectetur adipiscing elit:

   (a) **Should** lorem ipsum dolor sit amet, consectetur adipiscing elit;

## 2.3 Stakeholders and Values

S1. A - Values, etc.

S2. B - DfX, etc.

## 2.4 Problem-Solving Goals

HL1. Goal ABC (S1, R1, R1a)

## 2.5 Solution Objectives

LL1. Objective ABC (HL1)

## 2.6 Metrics

| # | Metric | | Units |
|---|---|---|---|
| M1 | Metric ABC | (LL1) | Yes/No |
| M2 | Metric XYZ | (LL1) | 0 - 100% |

## 2.7 Constraints

| Metric | Constraint | Justification |
|---|---|---|
| M1 | Yes | (S1) |

## 2.8 Criteria

| Metric | Criteria | Justification |
|---|---|---|
| M2 | Should Maximize | (R1a) |

# 3 Reference Designs

## 3.1 Reference Design XYZ

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