I^{2}CIP: Inter-Integrated Circuit Intra-networking Protocols

Requirements for a Hardware Design Specification for a Bus-Switched Intra-Network of Hot-Swap Modules of I^{2}C Targets and a Software Library of Intra-Network Communications Protocols for Rapid Implementation of Plug-and-Play Embedded Systems

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1   Introduction

1.1   Purpose

The purpose of this document is to two-fold:

1. Outline the categorical requirements (Section 2.2) of an intra-network design specification for hot-swap bus-switched modules of plug-and-play I²C devices, and a software library for communications protocols

2. Detail the scoped requirements (Section 1.3) for the design and protocols as-proposed by PeaPod Technologies Inc., namely **I²CIP**.

1.2   Design Paradigm

All Solutions provided by PeaPod Technologies are fully documented and backed by our rigorous top-down engineering-design paradigm, applied at all steps, enabling us to frame the Problem in such a way that a Solution is a provable and self-evident combination of our Services:

- **2.1 - Problem Statement**: A scoped overview of the opportunity or **Problem**. Anything not covered by this **Statement** is not considered in the execution of the project.

- **2.2 - Solution Requirements**: Categorical requirements for *any* solution to the problem, interpolated from the scope boundaries in the **Problem Statement**. If any of these are not met, the problem is not solved, providing a distinct *pass/fail threshold*, or "razor", for possible Solutions.

- **2.3 - Stakeholders and Values**: *Perspectives* in consideration (i.e. ITCGI, the client, client-of-client), along with a summarized *value proposition* for each person or group, derived from the **Problem Statement** and **Requirements**. These are the people who are and will be *directly affected* by the **Problem**, and as such their **Values** will influence the selection of factors about which we shall select the ideal **Solution**.

- **2.4 - Problem-Solving Goals**: *Conceptual* design goals (e.g. Safety, Efficiency) derived from **Requirements** and **Stakeholder Values**.

- **2.5 - Solution Objectives**: *Tactical* implementation targets derived from the **Requirements** and **Goals**.

- **2.6 - Metrics**: Granular, *quantitative* measures of design success/fit/utility/etc. derived from the **Objectives**, which are either Constrained or Graded according to the **Requirements**, **Goals**, and **Objectives**.

- **2.7 - Constraints**: *Mandatory* thresholds (i.e. true/false, pass/fail) and extrema (minima, maxima) for evaluating and disqualifying proposed solutions along Constrained **Metrics**.

- **2.8 - Criteria**: *Points-based* system for evaluating and ranking proposed solutions along Graded **Metrics**.

1.3   Scope and Justification

1.3.1   I²C Specification

From the I²C Specification Version 7 (2021, *NXP Semiconductors*): an 8-bit-oriented one-ended ("controller"-driven) bidirectional (read & write) serial communication over a 2-wire bus (data "SDA" & clock "SCL") for integrated circuit devices ("targets"), including (but not limited to):

- **Remote Multi-Channel Ports**: GPIO banks, internal-clock PWM drivers, Analog-to-Digital and Digital-to-Analog converters, etc.

- **System Devices**: real-time clocks, LCD screens, microcontrollers, etc.

- **Data Storage Devices**: EEPROM, SRAM, FRAM, etc.

- **Digital Sensors**: temperature, humidity, light, acceleration, pressure, etc.

1.3.2   OSI Model Analogue for I²C

The I²C Specification can be imagined as an incomplete analogue to the Internet's OSI Model, with the following layers defined:

SC1. **Physical Layer**

　(a) **VDD & GND**: +5 VDC

　(b) **SDA & SCL**: Pull-Up Bias Resistors (e.g. 10 kΩ)

SC2. **Data Link Layer**

　(a) **Controller**: Bus Speed Control, Start & Stop Conditions, Multi-Controller Arbitration

　(b) **Targets**: 7-bit Device Addressing, Acknowledgement ("ACK")

　(c) **Packet Structure**: "Read" & "Write" Flags, 8-/16-bit Register Addressing, Byte-Stream Data

　　The **Network** (data routing), **Transport** (data delivery), and **Session** (transmission context) layers of the OSI model analogy are not defined by the I²C Specification. The following proposed extensions to the I²C Specification, the focus of the **I²CIP** design, are intended to fill this gap, enabling **Presentation** and **Application** layer functionality to be rapidly implemented by developers for embedded systems (e.g. control systems).

1.3.3   Switched-Bus Intra-Networking

Suppose an I^{2}C target device D with N possible unique addresses. A standard I^{2}C bus controller C can communicate with N uniquely-addressed instantiations of D on each I^{2}C bus without modification to connections or encountering conflict.

Suppose a type of I^{2}C target device X with M possible unique addresses that acts as a multiplexer and repeater ("switch") for B bitwise-enabled output busses ("subnetworks"). Using this switch device X, the I^{2}C bus controller C can communicate with $M \cdot B \cdot N$ independently-addressable instantiations of the target device D across $M \cdot B$ subnetworks by setting ONE active output bus on each of the M switches (and disabling ALL on the remaining $M - 1$).

1.3.4   Extended OSI Model for I^{2}CIP

Supposing $M = 8$ switches with $B = 8$ subnetworks each, the total number of uniquely-addressable instantiations of D on an I^{2}CIP intra-network is $8 \cdot 8 \cdot N = 64N$, effectively enabling a 64-fold increase in independently-addressable targets of all types by a single controller.

For the purposes of effective intra-network communication across switched subnetworks, it is proposed that a "fully-qualified address" be implemented at the controller level, comprising routing information that encodes the I^{2}C bus, switch address, and subnetwork number, alongside the target device address, for each target device.

Suppose a dedicated target device E consisting of EEPROM memory containing routing information for all devices on all subnetworks of one switch. If this EEPROM device E is granted a fixed address on a consistent subnetwork on each switch, the controller can reliably retrieve routing information for all devices on all subnetworks of any switch by querying each switch's dedicated EEPROM device.

Together, the EEPROM device E, the switch device X, and all devices on all subnetworks of the switch X comprise a **Module**.

SC3. **Network Layer**: Fully-Qualified Addressing ("FQA")

SC4. **Transport Layer**: Switch & Target Ping Prior to Target Control with Quality-of-Service 2 ("only-once" delivery) via ACK

SC5. **Session Layer**: Target Discovery & Module Configuration via Dedicated EEPROM Target

1.4   Definitions

A number of useful definitions have emerged from the above scoping:

1. **Switch**: An I²C target device that acts as a repeater for bitwise multiplexed output busses.

2. **Subnetwork**: A specific output bus of a specific switch.

3. **Intra-Network**: A general term referring to all routable targets (not including switches) on all subnetworks across all of a controller's I²C busses.

4. **Fully-Qualified Address (FQA)**: A unique intra-network routing location identifier, encoding: a specific I²C bus, and; a specific subnetwork (i.e. switch and bus), and; a target's I²C address.

5. **Module**: A switch, and; a physical collection of targets located on the switch's subnetworks, and; a data storage target with a predetermined address with all routing information for all targets on this switch's subnetworks.

2 Framing

2.1 Problem Statement

2.2 Solution Requirements

The following are the overall challenge requirements compiled from A, B, and an excerpt from C:

R1. **Must** lorem ipsum dolor sit amet, consectetur adipiscing elit:

    (a) **Should** lorem ipsum dolor sit amet, consectetur adipiscing elit;

2.3 Stakeholders and Values

S1. A - Values, etc.

S2. B - DfX, etc.

2.4   Problem-Solving Goals

HL1. Goal ABC   (S1, R1, R1a)

2.5   Solution Objectives

LL1. Objective ABC   (HL1)

2.6   Metrics

#	Metric		Units
M1	Metric ABC	(LL1)	Yes/No
M2	Metric XYZ	(LL1)	0 - 100%

2.7   Constraints

Metric	Constraint	Justification
M1	Yes	(S1)

2.8   Criteria

Metric	Criteria	Justification
M2	Should Maximize	(R1a)

3   Reference Designs

3.1   Reference Design XYZ

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