

## Individual Assignment 2.1 - Document

I used Altium Designer 19 as my CAD tool.

### Footprint and Schematic Symbol Creation

From the parts list, I identified which parts I did not have generic footprints and/or schematic symbols for, and acquired them by either creating them with the help of datasheets or finding them on the Internet. Holes were sized using IPC standards<sup>1</sup>. To summarize this phase:

- a. I made the following footprints (stored in Common-Parts-Library.PcbLib):
  - i. Toroidal Inductor (vertically oriented)
  - ii. 3x2 ICSP header
  - iii. 1x2 header (replacing screw terminals, as suggested by TA on Discourse)
  - iv. Ceramic Capacitor
  - v. Oscillator
  - vi. Through-hole Resistor
- b. I made the following schematic symbols:
  - i. 3x2 ICSP header
  - ii. 1x2 header
  - iii. ATMEGA328P-PU
- c. I found the following footprints on SnapEDA:
  - i. ATMEGA328P-PU<sup>2</sup>
  - ii. MOSFET Gate Driver TC427CPA<sup>3</sup>
- d. I found the following schematic symbols on Altium's Part Manufacturer Search:
  - i. IRF3710

The above footprints are stored in Common-Parts-Library.PcbLib. The above schematic symbols are stored in PraxisIII.SchLib. For all other parts (regulators following TO-220-AB packaging, 2012 SMD resistors, and capacitors), I used generic footprints and schematic symbols, taking note of the physical properties of the part when selecting footprints. All these parts are contained in libraries provided with Altium.

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<sup>1</sup> IPC, "Sectional Design Standard for Rigid Organic Printed Boards," *ipc.org*, Feb-1988. [Online]. Available: <http://www.ipc.org/toc/ipc-2222.pdf>.

<sup>2</sup> N. Baker, "ATMEGA328P-PU," *SnapEDA*. [Online]. Available: <https://www.snapeda.com/parts/ATMEGA328P-PU/Microchip/view-part/649476/>. [Accessed: 10-Apr-2020].

<sup>3</sup> SnapEDA, "TC427CPA," *SnapEDA*. [Online]. Available: <https://www.snapeda.com/parts/TC427CPA/Microchip/view-part/127990/>. [Accessed: 10-Apr-2020].

## Schematic Creation

I created a new project in Altium called PraxisIII\_v2 (v1 was a failed attempt). I then made a schematic document in the project called Sheet1.SchDoc, and replicated the picture provided by the Teaching Team, using schematic symbols from above as necessary. I made use of all the same net labels and designators as the provided picture. The schematic is included in a PDF, as well as in the Altium project folder being submitted. At this point, I also made sure each component had the correct footprint assigned to it.

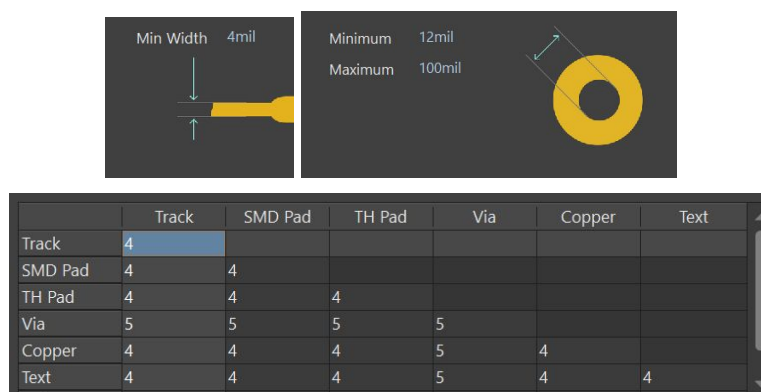
## Layout Creation

I created a layout in the same project called PCB1.PcbDoc, and used the “Import Changes from...” command. This automatically created all necessary components in my layout, while also linking them to the relevant components in the schematic. The nets were also imported.

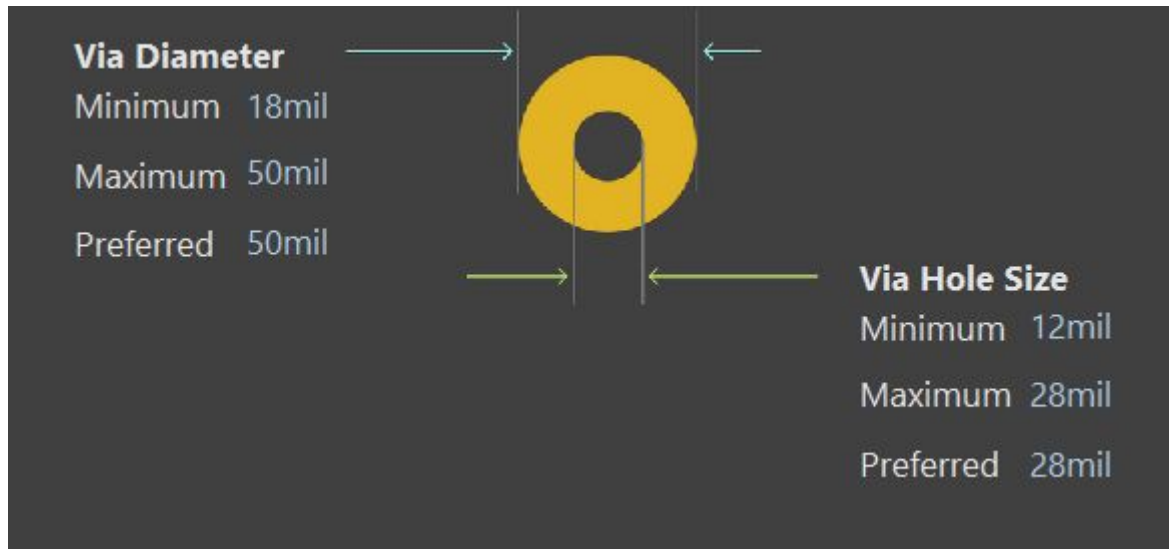
## Design Rules

In order to adhere to the provided design rules, I set the following rules under Design > Rules:

- Minimum trace width - set minimum width rule to 4mil
- Minimum trace spacing - set minimum clearance for all electrical components except vias to be 4mil
- Minimum hole diameter - set minimum hole size to 12mil (0.3mm, which is above 0.2mm)
- Minimum via diameter - minimum hole size set to 12mil, minimum via diameter set to 18mil (a bit more than 0.45mm)
- Minimum via to trace spacing - set minimum clearances for vias to be 5mil
- Via aspect ratio - All my via hole diameters are 28mil, as this is the “preferred” value. So, I need a via height of 168mil - so I made my board 168mil thick by making the dielectric thicker.
- Board dimensions - I checked my board dimensions at the end, and they fall well within constraints. Supporting screenshots are listed below.



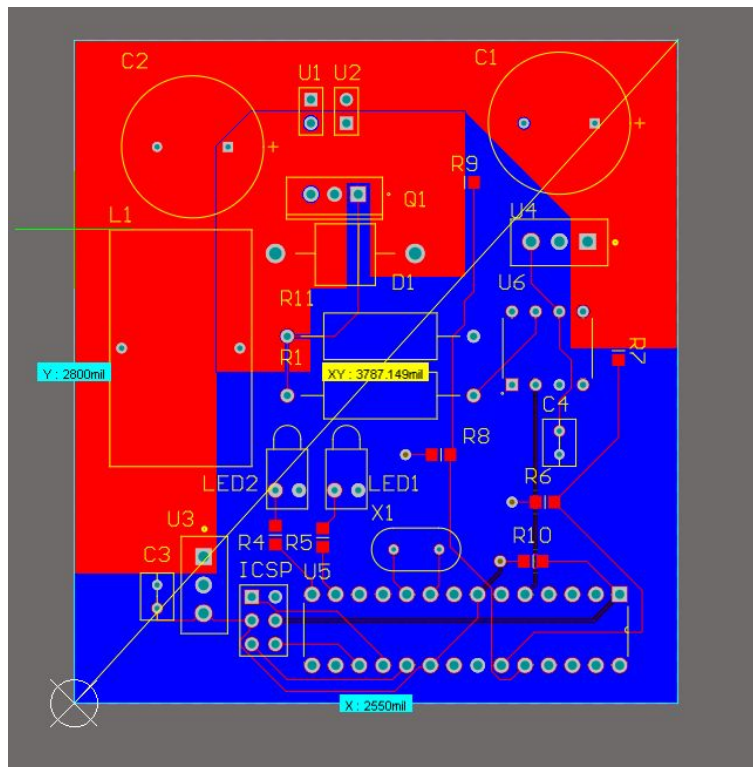
Figures 1 to 3. Evidence for Rule A (top left), C (top right), and both B and E (bottom).



Sheet1.SchDoc \* (2) Schematic Library Document PCB1.PcbDoc PCB1.PcbDoc [Stackup] Design Rule Verification Report

Features

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5	
1	Top Layer		Signal	1oz	1.4mil		
	Dielectric 1	FR-4	Dielectric		164.4mil	4.8	
2	Bottom Layer		Signal	1oz	1.4mil		
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5	
	Bottom Overlay		Overlay				



Figures 4 to 6: Evidence of Rules D, F, and G, from top to bottom.

## Component Arrangement

High power signals were physically separated from digital signals, and given ample room for large, high-current connections. Also, VIN\_ADC and VOUT\_ADC are important, analog signals, and were thus separated from IN\_A, which switches at a high speed and thus could cause noise. Then, the “rat’s nest” formed from the nets from the schematic was untangled, and components were arranged to save space and minimize messiness and trace length.

## Electrical Connections

A ground plane was used on the bottom layer of the PCB. Then, an online trace width calculator<sup>4</sup> was used to calculate required trace widths. From a TA’s suggestion on Discourse, it was assumed that all connections that were part of the DC-DC converter (that is, VIN, VOUT, NetD1\_1, and the GND connections for U1 and C1) would be required to handle 10A of current.

For VIN, VOUT, and NetD1\_1, the trace width calculator indicated that for 1.4mil thick traces handling 10A, 279mil traces are required. To prevent traces of this size from interfering with neighbouring connections, polygons were used instead for VIN, VOUT, and NetD1\_1, ensuring that all current-bearing portions of the polygon were above 300mil wide, and even larger if the shortest path between two connections was along the edge of the polygon. Thermal relief was disabled to allow the board to handle more current. I assumed voltages will not be high enough for electric breakdown under the design rules.

The GND connections for U1 and C1 are both through-hole, so it is assumed that the leads for the components themselves can handle the current required. No special sizing was done.

The other connections were analyzed as follows:

- +5V is used to power the ATMEGA328P-PU from the 5V regulator, which consumes 0.2mA of current while in operation<sup>5</sup>. +5V is also connected to the ICSP header, but that connection is just an alternative power source for the microcontroller for use when programming, and thus is subject to the same draw. +5V is also required to power other components such as the LEDs:
  - The LEDs are connected in series with 1k resistors, so they will draw less than  $5V/1000\text{ohms} = 5\text{mA}$  of current. This is safe for the MCU to supply through its I/O pins.

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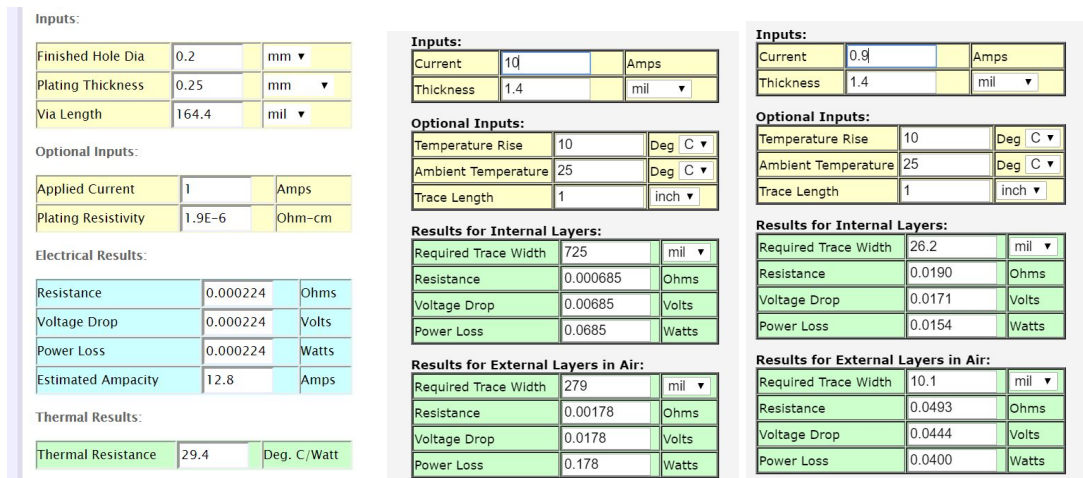
<sup>4</sup> B. Suppanz, “Printed Circuit Board Trace Width Tool,” *Advanced Circuits*, 2018. [Online]. Available: <https://www.4pcb.com/trace-width-calculator.html>. [Accessed: 10-Apr-2020].

<sup>5</sup> Atmel Corporation, “ATMEL 8-BIT MICROCONTROLLER,” *Mouser*, Nov-2015. [Online]. Available:

<https://www.mouser.ca/datasheet/2/268/Atmel-8271-8-bit-AVR-Microcontroller-ATmega48A-48P-1315288.pdf>.

- +12V is used to power the gate driver, which draws a maximum of 8mA of power while in operation<sup>6</sup>
- Every other signal is very low-current, due to being part of a voltage divider (like VIN\_ADC) or being some other kind of signal.

A 10mil trace can handle about 0.9A of current, which is much more than any of the above numbers combined. As such, 10mil traces should be sufficient for every other connection. Any via following the design rules will also be sufficient, as shown by an online via calculator<sup>7</sup>.



Figures 7 to 9: Calculations showing via ampacity, required current trace width for 10A, and ampacity for a 10mil trace

## Design Rule Check

A Design Rule Check was performed, that showed zero violations of the selected design rules (output can be found in submitted Altium project folder). An import of changes from the schematic was also performed, to confirm that no differences between the schematic and PCB exist.

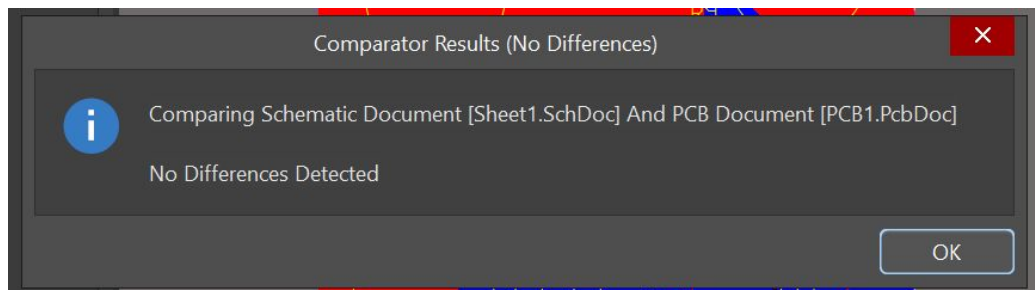


Figure 10. Evidence that the schematic and PCB are linked.

<sup>6</sup> Microchip Technology Inc., “1.5A Dual High-Speed Power MOSFET Drivers,” *microchip.com*, Dec-2012. [Online]. Available: <http://ww1.microchip.com/downloads/en/DeviceDoc/21415D.pdf>.

<sup>7</sup> “PCB Via Calculator,” *The CircuitCalculator.com Blog*, 21-Jun-2007. [Online]. Available: <http://circuitcalculator.com/wordpress/2006/03/12/pcb-via-calculator/>. [Accessed: 10-Apr-2020].