Electronics I

1st Semester 2010/2011

1 Laboratory Work
CMOS inverter

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Field of study Electronics

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1. Introduction

The aim of this laboratory work to analyze the operation of the CMOS inverter circuit Figure 1, consisting of two complementary MOS transistors (NMOS - channel and N PMOS - P channel). It will be considered various features of this inverter circuit, in particular, its transfer characteristic, noise margins and delay times propagation.

The realization of the inverter circuit is based on the use of HEF4007 integrated circuit (Philips Semiconductors) that contains six MOS enhancement transistors, and three N-channel and remaining P (see sheet of features attached to this working guide).

The completion of the laboratory work comprises the following steps:

i. before the first working session in the laboratory should be performed all the analysis theoretical circuit;

ii. the first lab session the simulations must be performed (with the program PSpice Schematics) and the results should be compared with the calculation theoretical (the necessary files to the simulations can be prepared before class Lab);

iii. components for the assembly of the circuit will be given in the first session laboratory. In case you have free time, can take advantage of the final part of the class to assemble the circuit. **note:** The bread-board board for mounting the circuit should be brought by the students;

iv. in the second laboratory session should be carried out experimental measurements and the results must be compared with the theoretical calculations and the Simulation results. The report is delivered at the end of this second class laboratory .

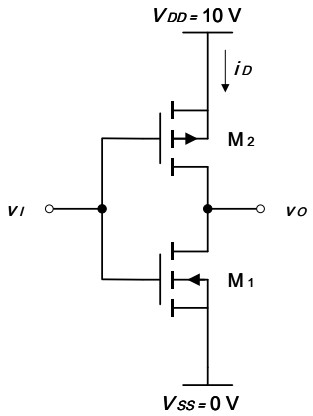


Figure 1 - Circuit CMOS inverter.

2. Laboratory Material and Equipment

To carry out the experimental work the following materials and equipment is required:

- 1 IC HEF4007
- 1 bread-board plate
- multimeter
- Oscilloscope
- Signal generator

3. Theoretical analysis

Consider the CMOS inverter circuit of Figure 1 with V_{DD} = V 10 and V_{SS} = 0V and the transistors

They are characterized by:

	W	L	•	k	V_t
NMOS	100 • m	5 • m	0	730 • / V_2	1.9 V
PMOS	300 • m	5 • m	0	480 • / V_2	1.7 V

3.1. Calculate the output voltage and current to the transistors v_I = 0 V; V_{DD} / 2; and V_{DD} and

indicate which the operating region of the transistor.

3.2. Determine the characteristic v transfer $_{O}$(v_I) circuit and indicating the different

operating zones of each of the transistors as well as the tensions in

transition points between operating areas.

3.3. Determine the current i_D Max.

3.4. Determine the voltages V_{OL}, V_{OH}, V_{IL}, V_{IH} and calculate the noise margins NMH and NML.

3.5. Consider the output capacitive load of 50 pF and determine the delay times of

propagating (t_{PHL}, t_{PLH} et $_P$).

In all previous issues justify the reported results. If you have made

some approximation calculations present in its justification.

4. Simulation

To perform the operation of the circuit simulation transistors characterized by

parameters indicated in the table below to enter the MBreakN component

the NMOS transistor and MBreakP for PMOS. Then you must change its parameters.

In the simulator available in the laboratory (program PSpice Schematics - Student version 9.1) to modification of the parameters of the transistors can be made as follows:

i. Select the component and enter the following command sequence: *Edit • Model ...*

- *Edit Instance Model (Text)* and in the window that is open should enter parameters according to the table (can be made "copy" and "paste" from a publisher not enter hidden characters, for example "notepad"). The CARACTERISTICS They are then saved in a file ***. lib, whose name and directory is shown in the window edition "Save To".

ii. **The W and L parameters must be entered directly after selection transistor (** double-click) in the window that opens automatically (the W parameters and L are the same as those shown in theoretical analysis).

Parameters of transistors to be used in PSpice	
NMOS	PMOS
.MODEL N4007 NMOS	.MODEL P4007 PMOS
TOX = 70N	TOX = 70N
KP = 73u	KP = 16U
VTO = 1.9V	VTO = -1.7V
GAMMA = 2.0	GAMMA = 1.0
CBD = 0.2p	CBD = 0.2p
CBS = 0.2p	CBS = 0.2p
MJ = 0.75	MJ = 0.75
LAMBDA = 20m	LAMBDA = 20m

Simulate the circuit operation considering • = 0 (Change the model of transistors), which corresponds to the theoretical analysis was made.

4.1. Determine the output voltage and current for transistors to $v_I = 0$ V; $V_{DD}/2$; and V_{DD}.

For it makes an analysis of the operating point at rest (*Bias Point Detail).*

4.2. Get feature v transfer $_O(v_I)$ making an analysis with a scan input signal (*DC Sweep).*

4.3. i also get the chart $_D(v_I)$.

4.4. From the results of the previous paragraphs determine the voltages V_{OL}, V_{OH}, V_{IL}, V_{IH} and calculate the noise margins NMH and NML. (Hint: may represent dv_O / dv_I)

4.5. Add in the output capacitive load of 50 pF, apply the input signal rectangular (VPULSE use the pulse generator) with voltage levels of 0 V and 10 V, frequency 500 kHz and negligible rise times and fall (e.g., 1 ps). Get a graph of the input and output voltages by making a domain analysis of time (*Transient ...).*

4.6. From the above graph to determine the propagation delay times (t_{PHL}, t_{PLH} et P). Hint: make "Zoom" in the transition zones of the signs and use the cursor to more accurate results.

now consider • = 20 mV^{-1}

4.7. Change the model of transistors and get the feature v transfer $O(v_I)$.

4.8. i also get the chart $D (v_I)$.

4.9. From the above results point to determine the voltages V_{OL}, V_{OH}, V_{IL}, V_{IH} and calculate the noise margins NMH and NML. (Hint: may represent dv_O / dv_I)

5. Experimental work

To carry out the work required circuit features Foil query integrated HEF4007 which is attached to this guide.

PRECAUTIONS / RECOMMENDATIONS:

- **Never apply signals in the input circuit without making sure that the circuit Integrated is already properly fed through pins 7:14.**
- **Before applying signals on the circuit input always check that they do not exceed the limits of the supply voltages: V_{DD} = V 10 and V_{SS} = 0 V.**
- **In this work, the oscilloscope channels must always be in DC mode.**

5.1. Identify in Figure 1 the pins of the integrated circuit corresponding to the terminal transistors and mount the inverter circuit on the bread-board plate (do not turn on the power food).

5.2. Adjust the supply voltage to 10 V. After verifying that the voltage level is correctly, connect to the circuit (14 pin (V_{DD}) and 7 (V_{SS}) Integrated Circuit).

5.3. Check operation of the circuit performing the following tests and recording the values :

The. Apply at the entrance a V sign $_{I}$ - 0 V and the voltmeter to measure the output voltage, v_O

B. Apply at the entrance a V sign $_{I}$ - 10 V and with the voltmeter to measure the output voltage, v_O

5.4. Connect the signal generator to the oscilloscope channel 1 and set it for a sign 1 kHz sine wave superimposed on a DC component, to obtain: v_{I}(t) 5 + 5 = cos (ω t) [V]. **Next, make sure that the circuit is powered and only then apply the sinusoidal signal.** Note the oscilloscope input signals (Channel 1) and output (channel 2). In Himes program get the feature transfer, v_{O}(v_{I}). Print the chart.

5.5. Keeping the preceding paragraph of the conditions, use the graph obtained to determine the voltages V_{OL}, V_{OH}, V_{IL}, V_{IH} and calculate the noise margins NMH and NML. Must use the Himes ZOOM function to achieve these values with any accuracy.

5.6. Use signals for generating a square wave frequency of 500 kHz and Extreme 0 V and 10 V. **Next, make sure that the circuit is powered and only then apply a square wave.** Note the oscilloscope input signals and output. Place the oscilloscope time scale at its minimum value to better visualization of transitions of waveforms. Resorting to Himes, get the corresponding graphics to L transitions • H and H • L. Using the ZOOM function Himes, determine the propagation delay times (t_{PHL}, t_{PLH} et $_{P}$).

6. Report

The report (delivered at the end of the second lab session) shall respect the following sequence of chapters / sections:

- **Theoretical analysis (** includes answers to questions 3.1 to 3.5)
- **simulation (** includes answers to questions 4.1 to 4.9 - where appropriate, check requests values on own graphics)
- **Experimental work (** includes responses and graphics relating to questions 5.3 to 5.6)
- **Analysis of results (** at least it includes comparisons of results that indicate in the tables below - **suggestion** : Use tables to summarize the values that got to throughout the work and enjoy the column "Comment" to enter its analysis of results)
- **conclusions**

Quantities to compare	theoretical	Experimental Comment simulation		
Voltages and currents at rest	3.1	4.1	5.3 [1]	
transfer characteristics	3.2	4.2	5.4	
current i_D maxim	3.3	4.3		
voltages V_{OL}, V_{OH}, V_{IL} and V_{IH} and noise margins NMH and NML	3.4	4.4	5.5	
propagation times t_{PHL}, t_{pLH} et P	3.5	4.6	5.6	

[1] As the voltages at rest

Quantities to compare	Simulation (with • = 0)	Simulation (with •• 0)	Comment
transfer characteristics	4.2	4.7	
current i_D maxim	4.3	4.8	
voltages V_{OL}, V_{OH}, V_{IL} and V_{IH} and margins noise NML and NMH	4.4	4.9	

As the second lab session is necessary to carry out the experimental work and complete the report, the report should be structured and partially performed before the second class laboratory so that in class you only need to complete the aspects relating to experimental results.

Should bring already printed report.

7. Features Sheet Integrated Circuit HEF4007

(See following pages)

For a complete data sheet, please Also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines / Information HEF, HEC

HEF4007UB
gates
Dual complementary pair and reverse

Product speci fi cation
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Dual complementary pair and reverse

HEF4007UB gates

DESCRIPTION

The dual HEF4007UB is complementary pair and an inverter with access to each device. It has three n-channel and p-channel three enhancement mode MOS transistors.

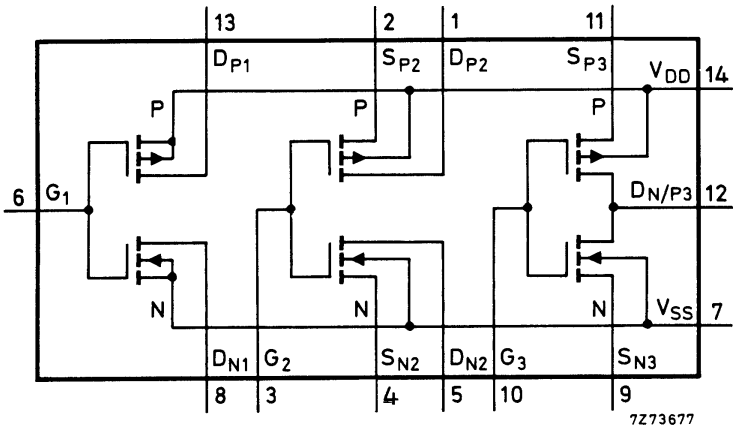


Fig.1 Schematic diagram.

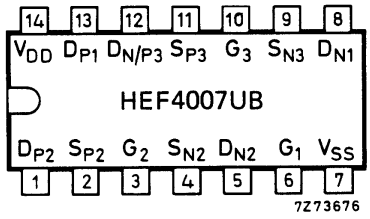


Fig.2 Pinning diagram.

HEF4007UBP (C): 14-lead DIP; plastic (SOT27-1)

HEF4007UBD (F): 14-lead DIP; ceramic (cerdip) (SOT73)

HEF4007UBT (D): 14-lead SO; plastic (SOT108-1)

(): Package Designator North America

pinning

	source connections to 2nd and 3rd p-channel transistors
D_{P1}, D_{P2}	drain connections from the 1st and 2nd p-channel transistors
D_{N1}, D_{N2}	drain connections from the 1st and 2nd n-channel transistors
S_{N2}, S_{N3}	source connections to the 2nd and 3rd n-channel transistors
$D_{N/P3}$	common connection to the p-channel and n-channel 3rd transistor drains
G_1 to G_3	gate connections to n-channel and p-channel transistors of the three pairs

FAMILY DATA, R_{DD} LIMITS category GATES

See Family Speci fi cations for V_{HI} / V_{IL} unbuffered stages S_{P2}, S_{P3}

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 ° W; W_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL extrapolation FORMULA
propagation delays						
$G_n \rightarrow D_N; D_P$	5		40	80	ns	13 + s (0.55 ns / pF) C_L
HIGH to LOW	10	t_{PHL}	20	40	ns	9 + s (0.23 ns / pF) C_L
	15		15	30	ns	7 + s (0.16 ns / pF) C_L
	5		40	75	ns	13 + s (0.55 ns / pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 + s (0.23 ns / pF) C_L
	15		15	30	ns	7 + s (0.16 ns / pF) C_L
Output transition times	5		60	120	ns	+ 10 ns (1.0 ns / pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 + s (0.42 ns / pF) C_L
	15		20	40	ns	6 + s (0.28 ns / pF) C_L
	5		60	120	ns	+ 10 ns (1.0 ns / pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 + s (0.42 ns / pF) C_L
	15		20	40	ns	6 + s (0.28 ns / pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (µ W)	
Dynamic power	5	4500 f_i + Σ (f_O W_L) × V_{DD2}	Onde
dissipation per	10	20, 000 f_i + Σ (f_O W_L) × V_{DD2}	f_i = input freq. (MHz)
package (P)	15	50 000. f_i + Σ (f_O W_L) × V_{DD2}	f_o = output freq. (MHz) C_L = load capacitance (pF) Σ (f_O W_G) = sum of outputs V_{DD} = voltage supply (V)

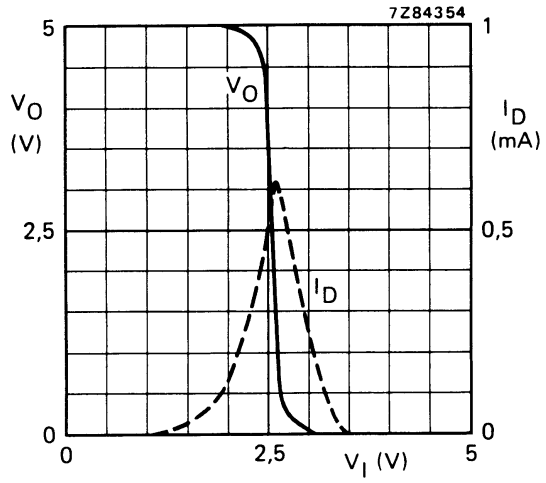


Fig.3 Typical drain current I_D and output voltage V_O at functions of input voltage; V_{DD} = 5 V; T_{amb} = 25 ° W.

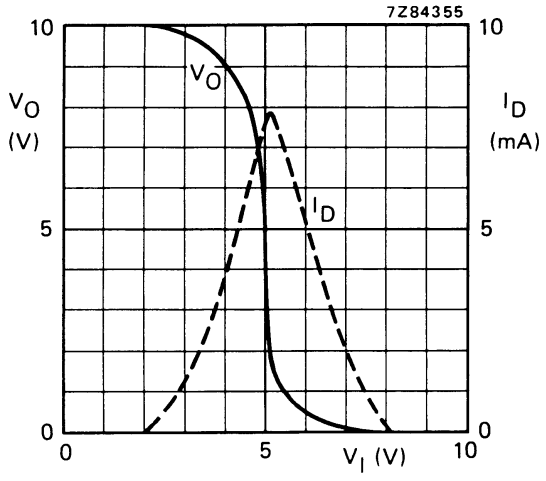


Fig.4 Typical drain current I_D and output voltage V_O at functions of input voltage; V_{DD} = 10 V; T_{amb} = 25 ° W.

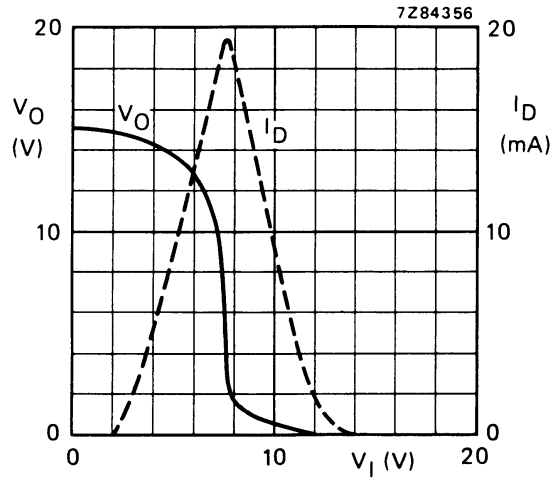


Fig.5 Typical drain current I_D and output voltage V_O at functions of input voltage; V_{DD} = 15 V; T_{amb} = 25 ° W.

APPLICATION INFORMATION

Some examples of applications for the HEF4007UB are:

- High input impedance amplifiers
- linear amplifiers
- (Crystal) oscillators
- High-current sink and source drivers
- High impedance buffer.

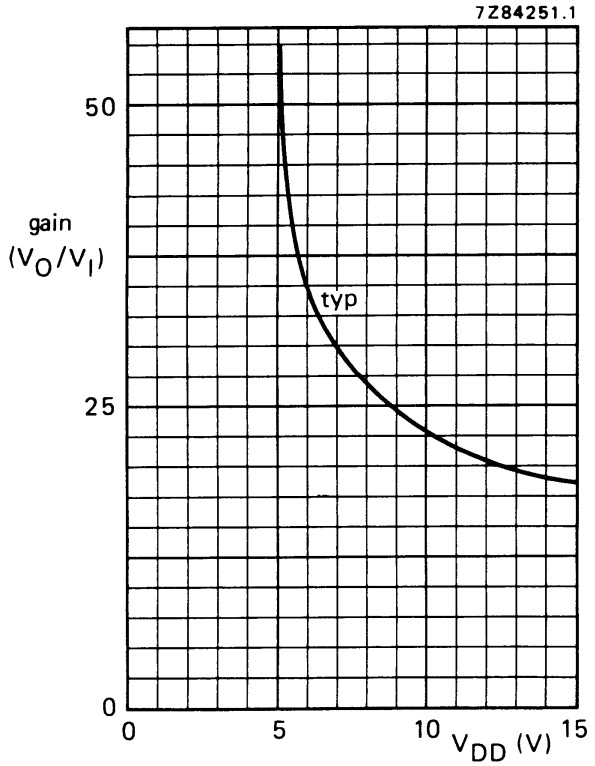


Fig.6 gain Voltage (V_O/V_i) as a function of supply voltage.

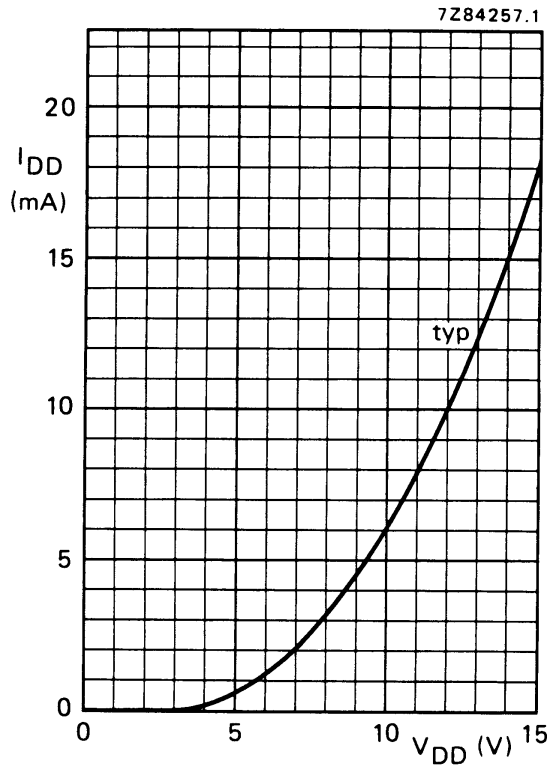
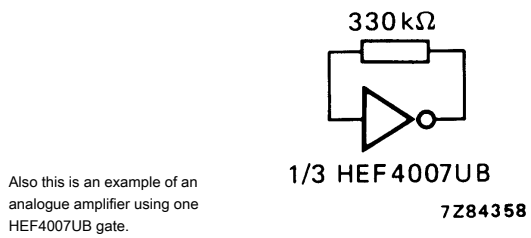


Fig.7 Supply current as a function of supply voltage.



Also this is an example of an analogue amplifier using one HEF4007UB gate.

Fig.8 Test set-up for measuring graphs of Figs 6 and 7.

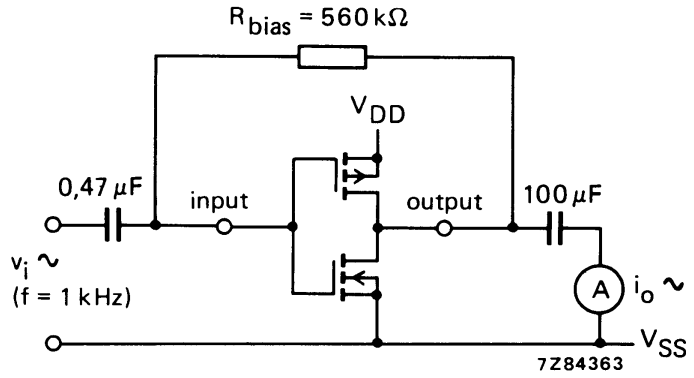
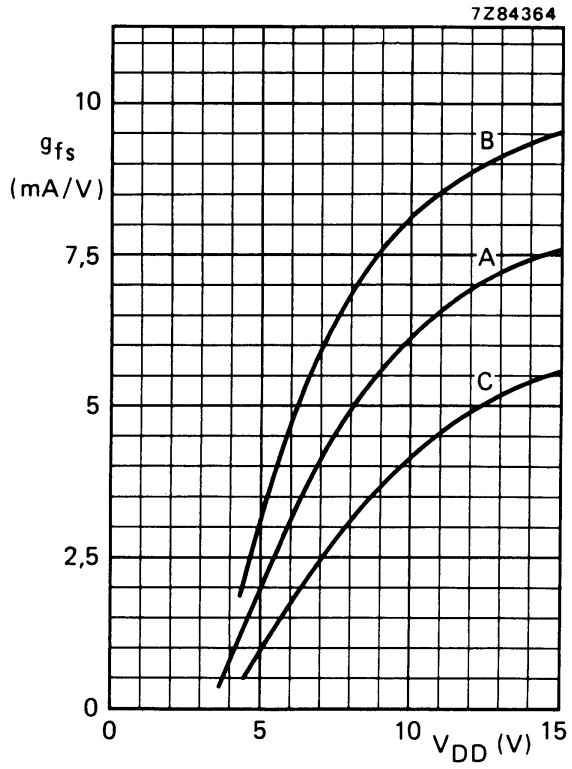


Fig.9 Test set-up for measuring forward transconductance g fs = di O/ dv i the TV O is constant (see also graph Fig.10).



A: average, B: Average + 2 s, C: average - 2 are in where 's' is the standard deviation Observed.

Fig.10 Typical forward transconductance g fs as a function of the supply voltage at T amb = 25 ° W.

Figures 11 to 14 show some applications in Which the HEF4007UB is used.

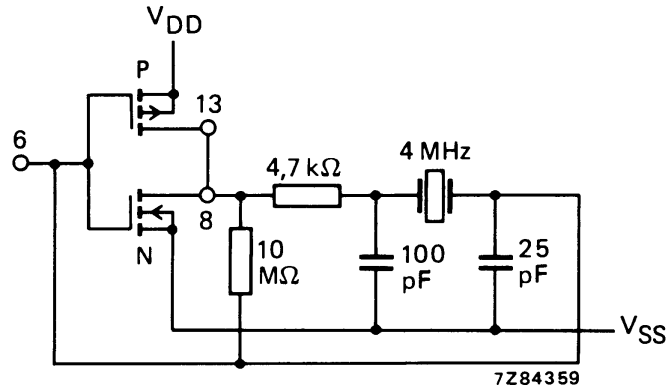


Fig.11 4 MHz crystal oscillator.

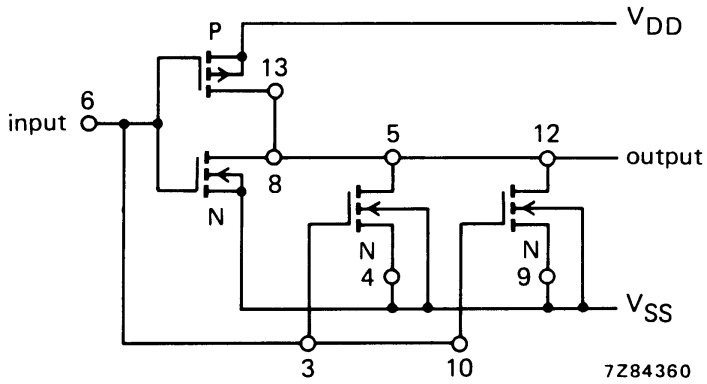


Fig.12 High current sink driver.

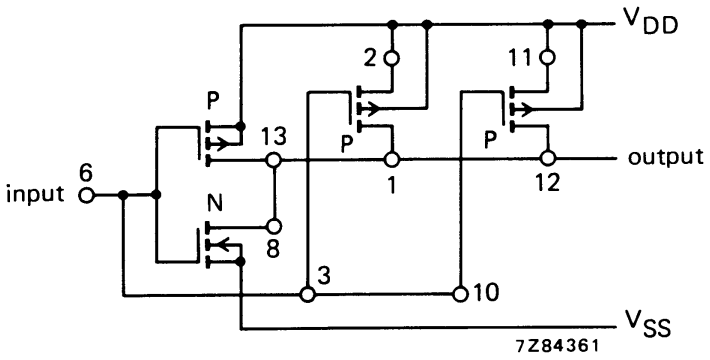


Fig.13 High current source driver.

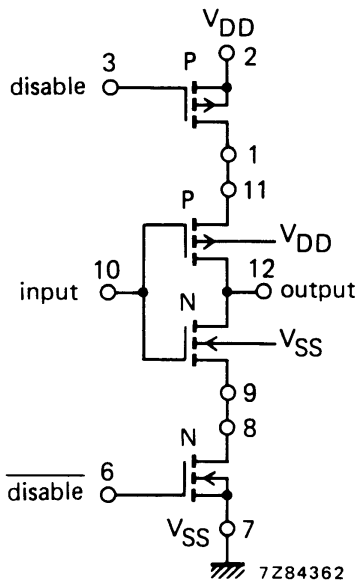


Fig.14 High impedance buffer.

FUNCTION TABLE Fig.14 is.

INPUT	DISABLE	OUTPUT
H	L	L
L	L	H
X	H	open

Notes

1. H = HIGH state (the more positive voltage) L = LOW state (the less positive voltage) state is immaterial X =

NOTE

Rules for Maintaining electrical isolation between transistors and monolithic substrate:

- Pin number 14 must be maintained at the most positive (or equally positive) potential with respect to any other pin of the HEF4007UB.
- Pin number 7 must be maintained at the most negative (or equally negative) potential with respect to any other pin of the HEF4007UB.

Violation of rules These transistors will result in improper operation and / or possible permanent damage to the HEF4007UB.