Design & Implementation of Timing and synchronization for an automotive amplifier

BITS ZG629T: Dissertation

By

Mohan Karthik p

id: 2011HZ12013

Agenda

- Problem Statement
- Introduction to the problem space
- Proposed solution (Designs)
- Testing and Results
- Conclusions
- Q & A

Problem Statement

- Design and Implement a precise time synchronization protocol as a foundation for an automotive audio amplifier.
  - Design a software architecture for implementation of time synchronization on Analog Devices® ADSP-BF518 Blackfin processor.
  - Utilize the open source ptpd implementation as the base source code.
  - Modify the open source implementation to utilize Blackfin's hardware time stamping features for precise accuracy.
  - Demonstrate the precise time synchronization features of the ADSP-BF518 with respect to another node (PC) executing the open source implementation to prove compatibility.

Introduction to the problem space

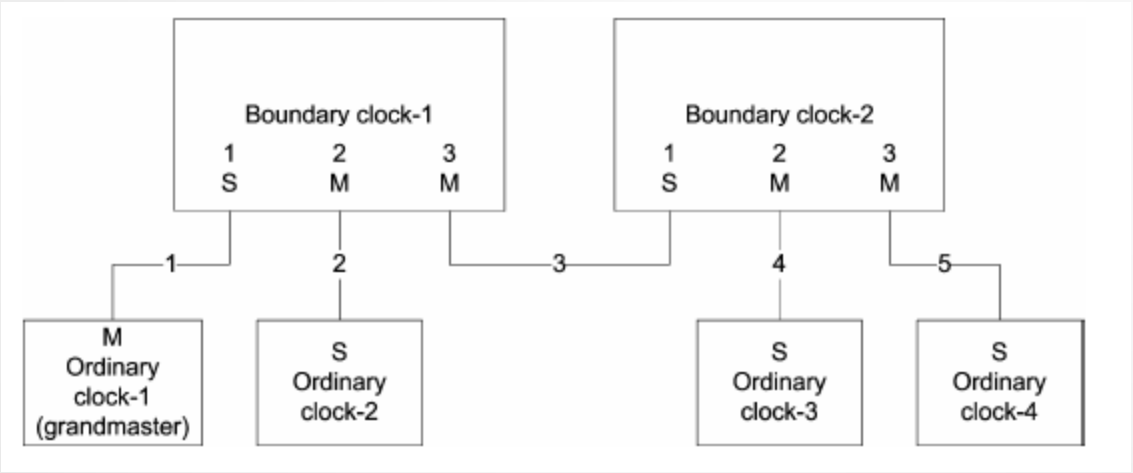
- Overview of traditional media streaming
  - Why point to point connections don't work anymore.
  - Requirements for A/V streaming
    - Synchronized media streams.
    - Worst case delays in the order of 2ms.
    - Assurance of network resources.
  - Problems with traditional IT networks
    - No inherent notion of time.
    - Delays and jitter.
    - Network congestion

Introduction to the problem space

- The Audio and Video Bridging Standard (IEEE Std 802.1BA)
  - Precise synchronization (IEEE Std 802.1 AS),
    - Best Master Clock algorithm
    - Precise clock synchronization
    - Clock syntonization
  - Traffic shaping for media streams (IEEE Std 802.1 Qav),
  - Admission controls (or stream reservation) (IEEE Std 802.1 Qat), and
  - Identification of non-participating devices (IEEE Std 802.1 BA).

Introduction to the problem space

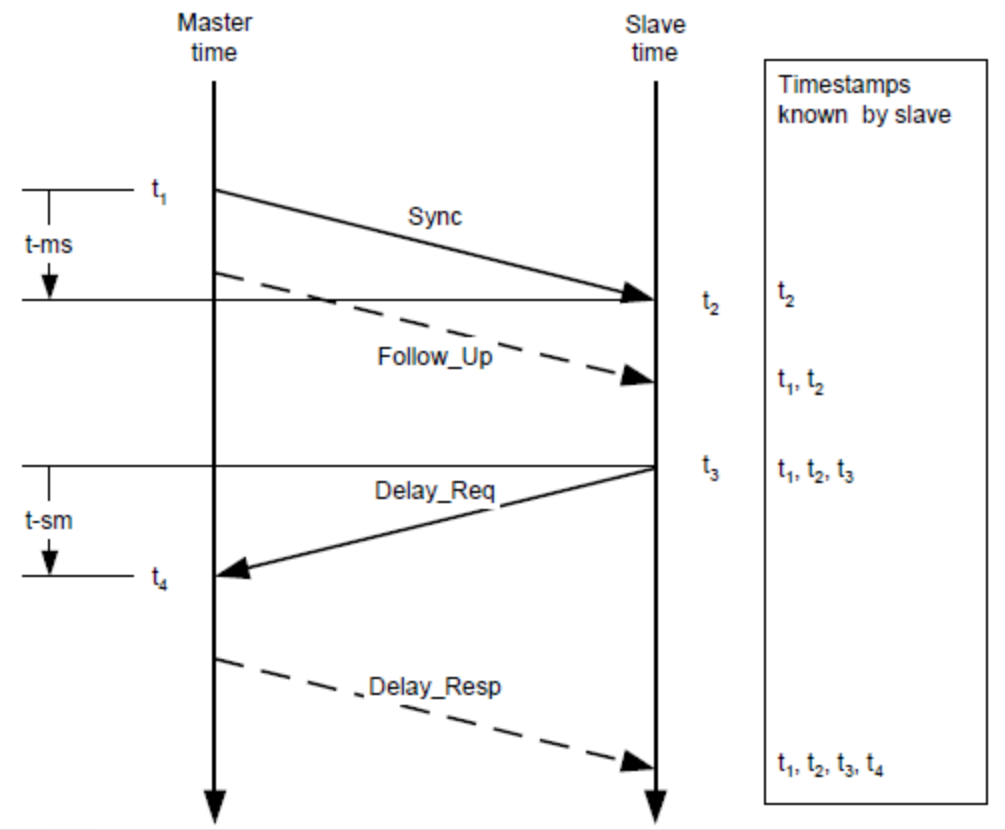
- Precise Time Synchronization (IEEE Std 1588)



- Single Grand Master clock on the system.
  - Grand master clock is chosen dynamically by a distributed protocol.
- Ordinary clocks participate and attempt to synchronize to the grand master precisely.
- Boundary clocks transport the time sensitive data reliably.

Introduction to the problem space

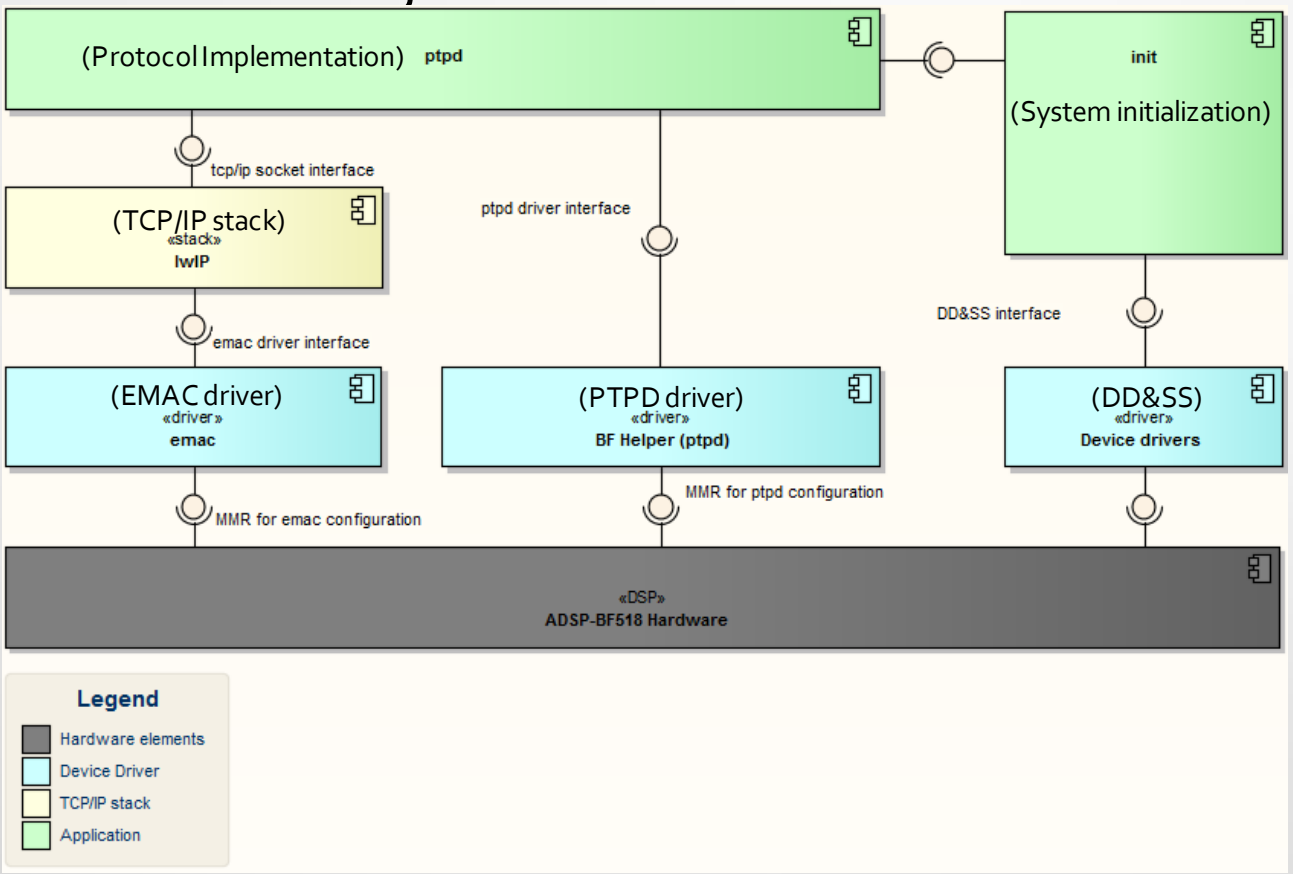
- Precise Time Synchronization (IEEE Std 1588)



- Message sequence followed by the IEEE Std 1588 in order to establish time synchronization across master and slave.

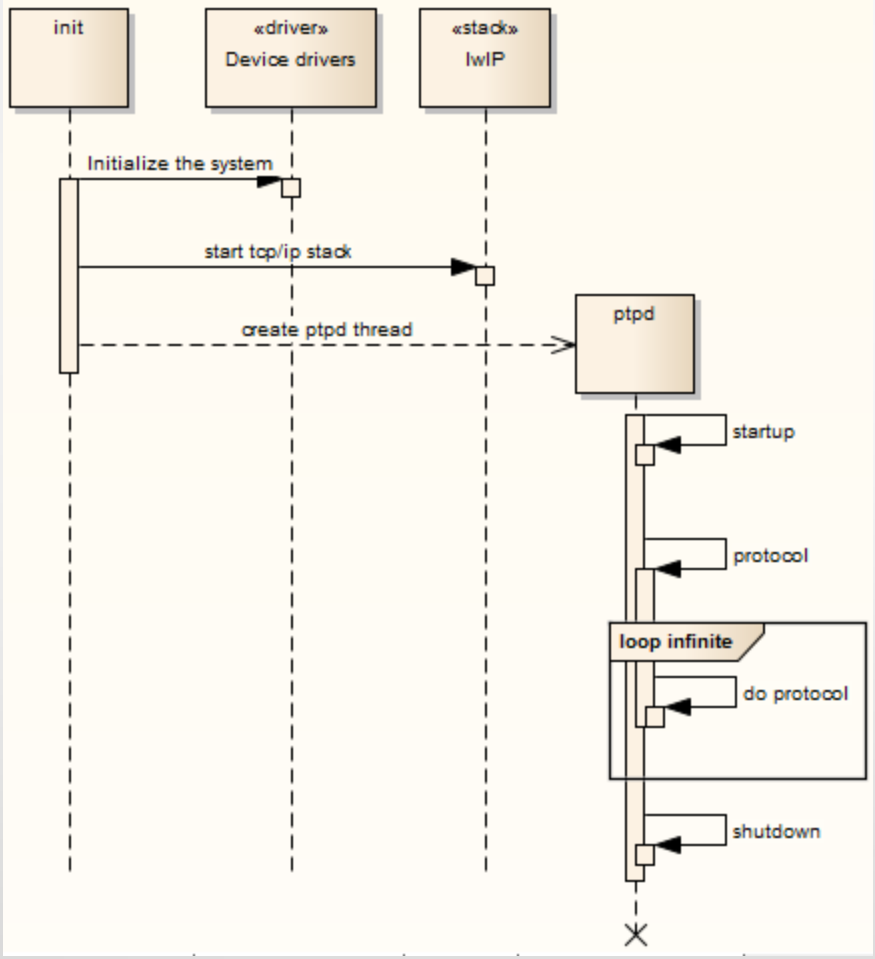
Proposed Solution

- Architectural Design



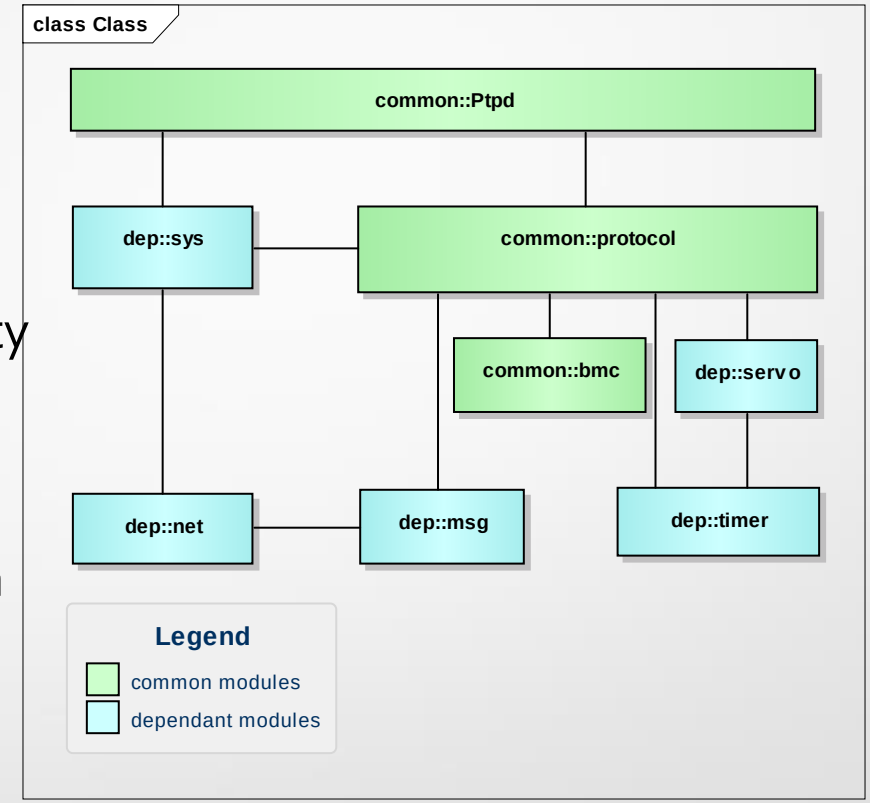
Proposed Solution

- System initialization



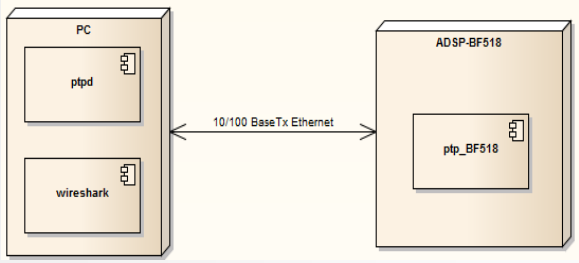
Proposed Solution

- Ptpd component
  - Ptpd: Active thread
  - Protocol: protocol implementation
  - Sys: init, shutdown & utility
  - Bmc: Best master clock algorithm
  - Servo: clock syntonization functionalities
  - Net: net services, sending receiving messages
  - Msg: message packing, unpacking
  - Timer: timer functionalities



Testing and Results

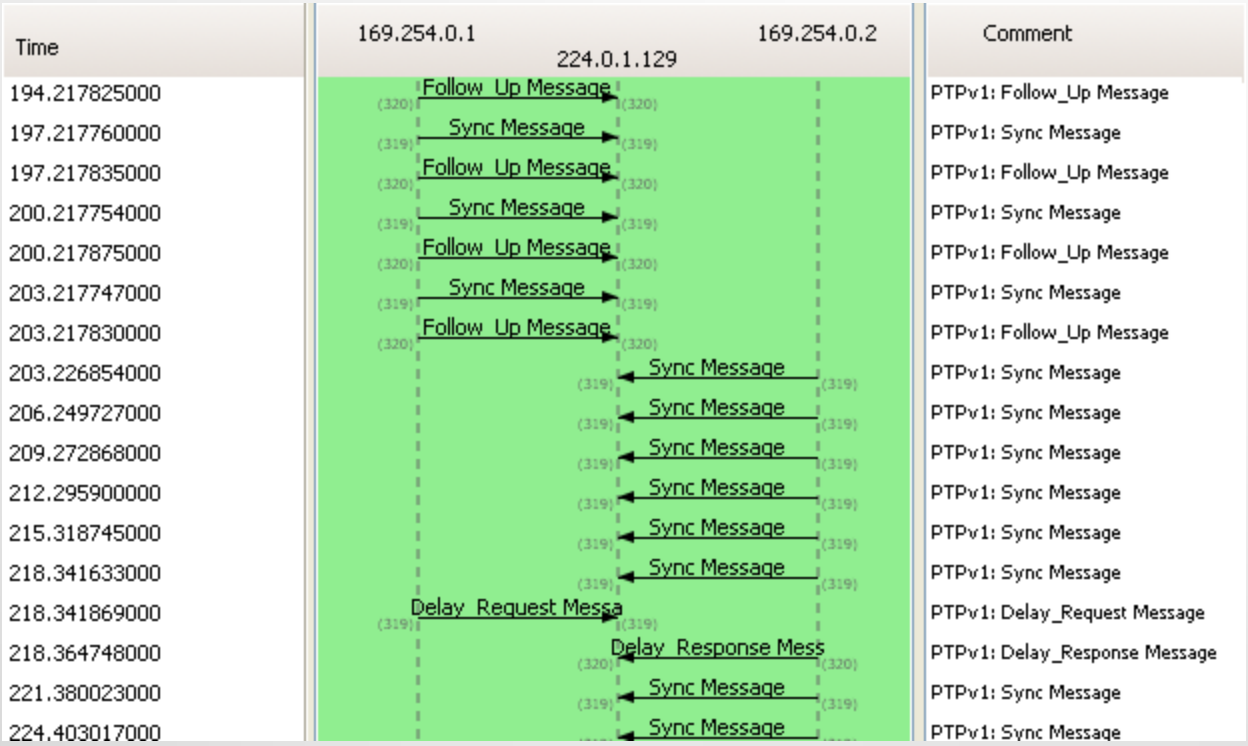
- Test Setup



- Test Sequence
  - Power on the PC
  - Connect the PC to the ADSP_BF518 via a direct 10/100BaseTx Ethernet cable
  - Configure the PC to static IP (169.254.0.1)
  - Start the wireshark application on the PC and set it to capture mode.
  - Start the UART terminal emulator on the PC to capture the BF518 logs
  - Start the ptpd application on the PC.
  - Configure BF518 to static IP (169.254.0.2)
  - Start the BF518 application.
  - Capture the logs from PC, BF518 and wireshark.

Testing and Results

- Ethernet Packet flow



Testing and Results

- ADSP-BF518 log

```
(ptpd debug) event POWERUP
(ptpd debug) state PTP_INITIALIZING  - BF518 has started initializing itself
(ptpd debug) state PTP_LISTENING     - BF518 has completed initializing and is listening for packets
(ptpd debug) updateForeign: new record (0,1) 1 1 70:f1:a1:20:b3:4c
(ptpd debug) state PTP_MASTER        - Receives a packet from the PC. Finds itself to be better
master via BMCA algorithm (since it has hardware ptp) and becomes PTP_MASTER.
BF518 now begins to transmit sync messages to the PC periodically with its internal PTP time being
displayed in seconds and nano seconds.
(ptpd debug) fromInternalTime:          4s   621956360ns ->          4s   621956360ns
(ptpd debug) fromInternalTime:          4s   621956360ns ->          4s   621956360ns
(ptpd debug) fromInternalTime:          4s   621956360ns ->          4s   621956360ns
(ptpd debug) fromInternalTime:          7s   645079440ns ->          7s   645079440ns
(ptpd debug) fromInternalTime:          7s   645079440ns ->          7s   645079440ns
(ptpd debug) fromInternalTime:          7s   645079440ns ->          7s   645079440ns
(ptpd debug) fromInternalTime:         10s   667979660ns ->         10s   667979660ns
(ptpd debug) fromInternalTime:         10s   667979660ns ->         10s   667979660ns
(ptpd debug) fromInternalTime:         10s   667979660ns ->         10s   667979660ns
(ptpd debug) fromInternalTime:         13s   690979520ns ->         13s   690979520ns
```

Testing and Results

- PC log

```
event POWERUP
state PTP INITIALIZING        - PC has powered up and begun to initialize.
state PTP LISTENING           - PC moves to state listening after initialization
timerUpdate: timer 0 expired
event SYNC_RECEIPT_TIMEOUT_EXPIRES - PC does not receive any master announcements, hence becomes
PTP_MASTER
state PTP MASTER
event SYNC_INTERVAL_TIMEOUT_EXPIRES - PC begins to send sync message (BF518 is still booting)
fromInternalTime: 1363946436s    15625000ns -> 1363946436s    15625000ns
updateForeign - BF518 has booted up, notices that PC has inferior clock and announces itself
updateForeign: new record (0,1) 1 1 00:e6:56:78:90:00
state PTP_SLAVE       - PC realizes that BF518 has better clock and becomes PTP_SLAVE
PC begins to receive clock from the BF518 PTP master and starts to adjust its own clock to it.
msgUnpackSync: originTimestamp.seconds 7
msgUnpackSync: originTimestamp.nanoseconds 645079440
msgUnpackSync: originTimestamp.seconds 10
msgUnpackSync: originTimestamp.nanoseconds 667979660
```

Conclusions

- Founding base for a complete Ethernet based audio amplifier
  - Establishes a common precise time reference across multiple nodes.
  - Media streaming protocols such as IEEE Std 1722 can harness the common time reference to implement schemes for media clock.
  - IEEE Std 802.1 Qat and IEEE Std 802.1 Qav complete the system.
- Proves the capability of Analog Devices Blackfin processor in the Ethernet AVB space.
  - Currently supported processors include ADSP-BF51x, ADSP-BF60x and ADSP-CM408.

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Questions?

With thanks

Mohan Karthik P (2011HZ12013)