TÉCNICO LISBOA

Linux capable RISC-V CPU for IOb-SoC

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Declaration

I declare that this document is an original work of my own authorship and that it fullfills all the requirements of the Code of Conduct and Good Practices of the Universidade de Lisboa.

Dedicated to someone special...

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Resumo

Resumo em Português

Palavras-chave: Detecção de Objectos, Redes Neuronais Convolucionais, Sistema num Chip, Matrizes Reconfiguráveis de Grão Grosso...

Abstract

Resumo em inglês

Keywords: Object Detection, Convolutional Neural Networks, Systems on Chip, Coarse Grained Reconfigurable Arrays.

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Listings

List of Acronyms

AGU Address Generator Unit
ALU Arithmetic and Logic Unit
AP Average Precision
API Application Programming Interface
AXI Advanced eXtensible Interface
BRAM Block RAM
CGRA Coarse Grained Reconfigurable Array
CM Configuration Module
CNN Convolutional Neural Network
COCO Common Images in Context
CPU Central Processing Unit
CRC Cyclic Redundant Check
DDR Double Data Rate
DE Data Engine
DFP Dynamic Fixed Point
DGU Data Generation Unit
DMA Direct Memory Access
DSP Digital Signal Processing
FF Flip-Flop
FM Feature Map
FP Fixed-Point
FPGA Field Programmable Gate Array
FPS Frames Per Second
FU Functional Unit
GPP General-Purpose Processor
GPU Graphical Processing Unit
IFM Input FM
IOb-SoC IObundle SoC
IoU Intersection over Union
IPv4 Internet Protocol
LRU Least Recently Used
LUT Look-Up Table
MAC (address) Media Access Control
MAC (block/unit) Multiply-Accumulate
mAP Mean Average Precision
MIG Memory Interface Generator
NMS Non-maximum Suppression

OFM Output FM

PE Processing Element

RAM Random Memory Access

ReLU Rectified Linear Unit

ROM Read Only Memory

SFD Start Frame Delimiter

SFP Static Fixed Point

SIMD Single Instruction Multiple Data

SoC System on a Chip

SRAM Static Random Access Memory

UART Universat Asynchronous Receiver-Transmitter

YOLO You Only Look Once

Chapter 1

Introduction

Introdução

1.1 Motivation

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