Linux capable RISC-V CPU for IOb-SoC

Thesis to obtain the Master of Science Degree in
Electrical and Computer Engineering

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Presentation Outline

TÉCNICO LISBOA

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Motivation

TÉCNICO LISBOA

- Object detection is usefull in multiple areas of application (navigation, medical, security)
  - Most accurate methods use CNN inference.
  - **Problem:** Computationally demanding process.
- Current solutions based on GPU acceleration.
  - Oversized and power-hungry.
- Alternative accelerators also have limitations:
  - FPGA: better size/power efficiency than GPU, with configuration overhead and increased development time.
  - ASIC: dedicated accelerators lack hardware programmability.
- **Proposed solution:** CGRA
  - Optimized area and power.
  - Faster reconfiguration for FPGA implementation.
  - Adds hardware programmability for ASIC implementation.

Thesis Goals

Main thesis goals:

- Accelerate a Convolutional Neural Network (CNN) for object detection, using the VersatCNN CGRA
  - Configure CGRA dataflow to efficiently implement the Tiny YOLOv3 application
- Target real-time processing (30 FPS)

IOb-SoC Hardware Platform

Open source RISC-V SoC platform by IObundle.

Main components:

- PicoRV32 RISC-V CPU
- Internal memory
- External memory
  - Single level cache
- UART
- Integrated Peripherals:
  - **Timer**
  - **Ethernet**
  - **VersatCNN**

Continuous integration of system and new components.
Development of testing environment.

IOb-SoC Profiling Results

Embedded version of Tiny YOLOv3 application:

- Executed exclusively on RISC-V CPU
- 143 MHz system clock.

Tiny YOLOv3 Part	Execution Time (s)
Pre-CNN	1.040
CNN	967.746
Post-CNN	0.014
Total	968.800
Target (30 FPS)	**0.033**

Table: Tiny YOLOv3 RISC-V-only performance.

Conclusion: all parts of the application require acceleration.