TÉCNICO LISBOA

Audio Amplifier

Laboratory Report

David Ferreira(93371), Mário Vaz(96553), Pedro Baptista(96560)

Group 54
Engineering Physics (MEFT), I. S. Técnico, University of Lisbon
Circuit Theory and Electronics Fundamentals - Prof. José Sousa
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Contents

1 Introduction

In this lab report we shall study the Audio Amplifier Circuit. The purpose of such a circuit is to increase the voltage of the input signal. We call Voltage Gain to the quotient between the output voltage and the input. The behavior of such a system is frequency-dependent, thus, we are interested in finding out from and to which frequency values the circuit behaves properly. To the pair of frequencies referred we call Lower Cutoff Frequency and Upper Cutoff Frequency, the difference between those is called the bandwidth. Our goal is to study how the different parameters of the circuit affect the mentioned quantities. The merit of our work is given by equation 1.

$$M = \frac{voltageGain \times bandWidth}{cost \times lowerCutoffFreq} \tag{1}$$

A simplified scheme of the circuit to be studied is presented in figure 1.

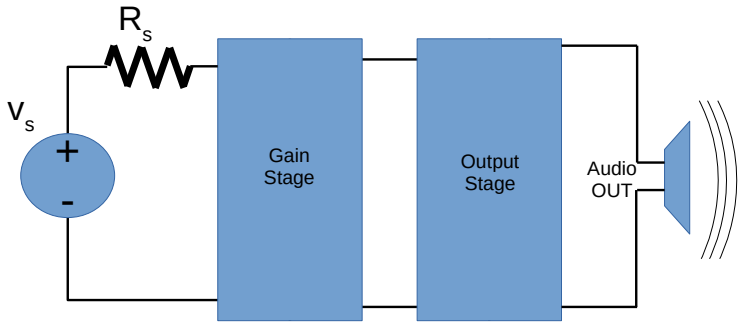

Figure 1: Scheme of the audio amplifier

In section 3 we will study both parts of the circuit to a deeper level. Our goal is to describe theoretically the behavior of the circuit (section 3), that will be done using *Octave*, and to describe it using a simulation software such as *Ngspice*, section 2. We will then compare both of them and see where they agree and disagree, presenting possible differences for such divergencies.

2 Simulation Analysis

We now proceed to perform a computational simulation of the amplifier, using the *Ngspice* software. The implemented gain stage circuit is represented in figure [2]. We started from the given script, making incremental changes to improve the merit figure and ensure impedance compatability.

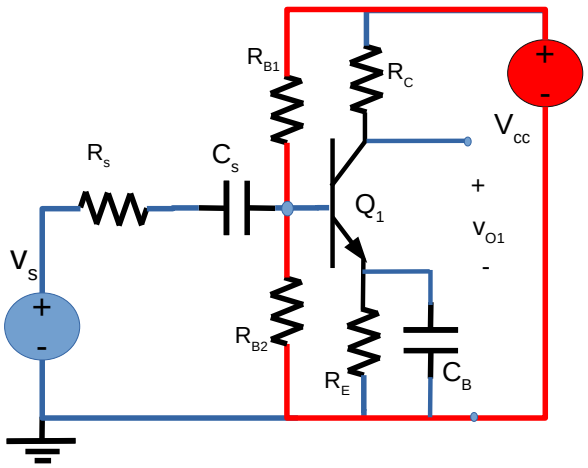

Figure 2: Gain stage circuit

This circuit is composed of the following components: four resistors ($R_{B1} = 80k\Omega$, $R_{B2} = 20k\Omega$, $R_C = 1k\Omega$ and $R_{E1} = 100\Omega$), a coupling capacitor ($C_s = 1mF$), a bypass capacitor ($C_b = 2.74mF$) a NPN transistor (Q_1, model BC547A) and a constant voltage source ($V_{cc} = 12V$). Identified with red, the bias circuit ensures the adequate voltage at Q_1's base terminal.

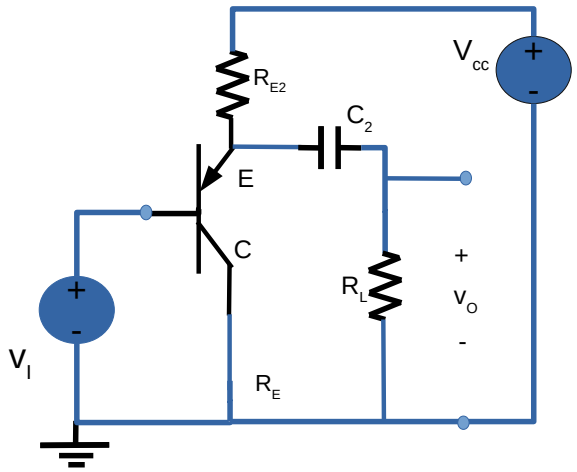

Figure 3: Output Stage circuit

The second stage, shown in figure 3, consists of a PNP transistor (Q_2, model BC557A), a resistor ($R_{E2} = 5\Omega$) and a coupling capacitor ($C_2 = 3mF$). It's purpose is to minimize the output impedance, so that the load ($R_L = 8\Omega$) can be safely conected and the signal isn't significantly damped.

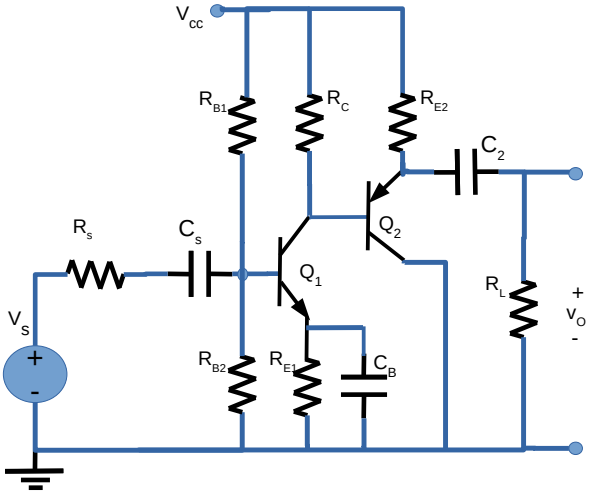

Figure 4: Audio Amplifier circuit, detailed scheme

The values of the components were optimized to satisfy the operation of Q_1 and Q_2 in the foward-active region (FAR), the minimization of the lower cutoff frequency, the maximization of the band width, as the adequate input and output impedances.

We now show the gain of the entire circuit v_o/v_s as a function of frequency, from $10Hz$ to $100MHz$, according to the *Ngspice* simulation. This is obtained through the voltage at node *out*, using the fact that the *ac* analysis of the software automatically uses an incremental version of the circuit, allowing the use of the source voltage amplitude as $v_s = 1V$, without further implications.

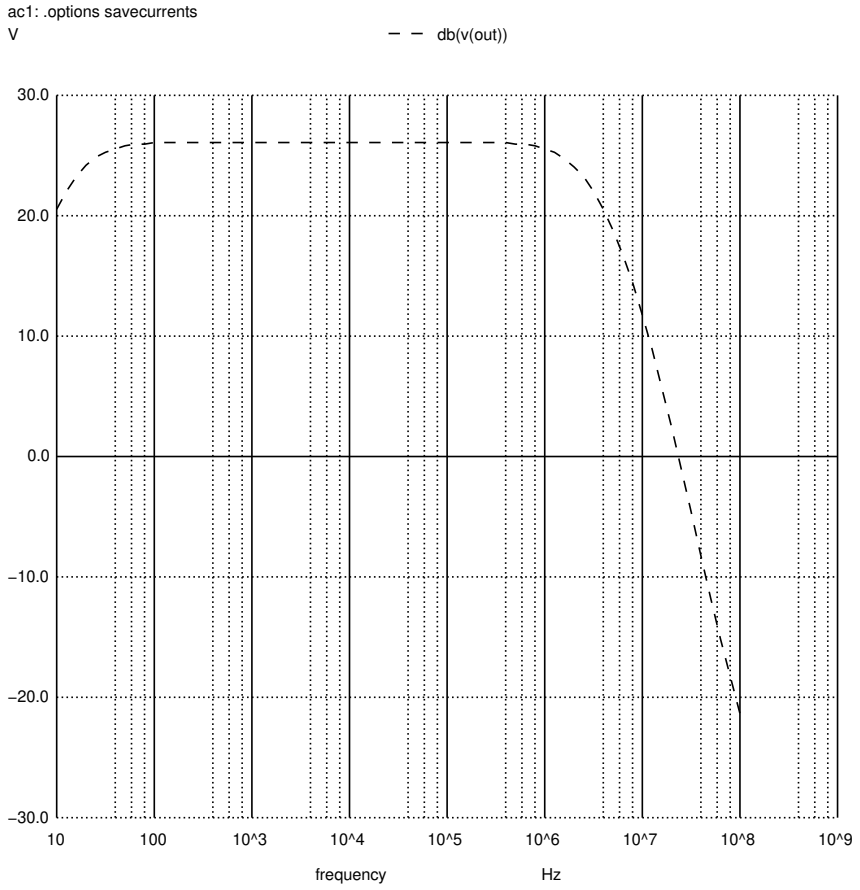

Figure 5: Gain's frequency response of the amplifier circuit, in dB

For these conditions, the voltage gain in the passband is $v_o/v_s = 26.142dB$. The lower and upper cutoff frequencies are, respectively and aproximately, $15.532Hz$ and $2.5446MHz$. Thus, the bandwidth is $2.5445MHz$. The input impedance is $Z_i = 606.40\Omega$. The output impedance is $Z_o = 4.1295\Omega$. These values have been taken from the *log* files in the *t4/sim* folder. The figure of merit obtained with these parameters is $M = 624.5$. These results are further discussed in the next section.

3 Theoretical Analysis

3.1 Gain Stage

The main purpose of this part of the circuit is, as the name suggests, to increase the voltage of the output signal, producing, therefore, a high Voltage Gain.
The figure of the circuit is presented in figure 2

We start by giving a simple explanation as to the existance of some of the presented components. For example, C_s is a coupling capacitor whose job is to eliminate the DC component from the voltage source v_s. The bias circuit (represented in red in figure 2) aims to guarantee that the voltage at the source is such that allows the transistor to conduct normally, making sure it is in the forward active region. Resistor R_E is used to stabilize the temperature effects on the circuit, however, it lowers the gain. For that reason, capacitor C_E is placed in parallel to it. With this configuration we can see that for low frequencies (DC) the capacitor works as an open circuit, for medium/high frequencies the capacitor works as a short circuit, bypassing R_E, thus increasing the gain again.

We are now interested in doing an operating point analysis of the circuit. To do so, we start by computing the Thevenin's equivalent of the bias circuit. At an operating point analysis, all capacitors behave as open circuits. We now present the circuit obtained with the Thevenin's equivalent.

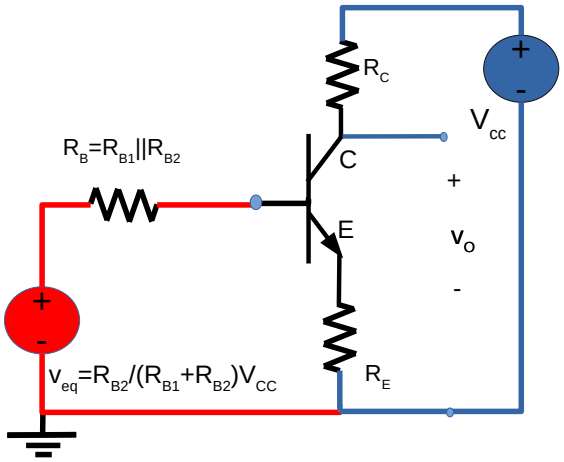

Figure 6: Gain Stage Circuit Thevenin's equivalent

In this stage, is particularly important that we calculate the voltage V_{CE} and make sure that it is greater than V_{BEON} confirming that the transistor is working in the forward active region (FAR).

The values for other important quantities will be presented alongside the ones obtained in the simulation in order to ease its analysis.

We shall now focus on finding a way to calculate the expected voltage gain of the circuit. We do so by considering an incremental circuit for medium frequencies. Remembering that for medium frequencies the capacitor C_E behaves like a short circuit which is equivalent to consider $R_E = 0$.

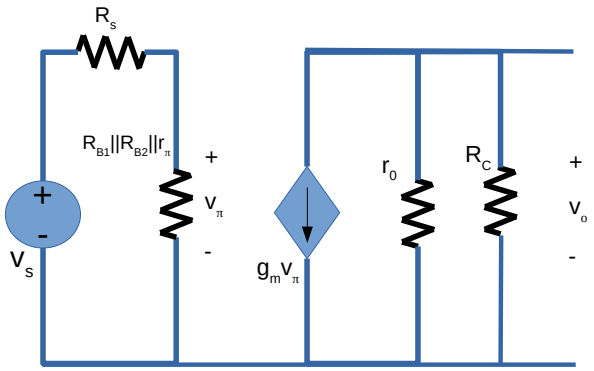

Figure 7: Gain Stage Incremental Circuit

Using mesh analysis one can derive the following expressions for the voltage gain of the circuit.

$$v_o = -g_m(R_C||r_o)v_\pi \tag{2}$$

$$v_\pi = \frac{r_\pi||R_{B1}||R_{B2}}{R_s + r_\pi||R_{B1}||R_{B2}} \tag{3}$$

$$gain = \frac{v_o}{v_s} = -g_m(R_C||r_o)\frac{r_\pi||R_{B1}||R_{B2}}{R_s + r_\pi||R_{B1}||R_{B2}} \tag{4}$$

One can also obtain expressions for the input and output impedances of the circuit gain. Those are as follows:

$$Z_I = R_{B1}||R_{B2}||r_\pi \tag{5}$$

$$Z_o = R_C||r_o \tag{6}$$

3.2 Output Stage

The impedances obtained from the Gain stage are not compatible neither with the input's resistance R_s nor with the resistance from the speaker $R_L = 8\Omega$. In order to maintain the integrity of the signal, one must aim for a large value for Z_I to not degrade the input signal and a low value for Z_o to not degrade the output signal.

The considered circuit can be observed in figure 3.

Much like in the previous section, we are interested in doing an operation point analysis. In such, the capacitor will behave as an open circuit and the figure 3 can be simplified to:

Computing the voltage gain for this section of the circuit, we end up with:

$$gain = \frac{v_o}{v_i} = \frac{g_m}{g_m + g\pi + g_E + g_o} \approx 1 \tag{7}$$

The impedances are given by:

$$Z_I = \frac{g_m + g\pi + g_E + g_o}{g\pi(g\pi + g_E + g_o)} \tag{8}$$

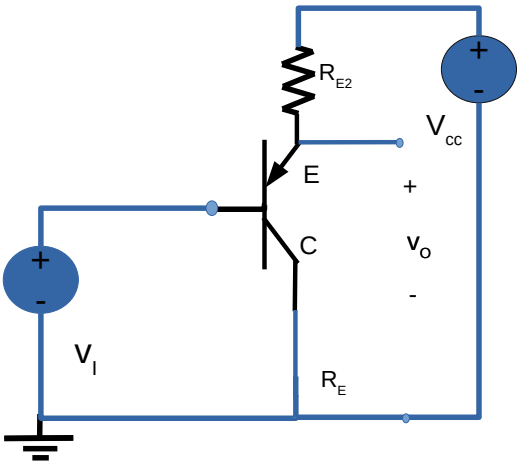

Figure 8: Output Stage Circuit for OP Analysis

$$Z_o = \frac{1}{g_m + g\pi + g_E + g_o} \tag{9}$$

3.3 Theoretical results and comparison

We now proceed to list some of the theoretical results and comparing them to the ones obtained in the simulation:

Quantity	Theoretical	Simulation
Lower Cut Frequency (Hz)	—-	15.532
Upper Cut Frequency (MHz)	—-	2.5446
Bandwidth (MHz)	—-	2.5445
$Gain_{gain-stage}$ (dB)	48.392	—-
$Gain_{output-stage}$	0.99195	—-
$Gain_{total}$ (dB)	42.585	26.142
ZI1(Ω)	484.43	—-
Z01(Ω)	886.28	—-
ZI2(Ω)	429.94	—-
Z02(Ω)	0.015109	—-
Zi (Ω)	484.43	606.40
Zo (Ω)	1.9972	4.1295

Table 1: *Octave*'s results vs. *ngspice*'s results

First we should take into account that the theoretical analysis was done assuming we were in a medium frequency regime in which the capacitor works as a short-circuit. This means that the $Gain$ values are the bandwidth gain values (we did not perform a frequency analysis in the theoretical analysis, we just assumed we were working on the bandwidth frequencies). $Gain_{gain_stage}$ is high and $Gain_{output-stage} \approx 1$ corroborating the correct performance of an Amplifier. The total gain, $Gain_{total}$, is still high but does not match the *ngspice*'s gain, presenting an error of $E(\%) = 62.9\%$. The decrease from $Gain_{gain-stage}$ to $Gain_{total}$ comes from (not only!) the impedances, which we will comment below:

The gain stage's input impedance, $ZI1$, is 484.43Ω, which is not a great input impedance when compared to $R_s = 100\Omega$. This means that the signal from V_s is attenuated in the gain stage's terminals. Ideally, we would want $ZI1 >> R_s$. The output stage's output impedance, $Z02 = 0.015109\Omega$, is very low compared to the Load resistance $R_L = 8\Omega$. Even though this is not the final output impedance, it showcases one ot the output stage's characteristcs : low output impedance, which is crucial for the signal to not be attenuated in the load resistance. Now $Z01$ and $ZI2$ are not ideal. We would prefer $ZI2$ to be way larger than $Z01$ so that the signal between the gain stage's terminals would not be damped when transitioning to the output stage's terminals. Effectively, this is what happens, meaning it's one of the reasons $Gain_{total}$ decreases when compared to $Gain_{gain-stage}$.

Zi=ZI1 and comparing it to *ngspice*'s input impedance we get an error of $E(\%) = 20.1\%$. The final output impedance is $Zo = 1.9972\Omega$ which is not ideal when comparing it to the load resistance. Ideally, we would want $Zo << R_L$. Comparing it to *ngspice*'s output impedance, we get an error of $E(\%) = 51.6\%$.

We would like to discuss the role of R_c in the $Gain_{gain-stage}$ of the circuit. The greater its value, the greater the gain will be yet when one increases R_c above a certain level, the transistor no longer works in the forward active region.

4 Conclusion

Comparing the results from the simulation with the ones gotten from the theoretical analysis, we can conclude that they show several discrepancies.

One thing we noticed is that the relations derived from the theoretical analysis don't always hold. For example, the expression for the final output impedance states that the lower the resistance RE2, the lower the impedance, yet many times lowering this value on *ngspice* would not lead to a decrease in this impedance. On the contrary, the impedance grew larger. This and other discrepancies show that the model we used to describe the system in the theoretical analysis doesn't exactly describe what happens in reality and is rather incomplete. This assumption is justified by comparing the simple transistor models used in the theoretical analysis with the simulator's transistor models, which are much more complex, having a large number of parameters to take into account and also introducing parasitic capacitors and inductors that better help describe the transistor's behaviour. This explains the large errors we got. We also noticed that small errors in the Operating Point Analysis propagated to larger errors in the incremental analysis.

The Amplifier we built is not ideal, even though the gain is acceptable, because the impedances are not really compatible, namely the input impedance with resistor R_s and, most importantly, the output impedance with the load resistor R_L. We tried to decrease this last impedance, lowering R_{E2} to a value of 1Ω. This showed to be great for Zo, but it would also lower the output stage's input impedance, which would make the whole output stage incompatible with the gain stage. ZO1 would become larger than ZI2 ($Z01 >> ZI2$) which is the opposite of what we want. This would take a toll on the amplifier's gain, since the gain stage's output signal would get damped in the output stage's terminals.

Nevertheless, the total cost of the circuit we built is 6857.4 monetary units, obtaining a merit of $M = 624.5$.