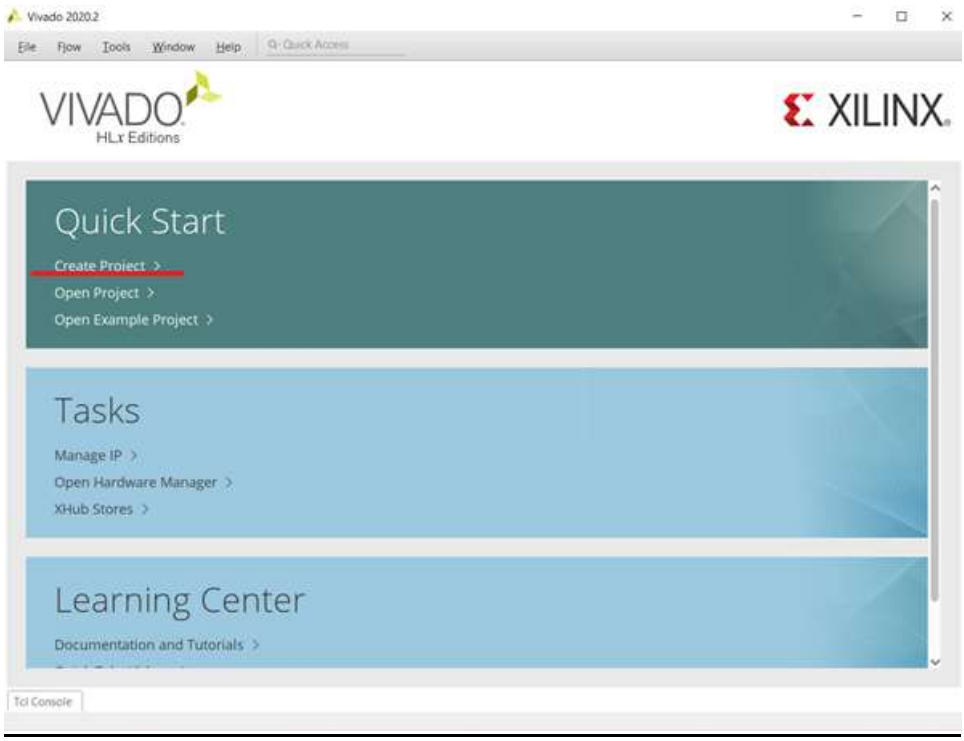
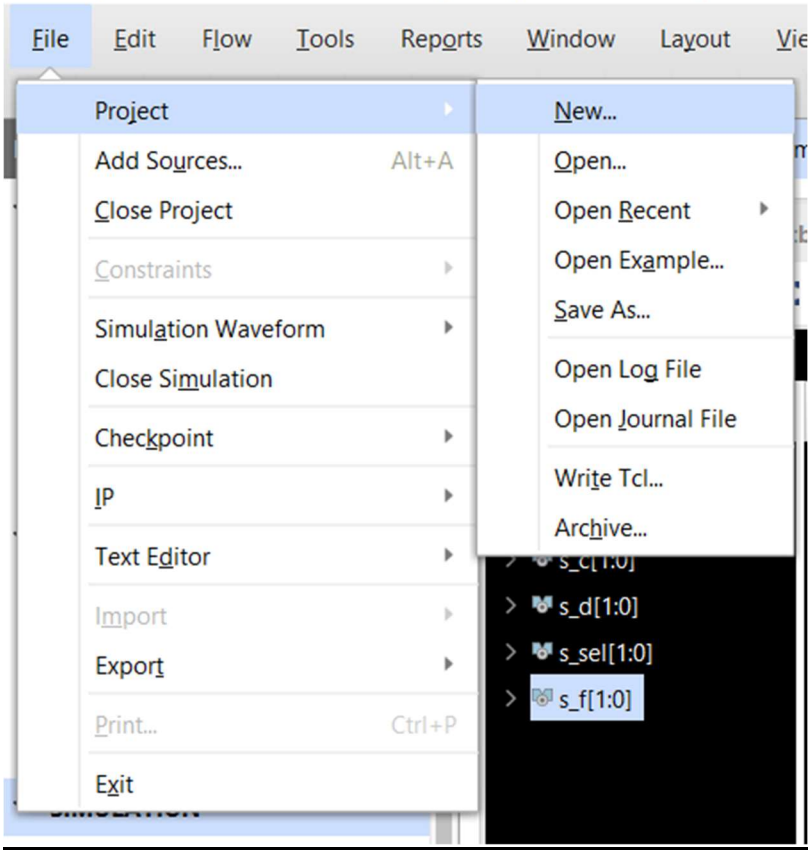
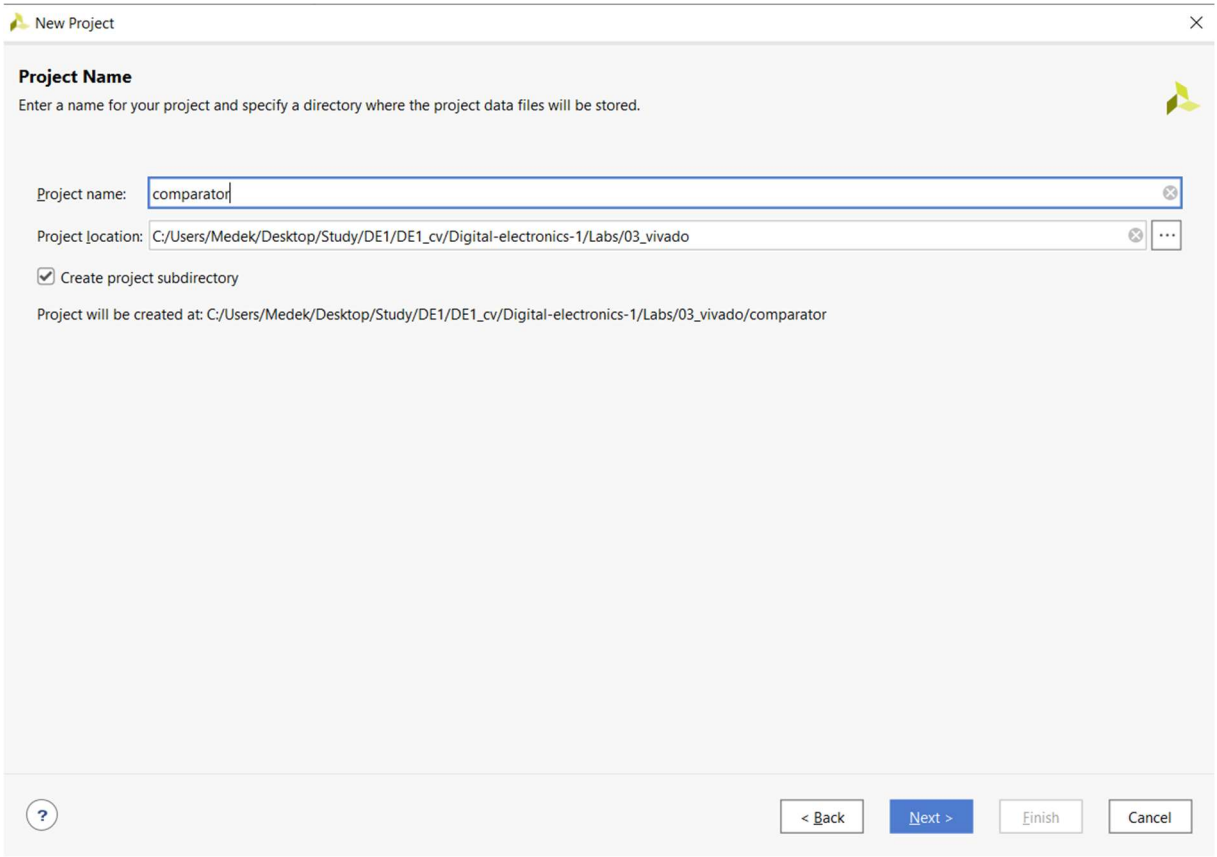
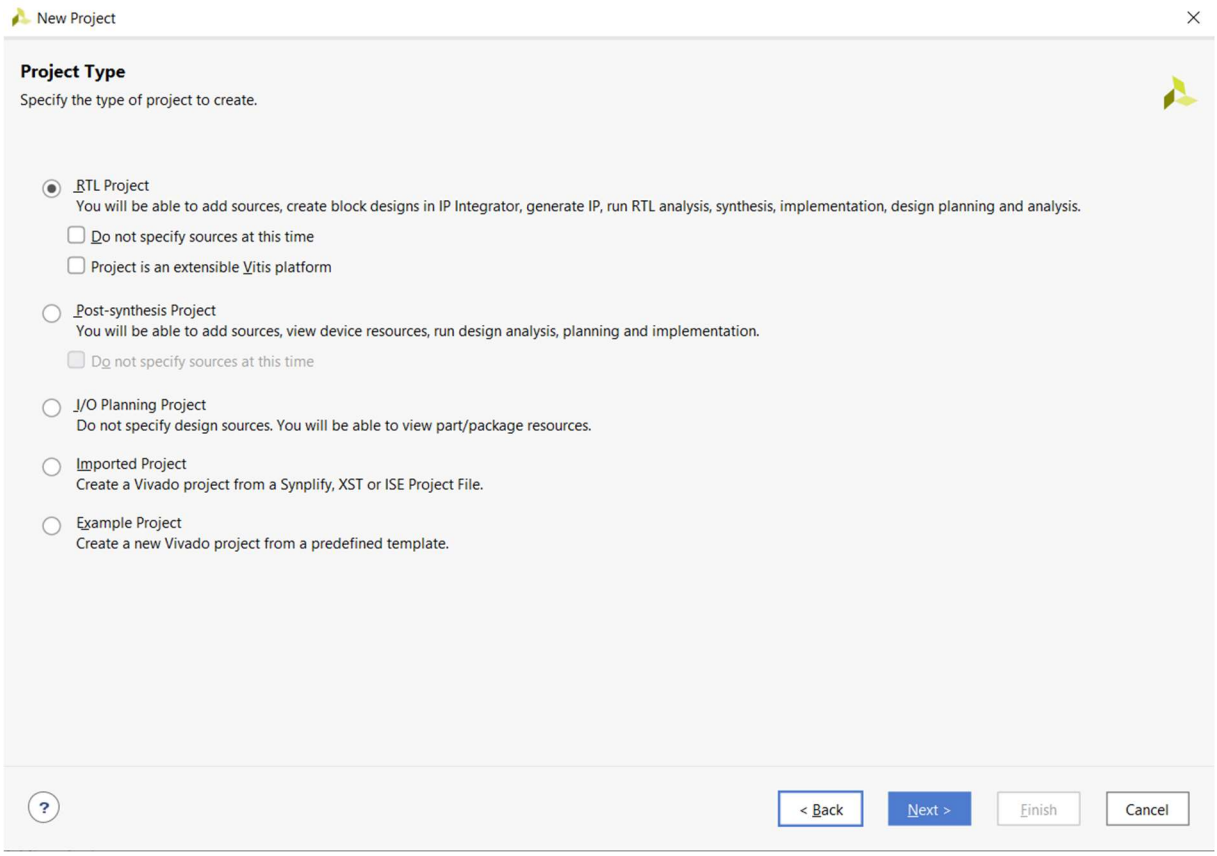
Vivado basic stuff

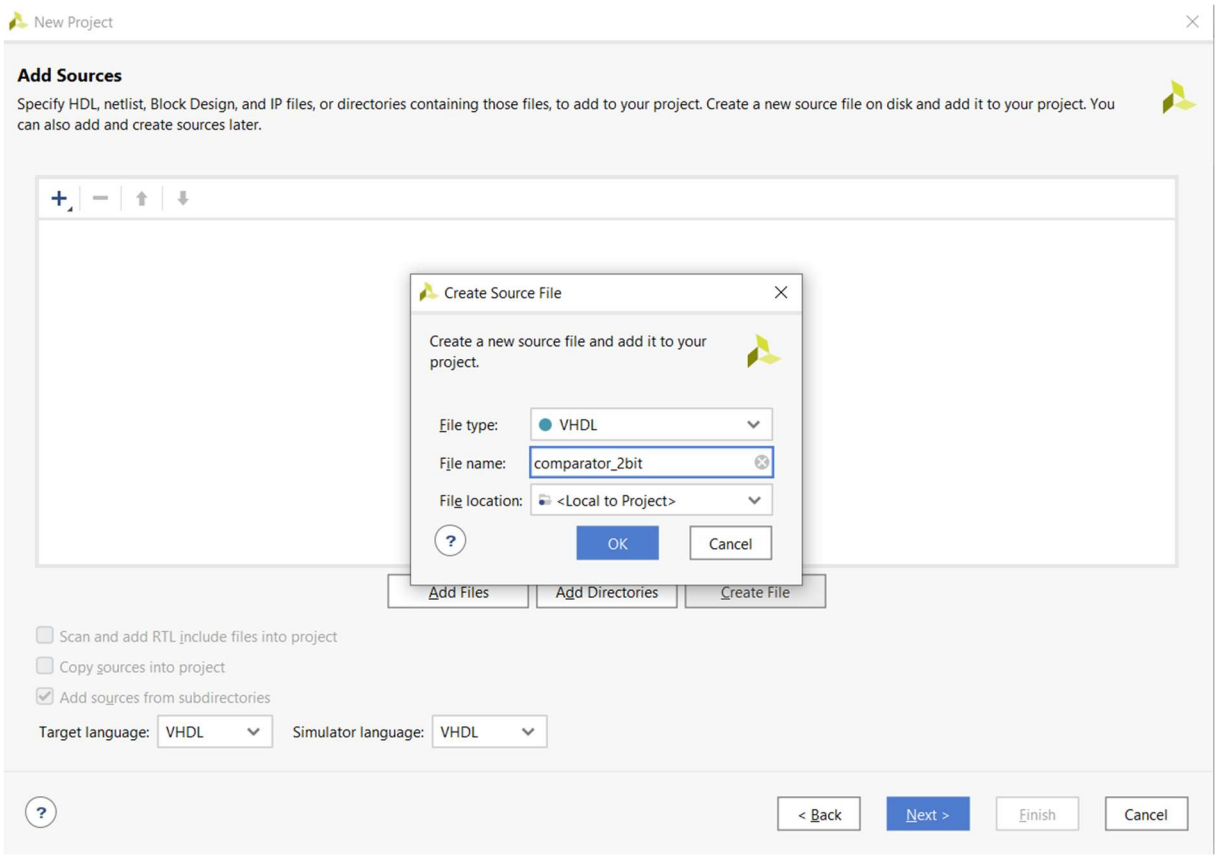
Project creation



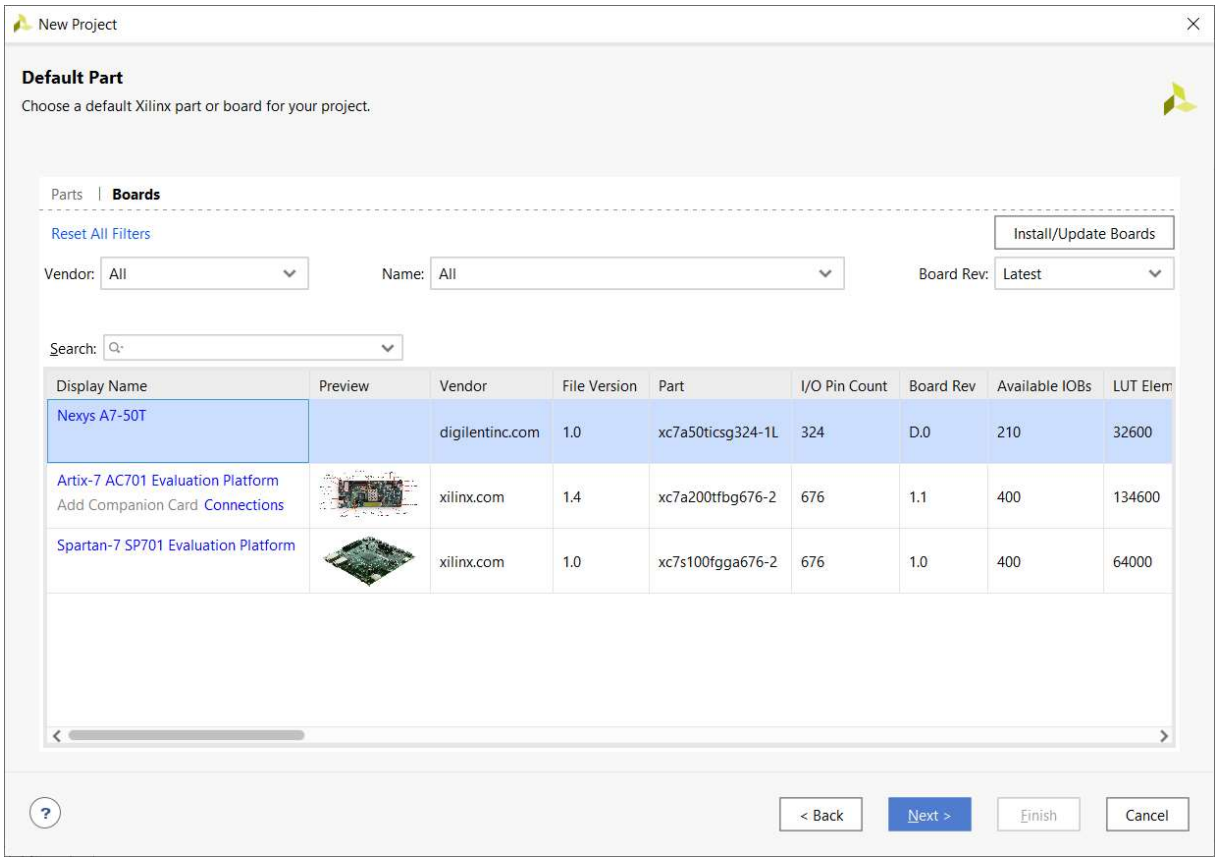


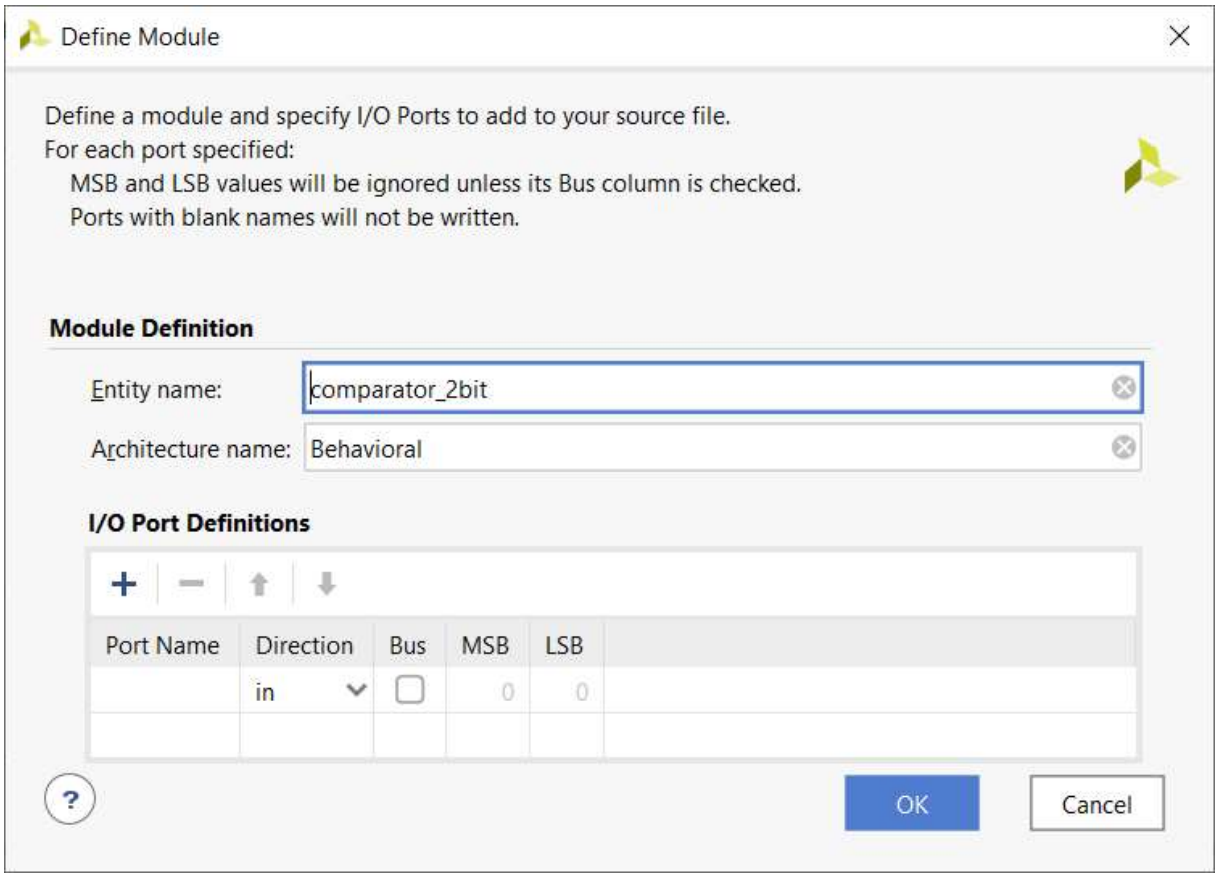

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
comparator
Project location:
C:/Users/Medek/Desktop/Study/DE1/DE1_cv/Digital-electronics-1/Labs/03_vivado
Create project subdirectory
Project will be created at: C:/Users/Medek/Desktop/Study/DE1/DE1_cv/Digital-electronics-1/Labs/03_vivado/comparator
< Back
Next >
Finish
Cancel


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

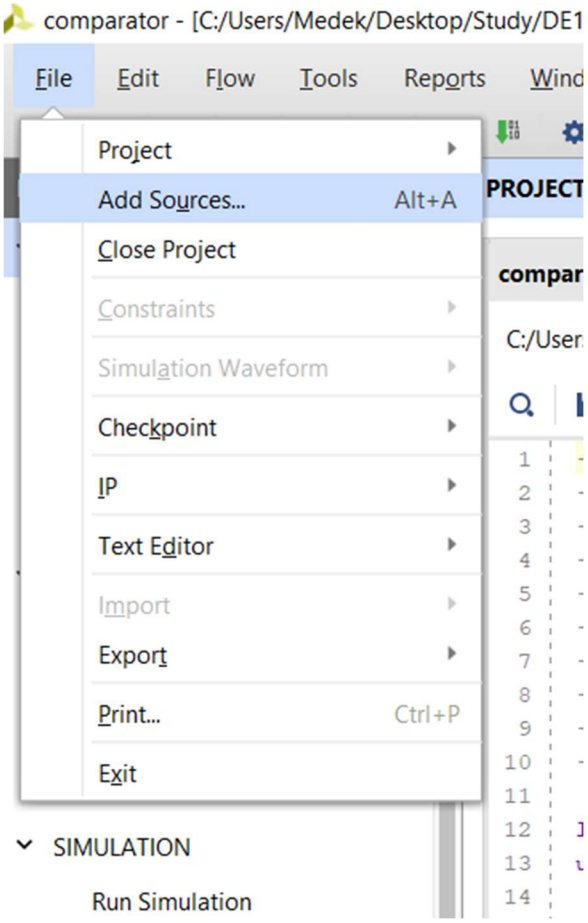


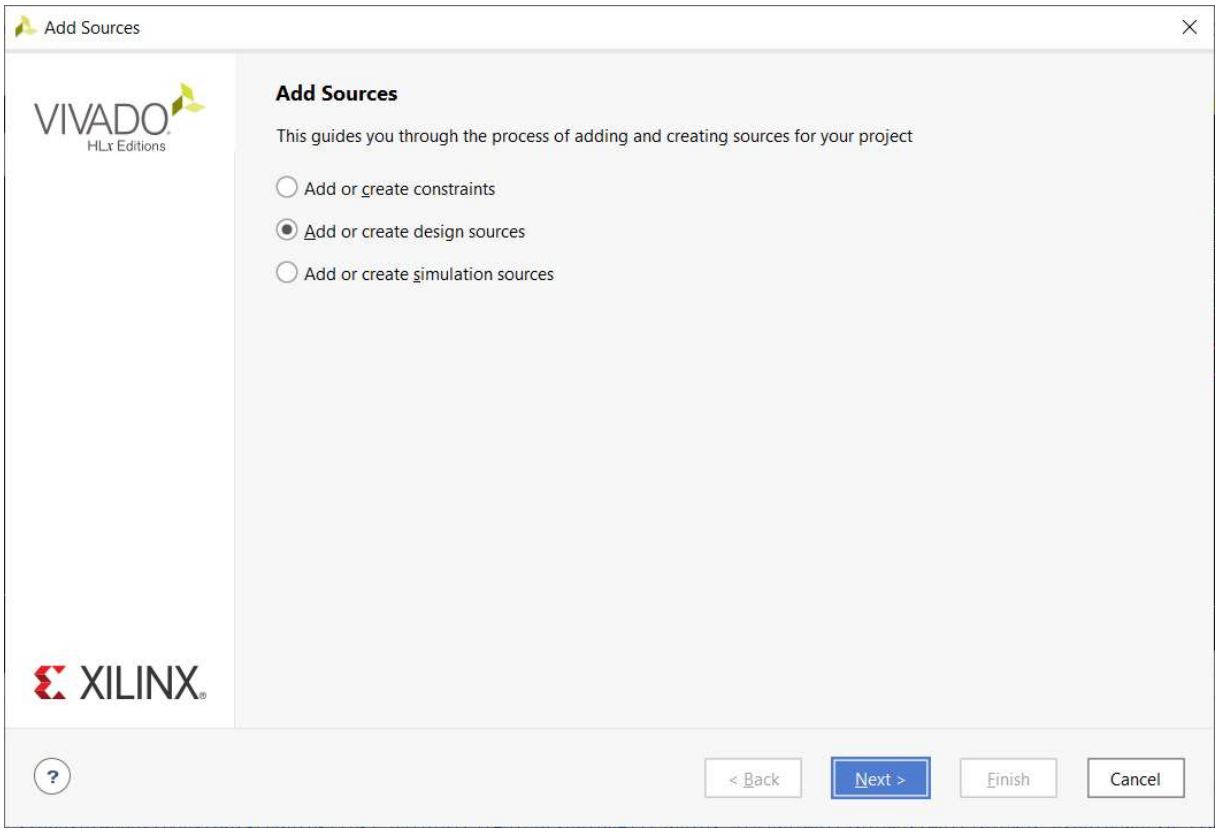
Here you have to set Target and Simulator language to VHDL

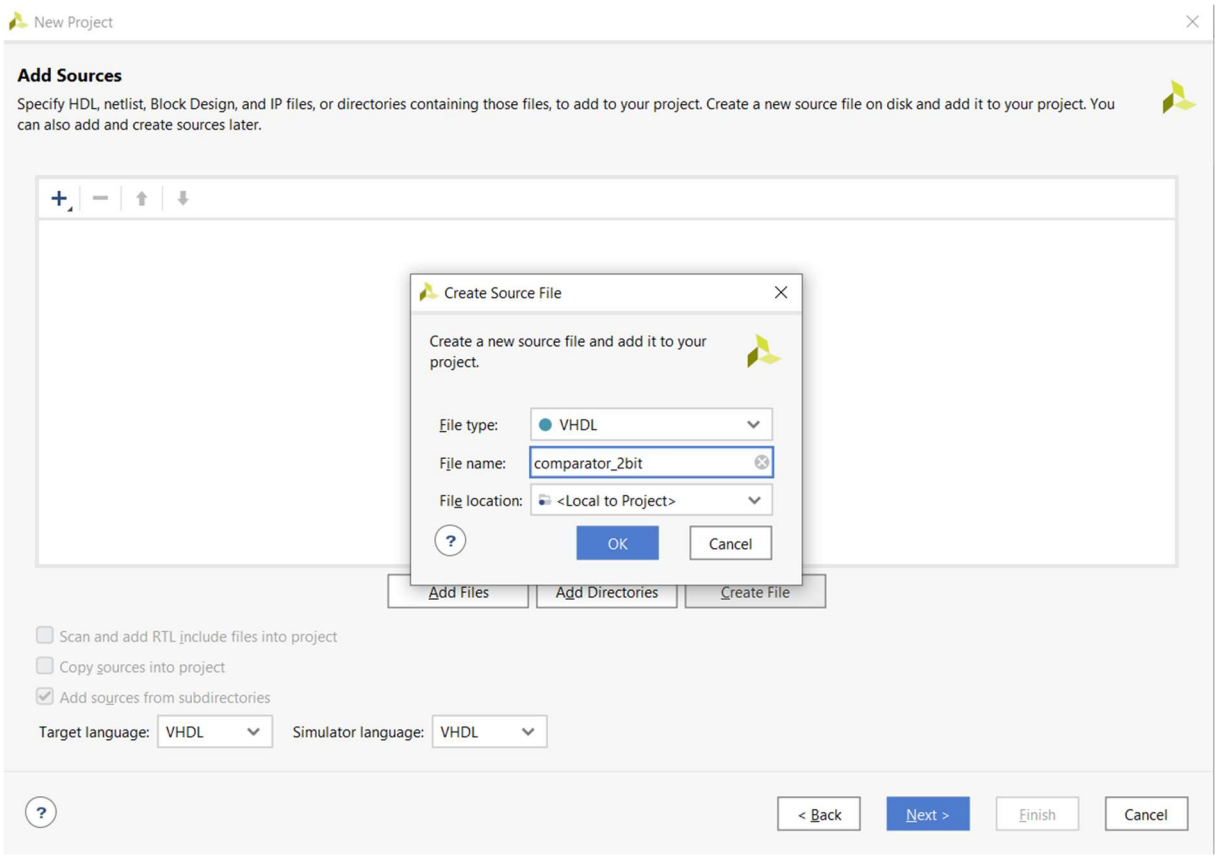


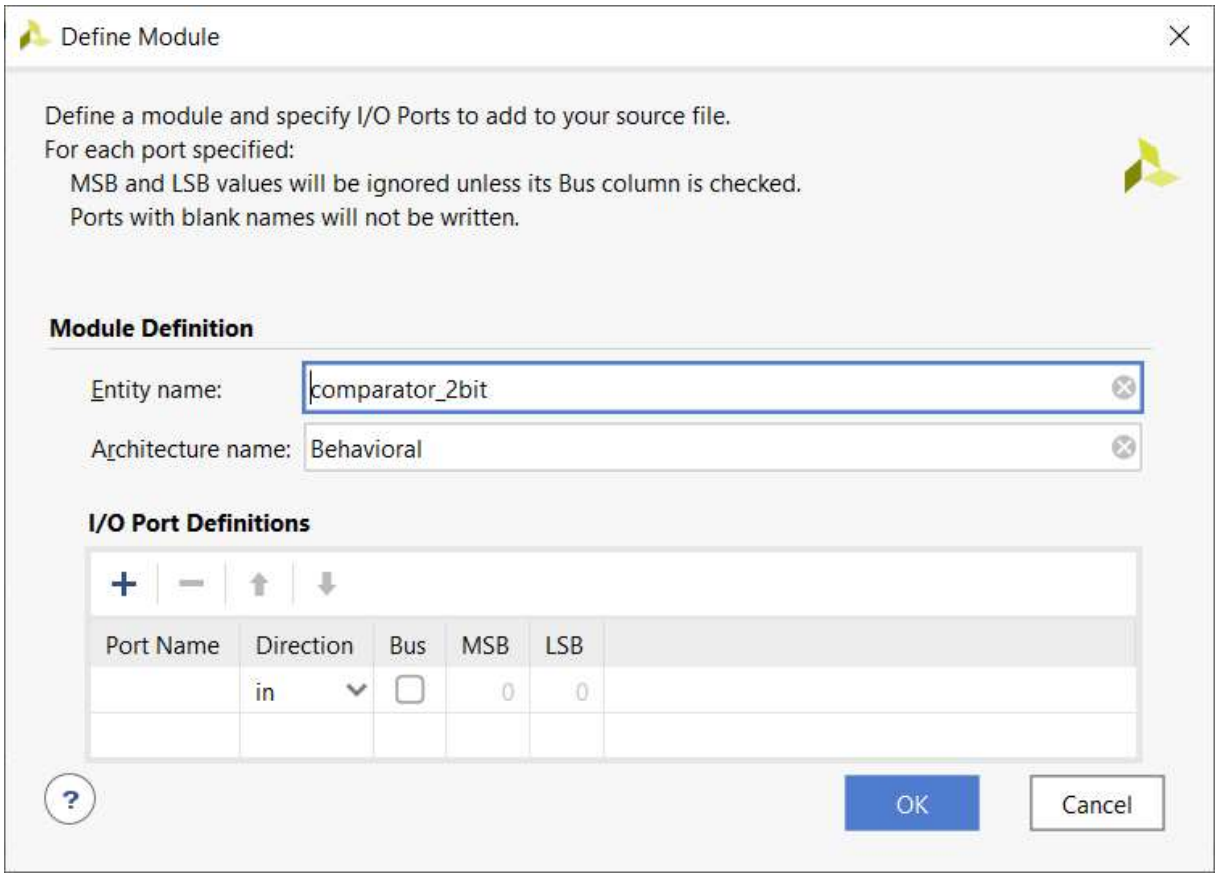

Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name:
comparator_2bit
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
?
OK
Cancel

Creating new source (design)






New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: comparator_2bit
File location: <Local to Project>
OK
Cancel
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

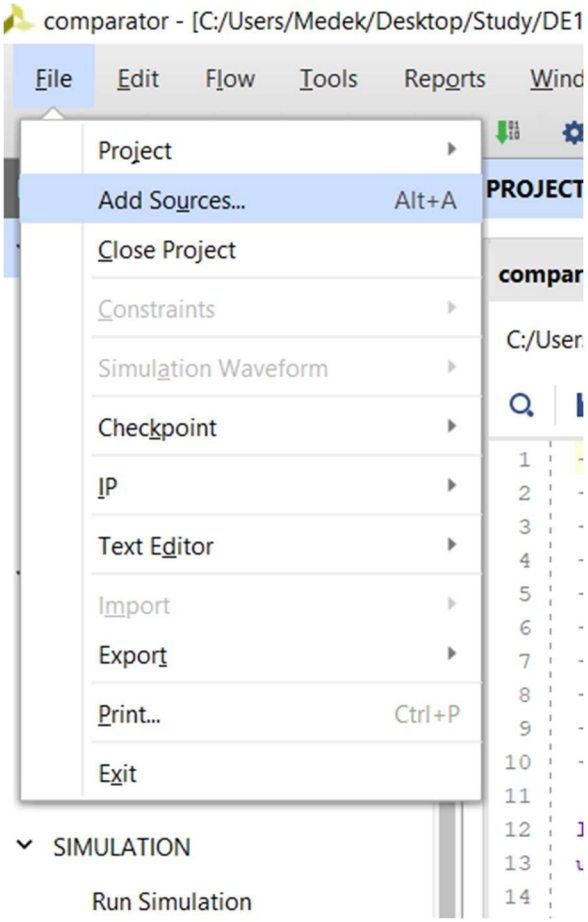

Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name: comparator_2bit
Architecture name: Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
OK
Cancel

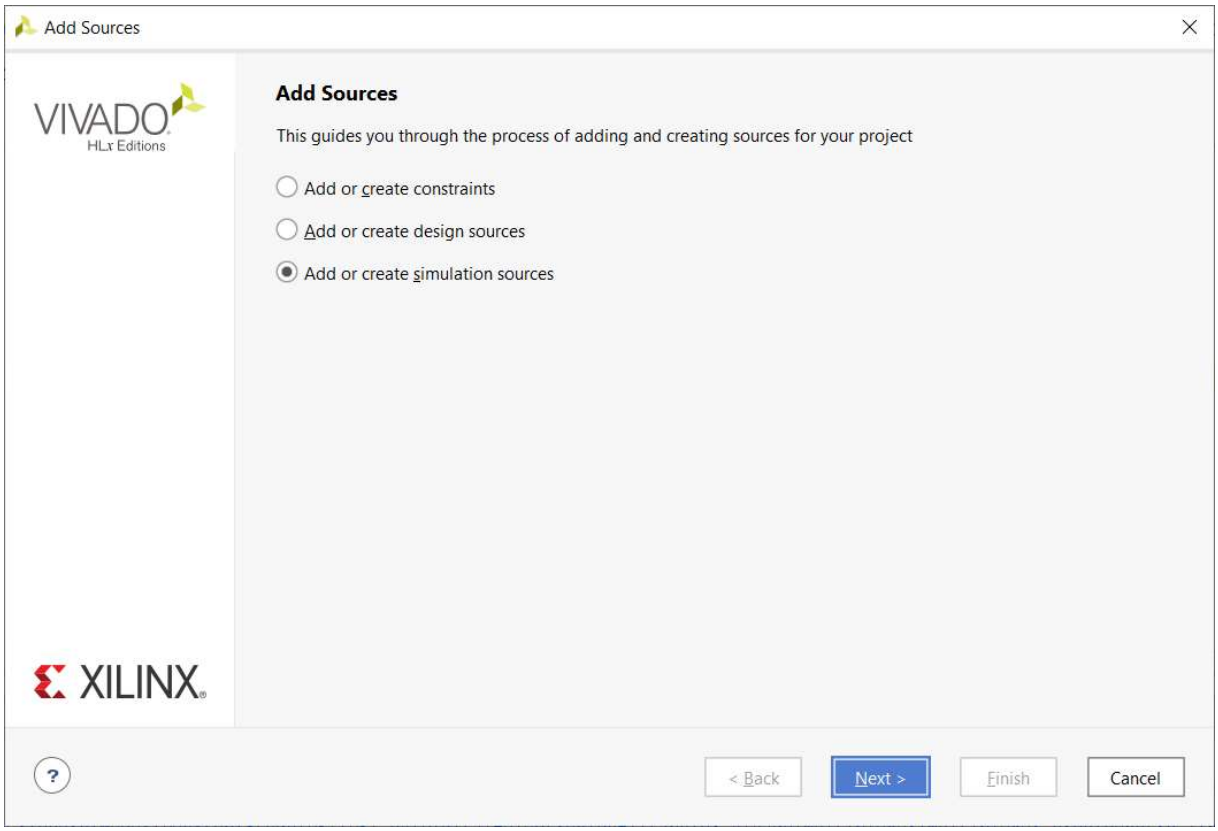
comparator_2bit.vhd

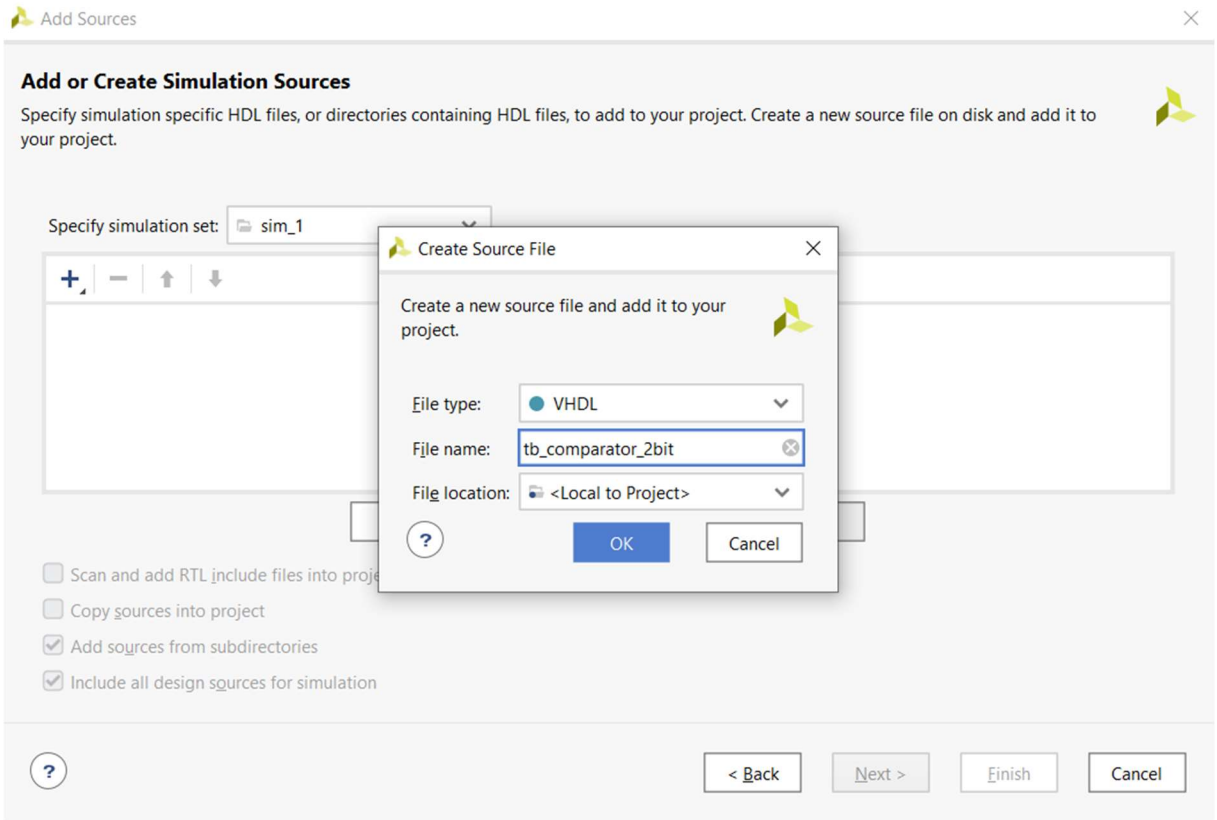
C:/Users/Medek/Desktop/Study/DE1/DE1_cv/Digital-electronics-1/Labs/03_vivado/comparator/comparator.srcs/sources_1/new/comparator_2bit.vhd

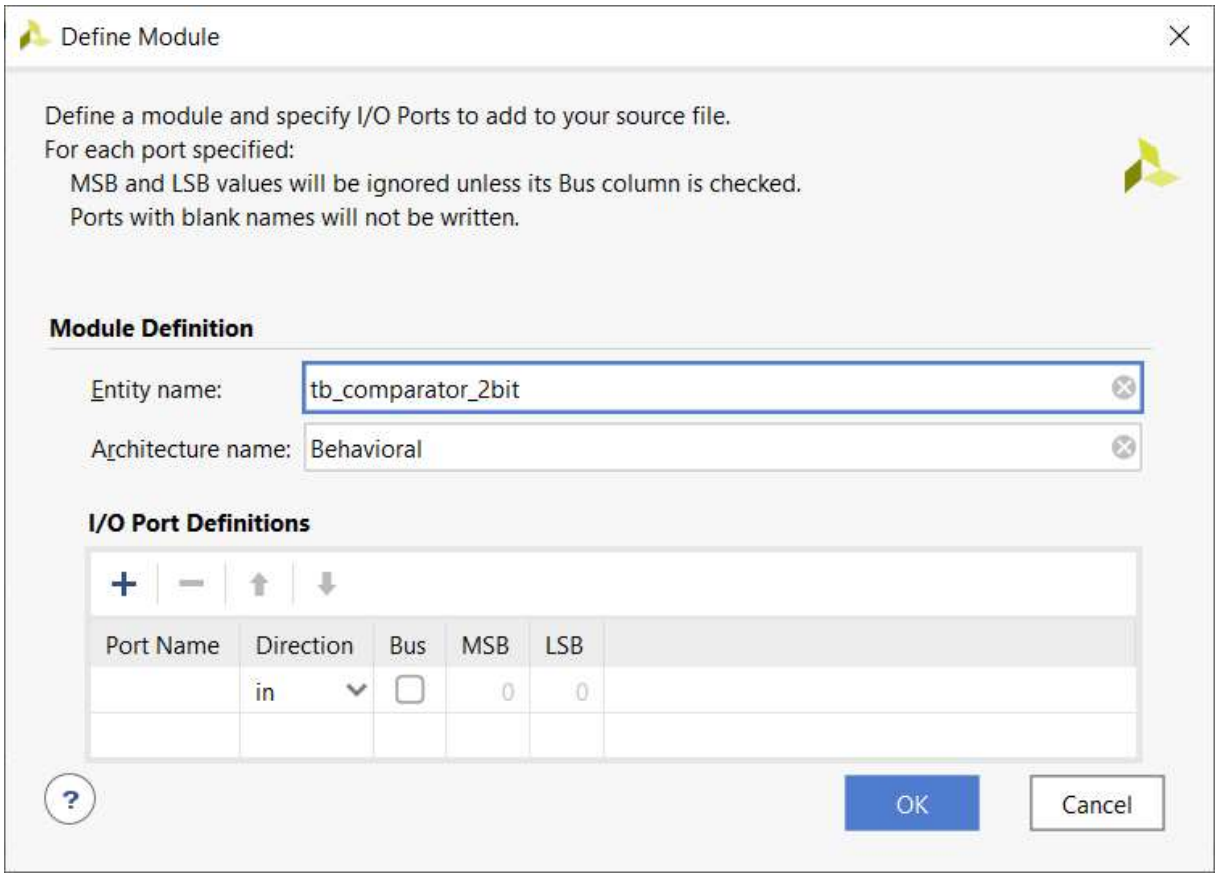
```
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity comparator_2bit is
35  --  Port ( );
36  end comparator_2bit;
37
38  architecture Behavioral of comparator_2bit is
```

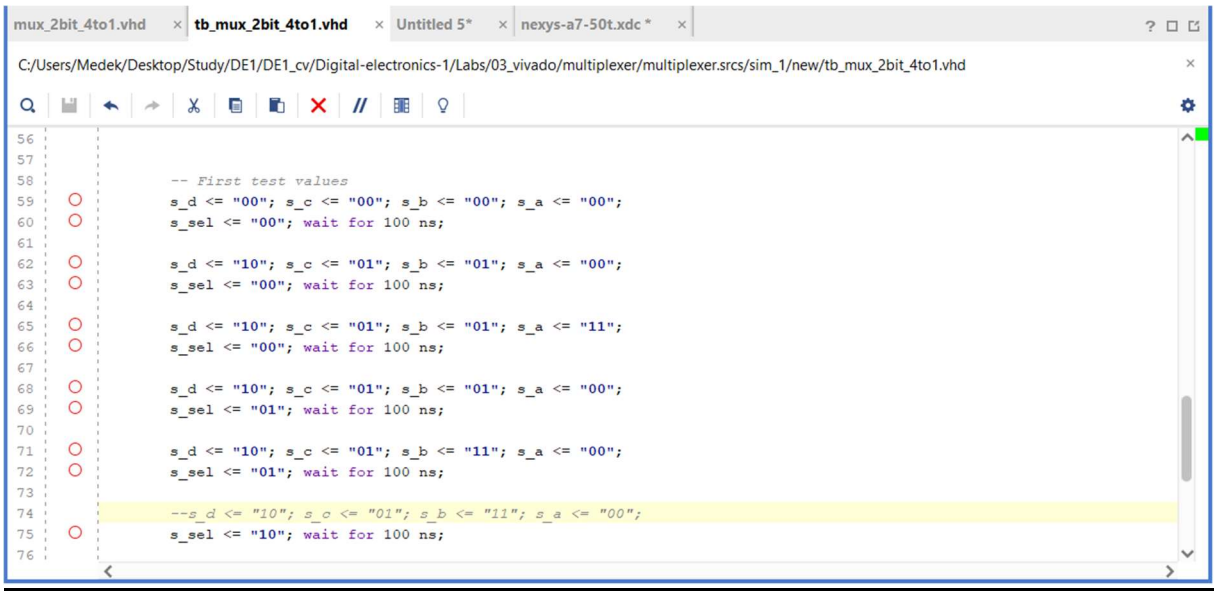
Creating new source (simulation)

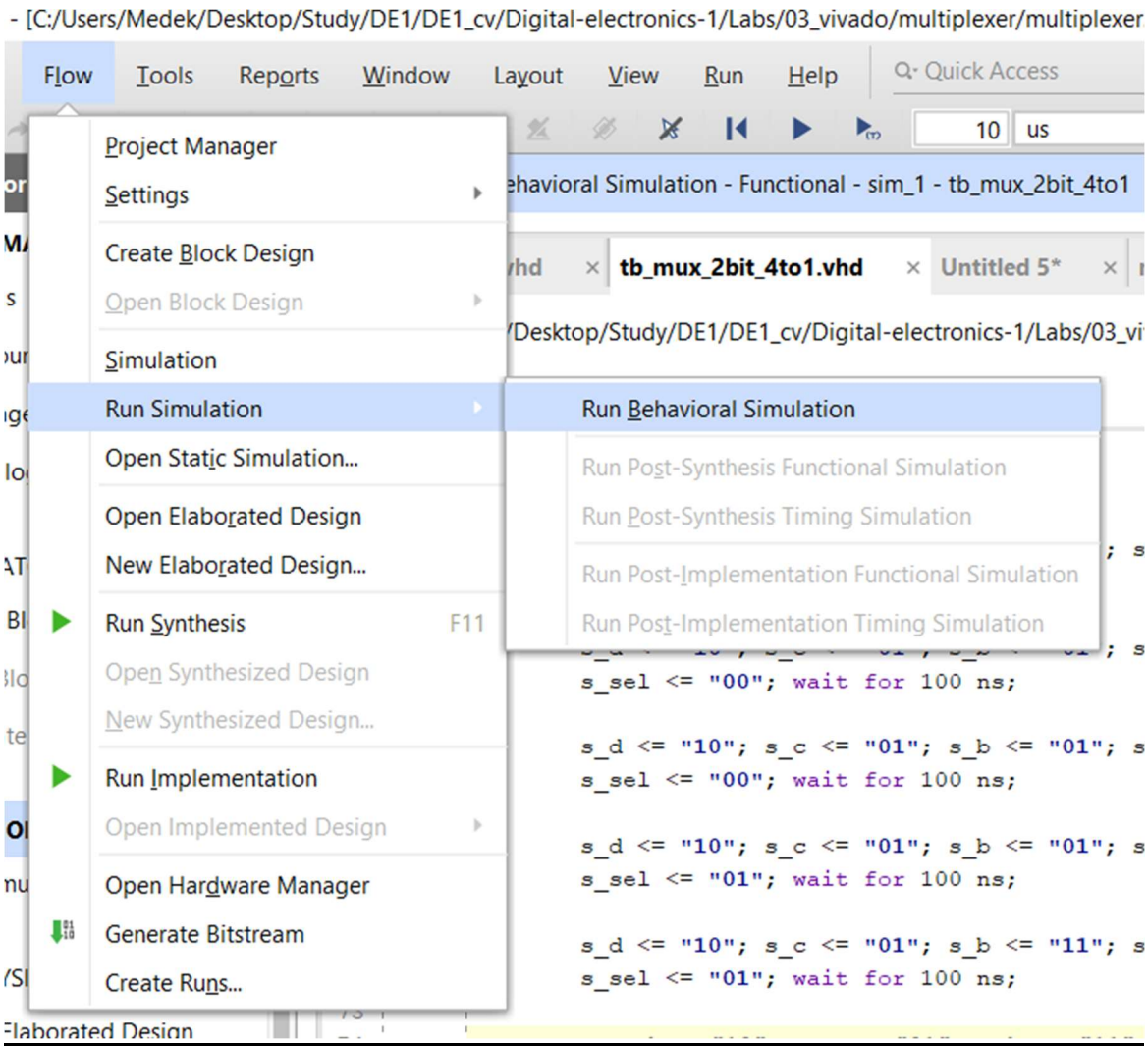


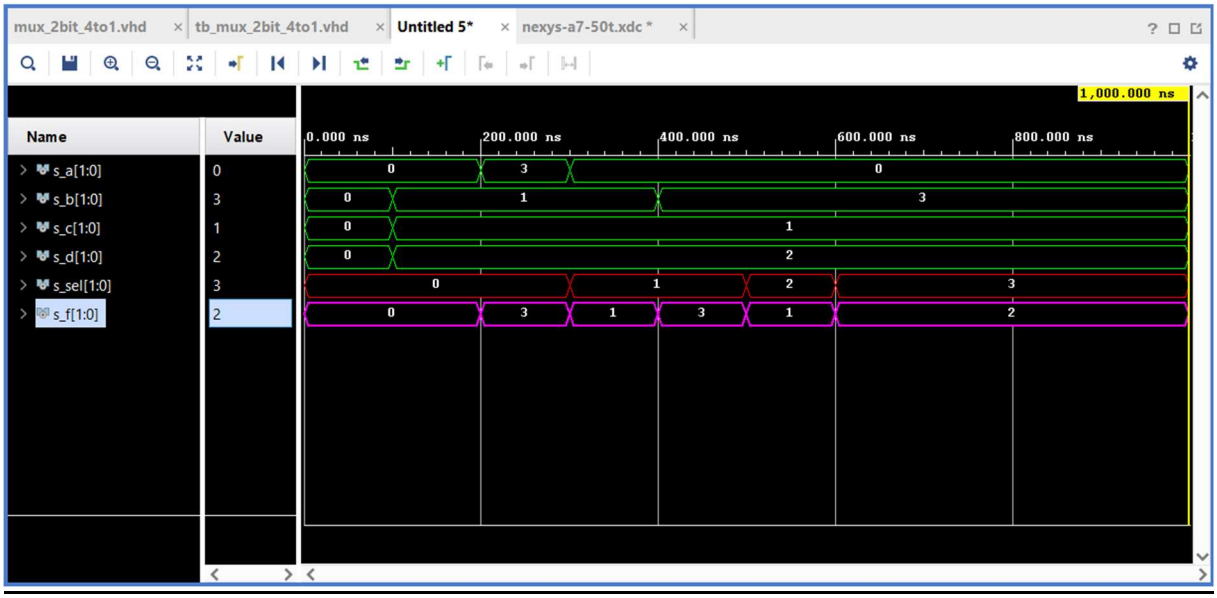

Add Sources
VIVADO
HLx Editions
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
XILINX
?
< Back
Next >
Finish
Cancel


Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
tb_comparator_2bit
File location:
<Local to Project>
?
OK
Cancel
Scan and add RTL include files into proje
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
?
< Back
Next >
Finish
Cancel

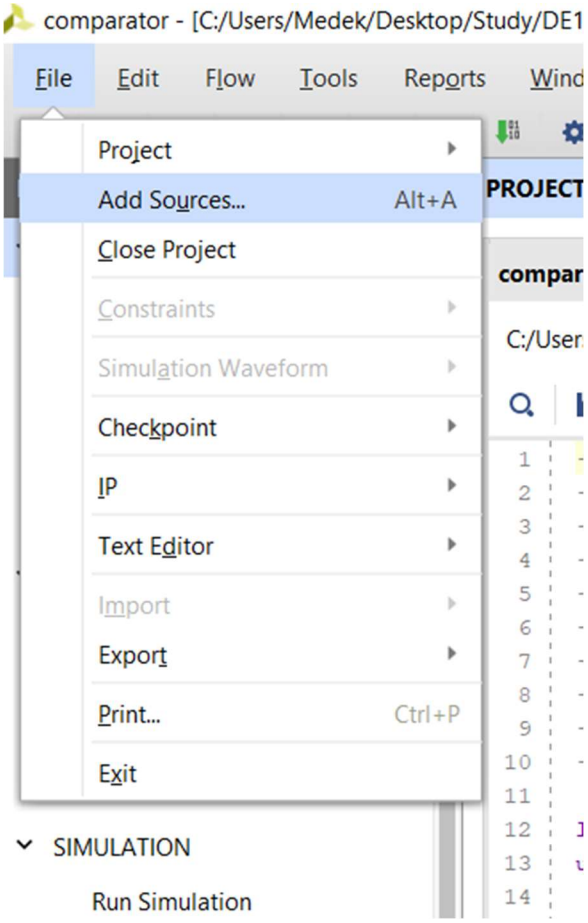

Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Entity name:
tb_comparator_2bit
Architecture name:
Behavioral
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
in
0
0
OK
Cancel

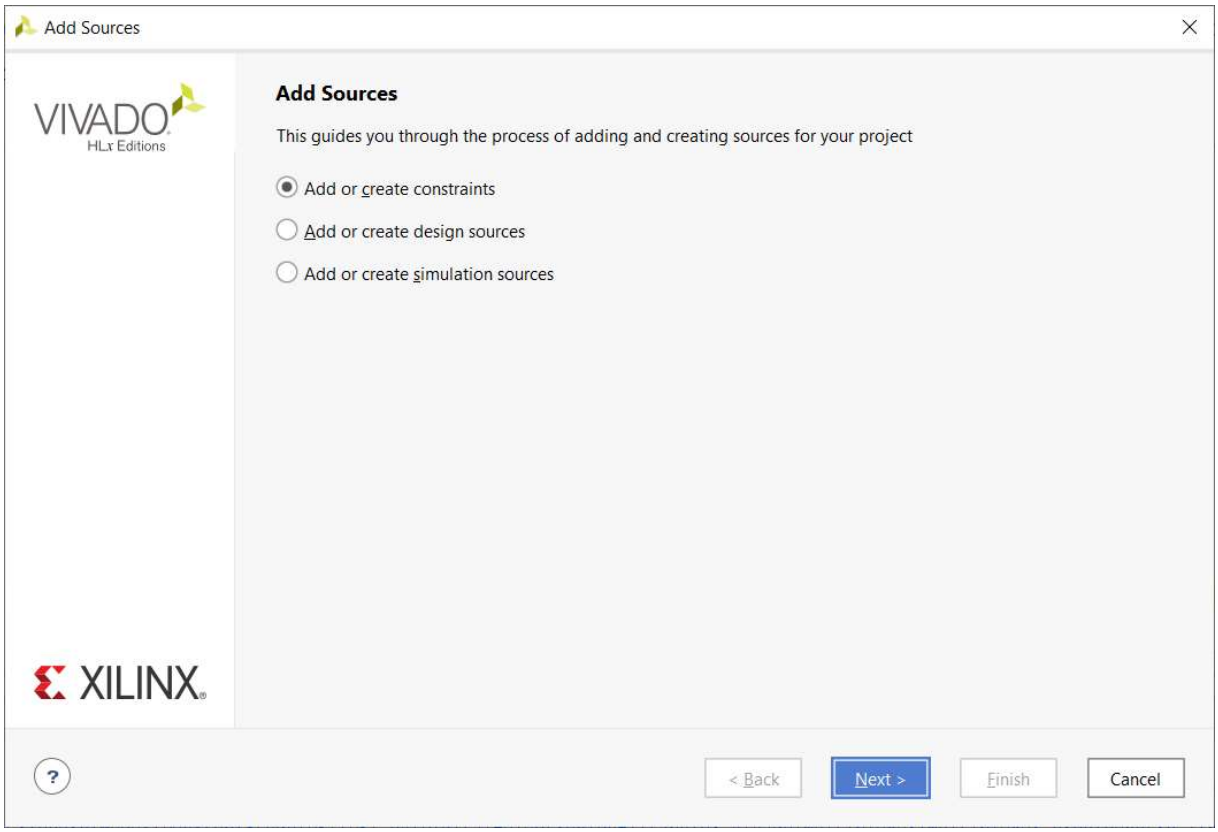

mux_2bit_4to1.vhd
tb_mux_2bit_4to1.vhd
Untitled 5*
nexys-a7-50t.xdc *
C:/Users/Medek/Desktop/Study/DE1/DE1_cv/Digital-electronics-1/Labs/03_vivado/multiplexer/multiplexer.srcs/sim_1/new/tb_mux_2bit_4to1.vhd
-- First test values
s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00";
s_sel <= "00"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "00";
s_sel <= "00"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "11";
s_sel <= "00"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "00";
s_sel <= "01"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "11"; s_a <= "00";
s_sel <= "01"; wait for 100 ns;
--s_d <= "10"; s_c <= "01"; s_b <= "11"; s_a <= "00";
s_sel <= "10"; wait for 100 ns;

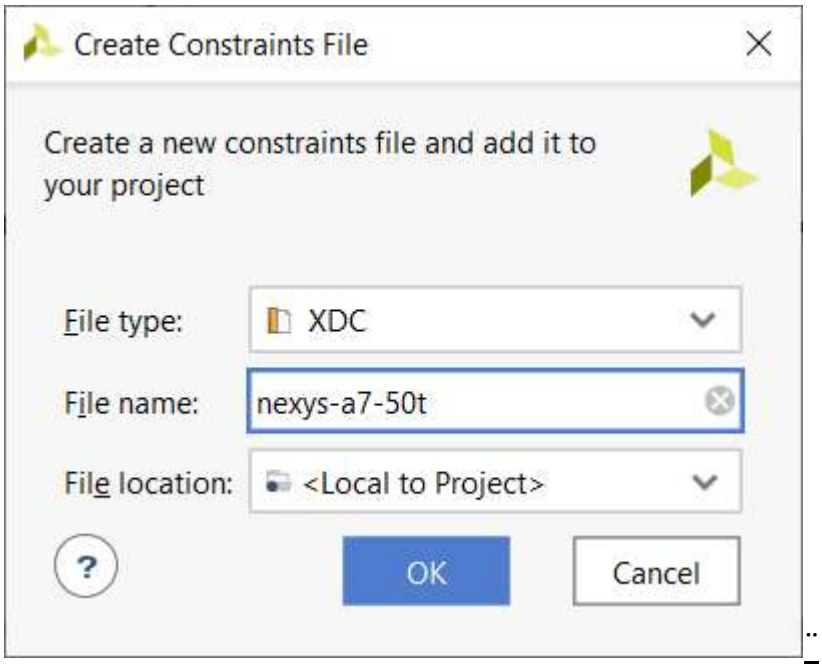

- [C:/Users/Medek/Desktop/Study/DE1/DE1_cv/Digital-electronics-1/Labs/03_vivado/multiplexer/multiplexer
Flow
Tools
Reports
Window
Layout
View
Run
Help
Quick Access
10
us
Project Manager
Settings
Create Block Design
Open Block Design
Simulation
Run Simulation
Open Static Simulation...
Open Elaborated Design
New Elaborated Design...
Run Synthesis
F11
Open Synthesized Design
New Synthesized Design...
Run Implementation
Open Implemented Design
Open Hardware Manager
Generate Bitstream
Create Runs...
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation
tb_mux_2bit_4to1.vhd
Untitled 5*
s_sel <= "00"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "01"; s
s_sel <= "00"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "01"; s
s_sel <= "01"; wait for 100 ns;
s_d <= "10"; s_c <= "01"; s_b <= "11"; s
s_sel <= "01"; wait for 100 ns;


mux_2bit_4to1.vhd
tb_mux_2bit_4to1.vhd
Untitled 5*
nexys-a7-50t.xdc *
Name
Value
s_a[1:0]
s_b[1:0]
s_c[1:0]
s_d[1:0]
s_sel[1:0]
s_f[1:0]
1,000.000 ns
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns

Creating new source (constrain)







mux_2bit_4to1.vhd | tb_mux_2bit_4to1.vhd | Untitled 5* | **nexys-a7-50t.xdc ***

C:/Users/Medek/Desktop/Study/DE1/DE1_cv/Digital-electronics-1/Labs/03_vivado/multiplexer/multiplexer.srcs/constrs_1/new/nexys-a7-50t.xdc

```
10
11  ##Switches
12  set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { a_i[0] }]; #IO_L24N_T3_RS0_15 Sch=sw[0]
13  set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { a_i[1] }]; #IO_L3N_T0_DQS_EMCCLK_14 Sch=sw[1]
14  set_property -dict { PACKAGE_PIN M13   IOSTANDARD LVCMOS33 } [get_ports { b_i[2] }]; #IO_L6N_T0_D08_VREF_14 Sch=sw[2]
15  set_property -dict { PACKAGE_PIN R15   IOSTANDARD LVCMOS33 } [get_ports { b_i[3] }]; #IO_L13N_T2_MRCC_14 Sch=sw[3]
16  set_property -dict { PACKAGE_PIN R17   IOSTANDARD LVCMOS33 } [get_ports { c_i[4] }]; #IO_L12N_T1_MRCC_14 Sch=sw[4]
17  set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports { c_i[5] }]; #IO_L7N_T1_D10_14 Sch=sw[5]
18  set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { d_i[6] }]; #IO_L17N_T2_A13_D29_14 Sch=sw[6]
19  set_property -dict { PACKAGE_PIN R13   IOSTANDARD LVCMOS33 } [get_ports { d_i[7] }]; #IO_L5N_T0_D07_14 Sch=sw[7]
20  #set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS18 } [get_ports { SW[8] }]; #IO_L24N_T3_34 Sch=sw[8]
21  #set_property -dict { PACKAGE_PIN U8    IOSTANDARD LVCMOS18 } [get_ports { SW[9] }]; #IO_25_34 Sch=sw[9]
22  #set_property -dict { PACKAGE_PIN R16   IOSTANDARD LVCMOS33 } [get_ports { SW[10] }]; #IO_L15P_T2_DQS_RDWR_B_14 Sch=sw[1
23  #set_property -dict { PACKAGE_PIN T13   IOSTANDARD LVCMOS33 } [get_ports { SW[11] }]; #IO_L23P_T3_A03_D19_14 Sch=sw[11]
24  #set_property -dict { PACKAGE_PIN H6    IOSTANDARD LVCMOS33 } [get_ports { SW[12] }]; #IO_L24P_T3_35 Sch=sw[12]
25  #set_property -dict { PACKAGE_PIN U12   IOSTANDARD LVCMOS33 } [get_ports { SW[13] }]; #IO_L20P_T3_A08_D24_14 Sch=sw[13]
26  set_property -dict { PACKAGE_PIN U11   IOSTANDARD LVCMOS33 } [get_ports { sel_i[14] }]; #IO_L19N_T3_A09_D25_VREF_14 Sch=
27  set_property -dict { PACKAGE_PIN V10   IOSTANDARD LVCMOS33 } [get_ports { sel_i[15] }]; #IO_L21P_T3_DQS_14 Sch=sw[15]
28
29  ## LEDs
30  #set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { LED[0] }]; #IO_L18P_T2_A24_15 Sch=led[0]
```