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The Instruction Set

The 6502 has a relatively basic set of instructions, many having similar functions (e.g. memory access, arithmetic, etc.). The following sections list the complete set of 56 instructions in functional groups.

Load/Store Operations

These instructions transfer a single byte between memory and one of the registers. Load operations set the negative (\underline{N}) and zero (\underline{Z}) flags depending on the value of transferred. Store operations do not affect the flag settings.

| <u>LDA</u> | Load Accumulator | <u>N,Z</u> |
|------------|-------------------|------------|
| <u>LDX</u> | Load X Register | <u>N,Z</u> |
| LDY | Load Y Register | <u>N,Z</u> |
| <u>STA</u> | Store Accumulator | |
| <u>STX</u> | Store X Register | |
| STY | Store Y Register | |

Register Transfers

The contents of the X and Y registers can be moved to or from the accumulator, setting the negative (N) and zero (Z) flags as appropriate.

| TAX | Transfer accumulator to X | <u>N,Z</u> |
|------------|---------------------------|------------|
| TAY | Transfer accumulator to Y | <u>N,Z</u> |
| <u>TXA</u> | Transfer X to accumulator | <u>N,Z</u> |
| <u>TYA</u> | Transfer Y to accumulator | <u>N,Z</u> |

Stack Operations

The 6502 microprocessor supports a 256 byte stack fixed between memory locations \$0100 and \$01FF. A special 8-bit register, S, is used to keep track of the next free byte of stack space. Pushing a byte on to the stack causes the value to be stored at the current free location (e.g. \$0100,S) and then the stack pointer is post decremented. Pull operations reverse this procedure.

The stack register can only be accessed by transferring its value to or from the X register. Its value is automatically modified by push/pull instructions, subroutine calls and returns, interrupts and returns from interrupts.

| <u>TSX</u> | Transfer stack pointer to X | <u>N,Z</u> |
|------------|----------------------------------|------------|
| <u>TXS</u> | Transfer X to stack pointer | |
| <u>PHA</u> | Push accumulator on stack | |
| PHP | Push processor status on stack | |
| <u>PLA</u> | Pull accumulator from stack | <u>N,Z</u> |
| <u>PLP</u> | Pull processor status from stack | All |

Logical

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The following instructions perform logical operations on the contents of the accumulator and another value held in memory. The BIT instruction performs a logical AND to test the presence of bits in the memory value to set the flags but does not keep the result.

| AND | Logical AND | <u>N,Z</u> |
|------------|----------------------|--------------|
| EOR | Exclusive OR | <u>N,Z</u> |
| <u>ORA</u> | Logical Inclusive OR | <u>N,Z</u> |
| BIT | Bit Test | <u>N,V,Z</u> |

Arithmetic

The arithmetic operations perform addition and subtraction on the contents of the accumulator. The compare operations allow the comparison of the accumulator and X or Y with memory values.

| <u>ADC</u> | Add with Carry | <u>N,V,Z,C</u> |
|------------|---------------------|----------------|
| <u>SBC</u> | Subtract with Carry | <u>N,V,Z,C</u> |
| <u>CMP</u> | Compare accumulator | <u>N,Z,C</u> |
| <u>CPX</u> | Compare X register | <u>N,Z,C</u> |
| <u>CPY</u> | Compare Y register | <u>N,Z,C</u> |

Increments & Decrements

Increment or decrement a memory location or one of the X or Y registers by one setting the negative (\underline{N}) and zero (\underline{Z}) flags as appropriate,

| <u>INC</u> | Increment a memory location | <u>N,Z</u> |
|------------|-----------------------------|------------|
| <u>INX</u> | Increment the X register | <u>N,Z</u> |
| INY | Increment the Y register | <u>N,Z</u> |
| <u>DEC</u> | Decrement a memory location | <u>N,Z</u> |
| <u>DEX</u> | Decrement the X register | <u>N,Z</u> |
| DEY | Decrement the Y register | <u>N,Z</u> |

Shifts

Shift instructions cause the bits within either a memory location or the accumulator to be shifted by one bit position. The rotate instructions use the contents if the carry flag ($\underline{\mathbb{C}}$) to fill the vacant position generated by the shift and to catch the overflowing bit. The arithmetic and logical shifts shift in an appropriate 0 or 1 bit as appropriate but catch the overflow bit in the carry flag ($\underline{\mathbb{C}}$).

| <u>ASL</u> | Arithmetic Shift Left | <u>N,Z,C</u> |
|------------|-----------------------|--------------|
| <u>LSR</u> | Logical Shift Right | <u>N,Z,C</u> |
| ROL | Rotate Left | <u>N,Z,C</u> |
| ROR | Rotate Right | <u>N,Z,C</u> |

Jumps & Calls

The following instructions modify the program counter causing a break to normal sequential execution. The <u>JSR</u> instruction pushes the old <u>PC</u> onto the stack before changing it to the new location allowing a subsequent <u>RTS</u> to return execution to the instruction after the call.

| <u>JMP</u> | Jump to another location | |
|------------|--------------------------|--|
| <u>JSR</u> | Jump to a subroutine | |
| RTS | Return from subroutine | |

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Branches

Branch instructions break the normal sequential flow of execution by changing the program counter if a specified condition is met. All the conditions are based on examining a single bit within the processor status.

| BCC | Branch if carry flag clear | |
|------------|-------------------------------|--|
| BCS | Branch if carry flag set | |
| BEQ | Branch if zero flag set | |
| <u>BMI</u> | Branch if negative flag set | |
| BNE | Branch if zero flag clear | |
| <u>BPL</u> | Branch if negative flag clear | |
| BVC | Branch if overflow flag clear | |
| <u>BVS</u> | Branch if overflow flag set | |

Branch instructions use relative address to identify the target instruction if they are executed. As relative addresses are stored using a signed 8 bit byte the target instruction must be within 126 bytes before the branch or 128 bytes after the branch.

Status Flag Changes

The following instructions change the values of specific status flags.

| CLC Clear carry flag | <u>C</u> |
|----------------------------------|----------|
| CLD Clear decimal mode flag | <u>D</u> |
| CLI Clear interrupt disable flag | <u>I</u> |
| CLV Clear overflow flag | <u>V</u> |
| SEC Set carry flag | <u>C</u> |
| SED Set decimal mode flag | <u>D</u> |
| SEI Set interrupt disable flag | <u>I</u> |

System Functions

The remaining instructions perform useful but rarely used functions.

| BRK Force an interrupt | <u>B</u> |
|---------------------------|----------|
| NOP No Operation | |
| RTI Return from Interrupt | All |

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