AKENTEN APPIAH-MENKA UNIVERSITY
of Skills Training and Entrepreneural Development

Vote

#1

ABIGAIL KOBINA

INFOTESS WOMEN'S COMMISSIONER (WOCOM)

Hopeful 2022

WOMEN EMPOWERMENT
A Skill, an Essential
Tool for Financial Independence

ROEVER ENGINEERING COLLEGE
ELAMBALUR, PERAMBALUR- 621 212
DEPARTMENT OF INFORMATION TECHNOLOGY

2 Marks and 16 marks Questions

Subject Code & Name: CS 2253-COMPUTER ORGANIZATION AND ARCHITECTURE

UNIT-I
BASIC STRUCTURE OF COMPUTERS

1.Define Computer Architecture.

Computer Architecture Is Defined As The Functional Operation Of The Individual H/W Unit In A Computer System And The Flow Of Information Among The Control Of Those Units.

2.Define Computer H/W.

Computer H/W Is The Electronic Circuit And Electro Mechanical Equipment That Constitutes The Computer

3. What are the functions of control unit ?

The memory arithmetic and logic ,and input and output units store and process information and perform i/p and o/p operation, the operation of these unit must be co ordinate in some way this is the task of control unit the cu is effectively the nerve center that sends the control signal to other units and sence their states.

4.What is an interrupt?

An interrupt is an event that causes the execution of one program to be suspended and another program to be executed.

5. What are the uses of interrupts?

- ✓ Recovery from errors
- ✓ Debugging
- ✓ Communication between programs
- ✓ Use of interrupts in operating system

6.What is the need for reduced instruction chip?

- ✓ Relatively few instruction types and addressing modes.
- ✓ Fixed and easily decoded instruction formats.
- ✓ Fast single-cycle instruction execution.
- ✓ Hardwired rather than microprogrammed control.

7. Name any three of the standard I/O interface.

- ✓ SCSI (small computer system interface),bus standards
- ✓ Back plane bus standards
- ✓ IEEE 796 bus (multibus signals)
- ✓ NUBUS
- ✓ IEEE 488 bus standard

8. Differentiate between RISC and CISC

Refer ur book

9. Explain the various classifications of parallel structures.

- ✓ SISD (single instruction stream single data stream
- ✓ SIMD(single instruction stream multiple data stream
- ✓ MIMD(multiple instruction stream multiple data stream
- ✓ MISD(multiple instruction stream single data stream

10. What is absolute addressing mode?

The address of the location of the operand is given explicitly as a part of the instruction.

Eg. Move a , 2000

11. Specify three types of data transfer techniques.

- ✓ Arithmetic data transfer
- ✓ Logical data transfer
- ✓ Programmed control data transfer

12. What is the role of MAR and MDR?

The MAR (memory address register) is used to hold the address of the location to or from which data are to be transferred and the MDR(memory data register) contains the data to be written into or read out of the addressed location.

13. What are the various types of operations required for instructions?

- ✓ Data transfers between the main memory and the CPU registers
- ✓ Arithmetic and logic operation on data
- ✓ Program sequencing and control
- ✓ I/O transfers

14. What is the role of IR and PC?

Instruction Register (IR) contains the instruction being executed. Its output is available to the control circuits, which generate the timing signals for controlling the processing circuits needed to execute the instructions. The Program Counter (PC) register keeps track of the execution of the program. It contains the memory address of the instruction currently being executed . During the execution of the current instruction, the contents of the PC are updated to correspond to the address of the next instructions to be executed.

15.What are the various units in the computer?

- ✓ Input unit
- ✓ Output unit
- ✓ Control unit
- ✓ Memory unit
- ✓ Arithmetic and logical unit

16.What is an I/O channel?

An i/o channel is actually a special purpose processor, also called peripheral processor.The main processor initiates a transfer by passing the required information in the input output channel. the channel then takes over and controls the actual transfer of data.

17.What is a bus?

A collection of wires that connects several devices is called a bus.

18.Define word length?

Each group of n bits is referred to as a word of information and n is called the word length.

19.Explain the following the address instruction?

- ✓ Three-address instruction-it can be represented as add a,b,c Operands a,b are called source operand and c is called destination operand.
- ✓ Two-address instruction-it can be represented as Add a,b
- ✓ One address instruction-it can be represented as add a

20.Zero address instruction.

It is also possible to use instruction where the location s of all operand are defined implicitly. This operand of the use of the method for storing the operand in which called push down stack. Such instructions are sometimes referred to us zero address instruction.

21.What is the straight-line sequencing?

The CPU control circuitry automatically proceed to fetch and execute instruction, one at a time in the order of the increasing addresses. This is called straight line sequencing.

22.What is the role of PC?

The CPU contains a register called the program counter, which holds the address of instruction to be executed next.. to begin the execution of the program the address of its

First instruction must be placed into the pc.

23. Define Signal

Signal - The binary information is represented in digital computers by physical quantities

called signals.

24. Define Gates

Gates – The manipulation of binary information is done by logic circuits called gates. Gates are blocks of hardware that produce signals of binary 1 or 0 where input logic requirements are satisfied.

25. Define Flip flop.

Flip flop – The storage elements employed in clocked sequential circuits are called flip

flops. A flip flop is a binary cell capable of storing 1 bit of information.

26.State and explain the performance equation?

Suppose that the average number of basic steps needed to execute one machine instruction is S, where each basic step is completed in one clock cycle. If the clock cycle rate is R cycles per second, the program execution time is given by

$$\mathbf{T = (N \times S) / R}$$

This is often referred to as the basic performance equation.

27. Define CPI

The term ClockCyclesPerInstruction Which is the average number of clock cycles each instruction takes to execute, is often abbreviated as CPI.

CPI= CPU clock cycles/Instruction count.

28. Define MIPS .

MIPS:One alternative to time as the metric is MIPS(Million Instruction Per Second) MIPS=Instruction count/(Execution time x1000000). This MIPS measurement is also called Native MIPS todistinguish it from some alternative definitions of MIPS.

29.Define MIPS Rate.

ate at which the instructions are The rexecuted at a given time.

30.Define Throughput and Throughput rate.

Throughput -The total amount of work done in a given time.

Throughput rate-The rate at which the total amount of work done at a given time.

POSSIBLE BIG QUESTIONS

1. Draw and explain the block diagram of a simple computer with five functional units.
2. What is RISC? Explain with proper example.
3. What is CISC ?Explain with proper example.
4. What are the techniques used to measure the performance of a computer?
5. What do you mean by addressing modes? Explain various addressing modes with the help of examples.
6. Briefly discuss about basic operational concepts in computer.
7. Explain in detail about instructions and instruction sequencing.
8. Write short notes on Hardware and Software interface.
9. Discuss about Bus Structures.
10. Explain the representation of floating point numbers in detail.

UNIT-II
BASIC PROCESSING UNIT

1.Specify the sequence of operation involved when an instruction is executed.

a)Instruction Fetch
b)Instruction Decode
c)Operand Fetch
d)Execute

e) Write Back

2.Define parallel processing.

Parallel processing is a term used to denote a large class of techniques that are used to provide simultaneous data-processing tasks for the purpose of increasing the computational speed of a computer system. Instead of processing each instruction sequentially as in a conventional computer, a parallel processing system is able to perform concurrent data processing to achieve faster execution time

3. Define sequential circuits.

A sequential circuit is an interconnection of flip-flops and gates. The gates by themselves constitute a combinational circuit, but when included with the flip flops, the overall circuit is classified as a sequential circuit.

4.Define interface.

The word interface refers to the boundary between two circuits or devices

5.Define processor clock.

Processor clock: Processor circuits are controlled by a timing signal called processor clock, the clock defines regular time interval called clock cycle.

6. Define latency.

The term memory latency is used to refer to the amount of time it takes to transfer a word of data to or from the memory. The term latency is used to denote the time it takes to transfer the first word of data. This time is usually substantially longer than the time needed to transfer each subsequent word of a block.

7. Define bandwidth.

Bandwidth is a product of the rate at which the data are transferred (and accessed) and the width of the data bus.

8. Define hit rate.

A successful access to data in a cache is called a hit. Number of hits stated as a fraction of all attempted accesses is called the hit rate.

9. Define miss rate.

A miss rate is the number of misses stated as a fraction of attempted accesses. Extra time needed to bring the desired information into the cache is called the miss penalty.

10.Define Clock Rate:

Clock rate, R=1/p cycles/sec(hz)

Where p is length of one clock cycle

11.Define Throughput:

The total amount of work done in a given time

12.Different types of buses.

1.Synchronous bus
2.Asynchronous bus

13. What is micro programming and micro programmed control unit?

Microprogramming is a method of control unit design in which the control unit selection and sequencing information are stored in ROM and RAM's called control store or control memory. Micro programmed control unit is a general approach used for implementation of control unit. Here control signals are generated by a program similar to machine language programs.

14. What is meant by hardwired control?

It is the one that contains control units that use fixed logic circuits to interpret instructions and generate control signals from them. Here, the fixed logic circuit block includes combinational circuit that generates the required control outputs for decoding and encoding functions.

15. What is Register Renaming?

If a temporary register assumes the role of the permanent register whose data it is holding and is given the same name is called as the Register Renaming.

16. What is the function of commitment unit?

When out-of-order execution is allowed, a s pecial control unit called as "commitment unit" is used to guarantee in-order commitment. It uses a queue called the "reorder buffer" to determine which instruction should be committed next. This is the function of commitment unit.

17. What is the neccesity of grouping signals?

It is used to reduce the number of the bits in the microinstruction. It is used to overcome the draw back of assigning individual bits to each control signal results in long microinstructions, because the number of the required signals is usually large, moreover only a few bits are used in any given instruction.

18.List the techniques used for grouping of the control signals?

a) Vertical organization
b) Horizontal organization

19 List out Various branching technique used in micro program control unit?

a) Bit-Oring
b) Using Conditional Variable
c) Wide Branch Addressing

20. Define the term Clock Rate.

They are two possibilities for increasing the clock rate, R. First, improving the IC technology makes logic circuits faster, which reduces the time needed to complete a basic step. This allows the clock period P to be reduce and the clock rate R to be increased Second, reducing the amount of processing done is one basic step makes it possible to reduce the clock period P.

21. What do you mean by out-of order execution? Is it Desirable?

In a pipelined processor with several instructions is process concurrently it is Possible for instruction to finish out of sequence, one instruction finishes before Another which is issuedearlier, as far as main computation is concerned no Hazards will happen but if an interrupts occurs it creates the problem.

22. Define Overflow

Overflow -In the single precision, if the number requires a exponent greater then +127 or in a double precision, if the number requires an exponent form the overflow occurs.

23.Define Underflow

Underflow-In a single precision ,if the number requires an exponent less than -26 or in a double precision, if the number requires an exponent less than -1022 to represent its normalized form the underflow occurs.

24. What are Condition Codes (CC)? Explain the use of them.

Condition Codes are the list of possible conditions that can be tested during conditional instructions.CC is used to test the condition (<, =,>).

Based on this result, Jump instructions move to specified loop.CC flags represent the value of processor that keeps the information about the results of various operations for use by conditional branches.

25. What is straight –line sequencing?

Process of fetching and executing an instruction; one at a time in order of increasing address with the help of information in program counter

POSSIBLE BIG QUESTIONS

1. a)How will you perform arithmetic or logic operation?
   b)How to fetch a word from memory and store a word in memory?
2. What is meant by hardwired control? Draw and explain typical hardwire control unit.
3. What is meant by microprogramming? Draw and explain the micro programmed control unit.
4. List the advantages and disadvantages of micro programmed control unit over hardwire control unit.
5. Explain in detail about nano programming and list out its benefits.

UNIT-III
PIPELINING

1.Define pipelining.

Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments.S

2.Define parallel processing.

Parallel processing is a term used to denote a large class of techniques that are used to provide simultaneous data-processing tasks for the purpose of increasing the computational mspeed of a computer system. Instead of processing each instruction sequentially as in a conventional computer, a parallel processing system is able to perform concurrent data processing to achieve faster execution time.

3.Define instruction pipeline.

The transfer of instructions through various stages of the CPU instruction cycle., including fetch opcode, decode opcode, compute operand addresses. Fetch operands, execute instructions and store results. This amounts to realizing most (or) all of the CPU in the form of multifunction pipeline called an instruction pipelining.

4. What are the steps required for a pipelinened processor to process the instruction?

□□F Fetch: read the instruction from the memory
□□D Decode: decode the instruction and fetch the source operand(s).
□□E Execute: perform the operation specified by the instruction.
□□W Write: store the result in the destination location

5. What are Hazards?

A hazard is also called as hurdle .The situation that prevents the next instruction in the instruction stream from executing during its designated Clock cycle. Stall is introduced by hazard. (Ideal stage)

6. State different types of hazards that can occur in pipeline.

The types of hazards that can occur in the pipelining were,
1. Data hazards.
2. Instruction hazards.
3. Structural hazards.

7. Define Data hazards

A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has to be delayed, and the pipeline stalls.

8. Define Instruction hazards

The pipeline may be stalled because of a delay in the availability of an instruction. For example, this may be a result of miss in cache, requiring the instruction to be fetched from the main memory. Such hazards are called as Instruction hazards or Control hazards.

9.Define Structural hazards?

The structural hazards is the situation when two instructions require the use of a given hardware resource at the same time. The most common case in which this hazard may arise is access to memory.

10. What are the classification of data hazards?

Classification of data hazard: A pair of instructions can produce data hazard by referring reading or writing the same memory location. Assume that i is executed before J. So, the hazards can be classified as,
1. RAW hazard
2. WAW hazard

3. WAR hazard

11.Define RAW hazard : (read after write)
Instruction ‘j’ tries to read a source operand before instruction ‘i’ writes it.
12. Define WAW hazard :(write after write)
Instruction ‘j’ tries to write a source operand before instruction ‘i’ writes it.
13.Define WAR hazard :(write after read)

Instruction ‘j’ tries to write a source operand before instruction ‘i’ reads it.

14. How data hazard can be prevented in pipelining?
Data hazards in the instruction pipelining can prevented by the following techniques.
a)Operand Forwarding

b)Software Approach

15.How Compiler is used in Pipelining?
A compiler translates a high level language program into a sequence of machine instructions. To reduce N, we need to have suitable machine instruction set and a compiler that makes good use of it. An optimizing compiler takes advantages of various features of the target processor to reduce the product N*S, which is the total number of clock cycles needed to execute a program. The number of cycles is dependent not only on the choice of instruction, but also on the order in which they appear in the program. The compiler may rearrange program instruction to achieve better performance of course, such changes must not affect of the result of the computation.
16. How addressing modes affect the instruction pipelining?
Degradation of performance is an instruction pipeline may be due to address dependency where operand address cannot be calculated without available informatition needed by addressing mode for e.g. An instructions with register indirect mode cannot proceed to fetch the operand if the previous instructions is loading the address into the register. Hence operand access is delayed degrading the performance of pipeline
17. What is locality of reference?
Many instruction in localized area of the program are executed repeatedly during some time period and the remainder of the program is accessed relatively infrequently .this is referred as locality of reference.
18. What is the need for reduced instruction chip?
□□Relatively few instruction types and addressing modes.
□□Fixed and easily decoded instruction formats.
□□Fast single-cycle instruction execution.
□□Hardwired rather than micro programmed control
19. Define memory access time?
The time that elapses between the initiation of an operation and completion of that operation ,for example ,the time between the READ and the MFC signals .This is Referred to as memory access time.
20. Define memory cycle time.
The minimum time delay required between the initiations of two successive memory operations, for example, the time between two successive READ operations.
21.Define Static Memories.
Memories that consist of circuits capable of retaining the state as long as power is applied are known as static memories.
22. List out Various branching technique used in micro program control unit?
a) Bit-Oring
b) Using Conditional Variable
c) Wide Branch Addressing

23. How the interrupt is handled during exception?

* CPU identifies source of interrupt
* CPU obtains memory address of interrupt handles
* pc and other CPU status information are saved
* Pc is loaded with address of interrupt handler and handling program to handle it.

24. List out the methods used to improve system performance.

The methods used to improve system performance are

1. Processor clock
2.Basic Performance Equation
3.Pipelining
4.Clock rate
5.Instruction set
6.Compiler

25. What is DMA?

A special control unit may be provided to enable transfer a block of data directly between an external device and memory without contiguous intervention by the CPU. This approach is called DMA.

POSSIBLE BIG QUESTIONS

1.State and explain the different types of hazards that can occur in a pipeline.
2.Draw and explain the structure of a superscalar processor. Also explain the flow of instruction execution in it.
3.what are the two aspects of machine instruction? Explain it .
4.Draw and explain the modified three-bus structure of the processor suitable for four -stage pipelined execution. How this structure is suitable to provide four-stage pipelined execution?

UNIT-IV
MEMORY SYSTEM

1.Give the classification of the Optical Media

Optical media can be classified as
CD-ROM – Compact Disk Read Only Memory
WORM – Write Once Read Many
Rewriteable - Erasable
Multifunction – WORM and Erasable

2. What is a Mini Disk?

Minidisk for data (MD-Data) is the data version of the new rewriteable storage format developed by Sony Corporation for both business and entertainment as a convenient medium for carrying music , video and data. MD can be used in three formats to support all potential uses as follows:
--A premastered optical disk
--A recordable magneto-optical disk
--A hybrid that is partially mastered and partially recordable

3. List some applications for WORM.

--Some of the application or WORM devices are
--On-Line catalogs such as automobile party's dealer
--Large Volume Distribution
--Transaction logging such as stock trading company
--Multimedia Archival

4. What are multifunctional drives

A multifunctional drive is a single unit which is capable of reading and writing a variety of disk media. This type of drive provides the permanence of a read-only device as well as full flexibility of a rewriteable device along with the powerful intermediate write once capability

5. What are types of technology used in s multifunctional drive?

Three types of technologies utilized for multifunctional drives are
*Magneto – Optical Disk for both rewriteable and WORM capability
*Magneto- Optical disk for rewriteable and dye polymer disk for WORM capability
*Phase change technology for both rewriteable and WORM capability

6.. What is Migration and Archiving?

The process of moving an object from one level in the storage hierarchy to another level in that hierarchy is called migration. Migration of Objects to off-line media and removal of these objects from on-line media is called archiving.

7. How do we use a jukebox?

A juke box is used for storing large volumes of multimedia information in one cost effective store . Jukebox – based optical disk libraries can be networked so that multiple users can access the information. Opticla disk libraries serve as nearline storage for infrequently use data.

8. List a few requirements imposed by advanced multimedia applications

Some of the requirements imposed by multimedia application are
*Support for windows – based GUI, such as Microsoft Windows
*Capability to run applications in Multitasking environments
*Support for Multi – User Applications
*Network – bases client –server distributed applications

9. What is the use of High water marks in a cache?

Cache design use a high-water mark and a low water mark to trigger cache management operations. When the cache storage fiklls up to the high – water mark , the cache manager starts creating more space in cache storage. Space is created by discarding objects that have not been modified and writing back those object that have been modified.

10. What are the various cache usage in a LAN –based system?

In a LAN – based system there can be as many as three stages of caches as follows

1. Disk Cache or System memory cache
2. Hard Disk cache for each object server
3. Shared network cache for all object servers

11. What are the multimedia applications which use caches?

Some Multimedia application areas where cache is extensively used are

*Multimedia Entertainment
*Education
*Office Systems
*Audio and video Mail
*Computer Architecture - Set 6

12. Explain virtual memory technique.

Techniques that automatically move program and data blocks into the physical memory when they are required for execution are called virtual memory technique

13. What are virtual and logical addresses?

The binary addresses that the processor issues for either instruction or data are called virtual or logical addresses.

14. Define translation buffer.

Most commercial virtual memory systems incorporate a mechanism that can avoid the bulk of the main memory access called for by the virtual to physical addresses translation buffer. This may be done with a cache memory called a translation buffer.

15. What is branch delay slot?

The location containing an instruction that may be fetched and then discarded because of the branch is called branch delay slot.

16. What is optical memory?

Optical or light based techniques for data storage, such memories usually employ optical disk which resemble magnetic disk in that they store binary information in concentric tracks on an electromechanically rotated disks. The information is read as or written optically, however with a laser replacing the read write arm of a magnetic disk drive. Optical memory offer high storage capacities but their access rate is are generally less than those of magnetic disk.

17. What are static and dynamic memories?

Static memory are memories which require periodic no refreshing. Dynamic memories are memories, which require periodic refreshing.

18. What are the components of memory management unit?

A facility for dynamic storage relocation that maps logical memory references into physical memory addresses.

A provision for sharing common programs stored in memory by different users .

19. What is the role of MAR and MDR?

The MAR (memory address register) is used to hold the address of the location to or from which data are to be transferred and the MDR(memory data register) contains the data to be written into or read out of the addressed location.

20. Distinguish Between Static RAM and Dynamic RAM?

Static RAM are fast, but they come at high cost because their cells require several transistors. Less expensive RAM can be implemented if simpler cells are used. However such cells do not retain their state indefinitely; Hence they are called Dynamic RAM.

21. Distiguish between asynchronies DRAM and synchronous RAM.

The specialized memory controller circuit provides the necessary control signals, RAS

And CAS ,that govern the timing. The processor must take into account the delay in the response of the memory. Such memories are referred to as asynchronous DRAMS.The DRAM whose operations is directly synchronized with a clock signal. Such Memories are known as synchronous DRAM.

22. What do you mean associative mapping technique?

The tag of an address received from the CPU is compared to the tag bits of each block of the cache to see if the desired block is present. This is called associative mapping technique.

23. What is SCSI?

Small computer system interface can be used for all kinds of devices including RAID storage subsystems and optical disks for large- volume storage applications.

24. What are the two types of latencies associated with storage?

The latency associated with storage is divided into 2 categories

1. Seek Latencies which can be classified into Overlapped seek,Mid transfer seek and Elevator seek
2. Rotational Latencies which can be reduced either by Zero latency read or Write and Interleave factor.

25. What are the data management activities involved in a storage?

a. Command queuing : allows execution of multiple sequential commands with system CPU intervention. It helps in minimizing head switching and disk rotational latency

b. Scatter – gather : Scatter is a process whereby data is set for best fit in available block of memory or disk. Gather reassembles data into contiguous blocks on disk or in memory

26. What do you mean by Disk Spanning?

Disk spanning is a method of attaching drives to a single host uadapter. All drives appear as a single contiguous logical unit. Data is written to the first drive first and when the drive is full, the controller switches to the second drive, then the second drive writes until its full.

28. List some objectives for using RAID Systems

-RAID systems are used to meet the following objectives
-Hot backup of disk systems
-Large volume storage at lower cost
-Higher performance at lower cost
-Ease of data recovery
-High MTBF

29. What are the different levels RAID?

There are six discrete levels of RIAD functionality. They are
-Level 0 – Disk Striping
-Level 1 – Disk Mirroring
-Level 2 – Bit Interleaving of Data
-Level 3 – Bit Interleaving with dedicated parity drives
- Level 4 – Sector interleaving of data with dedicated parity drive
-Level 5 – Block interleaving of data.

30.Two Types of storage devices.

1.Primary Memory
2.Secondary Memory

POSSIBLE BIG QUESTIONS

1.Define cache memory. Explain the mapping process followed in cache memory. Also discuss the relative advantages and disadvantages of the mapping techniques used.

2.What is virtual memory? Why is it necessary to implement virtual memory? Explain the virtual memory address translation.

3.Draw and explain the various types of secondary storage devices.

4.a)Explain about RAM.

b)Explain about ROM.

UNIT-V
I/O ORGANIZATION

1.Explain very briefly about ESDI Hard Drive

ESDI stands for enhanced small device interface was developed by a consortium of several manufacturers. ESDI converts the data into serial bit streams and uses the RLL encoding scheme to pack more bits per sector. ESDI drives store a defect map containing the locations of bad and defective sectors on the drive.

2. Explain in brief about IDE

Integrated device electronics contains an integrated controller with the drive as a single unit. Interface is a simple 16-bit parallel data interface and requires the data to be written and does not need to be told where and how to write the data on the disk. .IDE Interface supports 2 drives – one drive has to be configured as the master and the second as the slave.

3. What is SCSI?

Small computer system interface can be used for all kinds of devices including RAID storage subsystems and optical disks for large- volume storage applications.

4. Define the term RELIABILITY

.

"Means feature that help to avoid and detect such faults. A realible system does not silently continue and delivery result that include interrected and corrupted data, instead it corrects the corruption when possible or else stops

5.Define the term AVAILABLITY:

"Means features that follow the systerm to stay operational even offen faults do occur. A highly available systerm could dis able do the main functioning portion and continue operating at the reduced capacity"

6. How the interrupt is handled during exception?

* cpu identifies source of interrupt
* cpu obtains memory address of interrupt handles
* pc and other cpu status information are saved
* Pc is loaded with address of interrupt handler and handling program to handle it

7. What is IO mapped input output?

A memory reference instruction activated the READ M (or)WRITE M control line and does not affect the IO device. Separate IO instruction are required to activate the READ IOand WRITE IO lines ,which cause a word to be transferred between the address aio port and the CPU. The memory and IO address space are kept separate.

8.Specify the three types of the DMA transfer techniques?

--Single transfer mode(cyclestealing mode)
--Block Transfer Mode(Brust Mode)
--Demand Transfer Mode
--Cascade Mode

9. What is an interrupt?

An interrupt is an event that causes the execution of one program to be suspended and another program to be executed.

10.What are the uses of interrupts?

*Recovery from errors
*Debugging
*Communication between programs
*Use of interrupts in operating system

11.Define vectored interrupts.

In order to reduce the overhead involved in the polling process, a device requesting an

interrupt may identify itself directly to the CPU. Then, the CPU can immediately start executing the corresponding interrupt-service routine. The term vectored interrupts refers to all interrupthandling schemes base on this approach.

12. Name any three of the standard I/O interface.

*SCSI (small computer system interface),bus standards
*Back plane bus standards
*IEEE 796 bus (multibus signals)
*NUBUS
*IEEE 488 bus standard

13. What is an I/O channel?

An i/o channel is actually a special purpose processor, also called peripheral processor.
The main processor initiates a transfer by passing the required information in the input output channel. the channel then takes over and controls the actual transfer of data.

14.What is a bus?

A collection of wires that connects several devices is called a bus.

15.Define word length?

Each group of n bits is referred to as a word of information and n is called the word length.

16. Why program controlled I/O is unsuitable for high-speed data transfer?

In program controlled i/o considerable overhead is incurred.. because several program instruction have to be executed for each data word transferred between the external devices and MM.Many high speed peripheral; devices have a synchronous modes of operation.that is data transfer are controlled by a clock of fixed frequency, independent of the cpu.

17.what is the function of i/o interface?

The function is to coordinate the transfer of data between the cpu and external devices.

18.what is NUBUS?

A NUBUS is a processor independent, synchronous bus standard intended for use in 32 bit micro processor system. It defines a backplane into which upto 16 devices may be plugged each in the form of circuit board of standard dimensions

19. Name some of the IO devices.

*Video terminals
*Video displays
*Alphanumeric displays
*Graphics displays
* Flat panel displays
*Printers
*Plotters

20. What are the steps taken when an interrupt occurs?

*Source of the interrupt
*The memory address of the required ISP
* The program counter & cpu information saved in subroutine
*Transfer control back to the interrupted program

21.Define interface.

The word interface refers to the boundary between two circuits or devices

22.What is programmed I/O?

Data transfer to and from peripherals may be handled using this mode. Programmed I/O operations are the result of I/O instructions written in the computer program.

23.Types of buses.

-Synchronous bus
-Asynchronous bus

24.Define Synchronous bus.

- Synchronous bus on other hand contains synchronous clock that is used to validate each and every signal.
- Synchronous buses are affected noise only when clock signal occurs.
- Synchronous bus designers must control with meta stability when attempting different clock signal Frequencies
- Synchronous bus of meta stability arises in any flip flop. when time will be violated.

25. Define Asynchronous bus.

- Asynchronous buses can mistake noise pulses at any time for valid handshake signal.
- Asynchronous bus designer must deal with events that like synchronously.
- It must contend with meta stability when events that drive bus transaction.

-When flip flop experiences effects can occur in downstream circurity unless proper design technique which are used

POSSIBLE BIG QUESTIONS

1.List the different types of interrupts. Explain briefly about mask able interrupt.

2.What is DMA? Explain the block diagram of DMA .Also describe how DMA is used to transfer data from peripherals.

3.Explain the features of USB,PCI,SCSI bus.

AKENTEN APPIAH-MENKA UNIVERSITY
of Skills Training and Entrepreneural Development

Vote

#1

ABIGAIL KOBINA

INFOTESS WOMEN'S COMMISSIONER (WOCOM)

Hopeful 2022

WOMEN EMPOWERMENT
A Skill, an Essential
Tool for Financial Independence