Results of radiation tests of the ELMB (ATmega128L) at the CERN TCC2 area

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Abstract: Three ELMB boards were tested during summer 2002 at the CERN TCC2 facility. The ELMBs were part of the first prototype series production of 300 pieces. Two of the ELMBs were modified using the new processor ATmega128L with 0.35 μm technology. Results of both TID and SEE tests show the improved performance of the new technology. A fully automatic recovery method in order to cope with SEU was also tested successfully.

1 Introduction

Preliminary tests [1] at the CERN GIF facility have shown enhanced TID performance of the new version of the ELMB equipped with the processor ATmega128L, in 0.35 μm technology, compared with the older version, in 0.5 μm technology. The purpose of the present test was to confirm this result but also to determine the SEE sensitivity of the new technology. Previous tests with 60 MeV protons at Louvain-la-Neuve [2] and TCC2 in 2001 have shown that manual resets and restarts are necessary to keep the ELMB continuously working in presence of SEUs. In the final DCS system of ATLAS this is not acceptable. Therefore an automatic SEE monitoring system consisting of a CAN branch power monitoring box and software using a PVSSII script was developed and has been tested in TCC2.

1.1 TCC2 radiation

The ATLAS DCS group has made several radiation tests using the TCC2 experimental area with the help and support of the LHC Radiation Working Group [3]. During 2002, three ELMBs were tested for a total period of 6 weeks. They were placed around 50 m downstream of the target T6 at the side of the beam line M6, as shown in Figure 1.

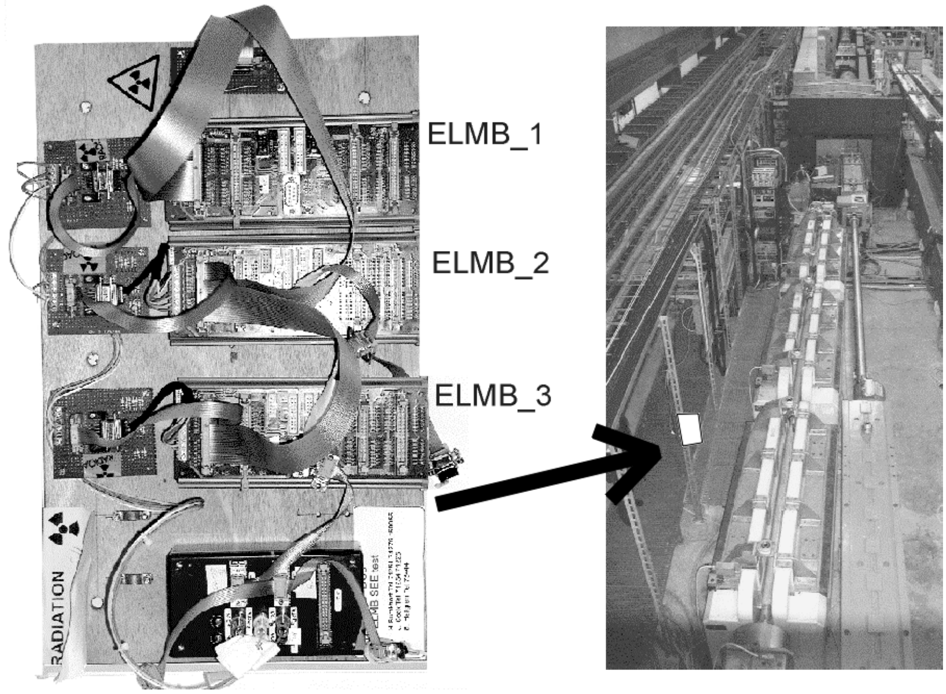

Figure 1: Three ELMBs mounted on a board and place of test at the TCC2 area

A radiation monitor PMITC10 has been installed, below the board on which the three ELMBs were mounted, which continuously measures the ionizing dose. In front of each ELMB a polymer-alanine dosimeter was placed. These were analyzed by the TIS-TE group and showed that the total dose at the place of test was 193 Gy for the first period of irradiation. After replacing some components, the ELMBs were returned for a second period of irradiation giving an additional 63 Gy. This amounts to a total of 256 Gy. Table 1 shows the total dose received by each ELMB and the time it ceased to function. Figure 2 shows that the daily dose was constant at about 5 Gy/day with the exception of the first days and the periods of SPS machine development.

Table 1: Received TID of each ELMB during different periods of test

	Date	TID (Gy)
Start of 1st period	23/05/2002 09:00	0
ELMB_1 stopped	01/07/2002 02:27	178
ELMB_2 stopped	30/06/2002 02:36	171
ELMB_3 stopped	23/06/2002 09:00	139
End of 1st period	03/07/2002 14:00	193
Start of 2nd period	18/07/2002 17:30	193
ELMB_1 stopped	19/08/2002 07:10	202
ELMB_2 stopped	22/07/2002 22:03	240
ELMB_3 stopped	23/07/2002 00:54	242
End of 2nd period	24/07/2002 14:00	256

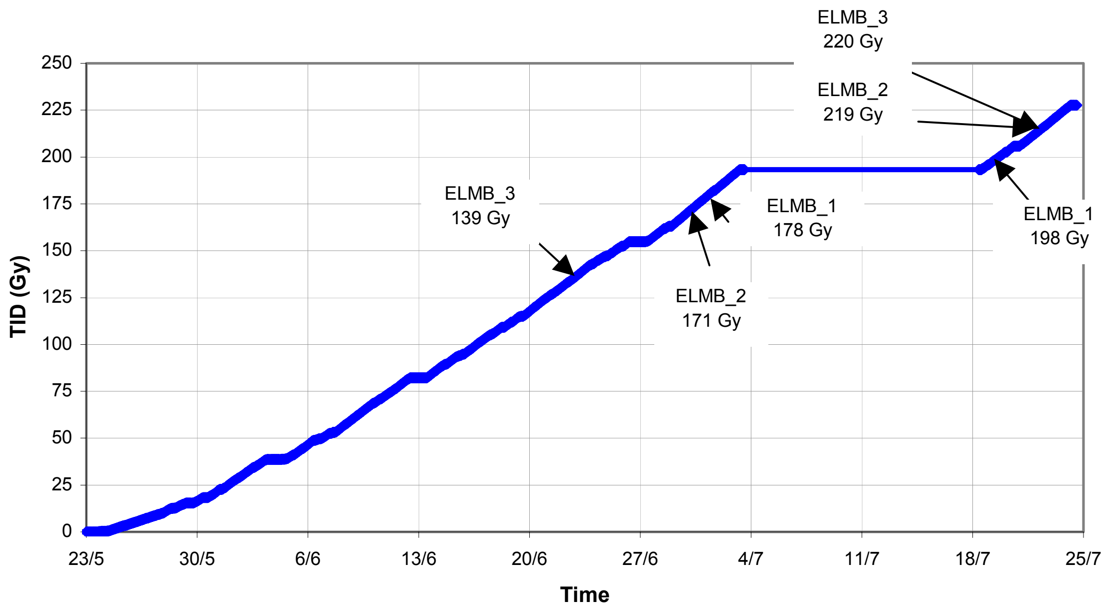

Figure 2: Daily variations of the radiation dose and the dose when each ELMB stopped working

2 ELMB test setup

The three ELMBs, named ELMB_1, ELMB_2 (both using ATmega128L processors) and ELMB_3 (using the ATmega103L processor), were each placed in a standard ELMB motherboard. The embedded software used in the ELMB was v3.6, which is a version with SEE tolerance. In addition there are special procedures incorporated in the program to identify SEE effects [4].

The three ELMBs were powered via a 180 m long CAN bus to the control room. In the control room a PC with PVSSII and the branch Power Monitor Box (PMB) [4] were installed. The aim of the PMB was to monitor the power consumption at a CAN branch. Slowly increasing currents are a sign of radiation damage while a SEE latch-up would cause a sudden increase in current. In this case power cycling is needed in order to restore normal operation. The PMB consists of a regulated power supply, an ELMB for monitoring of voltages and currents, power switching circuits and a number of connectors for the CAN branch and computer interfaces. In each ELMB placed in the radiation area, six analog inputs were used to measure the currents of the CAN, Analog and Digital power supply, the digital power supply voltage VDP, a short circuit and a reference voltage. Figure 3 shows the current measured for the digital part of the three ELMBs and the analog and CAN parts. There are large peaks in the digital current plot that coincide with a failure of an ELMB as detailed in Table 2 to Table 4, which are described in section 3. A possible explanation for these events is latch-up, where one was seen for each ELMB.

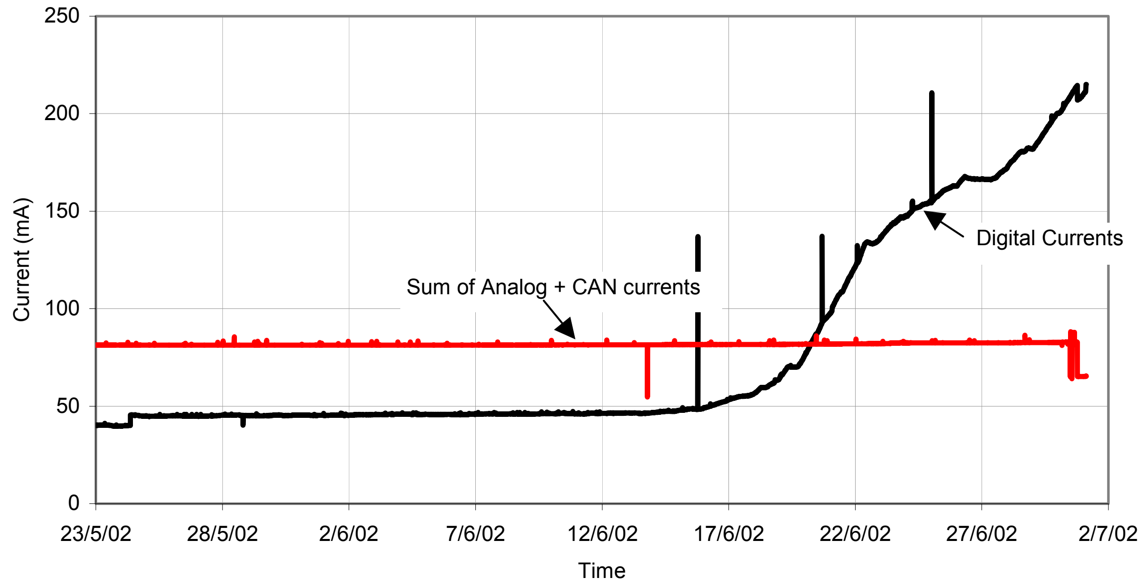

Figure 3: Measured current during the first part of the irradiation

2.1 Test software and automatic monitoring

A PVSS script was used to monitor each ELMB. It attempted to re-start an ELMB that had stopped responding for any reason. The basic process was to attempt up to three soft resets, and if this did not correct the problem, then a bus hard reset was attempted. The soft reset is a CANopen message involving only the specific node with a problem, while the hard reset involved switching off and on the power supply on the whole CAN branch.

In order to be able to analyze SEE, all messages on the CAN bus should be recorded. The most relevant data for each ELMB was stored each 10 minutes on the network, as well as using the PVSS archive.

3 Analysis and results of ELMB functional test

3.1 1st Period of test

A description of each of the soft and hard resets performed for each ELMB is given in Table 2 to Table 4. Any emergency messages or other information known about the cause of the reset is given. Only the effective control message, which cured the problem, is shown.

Table 2: Detailed description for each hard and soft reset for ELMB_1

Date/Time	*Brief Description*	*Details*
09.06.2002 11:23	Node Guard Failure	Single soft reset required. Emergency message seen at 11:21, indicating slave processor not responding
15.06.2002 18:39	Node Guard Failure (Possible latch-up)	1 hard reset required
28.06.2002 00:37	Node Guard Failure	1 hard reset required
28.06.2002 18:50	Node Guard Failure	Single soft reset required
01.07.2002 02:27	Node Guard Failure	Single soft reset required
01.07.2002 02:28	**No more response**	**ELMB_1 no longer functioning**

Table 3: Detailed description for each hard and soft reset for ELMB_2

Date/Time	*Brief Description*	*Details*
22.06.2002 01:58	Node Guard Failure	1 hard reset required
25.06.2002 00:39	Node Guard Failure (Possible latch-up)	1 hard reset required
28.06.2002 06:50	Node Guard Failure	Single soft reset required
30.06.2002 2:36	**No more response**	**ELMB_2 no longer functioning**

Table 4: Detailed description for each hard and soft reset for ELMB_3

Date/Time	*Brief Description*	*Details*
28.05.2002 19:33	Node Guard Failure	1 hard reset required
31.05.2002 23:51	Node Guard Failure	1 hard reset required
03.06.2002 06:15	Node Guard Failure	Single soft reset required
05.06.2002 05:07	Node Guard Failure	1 hard reset required
05.06.2002 08:21	Node Guard Failure	Single soft reset required. Communication error at 08:18 and Node Guard Failure at 08:20
11.06.2002 17:09	Node Guard Failure	Single soft reset required
20.06.2002 16:35	Node Guard Failure (Possible latch-up)	1 hard reset required
23.06.2002 09:00	**No more response**	**ELMB_3 no longer functioning**

3.2 Discussion of the results

The automatic monitoring system worked reliably. The ELMBs were giving data the full time, with only small gaps when resets were being performed. Earlier SEE tests of the ELMB required numerous manual interventions. The 0.35 μm technology gives about 3-4 times fewer errors than the older one, as seen in Table 5 and Table 6.

Table 5: Result for ELMB_1 and ELMB_2 together (ATmega128L 0.35 µm)

Recovery	Number of SEEs detected	Average fluence per error
Hard resets	4 for $5.9*10^{11}$ particles/cm^2	$1.5*10^{11}$ particles/cm^2
Soft resets	4 for $5.9*10^{11}$ particles/cm^2	$1.5*10^{11}$ particles/cm^2

Table 6: Result for ELMB_3 (ATmega103L 0.5 µm)

Recovery	Number of SEEs detected	Average fluence per error
Hard resets	4 for $2.2*10^{11}$ particles/cm^2	$5.5*10^{10}$ particles/cm^2
Soft resets	3 for $2.2*10^{11}$ particles/cm^2	$7.3*10^{10}$ particles/cm^2

3.3 2nd Period of test

The causes for the failures of each ELMB after the first test period were the three complex CMOS devices: the main processor, the slave processor and the CAN controller. The main processor and the CAN processor were replaced on each ELMB. The processor used was the ATmega128L for all ELMBs and no slave processor was mounted during this test.

ELMB_1, ELMB_2 and ELMB_3 stopped working after an additional 9, 47 and 49 Gy respectively due to failure of the 3.3V voltage regulators. The estimated number of particles received by the three ELMBs together was $9.2*10^{10}$ particles/cm^2. No functional miss-behavior was detected, which is compatible with the results from the first test period as shown in Table 6.

3.4 Discussions of Automatic Monitoring

Some monitoring actions should not be used such as monitoring for a SYNC response. This specific monitoring procedure is explained as follows. After every SYNC message, the ELMB should respond by sending data for all ADC channels that are being measured. Due to the OPC standard, only data that has changed will be sent to the OPC Client (in this case PVSS) through the OPC Server. Changes in values for the ADC counts are expected due to some noise. A "SYNC response warning" was defined as "when none of the relevant channels were updated after three successive SYNC messages had been issued from the server". Due to node guarding and emergency messages, it has been decided that this is not a valid parameter to measure whether an ELMB is functioning correctly or not. The soft and hard resets caused by a SYNC response warning have therefore not been taken as an ELMB error, unless another error was displayed.

4 Results of systematic study of SEUs in memories and registers

Systematic investigations were made of SEU in memories and registers using the same methods as described earlier [4]. Three types of memory, the master processor made with the two technologies (0.5 µm and 0.35 µm), as well as the static registers of the CAN controller and the ADC, were studied.

4.1 SRAM test of microcontroller

The tests were made on 2 Kbytes of the ELMB microcontroller's integrated SRAM. Figure 4 displays the total number of SEE detected during the irradiation for the three ELMBs. The daily variations are probably due to different beam operation. At the moment ELMB_3 stopped working it had registered 1593 SEE while, at the same moment, each of the other ELMBs had reached 337 SEU. The two ELMBs containing the ATmega128L are thus about a factor 4.7 less sensitive than the older technology ATmega103L.

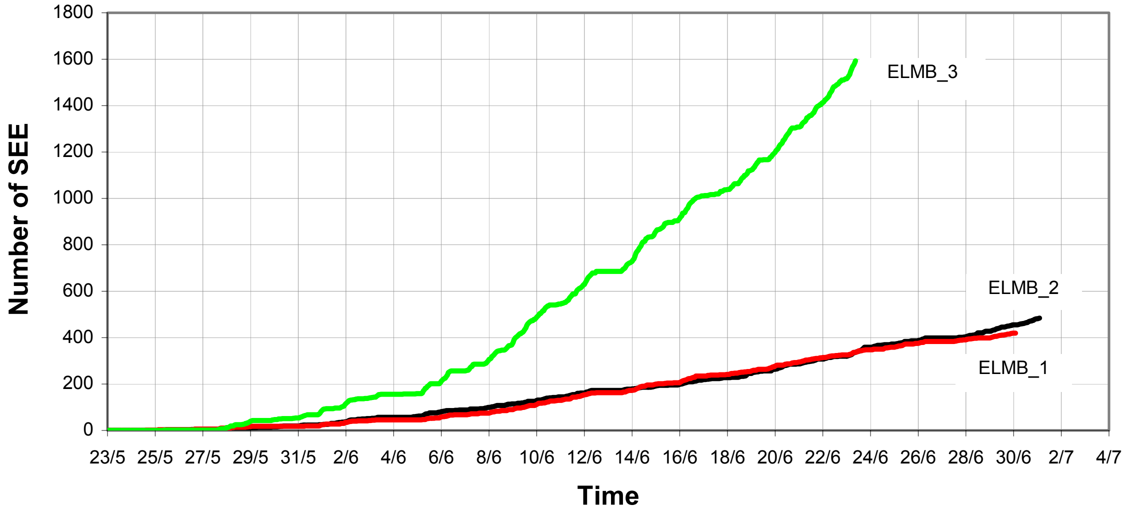

Figure 4: The accumulated number of SEEs in 2048 bytes detected in the SRAM of the ATmega128L (ELMB_1 and ELMB_2) and the ATmega103L (ELMB_3)

In order to estimate the number of high-energy particles in the TCC2 area, the known sensitivity of the 0.5 µm technology to SEE is used, as measured for 60 MeV protons at Louvain-la-Neuve [2]. The measurements showed that the common cross-section for all of the 11 ELMBs was $3.4*10^{-12}$ SEEs per byte and protons/cm^2. Since the SEU cross-section for high-energy hadrons is roughly energy-independent above 30 MeV [6], this value can be used to estimate the number of hadrons above this energy, as shown in Table 7.

Table 7: The number of SEU measured per ELMB and the corresponding estimated number of hadrons with energies > 30 MeV

Device	Number of SEU	Estimated hadrons > 30 MeV
ELMB_1 (ATmega128L)	508	$3.2*10^{11}$ hadrons/cm^2
ELMB_2 (ATmega128L)	420	$2.7*10^{11}$ hadrons/cm^2
ELMB_3 (ATmega103L)	1593	$2.2*10^{11}$ hadrons/cm^2

A detailed analysis of the data for ELMB_1 from the PVSSII database was done. The SEEs comprised 508 bit flips as shown in Figure 5. The number of changes from logic 0 to 1 was the same as the number of opposite changes within the statistical error.

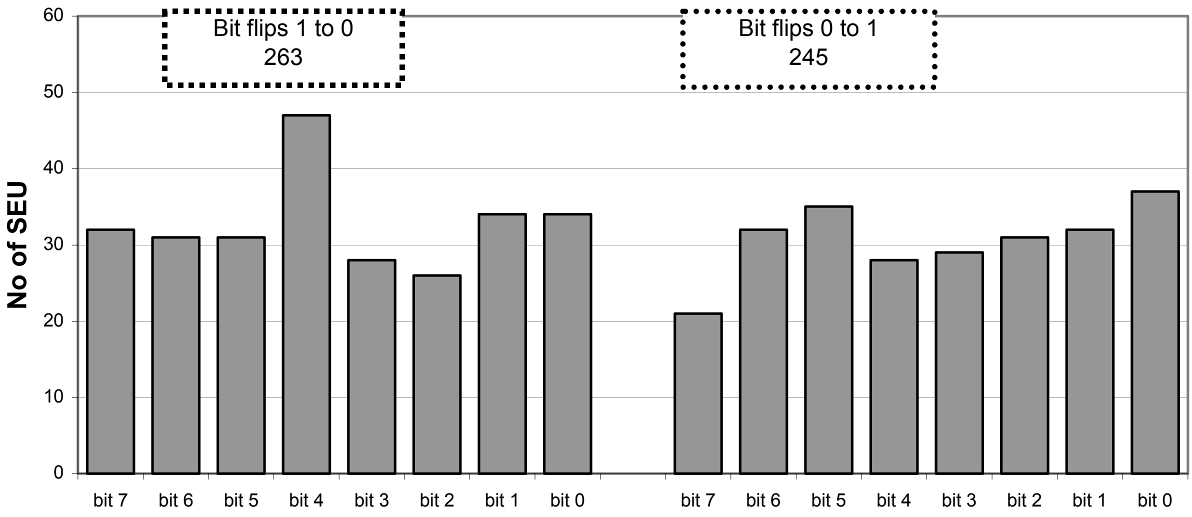

Figure 5: Number of changes from 1 to 0 and from 0 to 1 in the 8 bits of the SRAM bytes for ELMB_1

The SRAM test involved addresses 1024 to 3071. Figure 6 indicates the SRAM address versus time for each SEE. The SEEs were distributed randomly over the different addresses. The distribution of SEE per address is shown in Figure 7. The behavior is the same as previous tests for protons at Louvain-la-Neuve.

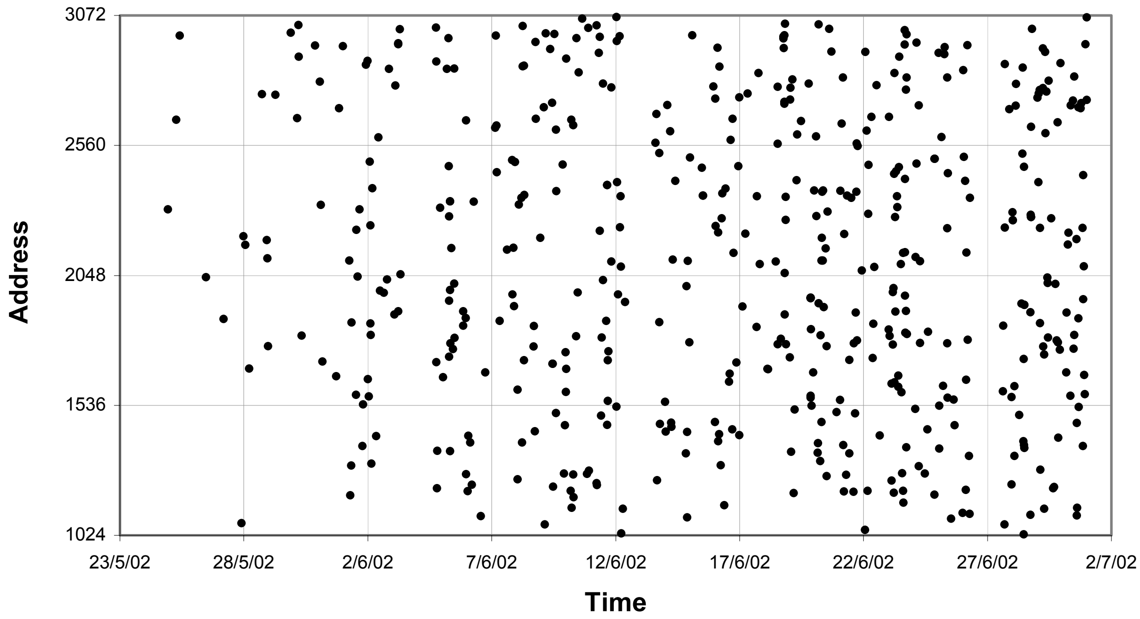

Figure 6: Addresses of the SRAM where the SEEs were located for ELMB_1 during the test

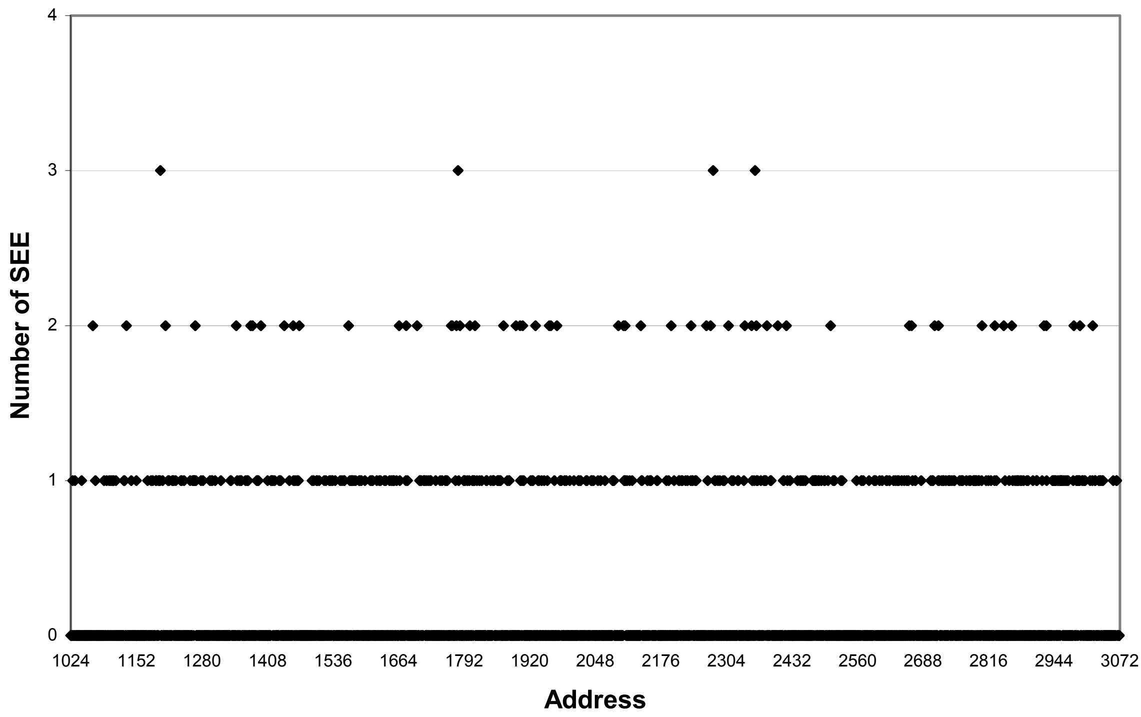

Figure 7: Number of SEEs detected for ELMB_1 per address in SRAM

4.2 EEPROM test of microcontroller

The tests were made on 3.5 Kbytes of the ELMB microcontroller's integrated EEPROM. No SEE was detected. However, the EEPROM showed readout errors at a TID > 130 Gy for ELMB_1 and ELMB_2 and this is discussed in the section 5. If one SEU error had occurred, the cross-section would have been $3*10^{-16}$ SEEs per byte and hadron/cm^2.

4.3 Flash memory

The tests were made on 64 Kbytes of FLASH memory. No SEE was detected. However, ELMB_2 showed readout errors at a TID greater than 180 Gy. This is discussed in section 5. One error in the memory would correspond to a cross-section of $2*10^{-17}$ SEEs per byte and hadrons/cm^2.

4.4 CAN controller register test

The tests were made on 40 bytes of the registers of the CAN chip SAE81C91. The evolution of the SEE is shown in Figure 8. The total number of SEEs for the three ELMBs amounted to 65, which corresponds to a cross-section of $7.6*10^{-13}$ per byte and hadron/cm^2.

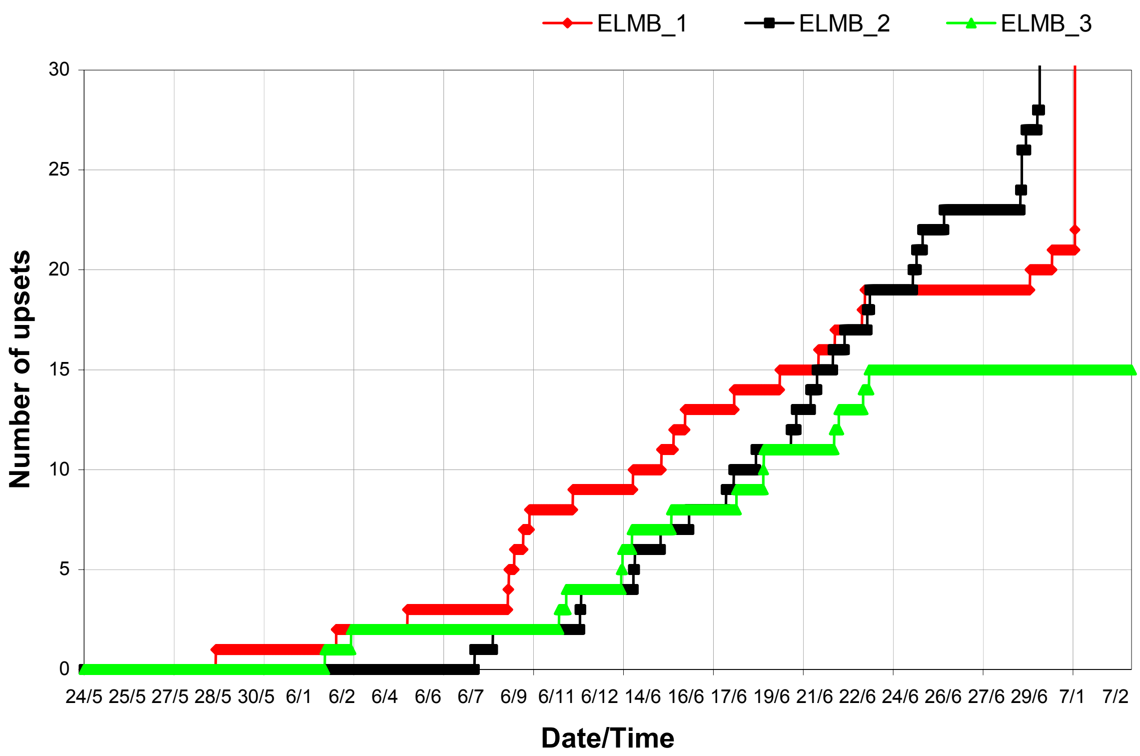

Figure 8: The accumulative number of SEE for the registers in the CAN controller for all ELMBs tested

4.5 ADC register test

The tests were made on 33 bytes of the registers of the ADC chip CS5523. The number of reported errors during the first test period is shown in Figure 9. The total number of errors for the three ELMBs was 327. However, as seen from Figure 9 there were many multiple errors, which could be caused by an error in the control or readout circuit and should be counted as one error. The number of errors counted in this way is then 54. This corresponds to a cross-section of $1.9*10^{-12}$ SEEs per byte and hadron/cm^2.

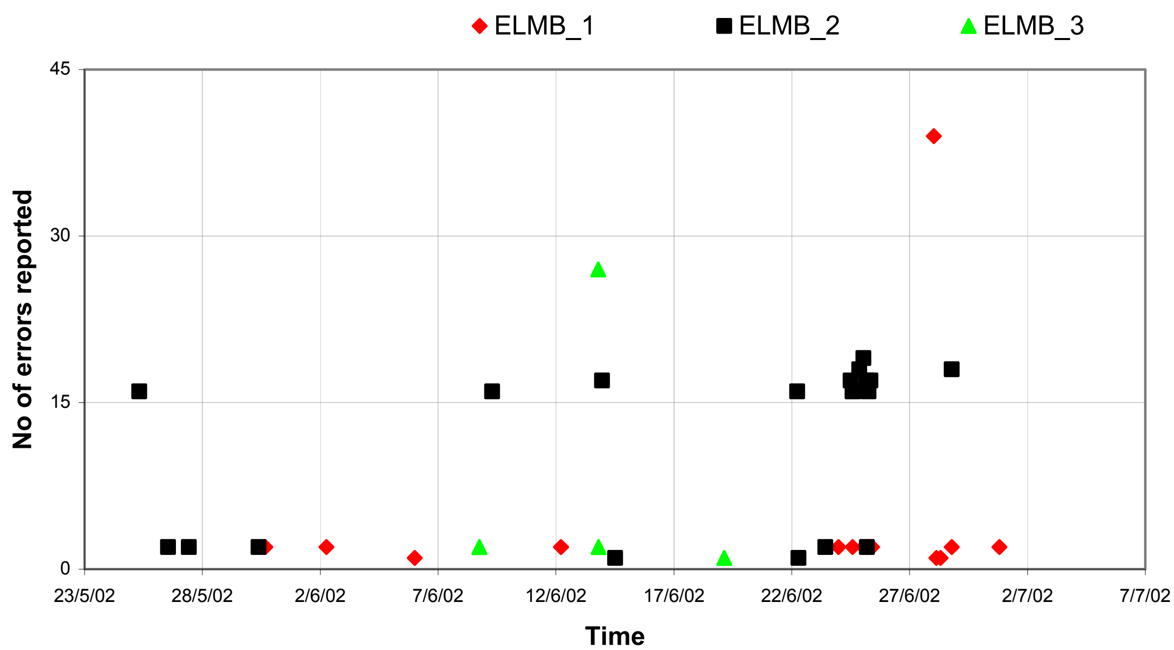

Figure 9: The number of ADC errors reported versus time for the three ELMBs

4.6 Summary of the SEUs in memories and registers

The results of the study of SEUs in memories and registers are summarized in Table 8.

Table 8: Results of the systematic SEU study

Device under test	Number of bits tested	Number of errors	Estimated fluency hadrons/cm^2 (1)	Cross-section cm^2/bit
SRAM 0.5 µm	16384	1593	$2.2*10^{11}$	$4.4*10^{-13}$
SRAM 0.35 µm	16384 x 2	904	$5.9*10^{11}$	$9.4*10^{-14}$
EEPROM	28762	<1	$8.1*10^{11}$	$< 4.3*10^{-17}$
FLASH	524288	<1	$8.1*10^{11}$	$< 2.4*10^{-18}$
CAN register	320	65	$8.1*10^{11}$	$1.0*10^{-13}$
ADC register	264	54	$8.1*10^{11}$	$2.5*10^{-13}$

(1) The fluency is estimated from the known cross-section of the SRAM 0.5 µm as measured with 60 MeV protons.

The results show that 0.35 µm technology has considerably better SEE behaviour. The results for CAN and ADC are similar to previous measurements [2].

5 *TID effects*

Numerous errors in the EEPROM of ELMB_1 were detected starting at a TID of about 140 Gy. Also in ELMB_2 errors were detected in the EEPROM and flash memory. Figure 10 shows the evolution of these errors versus the TID.

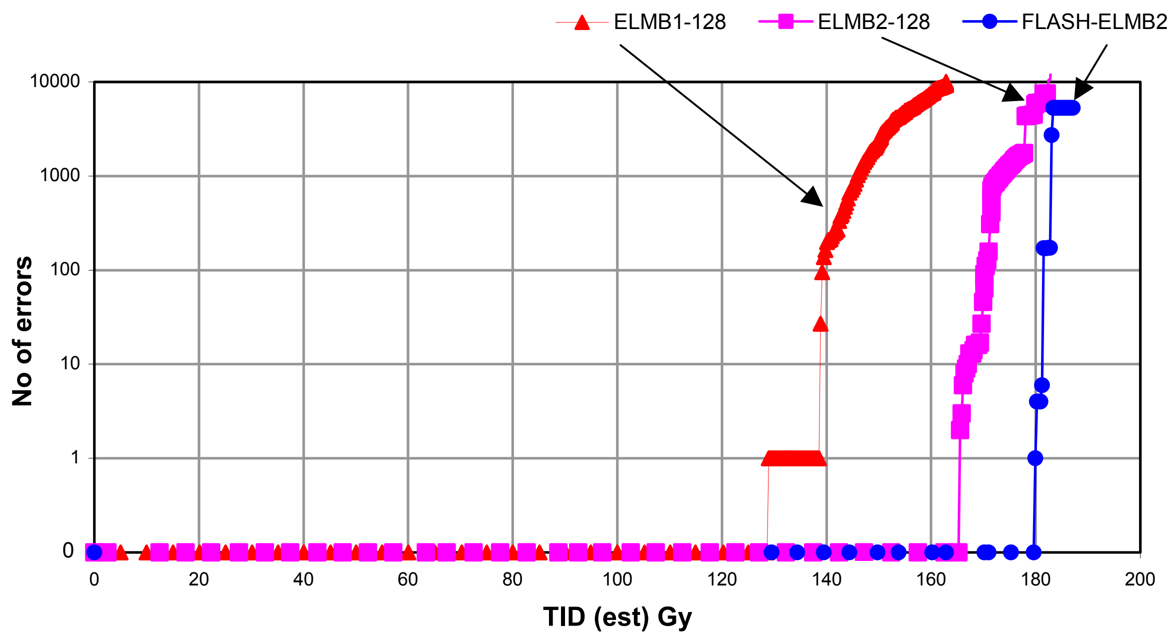

Figure 10: EEPROM and FLASH memory errors in ELMB_1 and ELMB_2

An analysis of the EEPROM errors of ELMB_1 showed that the error always occurred in bit 2 of the read byte. This bit was read out as logic one instead of logic zero for 24 addresses of the EEPROM (see Figure 11). These errors were detected even when there was no beam (27/6) and therefore, the conclusion is that these were not caused by SEE, but by functional errors in the readout circuit caused by TID.

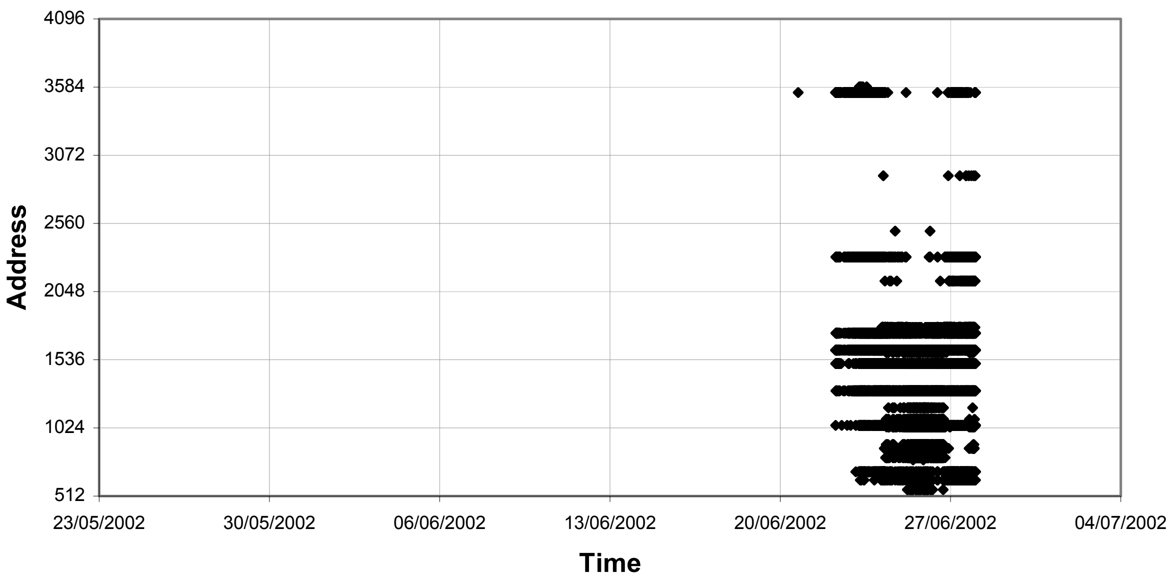

Figure 11: Errors occurring in the EEPROM of ELMB_1

5.1 Power supply current

The digital, analog and CAN power supply currents were continuously measured during the irradiation. Only the digital currents, shown in Figure 12, showed sizeable changes.

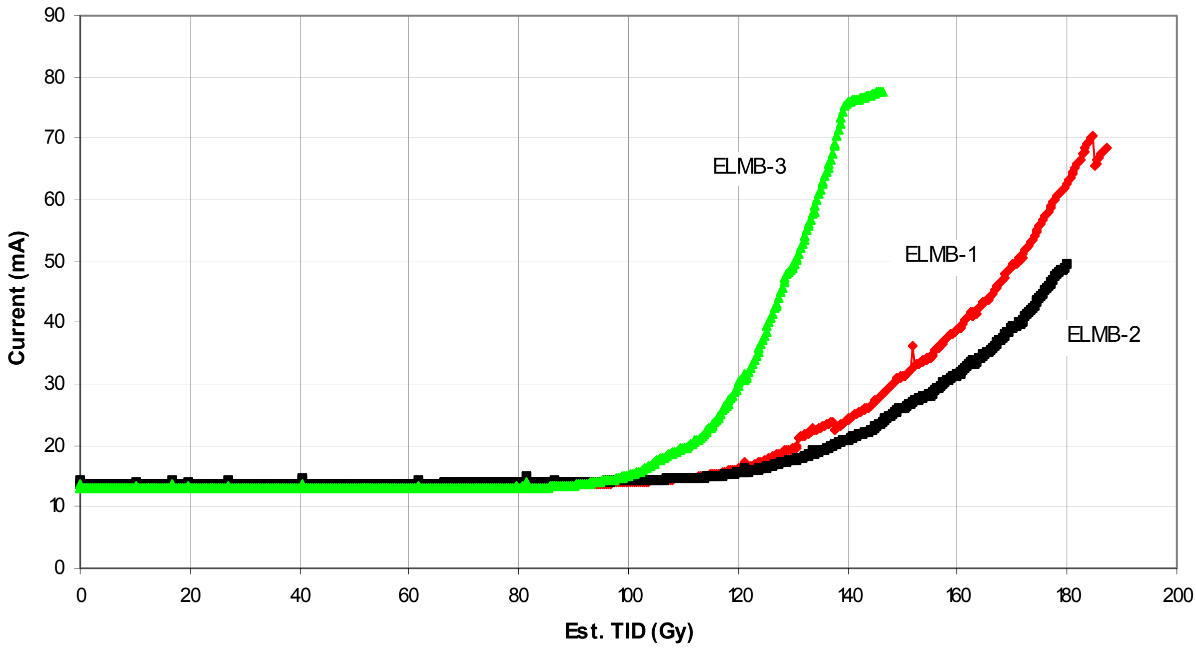

Figure 12: Digital current evolution for the different ELMBs for the 1st period of irradiation

ELMB_3, with 0.5 µm technology, reached the current limit of the power supply regulator, 75 mA, at a TID of 140 Gy. ELMB_1 stopped working at 179 Gy while ELMB_2 stopped at 170 Gy. The reason for the current increase was found to be the CMOS devices AT90S2313 (Slave processor) and SAE81C91 (CAN controller), which use 0.5 µm technology. The analog and CAN currents are essentially constant as shown in Figure 13 and Figure 14.

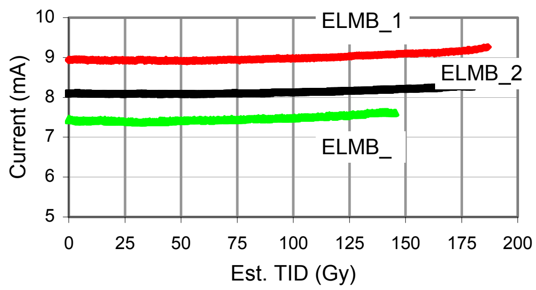

Figure 13: Analog currents

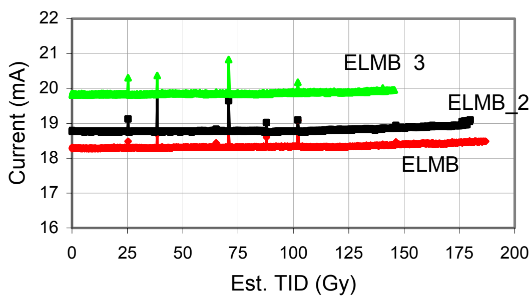

Figure 14: CAN currents

5.2 DC voltages

Table 9 shows the variations of the DC voltages of the ELMB due to radiation at TCC2. The voltage reference ADC680JR changes by 2 mV, while the 5V power supply regulators are just outside their specification of 3%. All of the ELMBs stopped working in the second period due to failure of the 3.3 V regulator.

Table 9: DC voltages of voltage regulator and voltage reference circuit

TID (Gy)	MIC5203-5V (V)	MIC5203-3.3V (V)	ADC680JR (V)
0	4.955	3.302	2.490
198	5.124	2.970	2.491
226	5.173	1.731	2.492

6 Conclusions

The ELMBs equipped with the microcontroller ATmega128L in 0.35 μm technology show a considerable improvement in radiation tolerance – a factor 3 for functional errors and almost a factor 5 for memory upsets. The TID level reached was 170 Gy. An automatic monitoring system has been shown to keep a CAN bus system working without interruption while receiving $8*10^{11}$ particles/cm^2 (>20 MeV).

7 References

[1] J.Cook and B.Hallgren, "TID radiation test at GIF of the ELMB with the ATmega128L processor", CERN ATLAS Internal Working Note DCS- IWN15, 19 April 2002.

[2] H. Boterenbrood, H.J. Burckhart, B. Hallgren, H. Kvedalen and N. Roussel, 'Single Event Effect Test of the Embedded Local Monitor Board, CERN ATLAS Internal Working Note DCS-IWN12, 452 kbytes, 20 September 2001 http://atlasinfo.cern.ch/ATLAS/GROUPS/DAQTRIG/DCS/ELMB/elmbsee1.pdf

[3] See detailed description: http://lhc-radwg.web.cern.ch/LHC-radwg/

[4] B.Hallgren, User manual, CAN BRANCH Power Monitoring Box ver 0.2, 26-Feb 2002

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[6] M.Huhtinen and F. Faccio, "Computational method to estimate Single Event Upset in accelerator environment", Nucl, Inst. and Meth., A450, p.155, August 2000.