Single Event Effect Test of the Embedded Local Monitor Board

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Abstract: Embedded Local Monitor Boards (ELMB) were exposed to proton radiation up to an overall fluence of $3.3*10^{11}$ protons/cm^2. The total number of soft SEEs detected amounted to 29, equally distributed among the different functional parts of the board. No destructive or permanent error occurred. The SRAM, EEPROM, flash memories of the master processor and the static registers were subject to a systematic study of the SEE cross-section.

1.0 Introduction

The proton irradiation of the ELMBs [1] was performed on 27 June 2001 at the CYClotron of LOuvain-la-NEuve (CYCLONE) of the Université Catholique de Louvain, in Belgium [2]. The main purpose was to study Single Event Effects (SEE) but some Total Ionising Dose (TID) measurements were also made. The ATLAS standard test method for SEE tests [3] was followed. In order to compare the results of the test with the requirements, a minimum integrated fluence of $3*10^{11}$ protons/cm^2 had to be reached. An upper limit to the fluence per ELMB was imposed by previous TID tests [4] [5] [6], which had shown that the performance of the device deteriorates from 35 Gy (Si) onwards. Therefore it was necessary to irradiate at least 10 ELMBs, each to a total of $3*10^{10}$ protons/cm^2. According to some calibrations of the 60 MeV proton beam of CYCLONE, this fluence corresponds to a TID of 39 Gy (Si). For that reason, the test involved 11 ELMBs of a series production comprising 300 units. Thus the integrated fluence added up to $3.3*10^{11}$ protons/cm^2. Concerning the flux, its value was chosen such that SEEs would not occur too often and therefore could all be recorded by the data acquisition system. For the first 5 ELMBs, it was set to $2.5*10^7$ protons*cm^{-2}*s^{-1}, which resulted in a test time of about 1000 seconds per ELMB. Then it was increased by a factor of two in order to decrease the total duration of the test.
Two categories of Single Event Effects were investigated: Single Event Upsets (SEU) and Single Event Latch-ups (SEL). A SEU is a change in a logic state while in the case of a SEL, the device is latched into a state where it consumes excessive current.

2.0 Experimental setup and test method

2.1 Test setup

11 ELMBs with the series numbers 61 to 72 (68 not included) were tested successively. The setup is shown in Figure 1. The ELMBs, plugged onto a motherboard, were exposed to a 60 MeV proton beam. Each of them absorbed a TID of 39 Gy (Si) and received $3*10^{10}$ protons/cm^2 - except ELMB 63, for which the TID was 44.5 Gy and the fluence $3.42*10^{10}$ protons/cm^2. Constant DC voltages were applied to 16 analog ADC inputs. They were derived from the ADC reference voltage through a resistor network. A CAN bus cable connected the ELMB to a computer. The CANalyzer from Vector Informatik [9] was used to record all CAN messages transmitted during the irradiation. Each of them was stored with time stamp (resolution 0.1 ms), CAN identifier and all data bytes in hex format. For each ELMB under test, a text file was generated. It contains the CAN messages that relate to the corresponding ELMB. A Pt100 temperature sensor was placed close to the ELMB. A LMB [7] (predecessor of the ELMB),

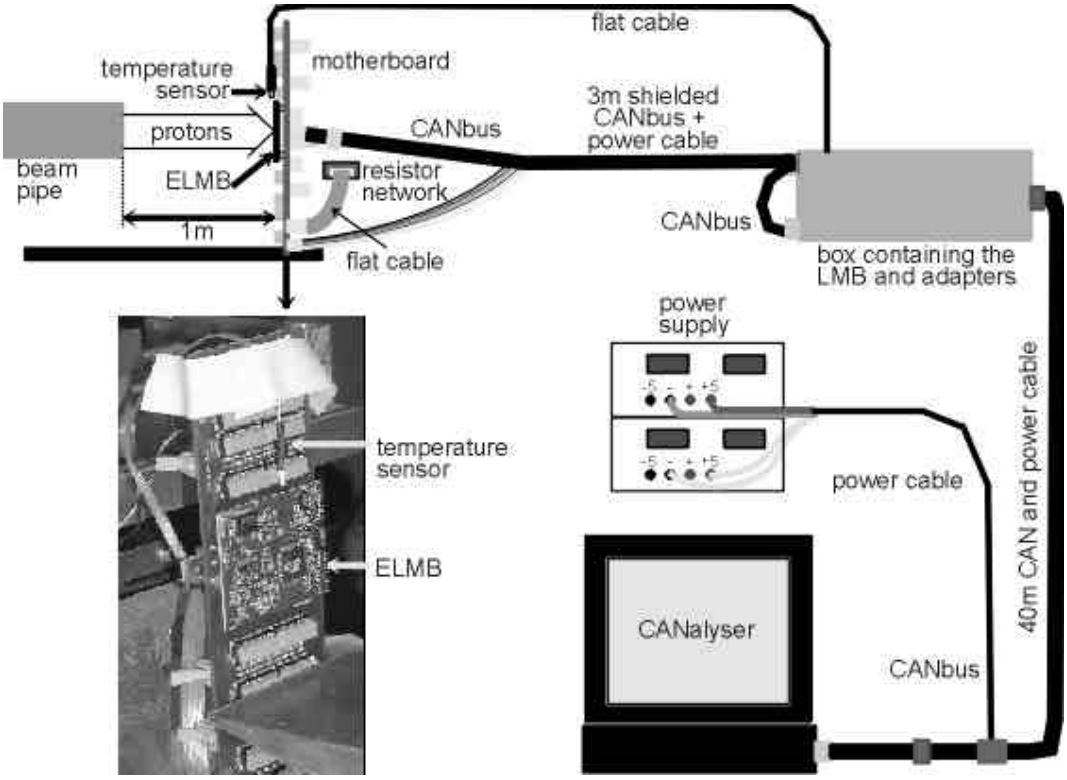

Figure 1: Experimental setup for the proton irradiation of the ELMB

equipped with some adapters, was also linked to the CAN bus in order to measure the temperature as well as the three power supply currents of the ELMB. Both the ELMB and the LMB were powered via the CAN bus cable.

2.2 Detection of Single Event Latch-ups

The ELMB has three independent power supplies (see Figure 2). The supply voltage is 5 V for

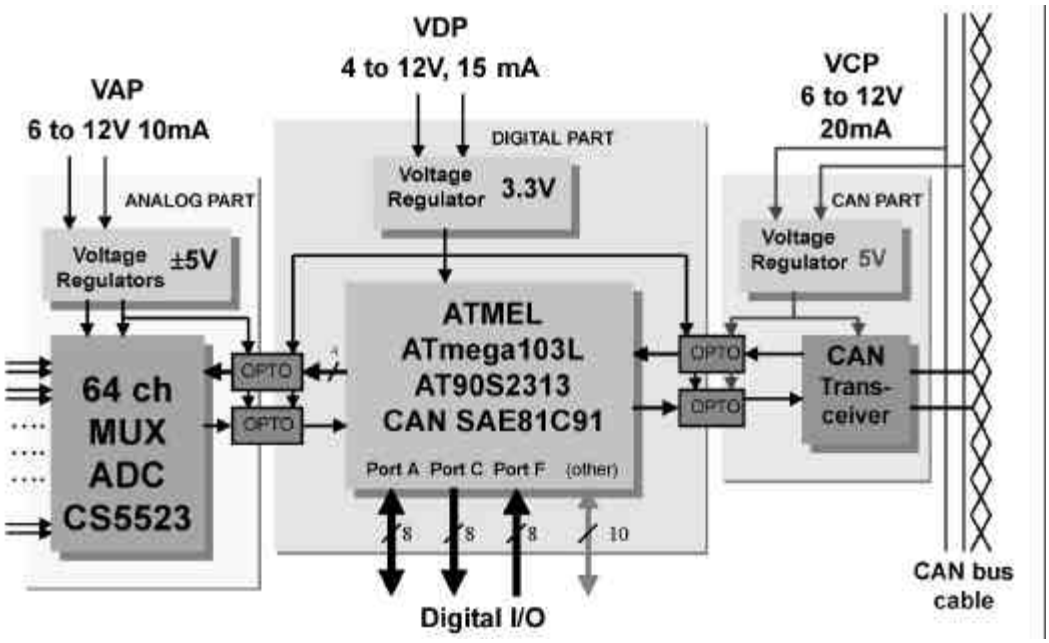

Figure 2: Block diagram of the ELMB showing the different power supplies.

the CS5523 ADC and 3.3 V for the ATmega103L Microcontroller as well as the SAE81C91 CAN controller. These 3 components are CMOS technology devices, which were expected to be susceptible to Single Event Latch-ups. The CAN transceiver (bipolar) and part of a high-speed optocoupler are powered by 5 V.
SELs result in an increase of the current consumed by the ELMB in the affected part. As mentioned before the 3 power supply currents were measured on-line by a separated LMB module.

2.3 Detection of SEE in memories and registers

The 3 CMOS integrated circuits of the ELMB comprise memories and registers that are particularly vulnerable to SEEs. Most of them are in the ATmega103L, which includes 4 Kbytes of SRAM, 4 Kbytes of EEPROM, 128 Kbytes of flash memory and 96 bytes of registers. The two other components contain registers: the number of registers actually used by ELMB software amounts to 72 bytes in the SAE81C91 CAN controller and 40 bytes in the CS5523 ADC. SEEs in the memories and registers could cause several types of functional errors in the operation of the software in the ELMB but also errors in the ADC data and CANbus messages.

2.4 SEE in other devices

SEEs might also be induced with low probability in other components of the ELMB, like the CMOS D-F/F MC7474 used to control the analog multiplexer or the high-speed optocouplers HCPL-0601. A SEE in this latter device could produce a transient erroneous signal on the CANbus. It would be detected by the error checking features of other CAN controllers connected to the bus and therefore an error message would be sent.

2.5 Dedicated software for systematic SEE study

In order to detect SEEs in the memories and registers, dedicated software [8] was added to the normal application programs running on the master processor of the ELMB. It repeats the same series of tasks every 5 seconds. The cycle includes several tests that are performed successively.

1) ADC read-out of 4 channels, at 1 V input range and 61.6 Hz conversion time. Different constant DC voltages are applied to the inputs. The output result is erroneous when it differs from the values that can be expected considering the normal fluctuations due to noise.

2) SRAM test of 2 Kbytes. The procedure, which is similar for all the memory and register tests (tests 2 to 6), is the following. Initially, the tested addresses are filled with a fixed pattern (alternating 0 and 1). In each test cycle, their contents are read. For the first 8 changed bytes detected, a CAN message is sent. It includes the number of the test cycle, a number that identifies the type of test, the address where the error was detected, the erroneous value and the expected one. In the case of SRAM, CAN-controller registers and ADC registers, the errors are corrected to prevent them from being reported in the next test cycle.

3) EEPROM test of 3.5 Kbytes.

4) Flash memory test of 64 Kbytes. In addition, the whole memory (128 Kbytes) was checked after the SEE test.

5) CAN register test of 40 bytes.

6) ADC registers test of 33 bytes.

7) CRC check on flash program code.

At the end of the memory and register tests (tests 2 to 6), a CAN message is sent to indicate the total number of errors detected during that test. Figure 3 represents the screen of the computer, where all CAN messages were displayed on-line. It shows that the 7 program steps are carried out in about 3 seconds and the test loop period is 5 seconds. By watching the list of messages on the screen, it was possible to detect very quickly the errors that were not automatically corrected

```
           CAN MESSAGE

 Time    ID  N b0 b1 b2 b3 b4 b5 b6
-------------------------------------
309.1120 2BF 4 02 27 C1 14
309.1484 2BF 4 03 27 6B 13
309.1552 33F 7 F0 46 01 70 06 8A AA
309.1690 33F 7 F0 46 00 01 00 00 00
309.2386 33F 7 F1 46 00 00 00 00 00
310.4835 33F 7 F2 46 00 00 00 00 00
310.4893 33F 7 F3 46 00 00 00 00 00
310.5988 33F 7 F4 46 00 00 00 00 00
311.7213 33F 7 F5 46 00 00 00 00 00
314.0326 2BF 4 00 27 CB 14          <-------  Start of test cycle
314.0691 2BF 4 01 27 9C 13
314.1056 2BF 4 02 27 C1 14
314.1421 2BF 4 03 27 75 13
314.1460 33F 7 F0 47 01 2E 05 BF FF
314.1602 33F 7 F0 47 01 EB 0A 1A 5A
314.1636 33F 7 F0 47 00 02 00 00 00
314.2330 33F 7 F1 47 00 00 00 00 00
315.4780 33F 7 F2 47 00 00 00 00 00
315.4838 33F 7 F3 47 00 00 00 00 00
315.5934 33F 7 F4 47 00 00 00 00 00
316.7159 33F 7 F5 47 00 00 00 00 00 <--------  End of test cycle
319.0257 2BF 4 00 27 CF 14          <--------  New cycle
319.0621 2BF 4 01 27 9A 13
319.0987 2BF 4 02 27 CE 14
319.1351 2BF 4 03 27 72 13
319.1548 33F 7 F0 48 00 00 00 00 00
319.2242 33F 7 F1 48 00 00 00 00 00
320.4692 33F 7 F2 48 00 00 00 00 00
320.4750 33F 7 F3 48 00 00 00 00 00
320.5846 33F 7 F4 48 00 00 00 00 00
321.7071 33F 7 F5 48 00 00 00 00 00
324.0196 2BF 4 00 27 C2 14
```

and therefore required a manual intervention.

Figure 3: Screen dump of ELMB SEE test program for ELMB 70

The following additional tests were performed with a period of 5 seconds by the program running on the control computer (SCADA).

1) The program sends a message to the ELMB to ask for the content of a specific memory address. The ELMB provides it in a reply message.
2) The program sends a “SYNC” message. The ELMB answers by sending the content of its 8-bit digital input.
3) The program reads the value of a power supply current from the second CAN node, the LMB.

2.6 Determining of the radiation periods

The ELMB had to be reset to recover from the SEEs that were not automatically corrected. Two types of manual resets were used, depending on the error. In general, the first attempt was a software reset. If it was not successful, a hardware reset consisting in cycling the power was performed. Unlike the software reset, which is executed in one second, this operation takes several hundreds of seconds, during which the read-out is suspended. As the fluence to which each ELMB could be exposed was limited, the irradiation was interrupted during power cycling resets.
In the off-line analysis, the read-out of the 8-bit digital input was used to determine precisely the irradiation periods. In fact, during the test, the digital ports were left floating and the decimal value of the digital input, which was zero when the beam was off, switched to 255 when it was on. In other words, the 8 input bit values were all equal to 0 in the absence of protons and to 1 during the irradiation periods. Although this behaviour turned out to be very convenient in the analysis of the test, it would be better to avoid leaving the ports floating in future.

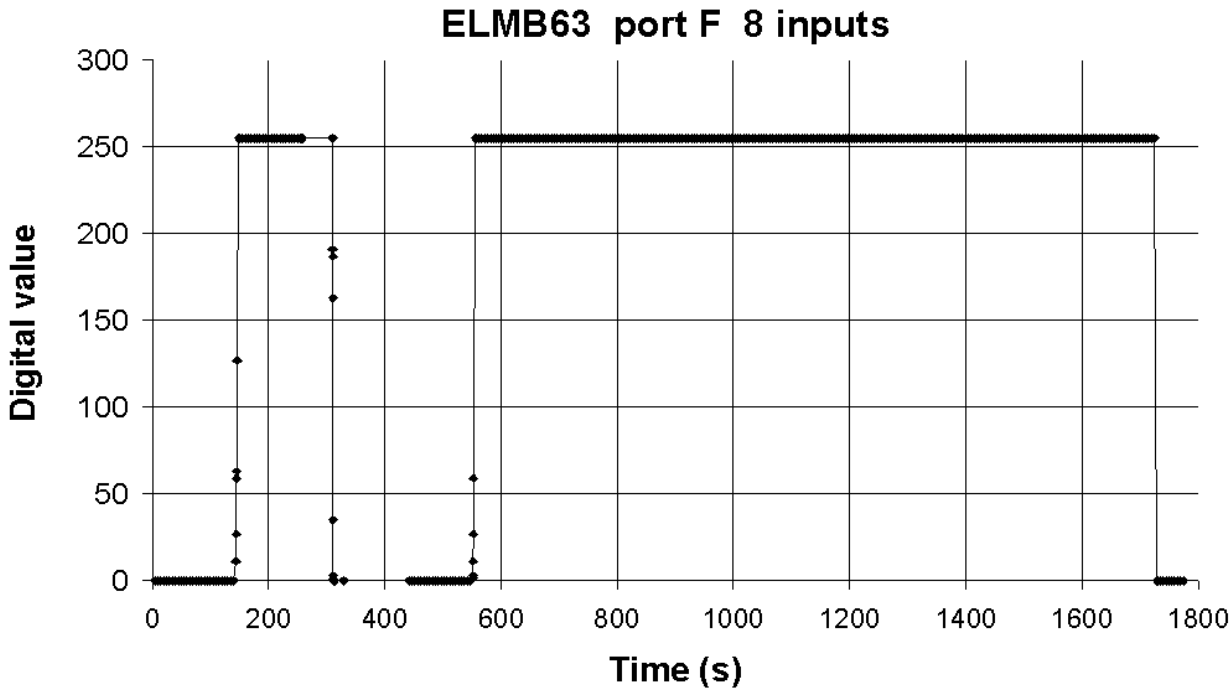

Figure 4: When ELMB 63 was tested, the beam was on { between t = 144 s and t = 311 s; between t = 555 s and t = 1729 s

3.0 Analysis and results of the functional SEE test

This chapter describes all functional SEEs, namely SEEs that disturbed the operation of the system. To list them, a total of 131157 items had to be examined. 3 analyses were carried out independently, using a different method each time in order to ensure the reliability of the results. 29 functional misbehaviours were detected, affecting the master controller, ADC and the CAN controller. They are divided in 3 categories, according to the way normal behaviour was restored.

A table summarises them in Appendix 1, where they are identified by means of indices. Those are mentioned in brackets in the present chapter.

3.1 SEEs that were cancelled by power cycling off-on reset

4 SEEs were cancelled by a manual power cycling reset to resume proper operation. All of them affected the master processor.

- The digital power supply increased abruptly to the limit fixed by the protection circuits. Simultaneously, the program running the tests in the ELMB stopped working. This SEE is believed to be a Single Event Latch-up. (61-1)
- The digital inputs of ELMB 63 were read every 1 millisecond. Such an overload of the CANbus would prevent the operation of all the other devices connected to it. (63-1)
- ELMB 71 stopped sending messages. (Before power cycling, a software reset was performed but it failed: the ELMB did not reply.) (71-1)
- The test loop period increased. The usual cure for that kind of SEE is a software reset (see paragraph 3.2) but by mistake it was not tried. Instead, it was directly resorted to power cycling to restore the period to 5 seconds. (65-1)

3.2 SEEs that required a software reset

5 SEEs required a manual software reset.

- In the master processor

Three times, a software reset had to be performed because the test loop period had increased. (61-2, 70-1, 72-1)

- In the CAN controller

Twice the data bytes were missing in one category of CAN messages sent by the EMLB:
- the replies to the requests received from the control computer in the first case (61-3)
- the messages providing the values of ADC inputs in the second case (64-2)

This type of anomaly results from a bit error in the Data Length Code byte, which defines the number of data bytes in CAN messages.

3.3 SEE with immediate, automatic recovery

As regards the 20 other SEEs, normal operation was always regained automatically in the next test cycle.

3.3.1 ADC

10 SEEs affected the ADC and all of them were automatically corrected. They are distributed into two classes: bit errors in the readings and errors in the control of the ADC.

- Bit errors in the readings

Only 4 of the 64 ADC channels were read. As indicated in the description of the experimental setup, different constant DC voltages were applied to them. The readings show small variations due to the noise. Their amplitude depends on the configuration of the ADC, which was set to 61.6 Hz and 1 V full scale during the test (see Figure 5).

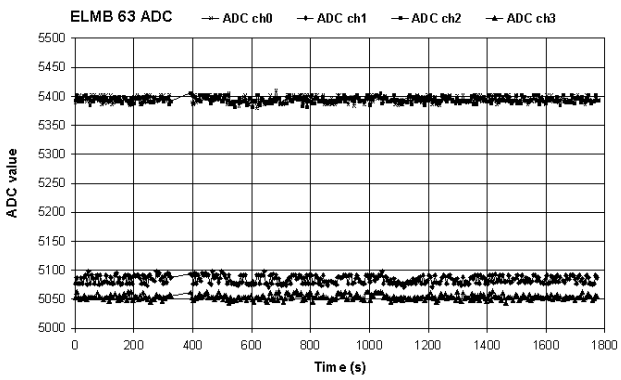

Figure 5: Normal fluctuations of ADC readings

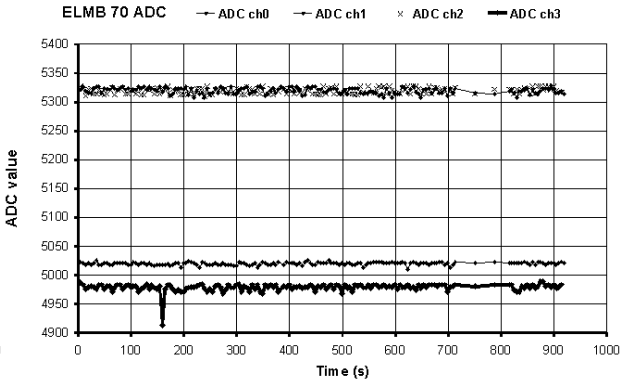

Figure 6: Bit error in channel 3 of ELMB 70

5 single bit errors were detected in the readings. They are displayed in Figures 6 and 7. (64-3, 64-4, 64-5, 64-6 and 70-2)

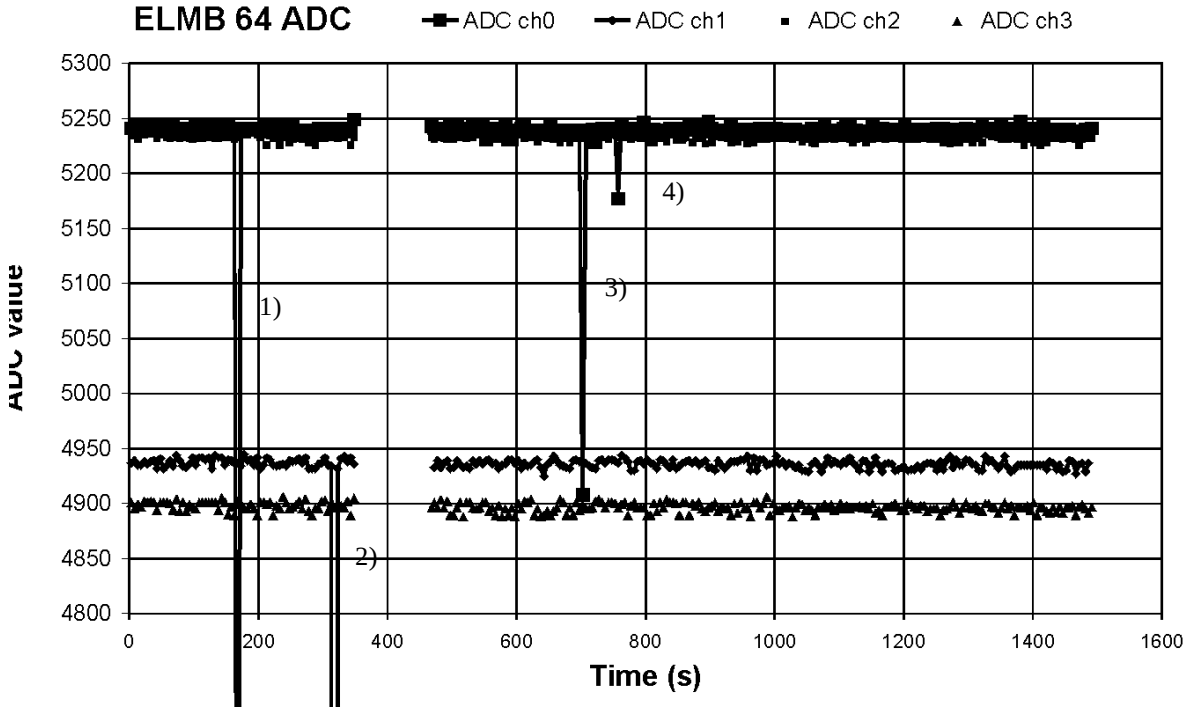

Figure 7: The following 4 bit errors were found in the readings of ELMB 64:

```
1) ADC ch0 bit error in data byte = 0x107C instead of 0x147C t=168 s
2) ADC ch1 bit error in data byte = 0x0344 instead of 0x1344 t=318 s
3) ADC ch0 bit error in data byte = 0x132C instead of 0x142C t=702 s
4) ADC ch0 bit error in data byte = 0x1439 instead of 0x1479 t=757 s
```

- Errors in the control of the ADC

4 errors affected the control of the ADC.

- In two test cycles, part of the 4 channels were not read. (70-3, 72-6)
- Two test cycles started 10 seconds after the previous one instead of 5 seconds. (62-2, 63-2)

3.3.2 Other SEE with automatic recovery

- In the master processor
- 3 consecutive messages reported 3 different changed values in the flash memory. As the memory content was unchanged after the test, they must be imputed to a corruption of the program running the tests. (65-2)
- ELMB 67 sent an unexpected boot-up message. (Normally, this kind of message follows a reset.) (67-1)
- ELMB 72 did not answer a request sent by the control computer. (72-2)

- In the CAN controller
- 5 CANbus error frame messages were reported. They were corrected by the CANbus built-in error checking circuits. (62-1, 64-1, 67-2, 72-4 and 72-5)
- 3 emergency messages indicated problems related to the CAN controller. (61-4, 71-2, 72-3)

3.4 Summary of the results

The integrated fluence of $3.3*10^{11}$ protons/cm^2 induced neither a hard SEE nor a destructive SEE. The results of the functional SEE test are summarized in Table 1.

Table 1: Number of soft SEEs for each means of recovery

Recovery	**Number of SEEs detected for $3.3*10^{11}$ protons/cm^2**	**Average fluence for 1 error**
Power cycling	4	$8.2*10^{10}$ protons/cm^2
Software reset	5	$6.6*10^{10}$ protons/cm^2
Automatic recovery	20	$1.6*10^{10}$ protons/cm^2
All types of recovery	**29**	**$1.1*10^{10}$ protons/cm^2**

4.0 Results of the systematic study of SEUs in memories and registers

This chapter reports the results of the systematic search for SEUs in memories and registers that was run by the dedicated ELMB software described in paragraph 2.5. This study involved the three types of memories of the master processor as well as the static registers of the CAN controller and the ADC. Note that the supply voltage was 3.3 V for the two first components and 5 V for the ADC.

4.1 SRAM test

The test involved 2 Kbytes of the SRAM embedded in the ATmega103L. Figure 8 displays the total number of SEEs detected since the beginning of the test versus fluence. The series number of the ELMB under test is indicated along the X-axis. The 11 ELMBs behaved in the same way, with a common cross-section of $3.4*10^{-12}$ SEEs per byte and proton/cm^2.

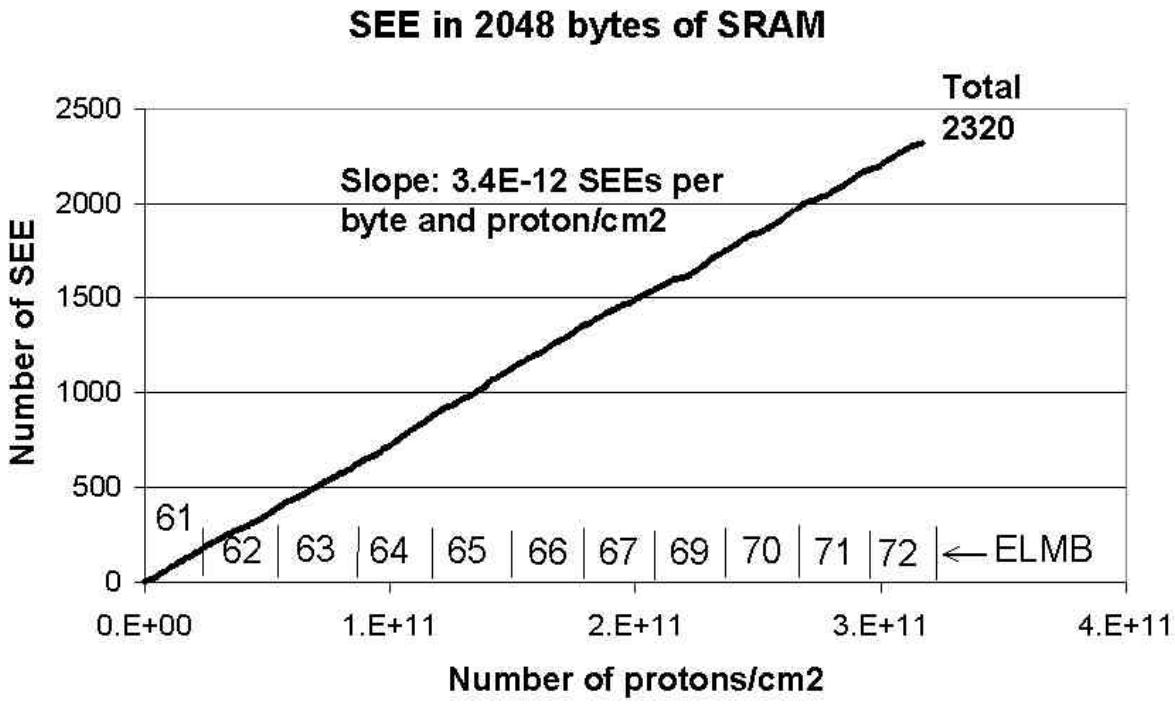

Figure 8: Total number of SEEs detected in the SRAM of the ATmega103L versus fluence

The SEEs comprised 2300 single bit flips and 3 double bit flips. There were 17 additional SEEs for which the erroneous byte value was not indicated, because more than 8 errors were detected in SRAM during each of the corresponding test cycles. The number of changes from logic 0 to logic 1 (1164) was within the statistical error the same as the number of opposite changes (1142). Moreover for both types of changes, the 8 bits were evenly affected.

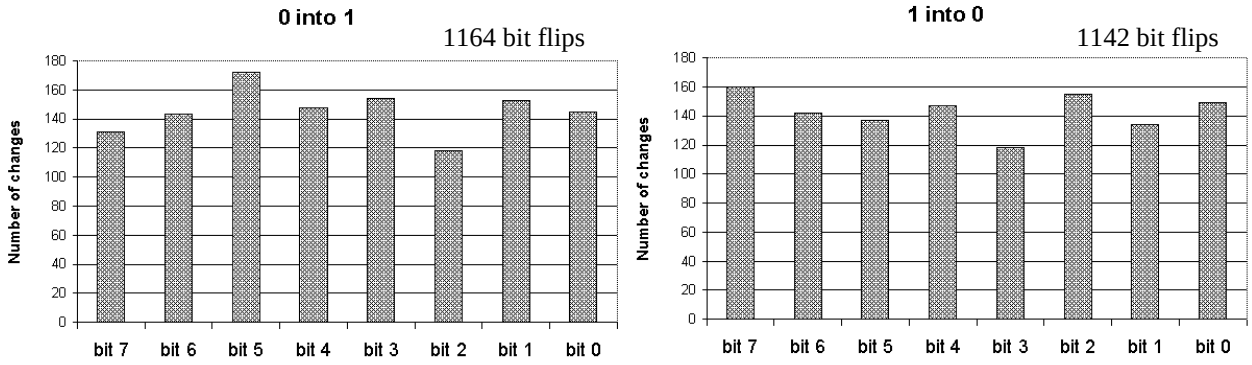

Figure 9: Number of changes from 0 to 1 (from 1 to 0, respectively)
in the 8 bits of the SRAM bytes

The test involved addresses 0x400 to 0xBFF (1024 to 3071 in decimal). Figure 10 indicates for each SEE in SRAM the address where it was located and the value of the fluence when it occurred. The projections of this chart onto each axis are displayed in Figures 11 and 12. They show that the SEEs were distributed evenly over the different addresses and independent from the fluence.

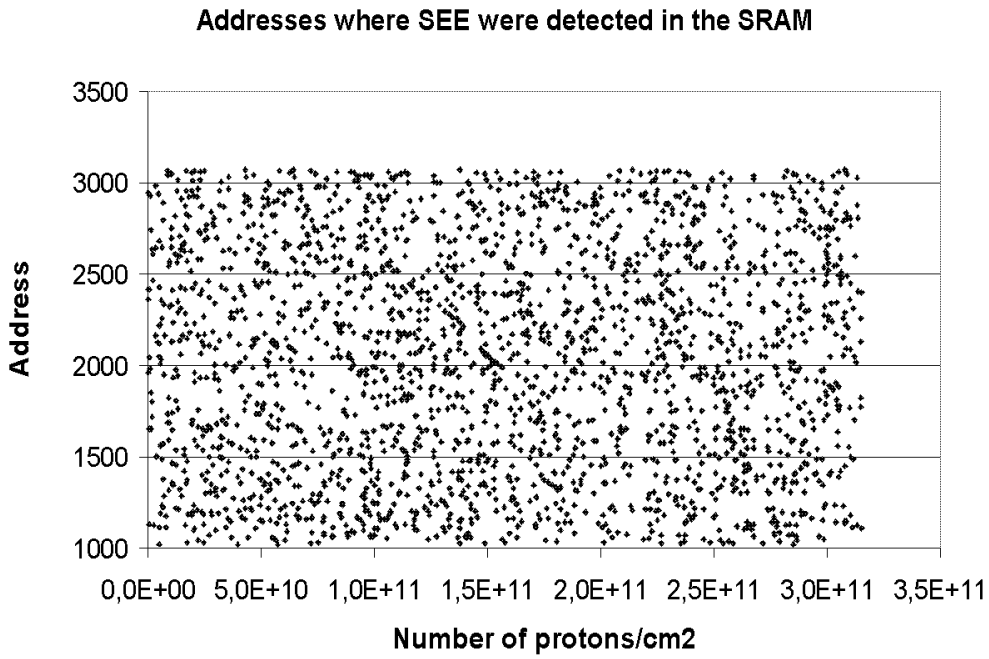

Figure 10: Addresses of the SRAM where the SEEs were located versus fluence

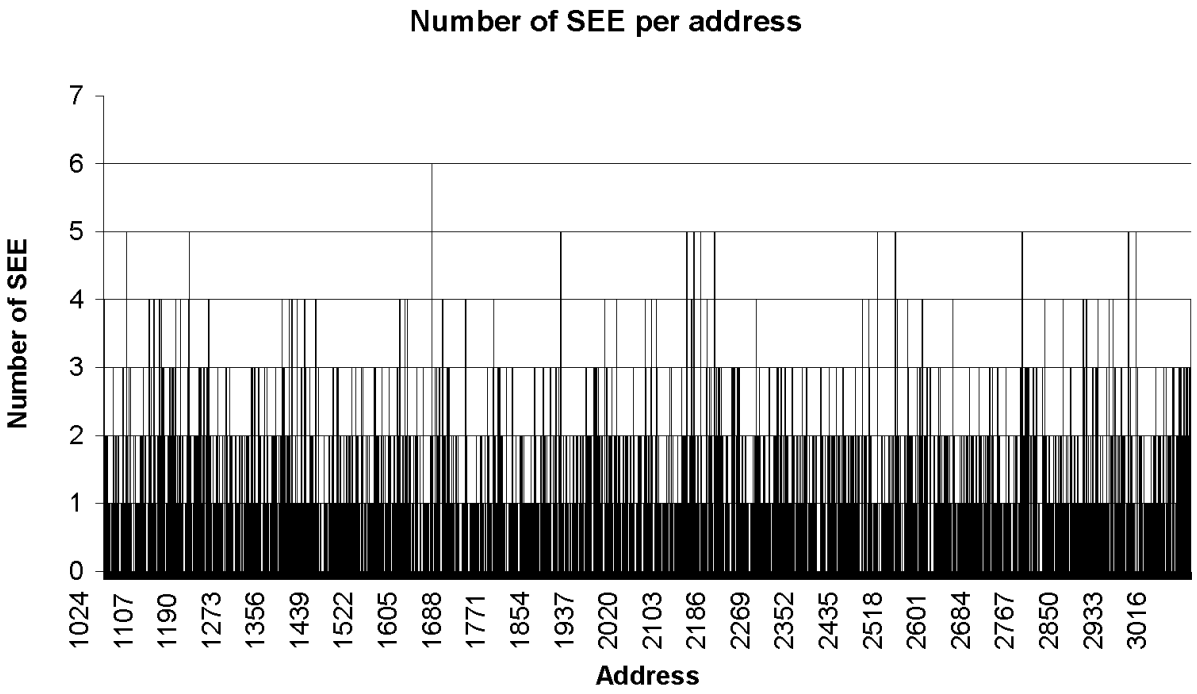

Figure 11: Number of SEEs detected in all the ELMBs per address in the SRAM

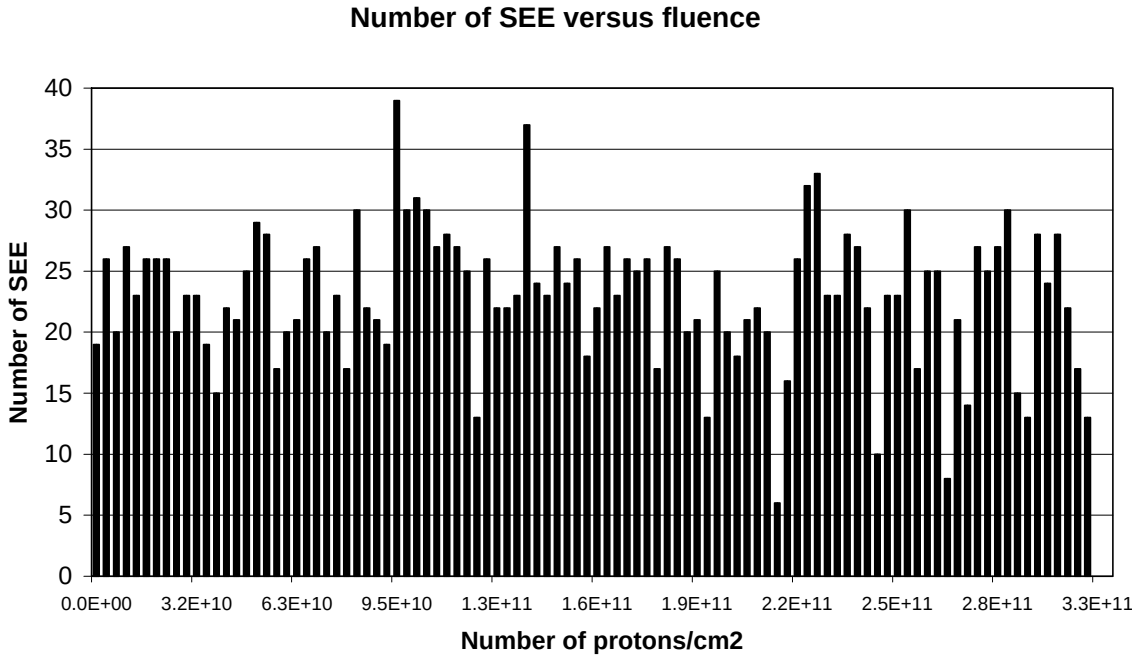

Figure 12: Number of SEEs in the SRAM versus fluence

4.2 EEPROM test

The test involved 3.5 Kbytes of the embedded EEPROM. No SEE was found. If one SEE had occurred, the cross-section would have been $8*10^{-16}$ SEEs per byte and proton/cm^2.

4.3 Flash memory test

Although the on-line test involved only 64 of the 128 Kbytes of the embedded flash memory, the whole memory had been filled with the same byte value. Its content was unchanged after the test for all ELMBs. Considering the whole memory, one error would have corresponded to a cross-section of $2*10^{-17}$ SEEs per byte and proton/cm^2.

4.4 CAN-controller register test

The test involved 40 bytes of the registers of CAN controller SAE81C91. The total number of SEEs amounted to 23, which corresponds to a cross-section of $1.7*10^{-12}$ SEEs per byte and proton/cm^2.

4.5 ADC register test

The test involved 33 bytes of ADC registers. The total number of SEEs amounted to 22, which corresponds to a cross-section of $2*10^{-12}$ SEEs per byte and proton/cm2.

4.4 Summary of the results

The results of the study of SEUs in memories and registers are summarized in Table 2. Similar proton SEE tests published in the database of Jet Propulsion Laboratory [10].

Table 2: Results of the systematic SEE study

Fluence: $3.28*10^{11}$ protons/cm^2

	Number of bits tested	Number of SEEs	Cross-section cm^2/bit
SRAM	16384	2320	$4.3*10^{-13}$
EEPROM	28672	<1	$<1.1*10^{-16}$
FLASH	1048576	<1	$<2.9*10^{-18}$
CAN registers	320	23	$2.2*10^{-13}$
ADC registers	264	22	$2.5*10^{-13}$

5.0 TID effects

The Total Ionizing Dose amounted to 39 Gy (Si) for 10 ELMBs and to 44.5 Gy for the other one. It corresponds to an average fluence of $3.3*10^{10}$ protons/cm^2 per ELMB.

5.1 Reprogramming function of flash memory and EEPROM

The reprogramming functions of all ELMBs were tested after the proton irradiation. They proved to work perfectly.

5.2 Power supply currents

The analog, digital and CAN power supply currents were measured during the test. When the results were analyzed, two values were calculated for each ELMB and each power supply:
- the average current before the irradiation
- the average current after the irradiation.

The differences between the two values are displayed in the charts below. They are all very small and within the specification.

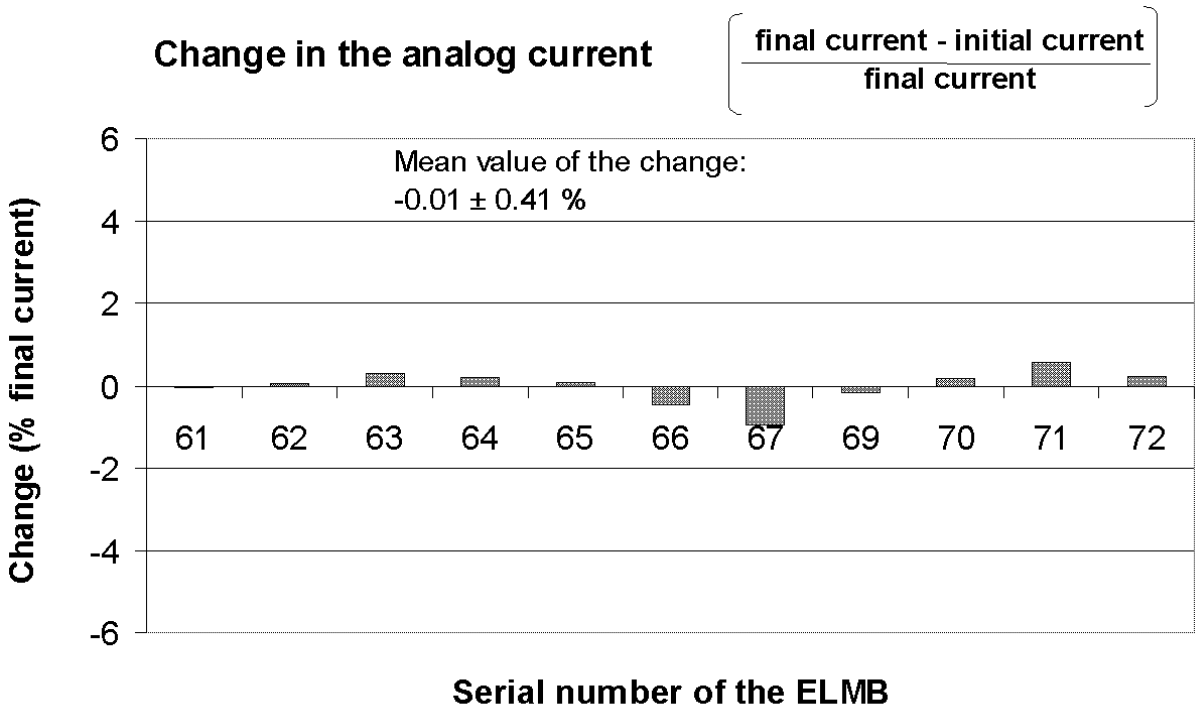

Figure 13: Change in the analog current between the beginning and the end of the test

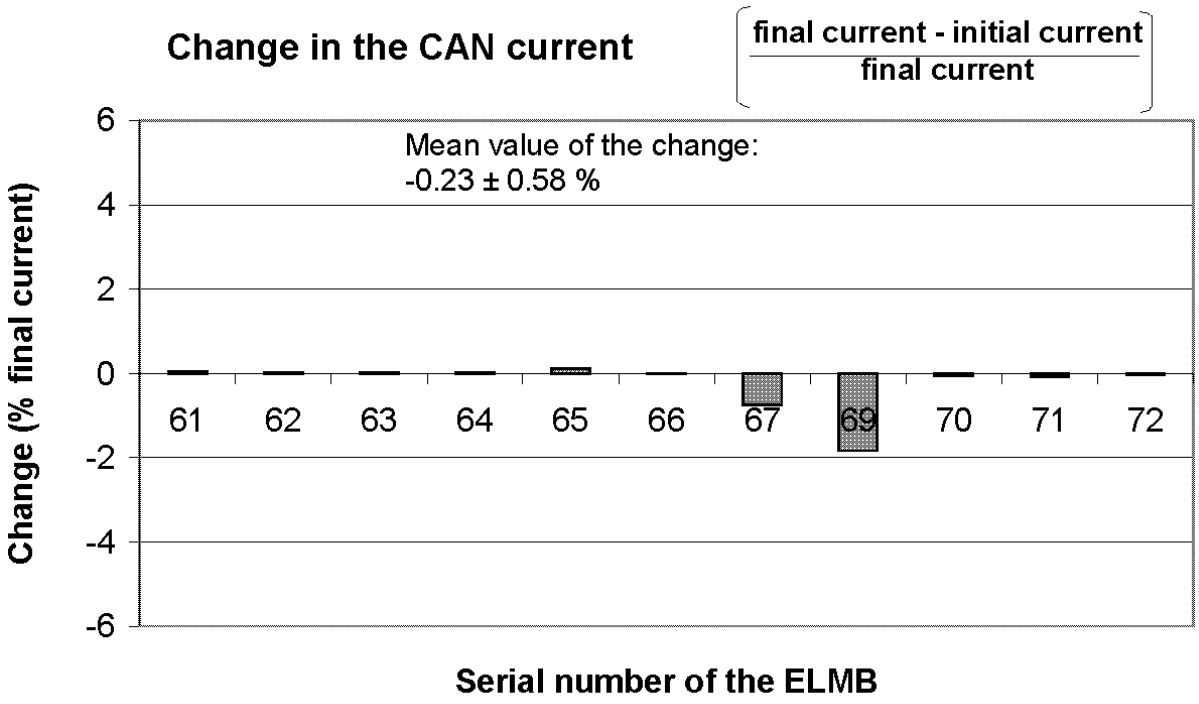

Figure 14: Change in the CAN current between the beginning and the end of the test

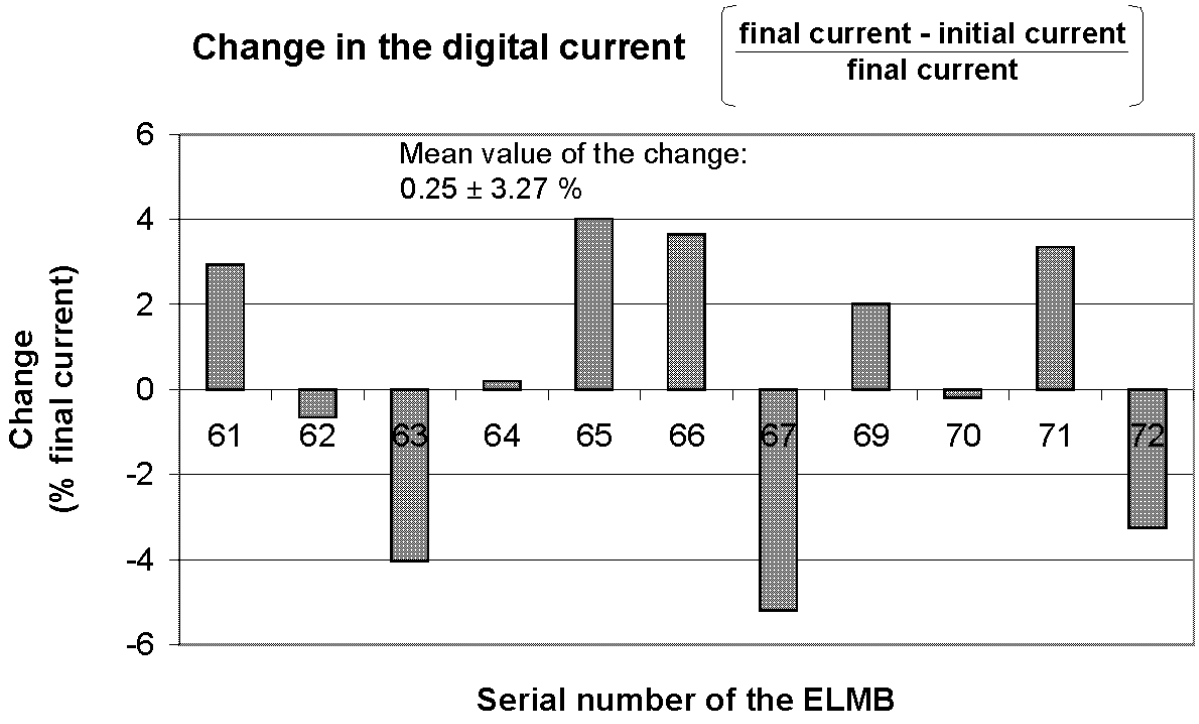

Figure 15: Change in the digital current between the beginning and the end of the test

5.3 DC voltages

4 DC voltages were measured before and after the test:

- the ADC voltage reference AD680JR, which was very stable (10^{-3}).

- the voltages at the output of the analog, CAN and digital regulators. All of them increased very slightly but stayed within the specification of ± 3 %.

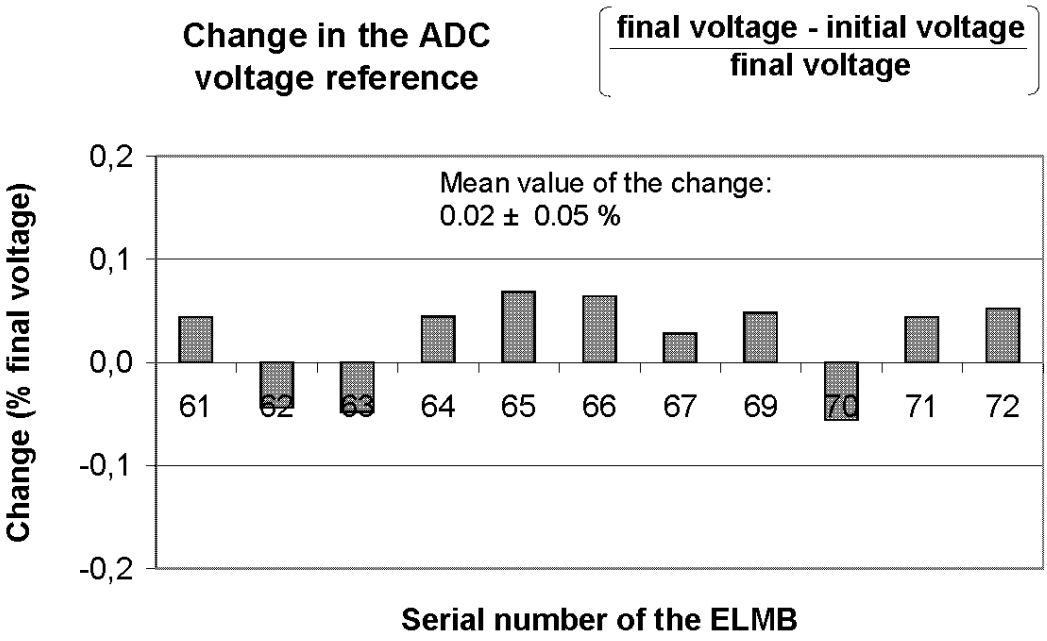

Figure 16: Change in the ADC voltage reference between the beginning and the end of the test

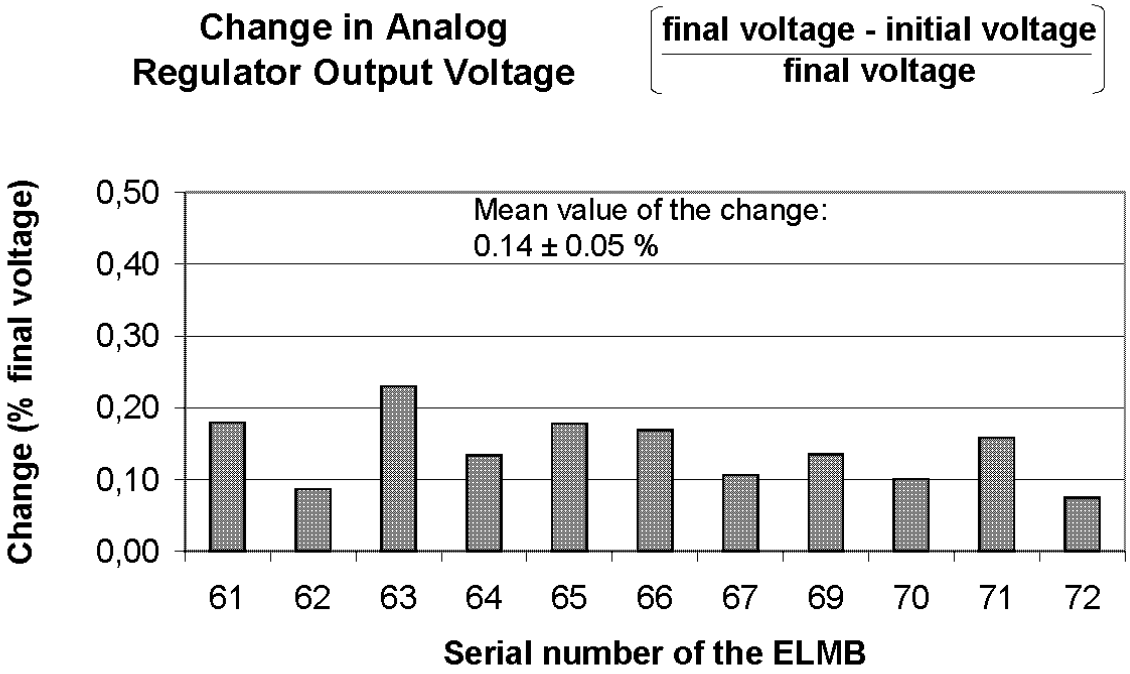

Figure 17: Change in the analog voltage between the beginning and the end of the test

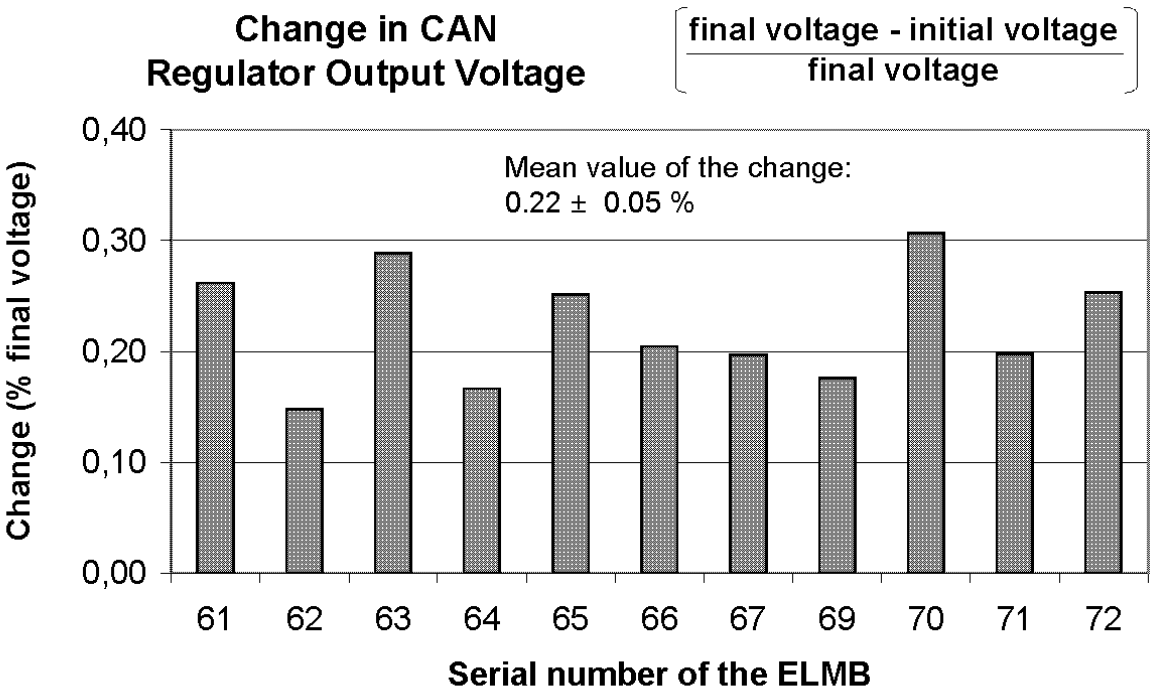

Figure 18: Change in the CAN voltage
between the beginning and the end of the test

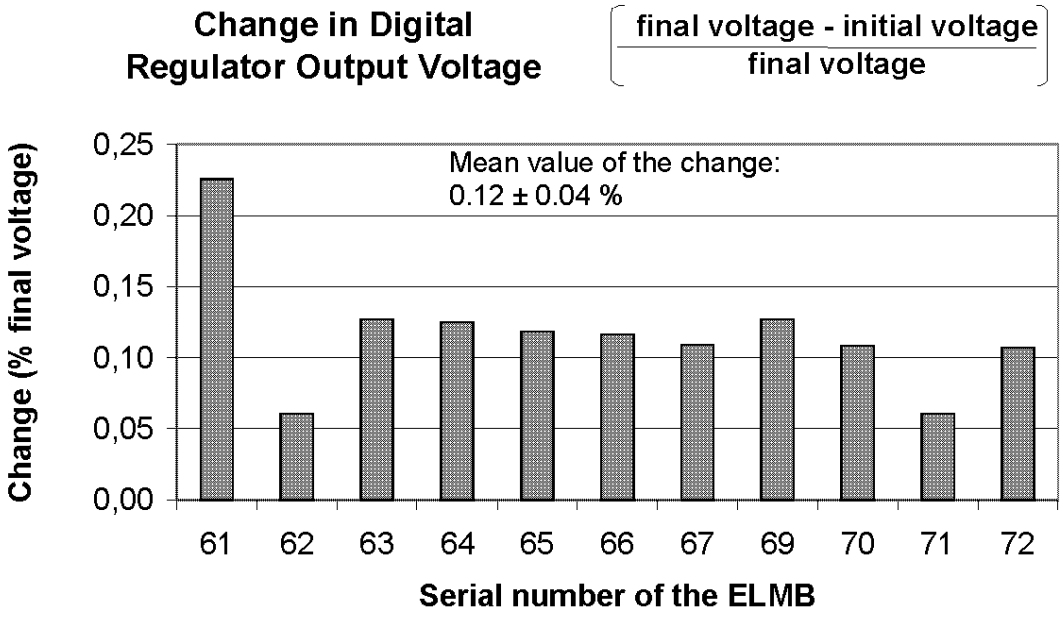

Figure 19: Change in the digital voltage
between the beginning and the end of the test

5.4 ADC readings

The readings of the 4 tested channels showed a standard deviation of 4.3 LSB (1 LSB = $1.53*10^{-5}$ V). The calculation has not included the wrong readings of ELMB 64 channels 0 and 1, mentioned in paragraph 3.3.1. This result is good in view of the specification indicated in the product data sheet, since the typical RMS noise is 6 LSB for the ADC configuration used during the test (1V input range and 61.6 Hz output rate). Moreover, fluence does not seem to have any influence on the noise amplitude.

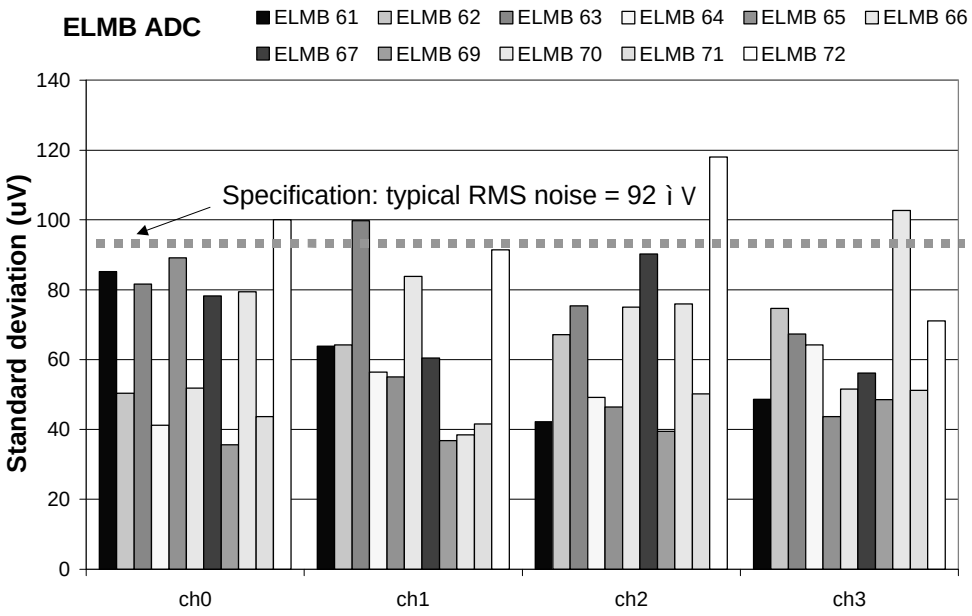

Figure 20: Standard deviations of the readings of the 4 ADC channels for each ELMB

5.5 Summary of the results

All 11 ELMBs could withstand an irradiation with 60 MeV protons to a TID of 39 Gy. No current increase or significant change of any other parameter was detected.

6.0 Description of the requirements and comparison with the results

6.1 Requirements for ATLAS

A CAN branch in the final ATLAS experiment will include 64 ELMBs at most. The whole system will comprise about 3000 ELMBs. During the 10 years lifetime of the experiment, the ELMB will be in active operation with beam for a time of the order of 10^8 s. The requirements assume that in the experimental cavern, each ELMB will receive a total of $4.83*10^{11}$ hadrons/cm^2. This number corresponds to the highest fluence that will be reached after 10 years in the MDT (End-cap 1) subdetector, multiplied by a safety factor of 10 [3].

Table 3 describes the different SEE categories and their maximum allowed rates

Table 3: Maximum allowed SEE rates

SEE category / Symptoms	Error recovery	Maximum allowed rate
Soft SEE/ Data readout errors	Automatic	1 every 10 minutes per CAN branch
Soft SEE / CAN node hangs	CANopen NMT reset	1 every 24 hours per CAN node
Soft SEE / CAN branch hangs	Power cycling	1 every 24 hours per CAN branch
Hard SEE / Permanent error	Replace ELMB	1 every 2 months for 3000 ELMBs
Destructive SEE / Damage	Power limitation	Not allowed

Each category of SEE is subject to a specific treatment.

- Data readout errors consist in random accidental events, the most frequent ones being bit errors. In physics experiments, they are caused not only by radiation but also by harsh electrical environments. Recovery from these errors is built into the software.
- The time needed to reset a single CAN node via a CANopen Network Management command is less than 1 second. This software reset, which will be undertaken by the slave processor of the ELMB, will have no influence on the other nodes of the CAN branch.
- No hardware-reset line is implemented in the ELMB system. Instead a reset of all ELMBs on a branch will be done via a power off/on cycle, which is foreseen to be executed under program control in the final ATLAS. A whole CAN branch will be reset in about 1 second.
- To reduce the risk of hard and destructive SEEs, the ELMB contains protection circuits that shut down the device if either the current or the temperature is too high.

6.2 Comparison with the results

For a total fluence of $3.3*10^{11}$ protons/cm^2, the irradiation with 60 MeV protons caused 29 SEEs in the ELMB. One Single Event Latch-up occurred, affecting the digital part. All the other SEEs are Single Event Upsets. For most SEEs (20), the recovery was automatic. In particular one never observed errors in two consecutive readings of an ADC channel. This result is important, as in final ATLAS two consecutive measurements will be required to detect a fault in a device. 9 resets were performed to resume normal operation: 5 software resets and 4 power cycling resets.

Table 4: Comparison between the requirements and the results of the SEE test

SEE category	Number of SEEs per CAN node		
	For $3.28*10^{11}$ hadrons/cm^2	For $4.83*10^{11}$ hadrons/cm^2	
	Raw result of the test	**Requirement**	**Result of the test after scaling**
Soft SEE, automatic recovery	20	2604	29
Soft SEE, software reset	5	1157	7
Soft SEE, power cycling	4	18	6
Hard SEE [1]	0	0.006	0

[1] The number of accumulated protons is not sufficient to judge whether the requirement is fulfilled. If one hard SEE had been observed, this would have corresponded to 1.5 SEEs for $4.83*10^{11}$ hadrons/cm^2.

7.0 Conclusion

All the SEE rates measured during the test except one could be compared with the requirements and they were much lower than the maximum allowed rates. The statistics was not sufficient to study hard and destructive SEEs. To get significant results with the 60 MeV proton beam, the fluence should be increased by a factor of the order of a few hundred, which is impracticable. Another approach would consist in performing the test at a higher energy. A systematic study of the SEE effects in different types of memories used in the ELMB yields that the SRAM of the microcontroller has a SEE cross-section of $4.3*10^{-13}$ per bit and proton/cm^2. For the EEPROM and the flash memory, the cross-sections are several orders of magnitude smaller. Therefore, it seems possible to decrease the sensitivity of the ELMB to SEEs further by taking some precautions. First the software should use the SRAM as little as possible and resort to the EEPROM and the flash memory instead. The constants stored in SRAM should also be regularly updated from the EEPROM and the flash memory.

References

[1] http://atlasinfo.cern.ch/ATLAS/GROUPS/DAQTRIG/DCS/ELMB/elmb.html

[2] http://www.cyc.ucl.ac.be/

[3] Appendix 2 of ATLAS doc. ATC-TE-QA-0001, 21 July 00, page 27

[4] H.Burckhart, B. Hallgren and H. Kvedalen, ' Irradiation Measurements of the ATLAS ELMB', CERN ATLAS Internal Working Note, DCS- IWN9, 8 March, 2001

[5] J. Cook, B. Hallgren and H. Kvedalen, ' Radiation test at GIF and accelerated aging of the ELMB ', CERN ATLAS Internal Working Note, DCS- IWN10, 2 May, 2001

[6] B. Hallgren and H. Kvedalen, ' Radiation test of the 3.3V version ELMB at GIF ', CERN ATLAS Internal Working Note, DCS- IWN11, 31 August, 2001

[7] http://atlasinfo.cern.ch/ATLAS/GROUPS/DAQTRIG/DCS/lmb.html

[8] H. Boterenbrood, ' ELMBIO (v3.3+) Test Objects ', NIKHEF, 19 June, 2001

[9] http://www.vector-informatik.com/english/products/index.html

[10] http://radnet.jpl.nasa.gov/Compendia/P/ProtonSeeCompendium.htm#rom

Appendix 1 List of all the Single Event Effects detected during the functional test

Device Under Test DUT	Serial number of the DUT	Number of soft SEEs / Effective fluence[1]	Recovery after power cycle reset (Y/N)[2]	Recovery after software reset (Y/N)[2]	Index of the SEE	Description: Failure mechanism	Description: Corrected by
1	ELMB 61	**4**	Y	-	61-1	ATmega SEL of digital power	Power cycling
		$2.4*10^{10}$	-	Y	61-2	ATmega (test loop timer)	software reset
			-	Y	61-3	CAN DLC of message	Software reset
			-	-	61-4	CAN Remote frame interrupt	auto recovery
2	ELMB 62	**2**	-	-	62-1	CAN Error frame	auto recovery
		$3.0*10^{10}$	-	-	62-2	ADC control error	auto recovery
3	ELMB 63	**2**	Y	-	63-1	ATmega too many CAN messages	power cycling
		$3.4*10^{10}$	-	-	63-2	ADC conversion time out	auto recovery
4	ELMB 64	**6**	-	-	64-1	CAN Error frame	auto recovery
		$3.0*10^{10}$	-	Y	64-2	CAN DLC of message	Software reset
			-	-	64-3	ADC Bit readout error	auto recovery
			-	-	64-4	ADC Bit readout error	auto recovery
			-	-	64-5	ADC Bit readout error	auto recovery
			-	-	64-6	ADC Bit readout error	auto recovery
5	ELMB 65	**2**	Y	-	65-1	ATmega (test loop timer)	power cycling
		$3.0*10^{10}$	-	-	65-2	ATmega error in i/o program	auto recovery
6	ELMB 66	**0**	-	-		No errors!	
		$3.0*10^{10}$					
7	ELMB 67	**2**	-	-	67-1	ATmega unexpected message	auto recovery
		$3.0*10^{10}$	-	-	67-2	CAN Error frame	auto recovery
8	ELMB 69	**0**	-	-		No errors!	
		$3.0*10^{10}$					
9	ELMB 70	**3**	-	Y	70-1	ATmega (test loop timer)	Software reset
		$3.0*10^{10}$	-	-	70-2	ADC Bit readout error	auto recovery
			-	-	70-3	ADC channel readout error	auto recovery
10	ELMB 71	**2**	Y	N	71-1	ATmega infinite program loop (unsuccessful software reset)	Software reset power cycling
		$3.0*10^{10}$	-	-	71-2	CAN Emergency message	auto recovery
11	ELMB 72	**6**	-	Y	72-1	ATmega (test loop timer)	Software reset
		$3.0*10^{10}$	-	-	72-2	ATmega no reply	auto recovery
			-	-	72-3	CAN Life guarding time out	auto recovery
			-	-	72-4	CAN Error frame	auto recovery
			-	-	72-5	CAN Error frame	auto recovery
			-	-	72-6	ADC channel readout error	auto recovery

[1]Fluence received by the ELMB while the test software was running.
[2]Y: successful operation- N: operation failed- minus sign: no operation was performed.