SULIT

SCHOOL OF COMPUTING
Faculty of Engineering

UNIVERSITI TEKNOLOGI MALAYSIA
FINAL EXAMINATION SEMESTER I 2019 / 2020

SUBJECT CODE : **SECR1013 / SCSR1013**

SUBJECT NAME : **DIGITAL LOGIC**

SECTION : **SECR/J/B/V/P / SCSR/J/B/V/P**

TIME : **3 HOURS**

DATE/DAY :

VENUES :

INSTRUCTIONS:

Answer all questions from PART A and PART B. Show all your works.

This test will contribute 35% towards the total marks of 100%.

(Please Write Your Lecturer Name And Section In Your Answer Booklet)

Name	
I/C No.	
Year / Course	
Section (Circle)	**01 / 02 / 03 / 04 / 05 / 06 / 07 / 08 / 09**
Lecturer Name (Circle)	**Mr Firoz / Mrs Zuriahati / Mrs Rashidah**

This question paper consists of 16 printed pages excluding this page.

PART A: OBJECTIVES

Answer ALL questions in answer booklet.

1. What is a multiplexer?
   A. It is a type of decoder which decodes several inputs and gives one output.
   B. A multiplexer is a device that has many inputs and a single output.
   C. It takes one input and results into many outputs.
   D. It is a type of encoder which decodes several inputs and gives one output.

2. How many outputs are in a BCD decoder?
   A. 4
   B. 5
   C. 15
   D. 10

3. In 1-to-4 demultiplexer, how many select lines are required?
   A. 2
   B. 3
   C. 4
   D. 5

4. In a multiplexer the output depends on its _____.
   A. data outputs
   B. select inputs
   C. select outputs
   D. rotate pin

5. Parity generators/checkers use which modulo summation?

   A. Modulo 8

   B. Modulo 16

   C. Modulo 2

   D. Modulo 10

6. A code converter is a logic circuit that _____.

   A. Inverts the given input

   B. Converts into decimal number

   C. Converts data of one type into another type

   D. Converts to hexadecimal

7. Which of the following is NOT a latch?

   A. S-R latch

   B. T latch

   C. Gated S-R latch

   D. Gated D latch

8. The invalid state of active HIGH S-R latch occurs when _____.

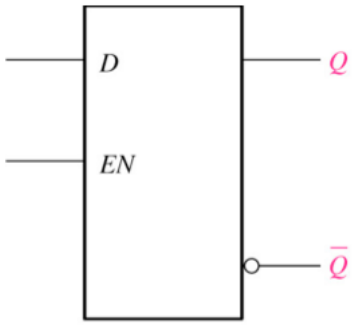
   A. S = 1, R = 0

   B. S = 0, R = 1

   C. S = 1, R = 1

   D. S = 0, R = 0

9. The diagram below shows what type of temporary storage device?



A. D flip flop

B. C-D flip flop

C. Gated S-R latch

D. Gated D latch

10. Which of the following is considered as highest priority asynchronous input(s)?

A. Clock

B. $\overline{PRE}$

C. T

D. J and K

11. When both inputs of a J-K pulse-triggered flip-flop are HIGH, and the clock triggers, what will the output be?

A. An invalid state will exist.

B. No change will occur in the output.

C. The output will reset.

D. The output will toggle.

12. Which statement is FALSE regarding universal bidirectional shift register (74HC194)?

A. Can implement Serial In Serial Out (SISO) operation

B. Can implement Serial In Parallel Out (SIPO) operation

C. Can implement Parallel In Serial Out (PISO) operation

D. Can implement Round Robin In Parallel Out (RRPO) operation

13. A modulus 16 ring counter requires how many flip-flops?

A. 2

B. 4

C. 8

D. 16

14. If a 10-bit ring counter has an initial state 1101000000, what is the state after the third clock pulse?

A. 1101000000

B. 0001101000

C. 1100000000

D. 0000000000

15. A modulus 12 Johnson counter requires a minimum of _____.

A. 10 flip-flops

B. 12 flip-flops

C. 6 flip-flops

D. 2 flip-flops

16. On the third clock pulse, a 4-bit Johnson sequence is $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, and $Q_3 = 0$. On the fourth clock pulse, the sequence is _____.

A. $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 1$, $Q_3 = 1$

B. $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, $Q_3 = 0$

C. $Q_0 = 1$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$

D. $Q_0 = 1$, $Q_1 = 0$, $Q_2 = 0$, $Q_3 = 0$

17. An asynchronous counter differ from a synchronous counter in _____.

A. the number of states in its sequence

B. the type of flip flop used

C. the method of clocking

D. the value of modulus

18. A modulus-12 asynchronous counter must have _____.

A. 12 flip-flops

B. 4 flip-flops

C. 3 flip-flops

D. 5 flip-flops

19. Four cascaded modulus-10 counters have an overall modulus of _____.

A. 40

B. 10

C. 1000

D. 10000

20. Which asynchronous counter mod is a truncated sequence?

A. mod 4

B. mod 8

C. mod 13

D. mod 16

PART B: STRUCTURED
Answer ALL questions in question and answer booklet.

Question 1 [16 Marks]

a) Draw the block diagram for a 3-bit parallel adder using full adder and label clearly the block diagram including the input, sum and carry. Perform addition $011_2 + 110_2$ **,** show the value for each label on the block diagram. [4]

$$\begin{array}{rcccc} & A_3 & A_2 & A_1 \\ + & B_3 & B_2 & B_1 \\ \hline \sum_4 & \sum_3 & \sum_2 & \sum_1 \end{array}$$

b) For set of binary numbers $A_3A_2A_1A_0 = 0010$ $B_3B_2B_1B_0 = 0101$ are assigned to comparator in Figure 1.

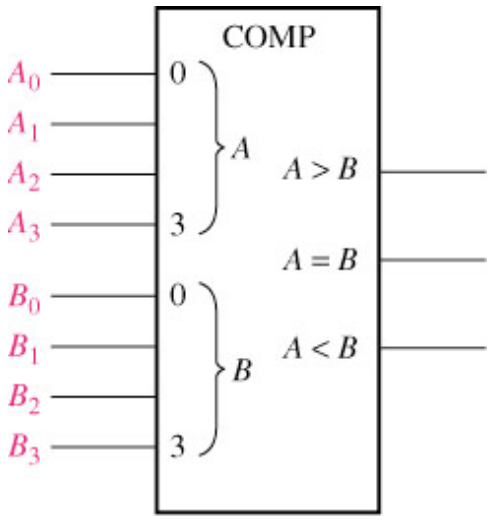


Figure 1

i. Based on Figure 1, explain how comparator works until final output results appear. [3]

ii. Determine the final output result for the comparator in Figure 1. [1]

c) Given an active HIGH 7-segment display in Figure 2 showing a digital number from a decoder that is based on the BCD value, **complete Table 1 in your question booklet APPENDIX A**. [4]

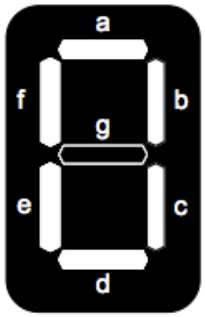


Figure 2

d) Figure 3 in APPENDIX A shows DEMUX connection with outputs labelled as Y_3 Y_2 Y_1 Y_0 and B is the input of DEMUX. Select bit for DEMUX are noted by C_1 and C_0 (C_1 is the MSB). **Draw the waveform for the DEMUX output based on the given values in question booklet Figure 3 APPENDIX A.** [4]

Question 2 [15 Marks]

a) Draw the output Q for a positive edge triggered D flip flop and assume initial Q is LOW. **Draw the waveform in question booklet Figure 4 APPENDIX A**. [4]

b) Complete Table 2 based on the output for all Q in Figure 4. **Complete Table 2 in your question booklet APPENDIX A.** [3]

c) Assume that Q is initially LOW, for gated S-R latch. **Draw the waveform for output Q in question booklet Figure 5 APPENDIX A.** [3]

d) Determine output Q in Figure 6 for a positive edge triggered JK flip-flop with $\overline{\text{PRE}}$, $\overline{\text{CLR}}$, and J, K inputs. Assume that Q is initially LOW. **Draw the waveform in question booklet Figure 6 APPENDIX A.** [5]

Question 3 [18 Marks]

Design a synchronous counter to produce the following binary sequence:

- 0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, 9… (recycle counter)
- Positive edge flip-flops
- Using T flip-flops, use Q_0 as LSB

a) Create state diagram [3]

b) Develop the next state table and flip-flops transition table. [6]

c) Determine the Boolean expression using K-Map. [4]

d) Draw the circuit. [5]

Question 4 [16 Marks]

a) An asynchronous counter with the following specification: [7]

- Recycle count up from 0 to 5
- Negative edge flip-flops
- Using JK flip-flops, use Q_0 as LSB

i. Determine the number of flip-flops required.

ii. Design an active low decoder (NAND) for the asynchronous counter.

iii. Draw the circuit connection for the asynchronous counter.

b) Analyze the following circuit as shown in Figure 7. [9]

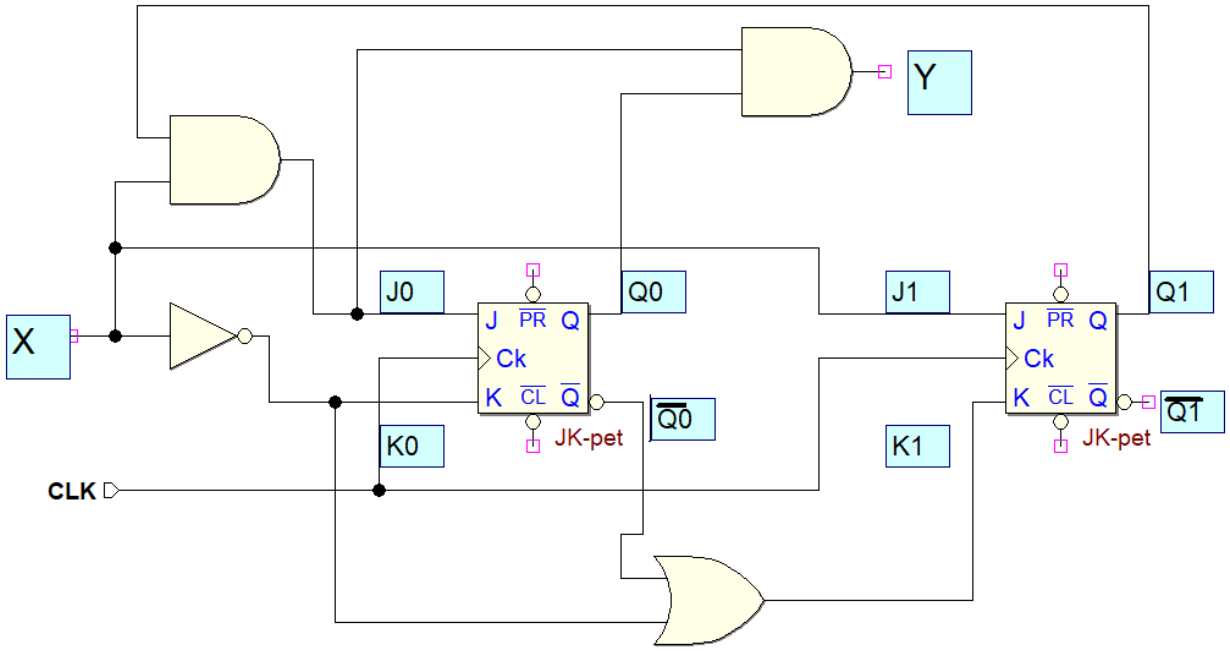


Figure 7

i. Derive Boolean expression for the J0, K0, J1, K1 and output Y.

ii. Use Method 2 to produce the next state and flip flop transition table. Use the following Table 3 header.

Table 3

Input	Present State		Next State		JK FF Transition				Output
X	Q1	Q0	Q1+	Q0+	J1	K1	J0	K0	Y

iii. Draw a complete state diagram for the circuit shown.

Question 5 [15 Marks]

a) A helpful analogy for a shift register is a conveyor belt. As illustrated in Figure 8 (i), (ii) and (iii) showing a single conveyor belt at four different times and determine which of the following shift register operations the sequence represents. Justify your answer. [4.5]

Answer options:

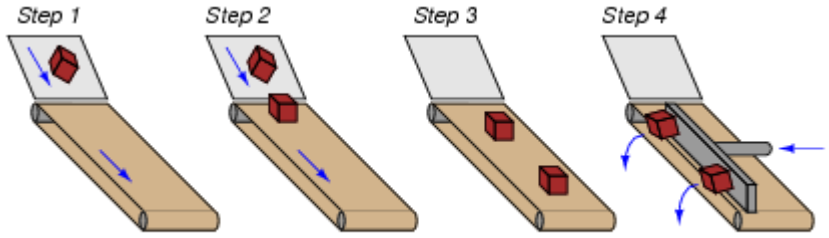
Parallel-in, serial-out

Serial-in, serial-out

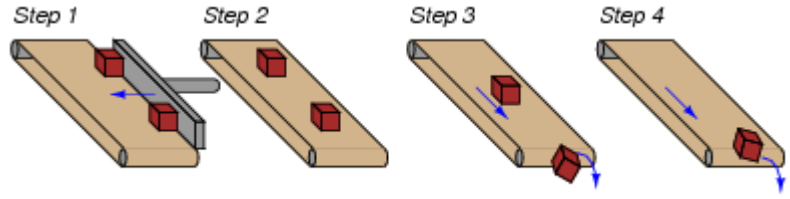
Parallel-in, parallel-out

Serial-in, parallel-out

(i)



(ii)



(iii)

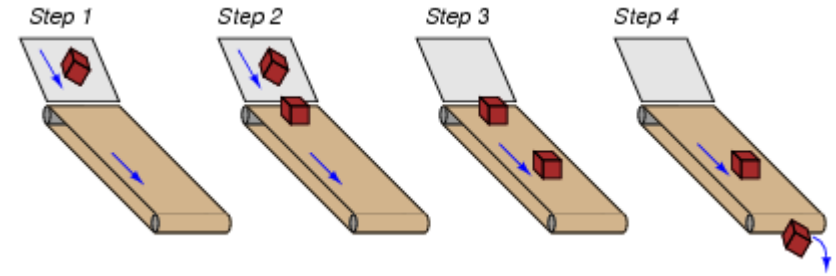


Figure 8

b) Draw and label clearly the logic diagram for 5 bit SISO (serial in serial out) shift register circuit using D flip flops. [4]

c) For 6 bit SIPO (serial in parallel out) shift register, [4]

i. Complete Table 4 header in answer booklet for 6 clock cycles. The following 6 bit data is used with MSB entered first.

Q5					**Q0**
1	**1**	**0**	**0**	**0**	**1**

Table 4

Clock	FF0	FF1	FF2	FF3	FF4	FF5
Initial	0	0	0	0	0	0

ii. At what clock cycle can all the input data be read at the output?

d) Draw the output waveform Q_4 of a 5-bit PISO (parallel in serial out) shift register if the data input entered is $D_4D_3D_2D_1D_0 = 11001_2$. D_4 represents MSB and it will be shifted out first. **Draw the waveform in question booklet Figure 9 APPENDIX A.** [2.5]

APPENDIX A

NAME			
METRIC NO.		SECTION	

Question 1

c)

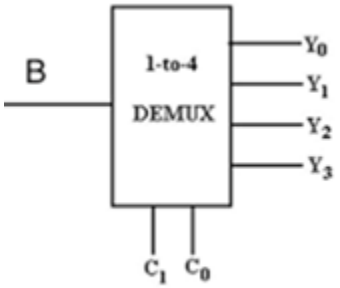
Table 1

BCD Input				Segment Output							Display
A	B	C	D	*a*	*b*	*c*	*d*	*e*	*f*	*g*	
											3
											6
1	0	0	0								8

APPENDIX A

NAME			
METRIC NO.		SECTION	

d)



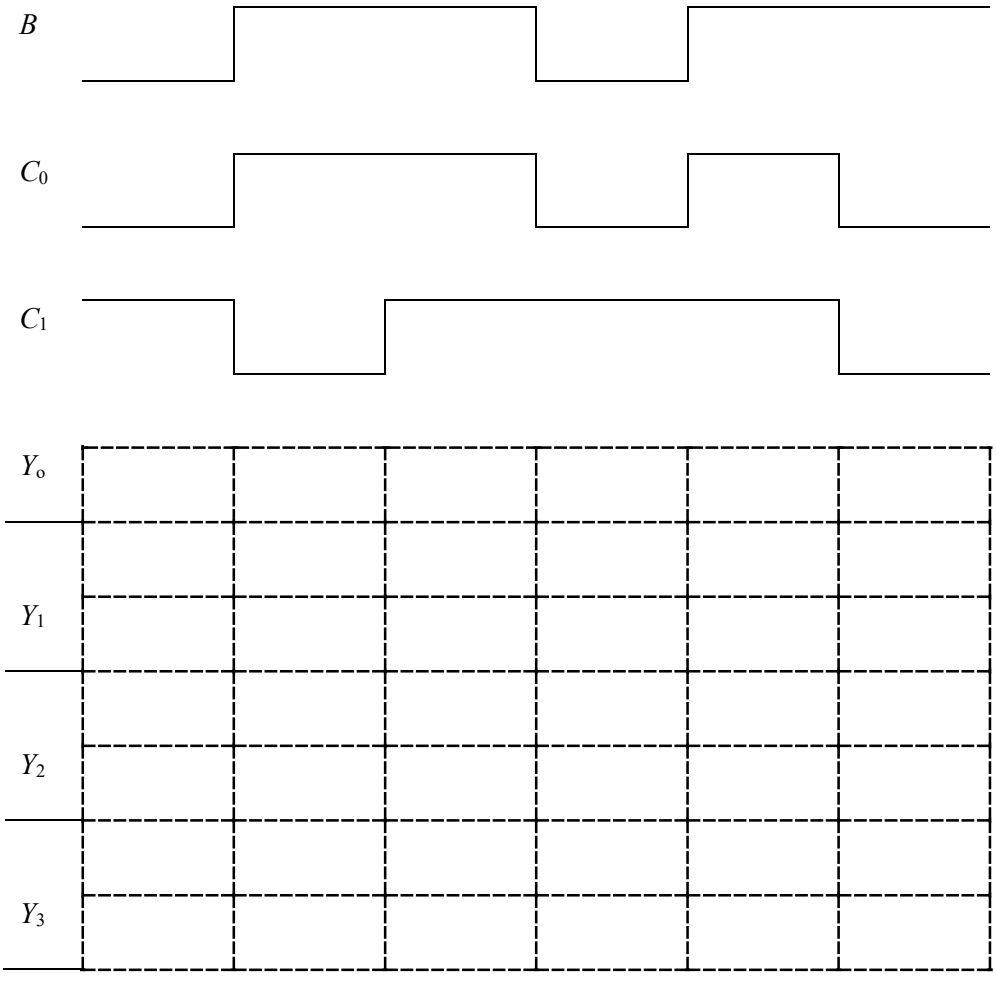


Figure 3

APPENDIX A

NAME			
METRIC NO.		SECTION	

Question 2

a)

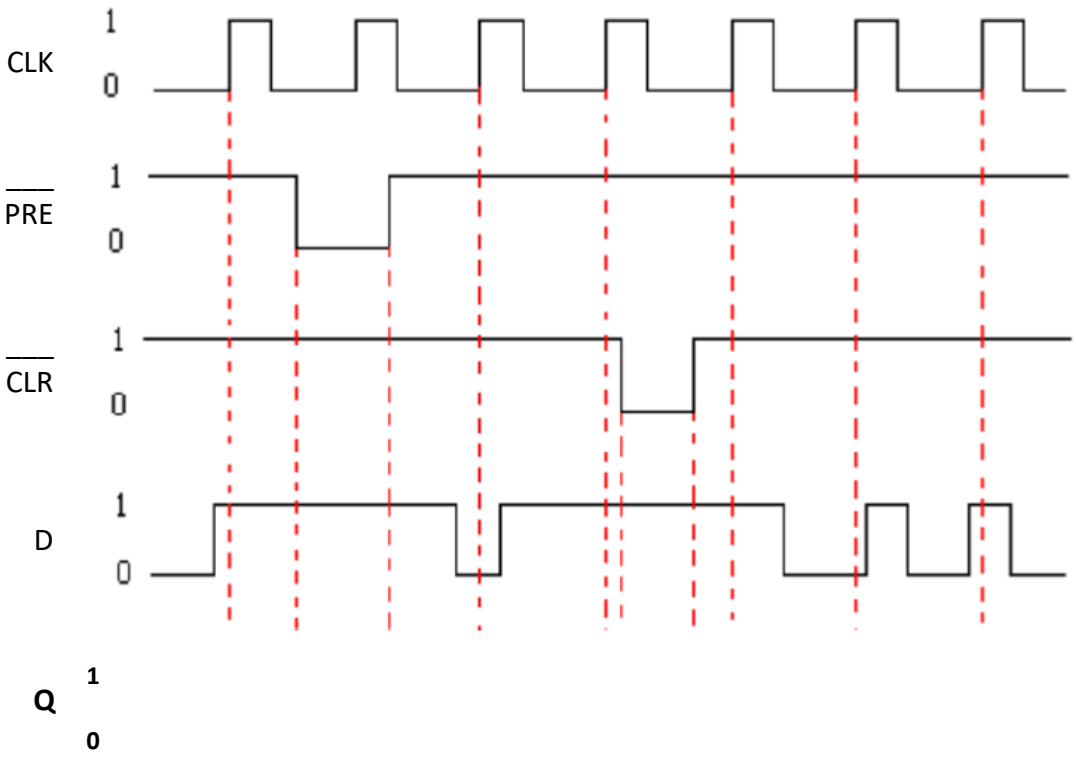


Figure 4

b)

Table 2

Clock Pulse (1 to 7)	$\overline{PRE}$	$\overline{CLR}$	D	FF State	Mode (Async/Sync)
	X	1			
	1	X			

APPENDIX A

NAME			
METRIC NO.		SECTION	

c)

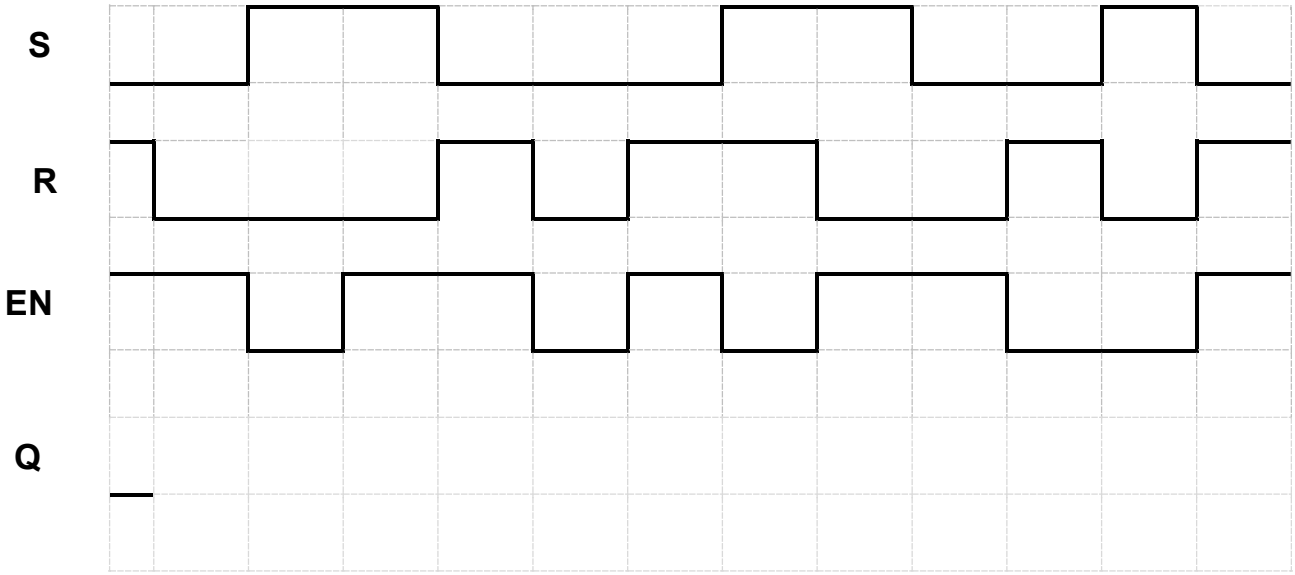


Figure 5

d)

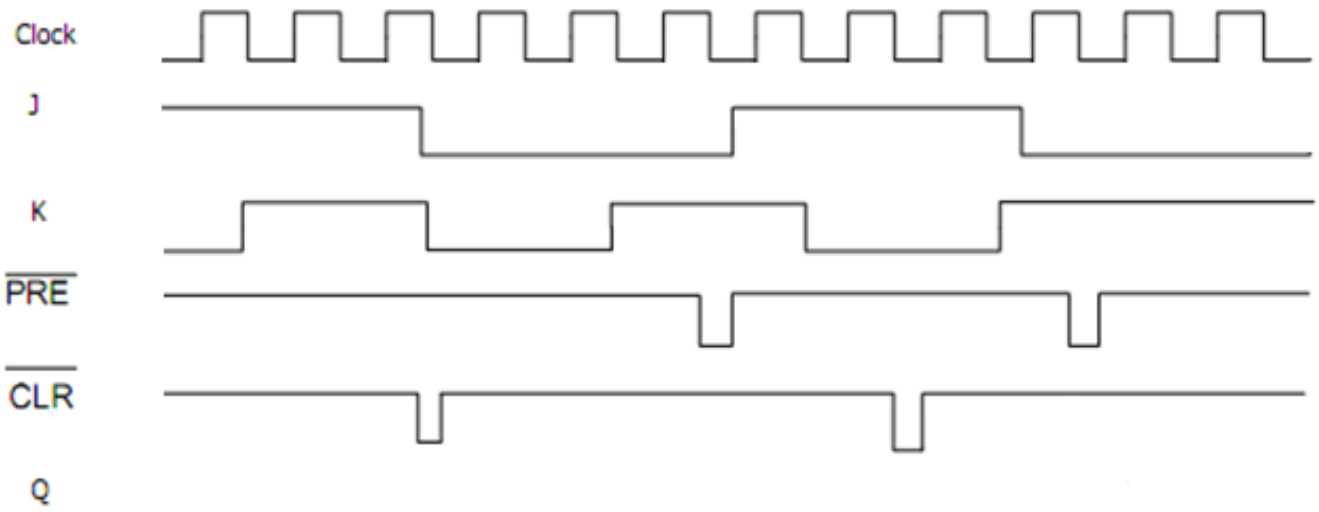


Figure 6

APPENDIX A

NAME			
METRIC NO.		SECTION	

Question 5

d)

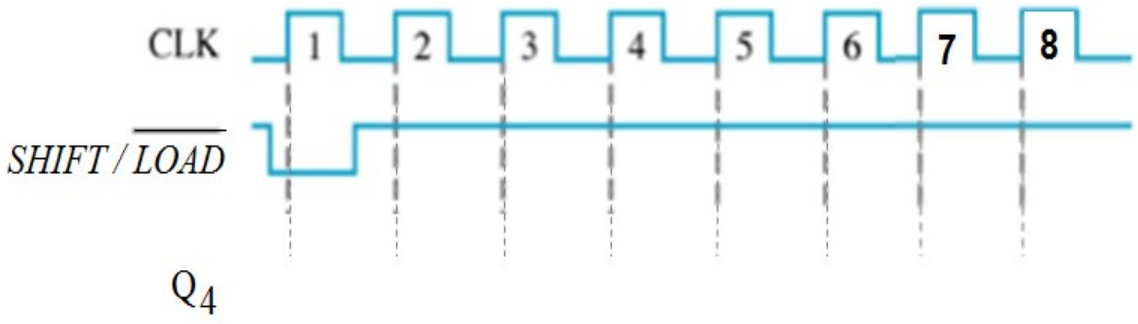


Figure 9