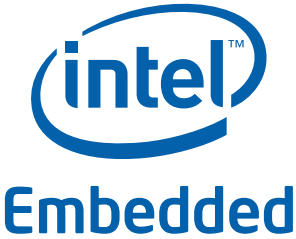

Intel® Atom™ Processor E6x5C Series

Platform Design Guide

June 2011

Intel Confidential

Revision 1.0

Document Number: 478304, Revision:1.0

Contents

Figures

Tables

Revision History

Date	Revision	Description
June 2011	1.0	Initial Public Release

Revision Number Descriptions

Revision	Associated Life Cycle Milestone	Release Information
0.0	POP L3 Closure	Initial Documentation - Typically Internal Only
0.1–0.4	When Needed	Project Dependent - Typically Internal Only
0.5	Design Win Phase	First, Required Customer Release
0.6–0.7	When Needed	Project Dependent
0.7	Simulations Complete	Second, Recommended Customer Release
0.8–0.9	When Needed	Project Dependent
1.0	First Silicon Samples	Required Customer Release
1.1–1.4	When Needed	Project Dependent (Recommended)
1.5	Qualification Silicon Samples	Project Dependent
1.6–1.9	When Needed	Project Dependent
NDA - 2.0 Public - XXXXXX-001	First SKU Launch	Required Customer Release - Product Launch
2.1 and up	When Needed	Project Dependent

Note: Rows highlighted in gray are required revisions.

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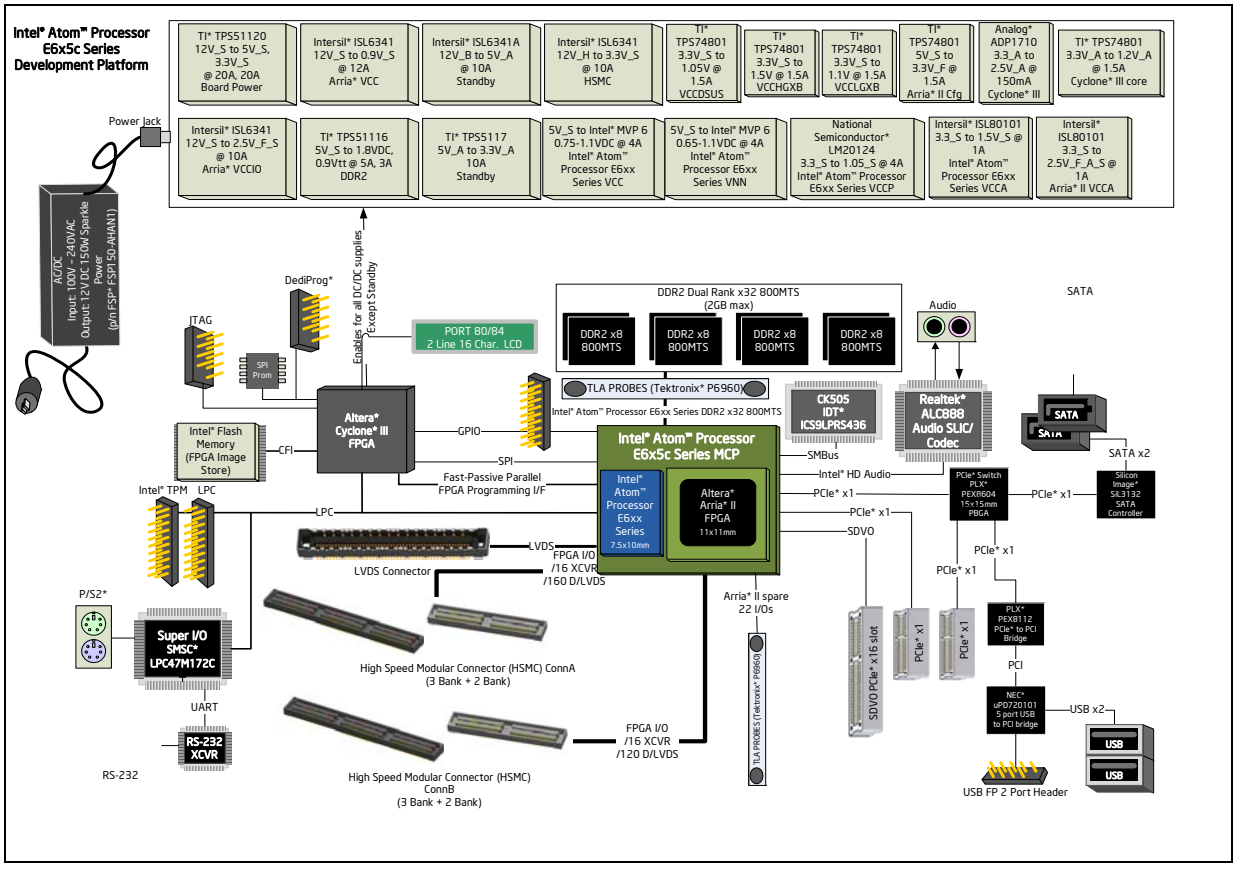
1.0 Introduction

This document provides schematic and PCB design recommendations for the Intel® Atom™ Processor E6x5C Series device used for embedded applications. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues, and the guidelines should be carefully followed.

This document applies to B0 and B1 steppings of the E6x5C device unless otherwise specifically noted.

The Intel® Atom™ Processor E6x5C Series is a muti-chip packaged (MCP) device comprising an Intel®Atom™ Processor CPU and an Altera* FPGA. Since there are essentially two independent devices within the package, this document is divided into chapters relevant to the CPU and the Altera FPGA. (e.g., there is a chapter dedicated to the power-delivery requirements of the CPU and a seperate chapter dedicated to the power delivery of the FPGA part.)

Figure 1. Fox Brook Development Platform



Note: Both metric and the U.S. customary system (USCS) of units are used throughout this design guide. If a discrepancy exists between the metric and USCS units stated, it should be assumed that USCS value is most accurate. The conversion factor used is 1 inch = 1000 mils = 25.4 mm.

1.1 Terminology

Table 1 defines the acronyms, conventions, and terminology that are used throughout this design guide.

Table 1. Conventions and Terminology (Sheet 1 of 2)

Terminology	Description
AC	Audio CODEC
ACPI	Advanced Configuration and Power Interface
BGA	Ball Grid Array
CRB	Customer Reference Board
DFM	Design For Manufacturing
DVI	Digital Video Interface
EBL	Extended Battery Life
EHCI	Enhanced Host Controller Interface
EM	Electromagnetic
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FSB	Front Side Bus, synonymous with Host Bus
FPGA	Field-programmable Gate Array
FWH	Firmware Hub
HDMI	High-definition Multimedia Interface
Intel® DPST	Intel® Display Power Saving Technology
Intel® HD Audioβ	Intel® High Definition Audioβ
Intel® MVP-6	Intel® Mobile Voltage Positioning – Generation 6
LPC	Low Pin Count
LVDS	Low Voltage Differential Signaling
MLCC	Multilayer Ceramic chip capacitors
PCIe*	PCI Express*
PWM	Pulse Width Modulation
RTC	Real Time Clock
RX	Receiver or Receive (in reference to PCI Express* differential signal pairs)
SDVO	Serial Digital Video Out
SJR	Solder Joint Reliability
SLI	Second Level Interconnect. Describes the connection between the package and the main PCB
SLIC	Standard Linear Integrated Circuit
SMBus	System Management Bus. A two-wire interface through which various system components can communicate
SPD	Serial Presence Detect
SRC	Serial Reference Clock – A differential clock pair

Table 1. Conventions and Terminology (Sheet 2 of 2)

Terminology	Description
TCO	Total Cost of Ownership
TX	Transmitter or Transmit (in reference to PCI Express* differential signal pairs)
VNA	Vector Network Analyzer

1.2 Reference Documents

Table 2. Reference Documents (Sheet 1 of 2)

Document	Document No./Location
Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)	CDI document number 461298 Note 1
Intel® Atom™ Processor E6x5C Series Datasheet	Order number 324602
Intel® Atom™ Processor E6x5C Series – Development Kit User Manual	CDI Document number 447729 Note 1
Intel® Atom™ Processor E6x5C Series – Boundary Scan Description Language (BSDL) File	CDI document number 456515 Note 1
Intel® Atom™ Processor E6x5C Series – I/O Buffer Information Specification (IBIS) Models	CDI document number 456989 Note 1
Intel® Atom™ Processor E6x5C Series – DDR2 Memory Interface – Trace Length Calculator	http://edc.intel.com/Link.aspx?id=3880
Intel® Atom™ Processor E6x5C Series – Specification Update - NDA	CDI document number 461297 Note 1
Intel® Atom™ Processor E6x5C Series Specification Update	Order number 324601
Intel® Atom™ Processor E6x5C Series Thermal Design Guide	CDI document number 447719 Note 1
RS - Intel® Atom™ Processor E6x5C Series BIOS Writer's Guide	Reference number 28971 Note 1
Fox Brook Platform – Bill of Materials (BOM) / Parts List	CDI document number 459905 Note 1
Fox Brook Platform – Customer Reference Board File	CDI document number 460266 Note 1
Fox Brook Platform – Customer Reference Board Schematic	CDI document number 447522 Note 1
Intel® Atom™ Processor E6x5C Series Symbol File	CDI document number 461023 Note 1
Power Delivery and Clock Related Documents	
CK505 Clock Synthesizer Specification – Product Specification	CDI document number 374802 Note 1
Intel® Display Power Saving Technology 5.0 and Intel® Automatic Display Brightness – Application Notes / Briefs	CDI document number 432409 Note 1
Intel® Mobile Voltage Positioning (Intel® MVP), 6 Voltage Regulation – Product Specification	CDI document number 414547 Note 1, Note 2
Extended Battery Life (EBL) Initiatives, Documents, and Utilities	
Device Driver Power and Performance White Paper	Note 1

Notes:
1. Contact your Intel Field Representative for the latest version of this document.
2. An Intel® MVP license agreement must be signed to obtain a copy of this document. Contact your Intel Field Representative for details.

Table 2. Reference Documents (Sheet 2 of 2)

Document	Document No./Location
Frequency Display Utility	Note 1
Narrow VDC Extended Battery Life (EBL) Technique Presentation	Note 1
Notebook Display Power Reduction EBL Technique	Note 1
RS - Narrow VDC EBL Technique Application Note	Note 1
WinMem 2.1.003 Register Viewing Tool	Note 1
Specifications	
Advanced Configuration and Power Interface, Version 3.0 (ACPI)	http://www.acpi.info/spec.htm
Alert Standard Format Specification, Version 1.03	http://www.dmtf.org/standards/asf
AP-728 ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	www.intel.com/Assets/PDF/appnote/292276.pdf
Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 0.96 (EHCI)	http://developer.intel.com/technology/usb/ehcispec.htm
Intel® High Definition Audio$^{\beta}$ Specification	http://www.intel.com/standards/hdaudio
RS - Serial Digital Video Out (SDVO) Port External Design Specification (EDS)	Reference number 26080 Note 1
JEDEC Standard DDR2 SDRAM Specification	http://www.jedec.org
Low Pin Count Interface Specification, Revision 1.1 (LPC)	http://developer.intel.com/design/chipsets/industry/lpc.htm
PCI Express* Card Electromechanical Specification Revision 1.0	http://www.pcisig.com/specifications
PCI Express* Specification, Revision 1.0a	http://www.pcisig.com/specifications
PCI Local Bus Specification, Revision 2.3 (PCI)	http://www.pcisig.com/specifications
PCI Mobile Design Guide, Revision 1.1	http://www.pcisig.com/specifications
PCI Standard Hot Plug Controller and Subsystem Specification Revision 1.0	http://www.pcisig.com/specifications
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
Application Notes	
Configuring the Altera* FPGA with Software on the Intel® Atom™ E6x5C Series Application Note	CDI document number 460147 Note 1
Altera* FPGA Design Software for the Intel® Atom™ E6x5C Series Application Note	CDI document number 460000 Note 1
Mapping Altera* FPGA Pins to Intel® Atom™ Processor E6x5C Series Pins Application Note	CDI document number 465465 Note 1
FPGA Documentation	
Altera Arria II Devices literature (including the Arria II GX Device Handbook)	http://www.altera.com/products/devices/arria-fpgas/arria-ii-gx/literature/aiigx-literature.jsp
Quartus II Subscription Edition Software	http://www.altera.com/products/software/quartus-ii/subscription-edition/qts-se-index.html

Notes:
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2.0 System Features

The Intel® Atom™ Processor E6x5C Series is a high-performance, ultra low power processor with several microarchitectural enhancements over existing Intel® embedded processors. The Intel® Atom™ Processor E6x5C Series is a multi-chip packaged device that consists of a low power IA CPU core (derived from the Intel® Atom™ processor) and an Altera ArriaII GX FPGA. The processor includes memory controller, 3D graphics, video decode and video encode engine, 2D display controller, SDVO and LVDS interfaces, Intel® High Definition Audio$^{\beta}$ Controller, GPIOs, SMBus, SPI interface connectivity to SPI flash, LPC, PCIe* controller, RTC, 8254 Timer and watchdog timer.

The Intel® Atom™ Processor E6x5C Series is an integrated open architecture device where users have complete flexibility over the functionality they implement in the FPGA. Users implement the FPGA functionality using the standard Altera QuartusII development tools (v10.1 & later). Users may also connect off-the-shelf PCIe IOH devices on the external PCIe ports. Figure 2 provides a diagram of the functional blocks in the E6x5C device.

Figure 2. Intel® Atom™ Processor E6x5C Series-based Platform Block Diagram

2.1 Intel® Atom™ Processor E6x5C Series System Features

- 600 MHz (Ultra Low Power SKU), 1.0 GHz (Entry SKU) and 1.3 GHz (Mainstream SKU)
- Macro-operation execution support
- 2-wide instruction decode and in-order execution
- On die, 32 kB 4-way L1 Instruction Cache and 24 kB 6-way L1 Data Cache
- On die, 512 kB, 8-way L2 cache
- L2 Dynamic Cache Sizing
- 32b physical address, 48b linear address size support
- Support for IA 32-bit architecture
- Supports Intel® Virtualization Technology for IA-32 and Intel® Architecture$^{\delta}$ (Intel® VT-x$^{\delta}$)

- Supports Intel® Hyper-Threading Technology$^{\alpha}$ (2-threads)
- Advanced power management features including Enhanced Intel SpeedStep® Technology$^{\theta}$
- Deep Power-down Technology (C6)
- Split VTT support for lowest processor power state
- Intel® Streaming SIMD Extension 2 and 3 (Intel® SSE2 and Intel® SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Supports single channel 32-bit data bus DDR2
- Supports up to 2GB of 800 MT/s memory
- Supports 1 or 2 ranks DDR2, memory down
- Integrated 2D/3D graphics engine running up to 320 MHz (ULP or entry SKUs) or 400 MHz clock (mainstream or premium SKU)
- High definition hardware video decode and video encoder engines
- LVDS display port and SDVO expansion port
- Intel® High Definition Audio$^{\beta}$ (Intel® HD Audio$^{\beta}$)
- Two external x1 PCI Express* ports which operate as independent PCIe* Gen 1 Controllers
- LPC interface
- 14 GPIO pins (5 powered by core power and turned off during sleep mode, 9 are powered by suspend power well and remained active during S3)
- SPI interface that supports boot from SPI flash (only for BIOS boot)
- Supports configurable watchdog timer
- Supports RTC that provides battery backed-up date and time keeping device.
- On-chip Altera ArriaII GX FPGA with the following features
  - Six High speed Transceivers (3.125Gbps)
  - Four Internal PLLs
  - Over 63,000 Logic elements
  - 39 DSP blocks
  - 312 Multipliers
  - 5.3 Mbits of FPGA Memory

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3.0 General Design Considerations

This chapter provides general motherboard design guidelines for the Intel® Atom™ Processor E6x5C Series-based platform. For interface-specific design guidelines, refer to the appropriate section of this document.

- The characteristic impedance (Z_0) of microstrip (external) and stripline (internal) traces is 50 Ω ± 10%. Intel's signal integrity and timing analyses assume nominal trace widths plus design and manufacturing tolerances. Customer stackups may lead to slightly narrower or wider nominal traces to meet the impedance targets used in these design guidelines.
- For all high-speed impedance-controlled signals, it is recommended to have the signals referenced to continuous ground planes and not routed over or under power/ground plane splits.
- Intel recommends that signal integrity and timing simulations be completed for any crucial signals and for any signals that deviate from these design guidelines.

3.1 General Stackup Recommendations

The Intel® Atom™ Processor E6x5C Series-based platform utilizes Type 4 PCB technology. The following general stackup recommendations apply to all interfaces and should be followed.

- Microstrip layers are assumed to be built from 0.5 ounce copper foil, plated with 1 ounce nominal. The trace thickness range defined, however, allows for significant process variance around this nominal.
- Stripline layers are assumed to be built from ½ ounce copper.
- Internal power plane layers are recommended to be 2 ounce thick copper.
- It is recommended that all high-speed signals should reference solid planes over the length of their routing and should not cross plane splits. Ground referencing is preferred.
- Reference plane stitching vias must be used in conjunction with high-speed signal layer transitions that include a reference plane change. Place at least one stitching via between the two reference planes for every four signals that transition. The stitching via should be placed within 100 mils of the signal transition via to improve signal integrity.
- Routing on external layers introduces different delays compared to internal layers. In general, interfaces that have length matching requirements also restrict routing for groups of signals to be on the same layer in order to avoid this situation.
- Customers using external layers as their main routing layer should be cautious of potential EMI issues.
- Final post-lamination, post-etching, and post-plating dimensions should be used for electrical model extractions.
- Maximize the use of copper fills on the PCB. There should be no large areas of the board without metal; widen the grounds and other power rails to fill any blank spots. Large metal fill areas improve heat conduction and allow components to run cooler. Large copper fill areas also help reduce stray resistance and inductance, and they help capture and dissipate RF energy by allowing eddy currents to flow.

3.1.1 Microstrip and Stripline Stackups

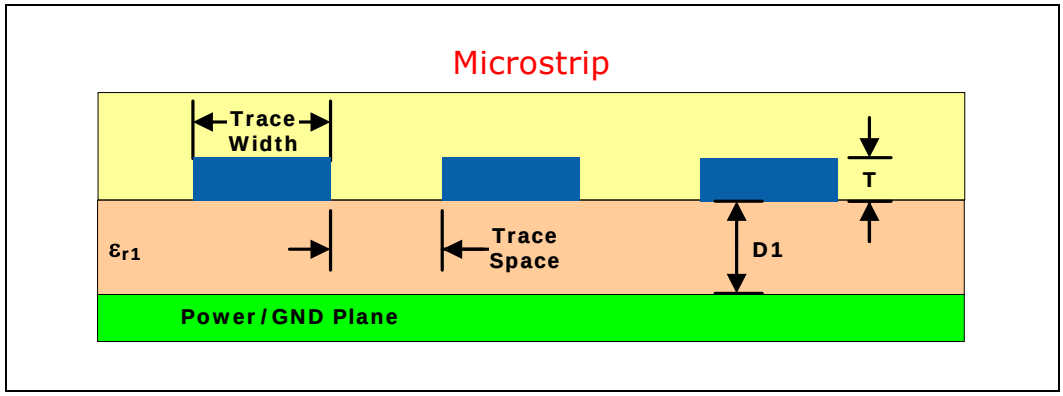
There are several layer count configurations that may be implemented on the Intel® Atom™ Processor E6x5C Series-based platform, provided the impedance specifications are met and microstrip/stripline trace geometries fall within the ranges specified in Table 3 and Table 4. Those tables list typical stackup parameters and design, material, and manufacturing tolerances assumed by Intel's simulations.

Below are general considerations for microstrip and stripline stackups:

- Design tolerances account for adjustments intentionally included in the design.
- Material tolerances account for any natural variation in the materials being used.
- Manufacturing tolerance considers variations that may occur during the manufacturing process.
- Customers may use the design tolerance values to re-center stackup impedance, but manufacturing tolerance impact must be considered when comparing their chosen stackup to the given recommendation.
- The stackup parameter value tables below apply to both generic single-ended motherboard routing and differential pair routing.
- Consider the minimum and maximum impedance of a trace based on the switching of neighboring traces, especially when calculating flight times.
- Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance.
- Using wider spaces between the traces can minimize trace-to-trace coupling and help reduce crosstalk and settling time. Follow the specific routing guidelines documented for each interface to minimize the effects of trace-to-trace coupling.

Note: The typical microstrip trace width of 4.5 mils listed in Table 3 is for the main route. Refer to individual interface sections for more details on breakout routing requirements.

Figure 3. Microstrip Diagram

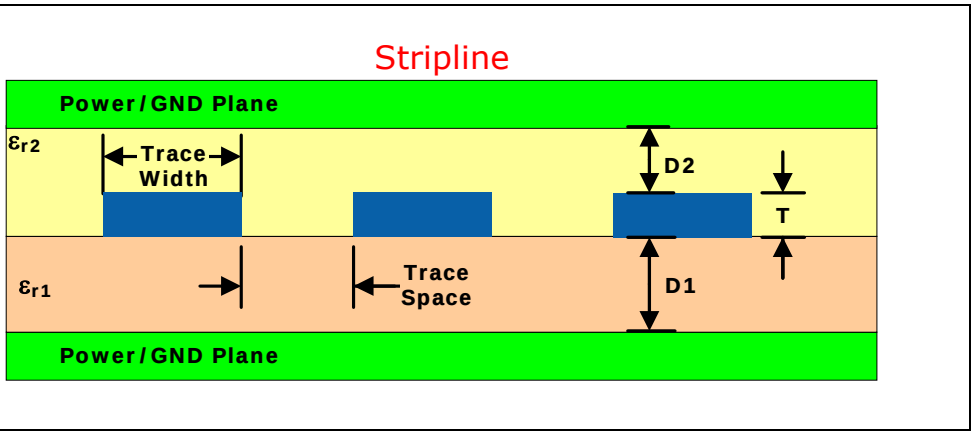


Notes:
1. The trace spacings vary from one signal group to the other. Each signal group's values are specified in their respective sections within this design guide.

Table 3. Microstrip Parameter Values

Parameter	Min	Typical	Max	Design / Materials Tolerance	Unit
ε_{r1}	n/a	4.32	n/a	n/a	
Mils					
D1	2.43	2.7	2.97	± 0.27	mil
Trace Thickness (T) (1/2 oz. + plating)	1.53	1.70	1.87	± 0.17	mil
Trace Width (W)	4.05	4.5	4.95	± 0.45	mil

Figure 4. Stripline Diagram



Notes:
1. The trace spacings vary from one signal group to the other. Each signal group's values are specified in their respective sections within this design guide.

Table 4. Stripline Parameter Values

Parameter	Min	Typical	Max	Design / Materials Tolerance	Unit
ε_{r1}	n/a	4.25	n/a	n/a	
ε_{r2}	n/a	4.30	n/a	n/a	
Mils					
D1	6.26	6.95	7.65	± 0.695	mils
D2	3.15	3.5	3.85	± 0.35	mils
Trace Thickness (T)	0.59	0.65	0.71	± 0.06	mils
Trace Width (W)	3.89	4.3	4.71	± 0.41	mils

Notes:
1. Some interfaces may specify a different nominal trace width and impedance for signal routing. Although these cases are not shown, a similar variance around the nominal trace width can be assumed.

3.1.2 Trace Impedance

3.1.2.1 Characteristic Impedance (Z_0) Targets

The trace dimension and spacing must be determined to ensure the optimal trace impedance for the given interface. Consideration must also be given to ensuring sufficient cross-talk immunity and cost effective PCB fabrication. (i.e. minimum trace widths and spacing rules must be observed while meeting desired impedance value).

Table 5. Characteristic Impedance Targets for Microstrip and Stripline Routing

PCB Stackup	Impedance Target (Z_0)	
	Microstrip	Stripline
Controlled impedance	50 Ω ± 15%	50 Ω ± 15%

3.1.2.2 Differential Impedance (Z_{DIFF}) Targets

Caution: Due to interconnect metrics (for example, loss), which are not sufficiently defined by impedance alone, it is important to maintain the geometry specifications and meet a particular differential impedance target. Any deviations in geometries beyond the tolerances defined in the following tables will invalidate the guidelines contained in this document.

Note: The nominal differential impedances do not generally fall on the exact impedance boundaries. Where differential interconnects are involved, Intel's electrical analysis utilized a tolerance of ±15% in order to compensate for the additional correlation error between the purely geometry-based implementations and those designed to the target impedance specifications.

Table 6 summarizes the routing geometries for various differential signaling interfaces on the platform. The differential impedance target for each type of routing is also specified.

Table 6. Differential Impedance Targets for Microstrip and Stripline Routing

Signal Type	Microstrip[1]			Stripline		
	Trace Width (mils)	Edge-to-edge Trace Spacing[2] (mils)	Z_{DIFF}	Trace Width (mils)	Trace Spacing (mils)	Z_{DIFF}
Mils						
Host Clock, PCLIE Clock, LVDS Clock, SDVO clock from clock chip, LVDS	3.51	6.99	100Ω ± 15%	3.76	6.24	100Ω ± 15%
SDVO, PCI Express*, SDVO clock from Intel® Atom™ Processor E6x5C Series	4.51	4.49	85Ω ± 15%	5.01	4.99	85Ω ± 15%
Millimeters						
Host Clock, PCLIE Clock, LVDS Clock, SDVO clock from clock chip, LVDS	0.089	0.178	100Ω ± 15%	0.096	0.158	100Ω ± 15%
SDVO, PCI Express*, SDVO clock from Intel® Atom™ Processor E6x5C Series	0.115	0.114	85Ω ± 15%	0.127	0.127	85Ω ± 15%

Notes:
1. For routing ease, microstrip breakout routing may have a nominal trace width of 3 mils. All other stackup parameters match the values for the main route in Table 3.
2. Breakout differential pair spacing may differ from main route spacing. Refer to individual interface sections for more specifics.

3.1.3 Signal Propagation Time-to-Distance Relationship

The routing recommendations for some high-frequency signals may include length-matching requirements (refer to Section 3.2.2). These requirements are expressed in millimeters or inches, or as a measurement of signal flight time. The correlation of flight time to trace length will depend on the specific board stackup used.

Based on the recommended stackup, the signal propagation time to distance relationship is as follows:

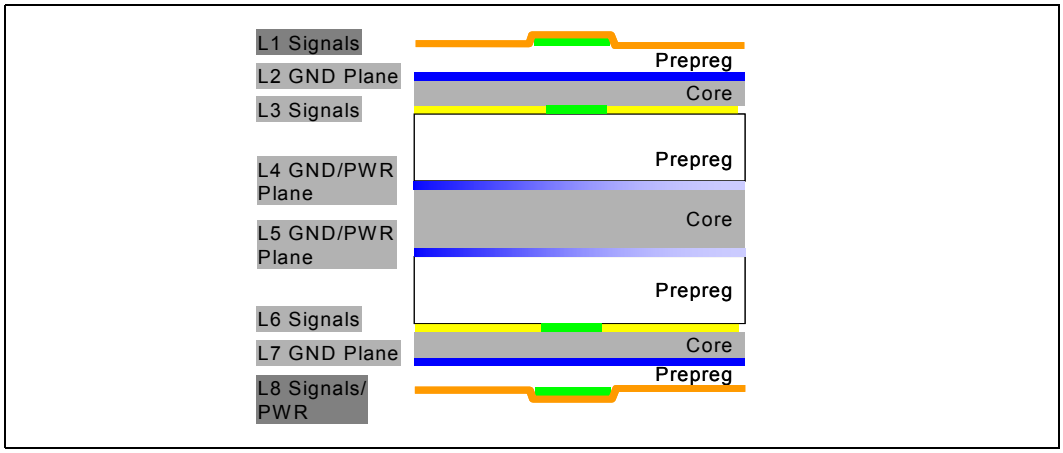
- Stripline (internal layer) Routing: 170 ps per inch
- Microstrip (external layer) Routing: 150 ps per inch

The time-to-distance relationship listed above assumes no trace coupling; design and manufacturing tolerances are also ignored. In cases that require worst-case stackup parameters and even or odd mode coupling, new extractions from the stackup model must be done to provide an accurate signal propagation time to distance relationship.

3.1.4 Generalized Motherboard Example

Figure 5 shows an example of a Type 3 PCB motherboard stackup (8 layer board, to be precise). This sample stackup is provided for illustrative purposes only.

Figure 5. Generalized Motherboard Stackup for Routing Example



The 8-layer motherboard example stackup consists of eight layers where the primary side layer (L1), Layer 3 (L3), Layer 6 (L6), and secondary side layer (L8) are used for signal routing, Layer 2 (L2), Layer 7 (L7) are solid ground planes, and Layer 4 (L4), Layer 5 (L5), and parts of Layer 8 (L8) are used for power delivery and ground floods.

To ensure impedance control, the primary and secondary side layer microstrips reference solid ground planes on Layer 2 and Layer 7, respectively. Internal signal traces on Layer 3 and Layer 6 are offset striplines. To meet the characteristic impedance target for these traces, they reference a solid ground plane on Layer 2 and Layer 7. Since the coupling to Layer 4 and Layer 5 is still significant, (especially true when thinner stackups use balanced striplines on internal layers) these layers are preferred to be converted to ground floods in the areas of the motherboard where the high-speed interfaces like the DDR2 system memory are routed. In the remaining sections of the motherboard layout, the Layer 4 and Layer 5 layers are used for power delivery. The outer layers (L1 and L8) may also be used for power delivery in many cases since they benefit from the thick plating on external layers, as well close referencing to layers 2 and 7 ground planes. The benefit of such a stackup is low inductance power delivery.

3.2 General Routing Recommendations

The following routing recommendations should be employed for robust platform signal integrity.

3.2.1 Reference Planes

Although solid ground plane references are preferred, it is possible to use a low-noise power layer as a reference plane. Proper decoupling stitching at reference plane transitions is needed to ensure return path continuity of high-frequency signals. However, this should only be considered as the secondary reference plane on internal stripline layers where a solid, continuous ground reference is already present.

3.2.2 Trace Length Equalization and Package Compensation

The internal package trace lengths of DDR2 signals are length-matched within a signal group, so PCB traces compensation is not required. The *Intel® Atom™ Processor E6x5C Series – DDR2 Memory Interface – Trace Length Calculator* can be used to aid in equalizing trace lengths on the PCB. Serpentines should maintain minimum spacing rules and not employ 90° bends.

Equalizing trace lengths can be CAD-tool-specific and is not defined here in detail.

3.3 Generic Guidance for PCB-Side Pad Design

The following guidelines are to improve mechanical robustness and solder joint reliability (SJR) of Pb-free SLI.

3.3.1 Pad Size and Shape

1. Maintain a package solder resist opening (SRO) to PCB pad size ratio of 1:1.1. Start with package side SRO size, divide it by 1.1, then round up to the next whole mil.

- For example, assuming the SRO of the processor package is 430 µm, then the PCB pad size would be:

  430 ÷ 1.1 = 390.91 µm

  390.91 µm ÷ 25.4 µm/mil =15.39 mils

  = ~15 mils

2. If SRO is not provided, the alternate method for calculating pad size is to multiply the nominal ball diameter by 0.8, and then rounding up to the nearest whole mil.

Exception: When this aspect ratio creates a routing restriction on the PCB, the pad diameter can be calculated using a ratio of 1.2 (instead of 1.1). The above exception is not applicable to the 3 ball locations at each of the package corners (for a total of 11 ball locations). Also, the exception can not be used under die-shadow region.

3.3.2 Pad Type

Selection of a pad type for a given solder ball depends on several factors: the ball's criticality to function, the type of expected mechanical stress, and use of board-level adhesives. In general, metal defined pads perform well in temperature cycling stress tests, while solder mask defined pads perform better in shock testing and mechanical performance.

3.3.3 Silk-Screen Guidance

Uniquely identify pin 1 location with component installed. Component outline need not be visible with component installed. Keep silk-screen a minimum of 0.010 inch from pads.

3.4 Via Guidelines

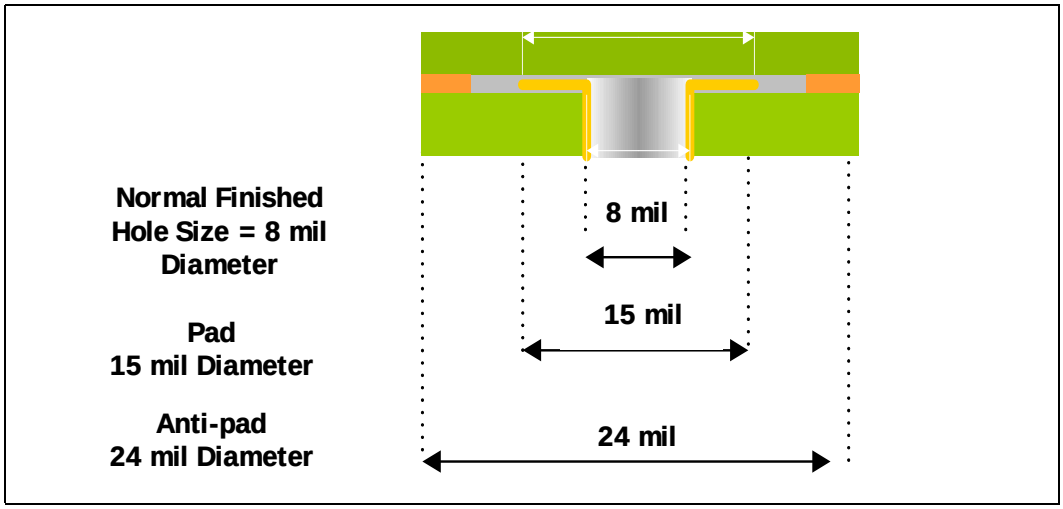
The following sections discuss the proper via drill, pad, and anti-pad sizes, as well as via spacing required to provide continuous return paths and uniform power distribution.

Warning: Improper selection of drill size, pad size, and anti-pad sizes, can adversely affect the cost of motherboard, reliability, manufacturability, as well as electrical efficiency.

Type 3 PCB technology uses plated through-hole (PTH) vias for breakout routing. Because PTH vias are used in less space-constrained areas outside the BGA field, the dimensions of PTH vias may vary depending on need.

Figure 6 shows the cross section of a typical PTH via.

Figure 6. PTH Via Dimensions



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4.0 System Memory Design Guidelines

4.1 Chapter Contents

This chapter contains information about:

- DDR2 System Memory Controller
- Intel® Atom™ Processor E6x5C Series DDR2 Signal Groups
- Supported Memory Configurations
- Overview and Design Considerations
- DDR2 Topology and Layout Design Guidelines
- SDRAM Considerations
- Compensation Requirements

4.2 DDR2 System Memory Controller

The Intel® Atom™ Processor E6x5C Series integrates a single-channel DDR2 system memory controller with a single, 32-bit wide data bus. The memory controller buffers support the SSTL_18 (1.8 V) logic switching ranges. The memory controller interface is fully configurable through a set of control registers.

4.3 Intel® Atom™ Processor E6x5C Series DDR2 Signal Groups

Table 7 summarizes the different signal groupings of the DDR2 interface. See *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for more details on specific pin functionality.

Table 7. Intel® Atom™ Processor E6x5C Series DDR2 Signal Groups (Sheet 1 of 2)

Signal Name	Description
Data Signal Group	
M_DQ[31:0]	Data bus
M_DQS[3:0]	Data strobes
M_DM[3:0]	Data mask
Command Signal Group	
M_RASB	Row address strobe
M_CASB	Column address strobe
M_WEB	Write enable
M_BS[2:0]	Bank select
M_MA[14:0]	Memory address bus
Clock Signal Group	
M_CKP, M_CKN	Differential DDR2 clock
Control Signal Group	
M_CSB[1:0]	Chip select (1 per rank)
M_CKE[1:0]	Clock enable (1 per rank)
M_ODT[1:0]	On-die Termination Enable (1 per rank)

Table 7. Intel® Atom™ Processor E6x5C Series DDR2 Signal Groups (Sheet 2 of 2)

Signal Name	Description
Feedback Signal Group	
M_RCVENIN	Receive enable in
M_RCVENOUT	Receive enable out
Self-refresh Signal	
M_SRFWEN	S3 Firewall self-refresh enable
Compensation Signals	
M_RCOMPOUT	System memory RCOMP

4.4 Supported Memory Configurations

The Intel® Atom™ Processor E6x5C Series single DDR2 channel supports up to 2 GB of 800 MT/s data rates and in one-rank or dual-rank configuration. The guidelines in this chapter support the memory configurations listed in Table 8.

Table 8. Memory Configurations Supported on Intel® Atom™ Processor E6x5C Series

Total System Memory Size and Technology	Topology	Ranks	Memory Down Device Placement	Memory Device Width
128 MB/256 MB/512 MB/ 1 GB/2 GB DDR2	Memory Down on PCB	One/Two	4 Top + 4 Bottom / 2 Top + 2 Bottom / 1 Top + 1 Bottom / 2 Top / 2 Bottom	x8 or x16

Notes:
1. M_CKP/M_CKN, M_CS[0], and M_CKE[0] will be used in single memory rank configuration.
2. M_CKP/M_CKN, M_CSB[1:0], and M_CKE[1:0] will be used in dual memory rank configuration.
3. Configuration of 8 x 1 Gbit DDR2 Memory, 4 Top + 4 Bottom memory down device placement and x8 mode memory device width are CRB and PDG design reference. The rest of the memory considerations should be re-verified through simulation.
4. If M_CSB[1] and M_CKE[1] are unused, they can be left unconnected.

4.5 Overview and Design Considerations

There are two kinds of length constraints placed on each signal group within the DDR2 interface:

- **Absolute length**: These constraints define the length range over which the signals will meet signal integrity rules.
- **Length matching**: These constraints define the length matching range over which the signals will meet signal integrity rules.

Intel recommends following a preliminary test route to establish the natural bounds on all signal groups. This route defines the target lengths for each signal group, and will provide an acceptable solution space when the length matching formulas are applied.

The control group should be routed as short as possible. Once the control group lengths are defined, the target clock length should be minimized while ensuring the control group length matching requirements are still met.

Unless otherwise specified, assume the nominal characteristic impedances specified in Section 3.1.2.1 apply to all DDR2 signal groups.

4.5.1 Length Matching

All signal groups are length matched to the DDR2 clocks/strobes, with the clocks themselves being length tuned to a fixed length across the SDRAM devices. Each signal group has unique length matching requirements and variances.

4.5.2 Optimizing Memory Signal Integrity

For all configurations in Table 8, the following list of recommendations should be followed:

- Branch topologies benefit when the length of each branch is as short as possible and equal to other branches.
- All branch segments should be on the same layer. For example, if there are four L4 segments, then all L4 segments should be within the range specified in routing guidelines and on the same layer.
- If surface mount components are needed (such as a series resistor) for stripline traces, the signal should return to the same internal layer after completing the short external layer route.

  Transition layer segment length should be minimized. See Section 3.2.2.
- For optimal signal integrity and adequate timing margins, have a continuous reference return plane, preferably ground, above and below the routing layer.
- To ease routing of the data signal group in certain layouts, bit-swapping may be used within a byte lane. See Section 4.7.2.
- Exceptions to the trace width and spacing geometries are allowed in the breakout region in order to fan out the interconnect pattern. Reduced spacing should be avoided as much as possible.

4.5.2.1 Stack-up and Layer Utilization

The guidelines in this chapter are targeted for platforms that use the stack-up dimensions outlined in Section 3.1.

While other stack-ups and layer utilization schemes are possible, ensure that the impedance, velocity, and coupling assumptions used in verifying the signal integrity and timing of the interface are not compromised.

When multiple layers are used, individual byte lanes should be routed as a group on the same layer.

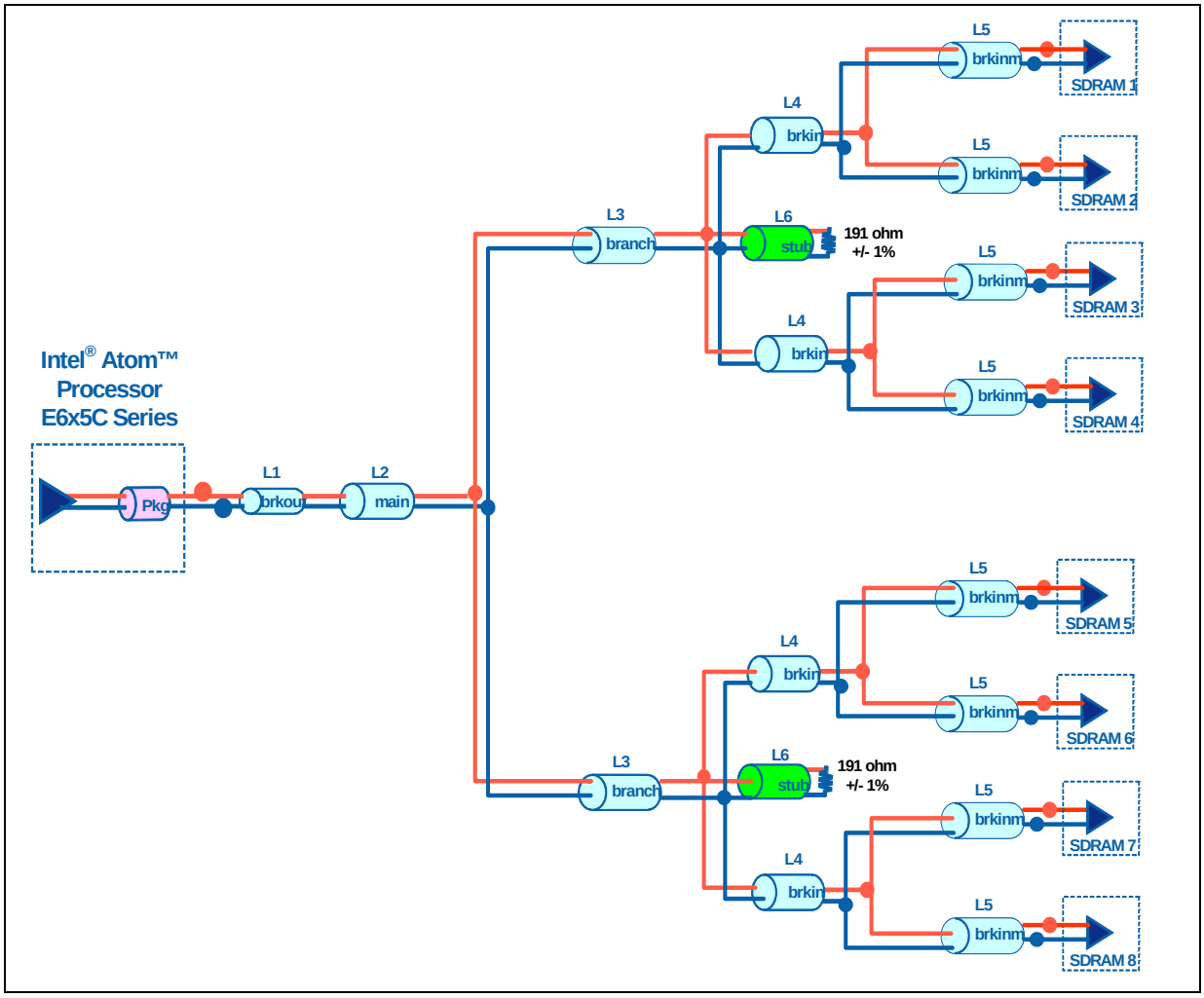
4.6 DDR2 Topology and Layout Design Guidelines

The guidelines in the following sub-sections relate to the 2-rank, 4-top +4-bottom configuration that has been implemented on the E6x5C development platform. It is recommended that other configurations be simulated by customers.

4.6.1 Clock Signals: M_CKP, M_CKN

The minimum spacing to other non-CLK DDR2 signals and non-DDR2 signals is 25 mils (0.635 mm), unless specified otherwise. The minimum spacing in breakout region to any signal is 5.5 mils (0.1397 mm) and the minimum spacing in breakin region to any signal is 5.5 mils (0.1397 mm). A maximum of 5 vias per path from Intel® Atom™ Processor E6x5C Series to the memory devices should be used for layer changes. A 191 Ω ± 1% resistor is recommended between L3 and L4 segments.

Figure 7. Clock Signal Routing Topology (4 Top + 4 Bottom)



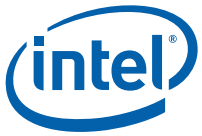


Table 9. DDR2 Clock Routing Guidelines (4 Top + 4 Bottom)

Segment	Description	Trace Width	Trace Space (Intra-spacing)	Trace Length	Target Differential Impedance
L1	Stripline breakout[2]	3.76 mils	6.24 mils	0.10 in. (100 mils)	100 Ω ±15%
L2	Stripline	5.51 mils	4.49 mils	0.10–0.70 in. (100–700 mils)	80 Ω ±15%
L3	Stripline	5.51 mils	4.49 mils	1.20–1.40 in. (1200–1400 mils)	80 Ω ±15%
L4[4]	Stripline breakin	5.51 mils	4.49 mils	0.25–0.40 in. (250–400 mils)	80 Ω ±15%
L5[4]	Stripline breakin	5.51 mils	4.49 mils	0.20–0.35 in. (200–350 mils)	80 Ω ±15%
L6	Microstrip	5.5 mils	4.5 mils	0.03–0.05 in. (30–50 mils)	80 Ω ±15%
Total	L1+L2+L3+L4+L5			2.00–2.60 in. max (2000–2600 mils max)	

Notes:
1. A short Microstrip routing (less than 0.025 in.) is allowed.
2. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan out the interconnect pattern and in the breakin region when going into SDRAM devices, as long as the targeted differential impedance is met. Reduced spacing should be avoided as much as possible.
3. Clocks must be ≥ 5.5 mils (0.1397 mm) away from other DDR2 signals within the breakout and breakin regions.
4. 0.55 in < L4 + L5 < 0.65 in
5. It is not mandatory to compensate the package mismatch in the motherboard

4.6.1.1 DDR2 Clock Length Matching

The following length matching requirements apply to the topologies depicted in Figure 7:

- Each segment length must be matched within ±10 mils of every other segment length in the topology for the same signal.
- For each routing segment, M_CKP must be within ±10 mils of its complement (M_CKN).

4.6.2 Command and Address Signals: M_RASB, M_CASB, M_WEB, M_BS[2:0], M_MA[14:0]

The minimum spacing between DDR2 Command and Address signals and other DDR2 signals is 10.6 mils (0.269 mm), and the minimum spacing to non-DDR2 signals is 25 mils (0.635 mm), unless specified otherwise. The minimum spacing in breakout region to any signal is 3.6 mils (0.091 mm) and the minimum spacing in breakin region to any signal is 5.6 mils (0.142 mm), unless specified otherwise. A maximum of 5 vias per path from Intel® Atom™ Processor E6x5C Series to memory devices should be used for layer changes.

Figure 8. Command and Address Signal Routing Topology (4 Top + 4 Bottom)

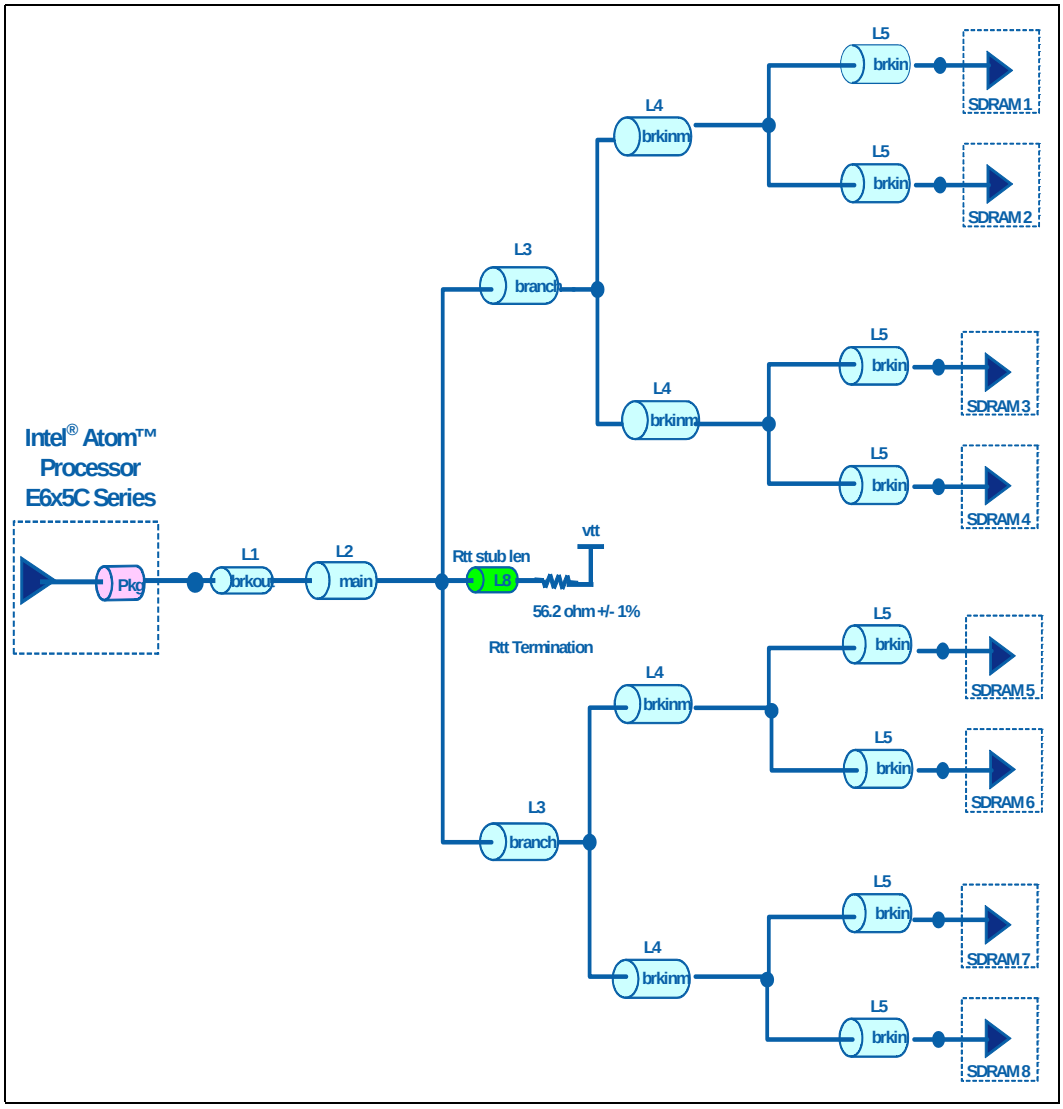


Table 10. DDR2 Command and Address Routing Guidelines (4 Top + 4 Bottom)

Segment	Description	Trace Width	Trace Spacing	Maximum Length	Target Impedance
L1	Stripline breakout[2]	3.5 mils	3.5 mils	0.25 in. (250 mils)	55 Ω ±10%
L2	Stripline	5.3 mils	10.6 mils	0.10–2.75 in. (100–2750 mils)	45 Ω ±10%
L3	Stripline	5.3 mils	10.6 mils	0.05–1.50 in. (50–1500 mils)	45 Ω ±10%
L4	Stripline	5.3 mils	10.6 mils	0.05–0.65 in. (50–650 mils)	45 Ω ±10%
L5	Microstrip breakin	5.3 mils	5.3 mils	0.05–0.20 in. (50–200 mils)	45 Ω ±15%
L6	Microstrip	5.3 mils	5.3 mils	0.01–0.10 in. (10–100 mils)	45 Ω ±15%
Total	L1+L2+L3+L4+L5			2.00–3.00 in. max (2000–3000 mils max)	

Notes:
1. A short Microstrip routing (less than 0.025 in.) is allowed.
2. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan out the interconnect pattern and in the breakin region when going into SDRAM devices, as long as the targeted differential impedance is met. Reduced spacing should be avoided as much as possible.
3. *The actual width and spacing may vary from the above table to meet the targeted impedance depending on the manufacturing process used.* The actual width and spacing ratio should be at least at 1:2, except breakin and breakout region at 1:1.
4. It is not mandatory to compensate the package mismatch in the motherboard

4.6.2.1 DDR2 Command and Address Length Matching

The following length matching requirements apply to the topology depicted in Figure 8:

- Each L3 segment in the topology must be matched with (max length L3 - min length L3) < = 100 mils
- Each L4 segment in the topology must be matched with (max length L4 - min length L4) < = 200 mils
- Each L5 segment in the topology must be matched with (max length L5 - min length L5) < = 100 mils
- Command and Address signals lengths must be less than or equal to CLK + 0.5 in. and greater than or equal to CLK - 0.5 in. CLK means M_CKP and M_CKN.

4.6.3 Data Signals: M_DQ[31:0], M_DQS[3:0], M_DM[3:0]

The data group signals are source synchronous signals. Each group has its own data signals, data mask signal, and data strobe signal.

Table 11. The Data and Data Strobe Signals Matching

Data Strobe	Data Mask	Data Bus
M_DQS0	M_DM0	M_DQ[0:7]
M_DQS1	M_DM1	M_DQ[8:15]
M_DQS2	M_DM2	M_DQ[16:23]
M_DQS3	M_DM3	M_DQ[24:31]

The minimum spacing between DDR2 DQ signals and other DDR2 signals is 10.6 mils (0.269 mm), and the minimum spacing to non-DDR2 signals is 25 mils (0.635 mm), unless specified otherwise. The minimum spacing in the breakout region (from the Intel® Atom™ Processor E6x5C Series) to any signal is 3.5 mils (0.089 mm), and the minimum spacing in the breakin region (to the SDRAM device) to any signal is 5.3 mils (0.135 mm).

The minimum spacing between DDR2 DQS signals and other DDR2 signals is 15.9 mils (0.404 mm), and the minimum spacing to non-DDR2 signals is 25 mils (0.635 mm), unless specified otherwise. The minimum spacing in the breakout region (from the Intel® Atom™ Processor E6x5C Series) to any signal is 3.5 mils (0.089 mm), and the minimum spacing in the breakin region (to the SDRAM device) to any signal is 5.3 mils (0.135 mm).

A maximum of 3 vias should be used for layer changes over the entire DQ and DQS signal route from the Intel® Atom™ Processor E6x5C Series pin to SDRAM pin.

Figure 9. Data/Data Strobe Signal Routing (Dual Rank)

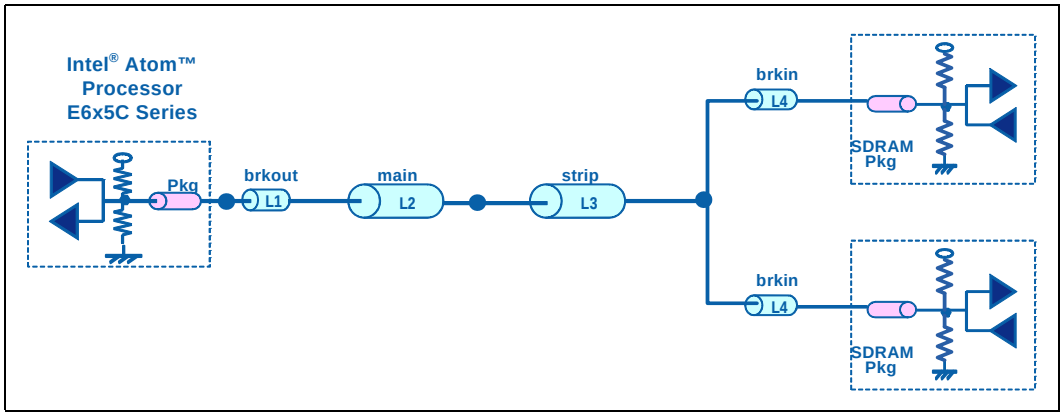


Table 12. DDR2 Strobe Routing Guidelines

Segment	Description	Trace Width	Trace Spacing	Trace Length	Target Differential Impedance
L1	Microstrip breakout[1]	3.5 mils	3.5 mils	0.15 in. (150 mils)	55 Ω ±15%
L2	Microstrip	5.5 mils	16.5 mils	0.05–2.50 in. (50–2500 mils)	45 Ω ±15%
L3	Stripline	5.3 mils	15.9 mils	0.35–0.42 in. (350–420 mils)	45 Ω ±10%
L4	Microstrip breakin	5.5 mils	5.5 mils	0.10–0.16 in. (100–160 mils)	45 Ω ±15%
Total	L1+L2+L3+L4			2.25–2.85 in. max (2250–2850 mils max)	

Notes:

1. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan out the interconnect pattern and in the breakin region when going into SDRAM devices, as long as the targeted differential impedance is met. Reduced spacing should be avoided as much as possible.
2. *The actual width and spacing may vary from the above table to meet the targeted impedance depending on the manufacturing process used.* The actual width and spacing ratio should be at least at 1:3, except breakin and breakout region at 1:1.
3. It is not mandatory to compensate the package mismatch in the motherboard.
4. Motherboard termination is not required for any of the data group signals. The termination for these source synchronous signals is located and handled on the DDR2 SDRAM devices, the On-Die Termination (ODT).

Table 13. DDR2 Data Routing Guidelines

Segment	Description	Trace Width	Trace Spacing	Trace Length	Target Differential Impedance
L1	Microstrip breakout[1]	3.5 mils	3.5 mils	0.25 in. (250 mils)	55 Ω ±15%
L2	Microstrip	5.5 mils	11.0 mils	0.05–2.50 in. (50–2500 mils)	45 Ω ±15%
L3	Stripline	5.3 mils	10.6 mils	0.40–0.65 in. (400–650 mils)	45 Ω ±10%
L4	Microstrip breakin	5.5 mils	5.5 mils	0.10–0.25 in. (100–250 mils)	45 Ω ±15%
Total	L1+L2+L3+L4			2.25–2.85 in. max (2250–2850 mils max)	

Notes:
1. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan out the interconnect pattern and in the breakin region when going into SDRAM devices, as long as the targeted differential impedance is met. Reduced spacing should be avoided as much as possible.
2. *The actual width and spacing may vary from the above table to meet the targeted impedance depending on the manufacturing process used.* The actual width and spacing ratio should be at least at 1:2, except breakin and breakout region at 1:1.
3. It is not mandatory to compensate the package mismatch in the motherboard.
4. Motherboard termination is not required for any of the data group signals. The termination for these source synchronous signals is located and handled on the DDR2 SDRAM devices, the On-Die Termination (ODT).

4.6.3.1 DDR2 DQ and DQS Length Matching

The total length for DQ and DQS for each byte group is summarized below:

- The total length of DQ within the byte group must be greater than or equal to DQS - 0.1 in., and must be less than or equal to DQS + 0.1 in.
- The total length of DQS of each byte group must be greater than or equal to CLK + 0.15 in., and must be less than or equal to CLK + 0.5 in.

4.6.4 Control Signal: M_CSB[1:0], M_CKE[1:0], M_ODT[1:0]

The minimum spacing to other non-control DDR2 signals is 11.2 mils (0.284 mm), and the minimum spacing to non-DDR2 signals is 25 mils (0.635 mm), unless specified otherwise. The minimum spacing in the breakout region (from the Intel® Atom™ Processor E6x5C Series) to any signal is 3.5 mils (0.089 mm), and the minimum spacing in the breakin region (to the SDRAM device) to any signal is 5.5 mils (0.140 mm). A maximum of 5 vias should be used for layer changes over the entire route from the Intel® Atom™ Processor E6x5C Series pin to SDRAM pin.

Figure 10. Control Signal Routing Topology (4 Top + 4 Bottom)

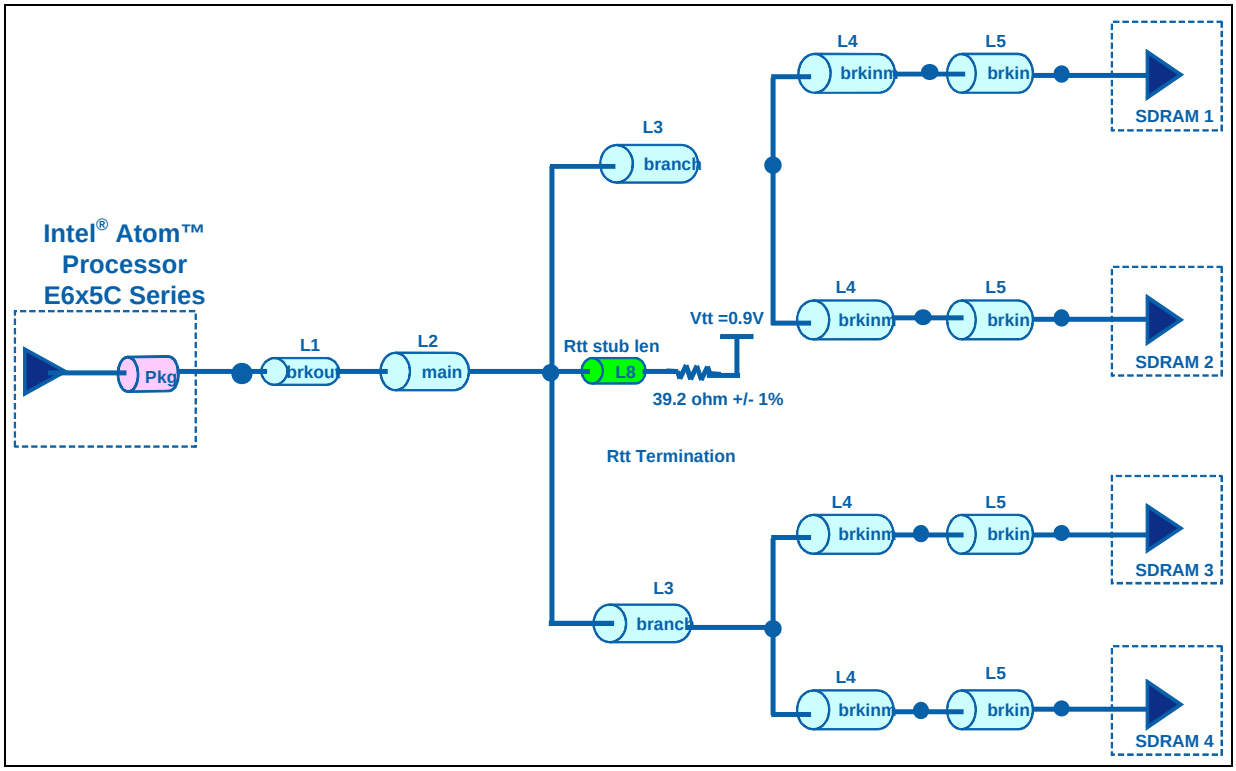


Table 14. DDR2 Control Routing Guidelines (4 Top + 4 Bottom) (Sheet 1 of 2)

Segment	Description	Trace Width	Trace Spacing	Trace Length	Target Differential Impedance
L1	Stripline breakout[2]	3.5 mils	3.5 mils	0.25 in. (250 mils)	55 Ω ±10%
L2	Stripline	5.3 mils	10.6 mils	0.10–2.00 in. (100–2000 mils)	45 Ω ±10%
L3	Stripline	5.3 mils	10.6 mils	0.05–1.50 in. (50–1500 mils)	45 Ω ±10%
L4	Stripline[3]	5.3 mils	10.6 mils	0.05–0.60 in. (50–600 mils)	45 Ω ±10%
L5	Microstrip breakin[3]	5.5 mils	5.5 mils	0.05–0.25 in. (50–250 mils)	45 Ω ±15%
L6	Microstrip	5.5 mils	10.6 mils	0.01–0.10 in. (10–100 mils)	45 Ω ±15%

Notes:
1. A short Microstrip routing (less than 0.025 in.) is allowed.
2. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan out the interconnect pattern and in the breakin region when going into SDRAM devices, as long as the targeted differential impedance is met. Reduced spacing should be avoided as much as possible.
3. L4 + L5 < 0.63 in.
4. *The actual width and spacing may vary from the above table to meet the targeted impedance depending on the manufacturing process used.* The actual width and spacing ratio should be at least at 1:2, except breakin and breakout region at 1:1.
5. It is not mandatory to compensate the package mismatch in the motherboard.

Table 14. DDR2 Control Routing Guidelines (4 Top + 4 Bottom) (Sheet 2 of 2)

Segment	Description	Trace Width	Trace Spacing	Trace Length	Target Differential Impedance
Total	L1+L2+L3+L4+L5			2.00–2.75 in. max (2000–2750 mils max)	

Notes:
1. A short Microstrip routing (less than 0.025 in.) is allowed.
2. Exceptions to the trace width and spacing geometries are allowed in the breakout region to fan out the interconnect pattern and in the breakin region when going into SDRAM devices, as long as the targeted differential impedance is met. Reduced spacing should be avoided as much as possible.
3. L4 + L5 < 0.63 in.
4. *The actual width and spacing may vary from the above table to meet the targeted impedance depending on the manufacturing process used.* The actual width and spacing ratio should be at least at 1:2, except breakin and breakout region at 1:1.
5. It is not mandatory to compensate the package mismatch in the motherboard.

4.6.4.1 DDR2 Control Length Matching

The following length matching requirements apply to the topology depicted in Figure 10:

- Each L3 segment in the topology must be matched with (max length L3 - min length L3) < = 100 mils
- Each L4 segment in the topology must be matched with (max length L4 - min length L4) < = 200 mils
- The total length of Control signal must be greater than or equal to CLK - 0.50 in., and must be less than or equal to CLK + 0.15 in.

4.7 SDRAM Considerations

4.7.1 SDRAM DQS# Signals

The Intel® Atom™ Processor E6x5C Series does not employ the use of differential strobes on the DDR2 interface. All DQS# signals on the SDRAM devices may be tied together and connected to ground using a 150-Ω pull-down resistor, but please confirm with your SDRAM vendor. The signals may alternatively be tied directly to ground at the SDRAM device with SDRAM vendor approval.

4.7.1.1 Feedback Signals: M_RCVENIN, M_RCVENOUT

The M_RCVENIN and M_RCVENOUT signals are used by the Intel® Atom™ Processor E6x5C Series for timing purposes during source synchronous read operations. There are no routing rules; they are required to be shorted under the package.

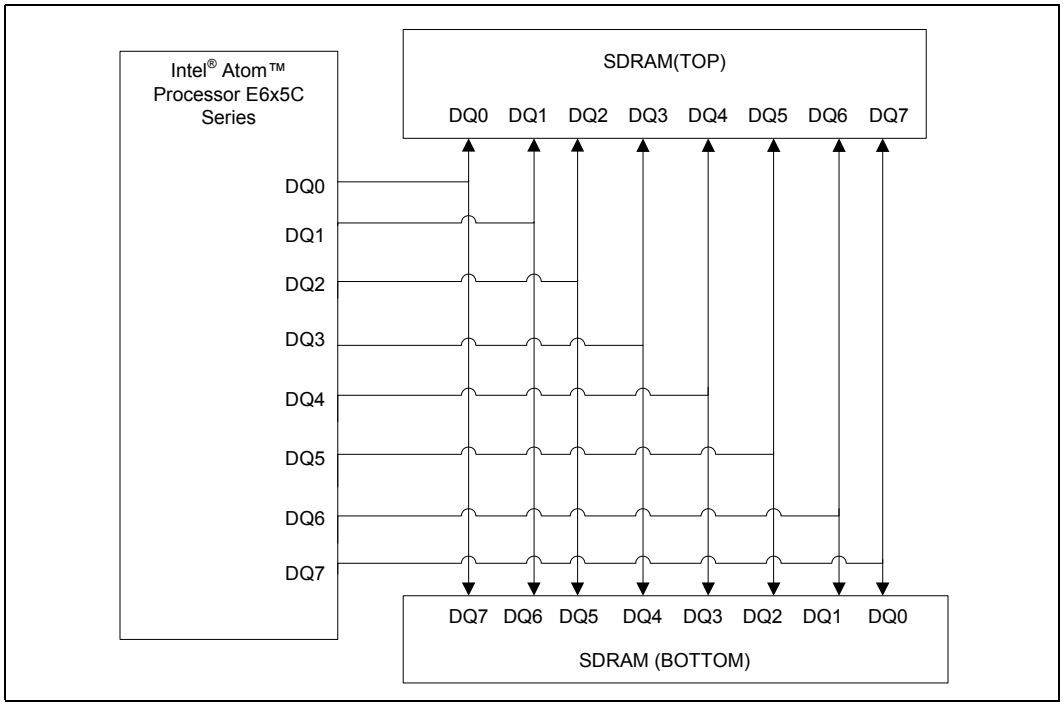
4.7.1.2 Self Refresh Signal: M_SRFWEN

The M_SRFWEN signal is used by the Intel® Atom™ Processor E6x5C Series to enable the DDR go into self refresh mode. This signal is routed using 50 Ω trace impedance. For the current CRB design, this signal should be connected to 10 KΩ ± 1% pull-up to V1P8.

4.7.2 Bit-swapping

DQ bit-swapping within a byte lane is allowed to the memory-down SDRAM components. Bit-swapping works best for the memory-down configurations that use a total of eight components with four on top and four on bottom, as these configurations may be difficult to length match. Figure 11 shows an example of DQ bit-swapping topology.

Figure 11. DQ Bit-Swapping Topology



Note: This topology is not used on Little Bay or any of Intel® Atom™ Processor E6x5C Series-based platforms. This is just an example of DQ bit-swapping topology and it is not validated.

4.8 Compensation Requirements

M_RCOMPOUT is used to dynamically calibrate the Intel® Atom™ Processor E6x5C Series DDR2 drive strengths. Connect M_RCOMPOUT to a 49.9 Ω ± 1% pull-down to V_{SS}. Recommend route the signal as microstrip, with a maximum length of 500 mils (12.7 mm) and minimized DC resistance. The signal should be routed ground referenced.

§ §

5.0 Display Subsystem

5.1 Chapter Contents

This chapter contains information about the LVDS and SDVO display ports in the Intel® Atom™ Processor E6x5C Series.

5.2 Overview

The Intel® Atom™ Processor E6x5C Series contains two display ports:

- Low Voltage Differential Signaling (LVDS)
- Serial Digital Video Out (SDVO)

5.3 LVDS Interface

The LVDS (Low Voltage Differential Signaling) transmitter serializer converts up to 24 bits of parallel digital RGB data, along with up to 3 bits for control (HSYNC, VSYNC, and DE) into one, single channel serial-bit stream for output by the LVDS Transmitter.

The transmitter is fully differential and utilizes a current mode drive with a high impedance output. The drive current develops a differential swing in the range of 250-450 mV across a 100-Ω termination load.

With data cycle times as small as 1.8 ns, propagation delay mismatch is critical, in such a way that intra-pair skew (skew between the inverting and non-inverting output) must be kept to a minimum.

5.3.1 LVDS Interface Signals

Table 15. LVDS Interface Signals

Signal Name	Direction/Type	Description
Data Signal Group		
LVD_DATAN[3:0]	O LVDS	Differential Data Output (Negative)
LVD_DATAP[3:0]	O LVDS	Differential Data Output (Positive)
Clock Signal Group		
LVD_CLKN	O LVDS	Differential Clock Output (Negative)
LVD_CLKP	I/O LVDS	Differential Clock Output (Positive)
Voltage Signal Group		
LVD_IBG	I Analog	External Current Reference: Connected to high-precision (1% or less) 2.43K Ω resistor on the motherboard to V_{SS}.
LVD_VBG	I Analog	External Voltage Reference: Requires external 1.25 V ±1.5% supply.
LVD_VREFL	I Analog	VREFL: Needed for analog loop back.
LVD_VREFH	I Analog	VREFH: Needed for analog loop back.

5.3.2 LVDS Routing Guidelines

The LVDS interface should be routed as differential stripline pairs following the general guidelines below:

- LVDS signals should be ground-referenced.
- Clock and data groups should be routed on the same layer for both breakout and main route to minimize skew.
- Isolate all other signals from the LVDS signals with spacing of 20mils to prevent coupling from other sources onto the LVDS lines.
- Use controlled impedance traces that match the differential impedance of your transmission medium and termination resistor.

When choosing cables, it is important to remember to apply the following:

- Use controlled impedance cables that target 100 Ω ± 15%. Cables should not introduce major impedance discontinuities that cause signal reflections.
- The maximum supported cable length is 24 inches.

5.3.2.1 Length Matching

LVDS signals must be length-matched to minimize skew and achieve proper operation of the interface. Observe the following length matching guidelines:

- Each LVDS signal (data, control, and clocks) should be length matched to within ± 5 mils of the other LVDS signal within the same pair and ± 20 mils of other LVDS differential pair signals. This includes data-to-data, clock-to-clock, and clock-to-data relationships.

5.3.3 LVDS Point-to-point Topology

The below routing guidelines are also applicable to single board design (without a COM Express* connector).

Figure 12. LVDS Signal Routing Topology

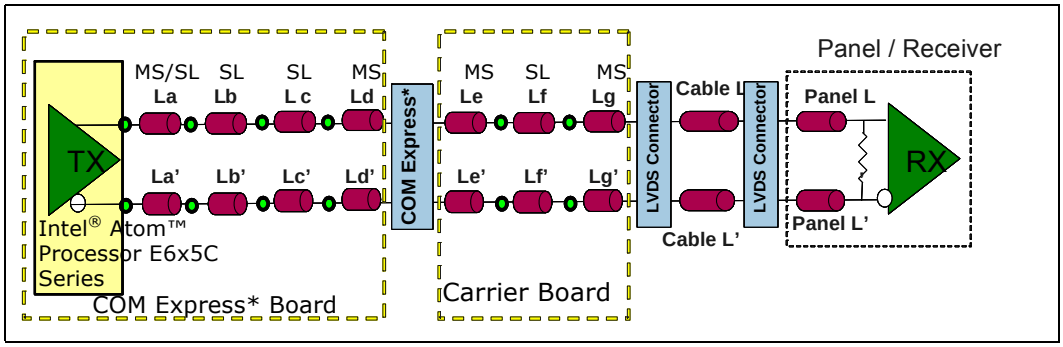


Table 16. LVDS Routing Guidelines

Segment	Description	Trace Width	Trace Space	Trace Length	Differential Impedance
La/La'	Breakout (microstrip/stripline)	3.51/ 3.76 mils	6.99/ 6.24 mils	0.75 in. (max)	100 Ω ± 15%
Lb/Lb'	Main (stripline)	3.76 mils	6.24 mils	0.1 - 2.25 in.	100 Ω ± 15%
Lc/Lc'	Main (stripline)	3.76 mils	6.24 mils	0.1 - 2.25 in.	100 Ω ± 15%
Ld/Ld'	Breakin (microstrip)	3.51 mils	6.99 mils	0.75 in. (max)	100 Ω ± 15%
Le/Le'	Breakout (microstrip)	3.51 mils	6.99 mils	2.5 in. (max)	100 Ω ± 15%
Lf/Lf'	Main (stripline)	3.76 mils	6.24 mils	0.1 - 5.0 in.	100 Ω ± 15%
Lg/Lg'	Breakin (microstrip)	3.51 mils	6.99 mils	1 in. (max)	100 Ω ± 15%
Total	La + Lb + Lc + Ld + Le + Lf + Lg / La' + Lb' + Lc' + Ld' + Le' + Lf' + Lg'			12 in. (max)	

Notes:
1. The maximum vias supported on COM Express* is 4.
2. The maximum vias supported on the Carrier board is 2.
3. The total of Le/Le' + Lf/Lf' + Lg/Lg' < 6.0 in.
4. These routing guidelines are applicable to a single board design where the total trace length is still 12 in. (max). For this case, Ld/Ld' and Le/Le' can be removed.

5.3.4 LVDS Interface Disable Guidelines

Table 17 shows the recommended connections when internal graphics LVDS is unused.

Table 17. Disable LVDS Graphics Connection Recommendations

Signal Name	Recommended Connection
LVD_VREFH	Tie to GND
LVD_VREFL	Tie to GND
LVD_IBG	Tie to GND
LVD_VBG	Connect to V1P25_S voltage rail.
LVD_CLKP	NC
LVD_CLKN	NC
LVD_DATAP_0	NC
LVD_DATAP_1	NC
LVD_DATAP_2	NC
LVD_DATAP_3	NC
LVD_DATAN_0	NC
LVD_DATAN_1	NC
LVD_DATAN_2	NC
LVD_DATAN_3	NC
VCCD180	Tie to V1P8_S
VCCA180	Tie to V1P8_S

Notes:
1. Refer to the *RS - Intel® Atom™ Processor E6x5C Series BIOS Writer's Guide* PCI Function Disables section for BIOS considerations when disabling the internal graphics.

5.4 Serial Digital Video Out (SDVO) Interface

The Intel® Atom™ Processor E6x5C Series's single Serial Digital Video Out (SDVO) port interface represents significant enhancements over the Digital Video Out (DVO) port interface. Rather than providing data in parallel format, SDVO serially transmits digital display data to the SDVO port based on PCI Express* signaling. The SDVO interface can support a wide variety of third-party SDVO compliant devices (for example, DVI, TV-out, LVDS, and HDMI).

5.4.1 SDVO Interface Signals

Table 18. SDVO Signals

Signal	Direction / Type	Description
SDVO_REDP SDVO_REDN	O PCIe*	**Serial Digital Video Red:** SDVO_RED[±] is a differential data pair that provides red pixel data for the SDVO channel during Active periods. During blanking periods it may provide additional data such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVO_CLK[±] signal pair.
SDVO_GREENP SDVO_GREENN	O PCIe*	**Serial Digital Video Green:** SDVO_GREEN[±] is a differential data pair that provides green pixel data for the SDVO channel during Active periods. During blanking periods it may provide additional data such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVO_CLK[±] signal pair.
SDVO_BLUEP SDVO_BLUEN	O PCIe*	**Serial Digital Video Blue:** SDVO_BLUE[±] is a differential data pair that provides blue pixel data for the SDVO channel during Active periods. During blanking periods it may provide additional data such as sync information, auxiliary configuration data, etc. This data pair must be sampled with respect to the SDVO_CLK[±] signal pair.
SDVO_CLKP SDVO_CLKN	O PCIe*	**Serial Digital Video Clock:** This differential clock signal pair is generated by the internal PLL and runs between 100 MHz and 200 MHz. If TV-out mode is used, the SDVO_TVCLKIN[±] clock input is used as the frequency reference for the PLL. The SDVO_CLK[±] output pair is then driven back to the SDVO device.
SDVO_INTP SDVO_INTN	I PCIe*	**Serial Digital Video Input Interrupt:** Differential input pair that may be used as an interrupt notification from the SDVO device. This signal pair can be used to monitor hot plug attach/detach notifications for a monitor driven by an SDVO device.
SDVO_TVCLKINP SDVO_TVCLKINN	I PCIe*	**Serial Digital Video TV-out Synchronization Clock:** Differential clock pair that is driven by the SDVO device. If SDVO_TVCLKIN[±] is used, it becomes the frequency reference for the dot clock PLL, but will be driven back to the SDVO device through the SDVO_CLK[±] differential pair. This signal pair has an operating range of 100–200 MHz, so if the desired display frequency is less than 100 MHz, the SDVO device must apply a multiplier to get the SDVO_TVCLKIN[±] frequency into the 100- to 200-MHz range.
SDVO_STALLP SDVO_STALLN	I PCIe*	**Serial Digital Video Field Stall:** Differential input pair that allows a scaling SDVO device to stall the pixel pipeline.
SDVO_CTRLCLK	I/O CMOS3.3_OD	**SDVO Control Clock:** Single-ended control clock line to the SDVO device. Similar to I^2C* clock functionality, but may run at faster frequencies. SDVO_CTRLCLK is used in conjunction with SDVO_CTRLDATA to transfer device config, PROM, and monitor DDC information. This interface directly connects to the SDVO device.
SDVO_CTRLDATA	I/O CMOS3.3_OD	**SDVO Control Data:** SDVO_CTRLDATA is used in conjunction with SDVO_CTRLCLK to transfer device config, PROM, and monitor DDC information. This interface directly connects to the SDVO device.
SDVO_REFCLKP SDVO_REFCLKN	I SDVO	Display PLL Positive/Negative Ref Clock

5.4.2 SDVO Topology for Data and CLK on COM Express*

Figure 13. SDVO Routing Topology for SDVO RED[P:N], GREEN[P:N], BLUE[P:N], CLK[P:N] Signals

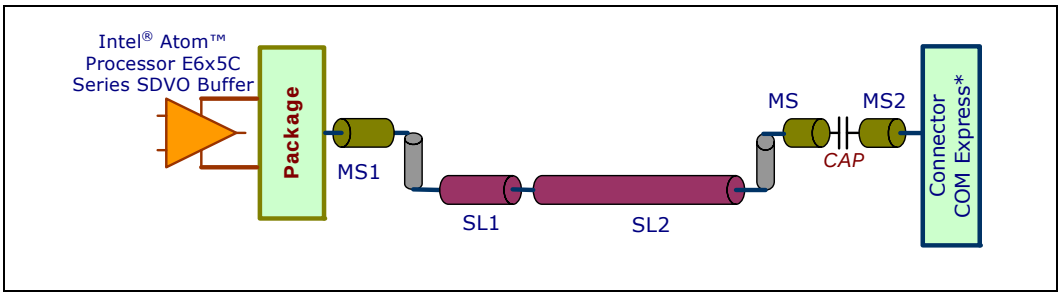


Figure 14. SDVO Routing Topology for SDVO INT[P:N],TVCLKIN[P:N], STALL[P:N] Signals

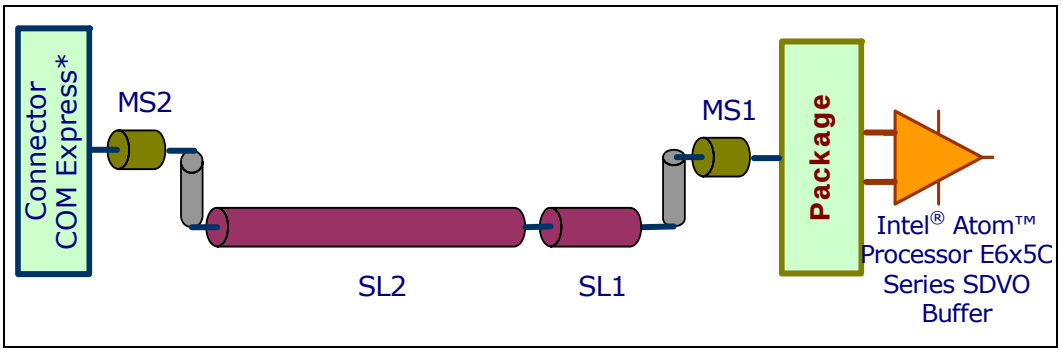


Table 19. SDVO Routing Guidelines for COM Express* Only

Segment	Description	Trace Width	Trace Space	Trace Length	Differential Impedance
MS1	Intel® Atom™ Processor E6x5C Series breakout (microstrip/stripline)	4.51/ 3.50 mils	4.49/ 3.70 mils	<0.25 in.	85 Ω ± 15%
SL1	Main route (microstrip/stripline)	5.01 mils	4.99 mils	0.1 - 0.5 in.	85 Ω ± 15%
SL2	Main route (microstrip/stripline)	4.51/ 5.01 mils	4.49/ 4.99 mils	0.5 - 3.50 in.	85 Ω ± 15%
MS2	Main route to COM Express* connector breakin (microstrip)	4.51 mils	4.49 mils	<0.25 in.	85 Ω ± 15%
MS	COM Express* connector breakin (microstrip)	4.51 mils	4.49 mils	<0.05 in.	85 Ω ± 15%
Total	MS1 + SL1 + SL2 + MS + MS2			<4.55	

Notes:
1. Maximum via count is 4 per line for COM Express* CPU module.
2. Maximum via count is 4 per line for Carrier Board.
3. Characteristic Differential Impedance is 85 Ω ± 15%.
4. These routing guidelines are applicable to a single board design. For this case, SL1 and SL2 can be merged.
5. AC coupling capacitor should place as near as possible to the COM Express* connector.

5.4.2.1 SDVO Length Matching Requirements

Trace lengths greatly impact the loss and jitter budgets of the interconnection. Though maximum trace routing lengths are given below, shorter lengths may be used and subsequent trade-offs can be made with the other restrictions placed on the interconnection, such as vias, spacing, and so forth. **It is recommended that any deviations from the recommendations made in this Datasheet be fully simulated and validated.**

The recommendation is to length match both nets within a differential pair to have a length mismatch of no more than 5 mils. Length mismatch between differential pairs within an SDVO channel is recommended to be within 3000 mils to minimize latency.

It is recommended to isolate all other signals from the SDVO signals with inter group spacing of 15 mils and intra group spacing of 20 mils to prevent coupling from other sources onto the SDVO lines.

5.4.3 SDVO Topology on Carrier Board

There are two SDVO topologies for the Intel® Atom™ Processor E6x5C Series. They consist of:

- SDVO connector
- Device down

Figure 15. SDVO Differential Signal Routing Topology for SDVO Connector

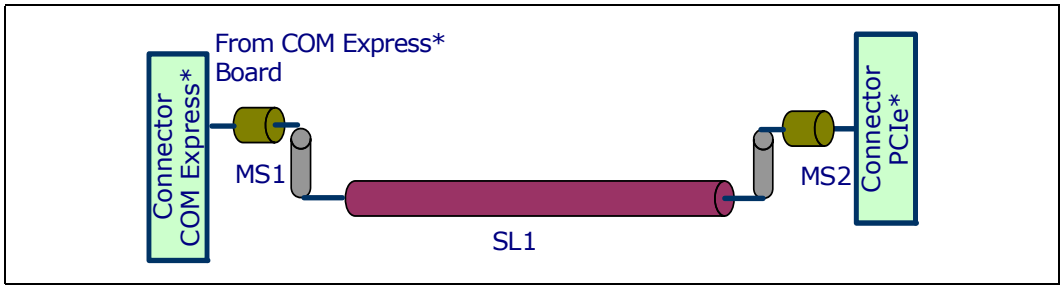


Table 20. SDVO Differential Signal Connector Routing Guidelines

Segment	Description	Trace Width	Trace Space	Trace Length	Differential Impedance
MS1	COM Express* breakout (microstrip)	4.51 mils	4.49 mils	< 0.25 in.	85 Ω ± 15%
SL1	Main route (stripline)	5.01 mils	4.99 mils	2.5 - 8.5 in.	85 Ω ± 15%
MS2	Breakin to connector	4.51 mils	4.49 mils	< 0.25 in.	85 Ω ± 15%
Total	MS1 + SL1 + MS2			<9.0 in. (max)	

Notes:
1. Maximum via count is 4 per line for COM Express* CPU module.
2. Maximum via count is 4 per line for Carrier Board.
3. These routing guidelines are applicable to a single board design. For this case, MS1 can be removed.

Figure 16. SDVO RED[P:N], GREEN[P:N], BLUE[P:N], CLK[P:N] Differential Signal Topology for Device Down

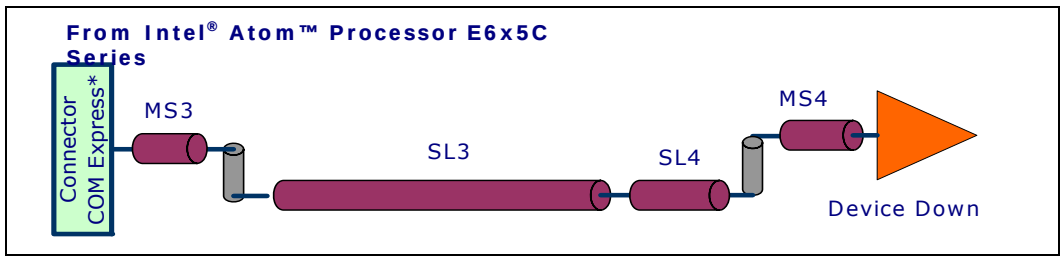


Figure 17. SDVO INT[P:N],TVCLKIN[P:N], STALL[P:N] Differential Signal Topology for Device Down

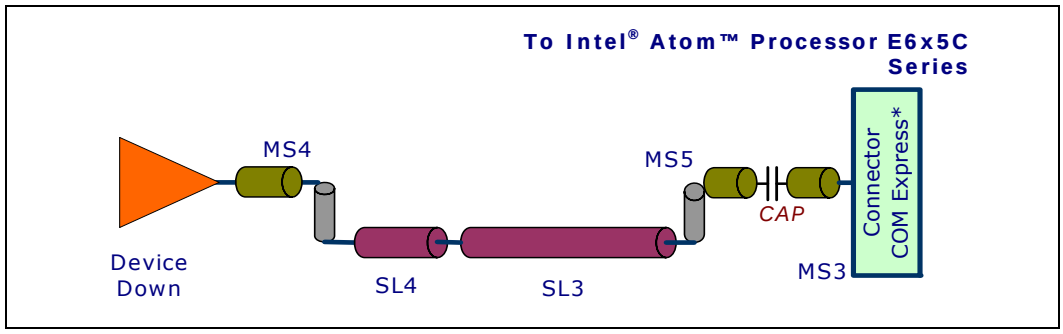


Table 21. SDVO Differential Signal Device Down Routing Guidelines

Segment	Description	Trace Width	Trace Space	Trace Length	Differential Impedance
MS3	COM Express* breakout (microstrip)	4.51 mils	4.49 mils	< 0.25 in.	85 Ω ± 15%
SL3	Main route (stripline)	5.01 mils	4.99 mils	2.5 - 8.5 in.	85 Ω ± 15%
SL4	Main route (stripline)	5.01 mils	4.99 mils	0.1 - 0.5 in.	85 Ω ± 15%
MS4	Breakin to device (microstrip)	4.51 mils	4.49 mils	< 0.25 in	85 Ω ± 15%
MS5	Breakin to COM Express* connector	4.51 mils	4.49 mils	< 0.05 in.	85 Ω ± 15%
Total	MS3 + SL3 + SL4 + MS4			< 9.5 in (max)	
Total	MS3 + SL3 + SL4 + MS4 + MS5			< 9.55 in (max)	

Notes:
1. These routing guidelines are applicable to a single board design. For this case, MS3 can be removed.
2. AC coupling capacitor should be place as near as possible to the COM Express* connector.

5.4.4 SDVO Single Board Routing Topology

Below figures show the topologies for single board routing. Trace geometries for the single board routing are the same as in Section 5.4.2 and Section 5.4.3. The length requirements are as shown in Figure 18 and Figure 19.

For single board routing, AC coupling capacitors should be placed as near as possible to the driver for device down topology. AC coupling capacitor is not require if Intel® Atom™ Processor E6x5C Series SDVO signals are connected to SDVO connector.

Figure 18. SDVO RED[P:N], GREEN[P:N], BLUE[P:N], CLK[P:N] Differential Signal Topology

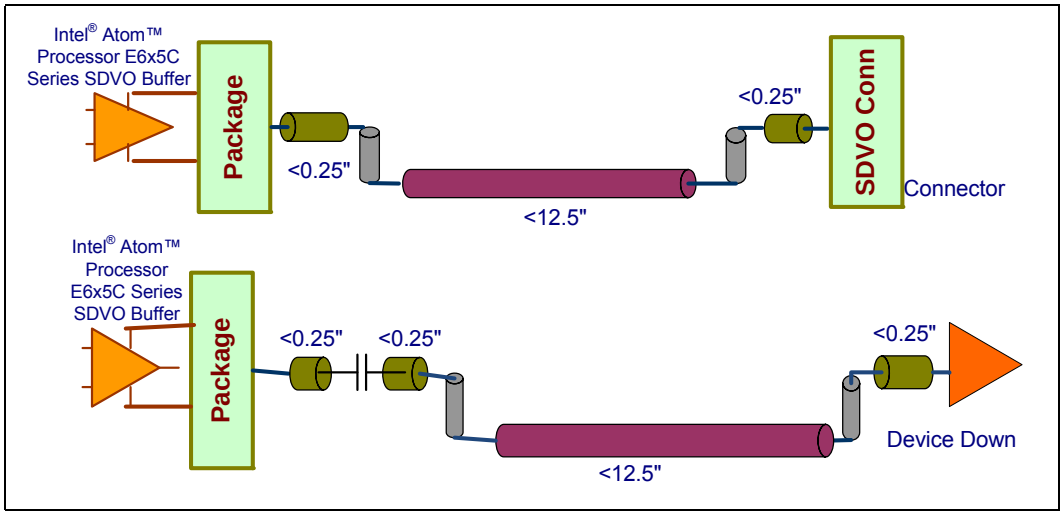
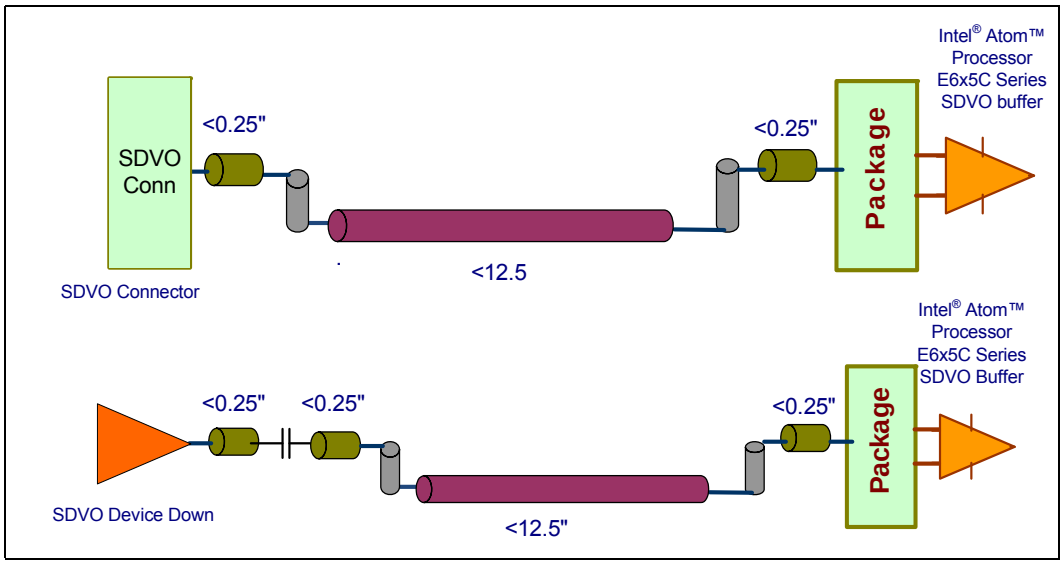


Figure 19. SDVO INT[P:N],TVCLKIN[P:N], STALL[P:N] Differential Signal Topology



5.4.5 SDVO Control Bus Signals

SDVO_CTRLCLK and SDVO_CTRLDATA are two control signals used for communications between the processor and an SDVO device. They are single-ended signals and do not need to meet the strict routing requirements outlined above. The following guidelines should be adhered to:

- These signals should be routed with the same single-ended routing specifications as mentioned in Section 3.1.
- The control bus outputs from the SDVO device (for PROM or DDC) may have a different signaling voltage other than the 2.5 V used by the SDVO_CTRLCLK and SDVO_CTRLDATA signals. If 2.5 V signaling is not supported by the SDVO device's buffers, then a bi-directional level shifting device will be required to properly translate the voltage levels.

- The minimum edge to edge spacing of the SDVO control bus signals (SDVO_CTRLCLK and SDVO_CTRLDATA) to all the other SDVO signals should be 20 mils in order to avoid potential noise issues. Please note that this spacing requirement should be met throughout the board routes.
- The maximum routing length for SDVO_CTRLCLK and SDVO_CTRLDATA should be limited to 7 inches. Length matching between SDVO_CTRLCLK and SDVO_CTRLDATA to within 500 mils is sufficient.

5.4.6 SDVO Interface Disable Guidelines

Table 22 shows the recommended connections when internal graphics SDVO is unused.

Table 22. Disable SDVO Graphics Connection Recommendations

Signal Name	Recommended Connection
SDVO_REFCLKP	Connect to 96 MHz pins on the clock chip generator.
SDVO_REFCLKN	Connect to 96 MHz pins on the clock chip generator.
SDVO_TVCLKINP	Tie to GND
SDVO_TVCLKINN	Tie to GND
SDVO_INTP	Tie to GND
SDVO_INTN	Tie to GND
SDVO_STALLP	Tie to GND
SDVO_STALLN	Tie to GND
SDVO_REDP	NC
SDVO_REDN	NC
SDVO_BLUEP	NC
SDVO_BLUEN	NC
SDVO_GREENP	NC
SDVO_GREENN	NC
SDVO_CTRLDATA	NC
SDVO_CLKP	NC
SDVO_CLKN	NC
SDVO_CTRLCLK	NC
VCCSFRDPLL 1.8V	Tie to V1P8_S

Notes:
1. Refer to the *RS - Intel® Atom™ Processor E6x5C Series BIOS Writer's Guide* — the "PCI Function Disables" section — for BIOS consideration when disabling the internal graphics.

§ §

6.0 Platform Clock Design Guidelines

6.1 Chapter Contents

This chapter contains information about:

- An overview of Platform Clock Design Guidelines
- Host Clocks Group
- 33 MHz Clocks Group
- 14 MHz Clock Group
- SRC Clock Group
- 96 MHz Clock Group
- Clock Enable
- EMI Constraints
- Miscellaneous Clock Signal Guidelines

6.2 Overview

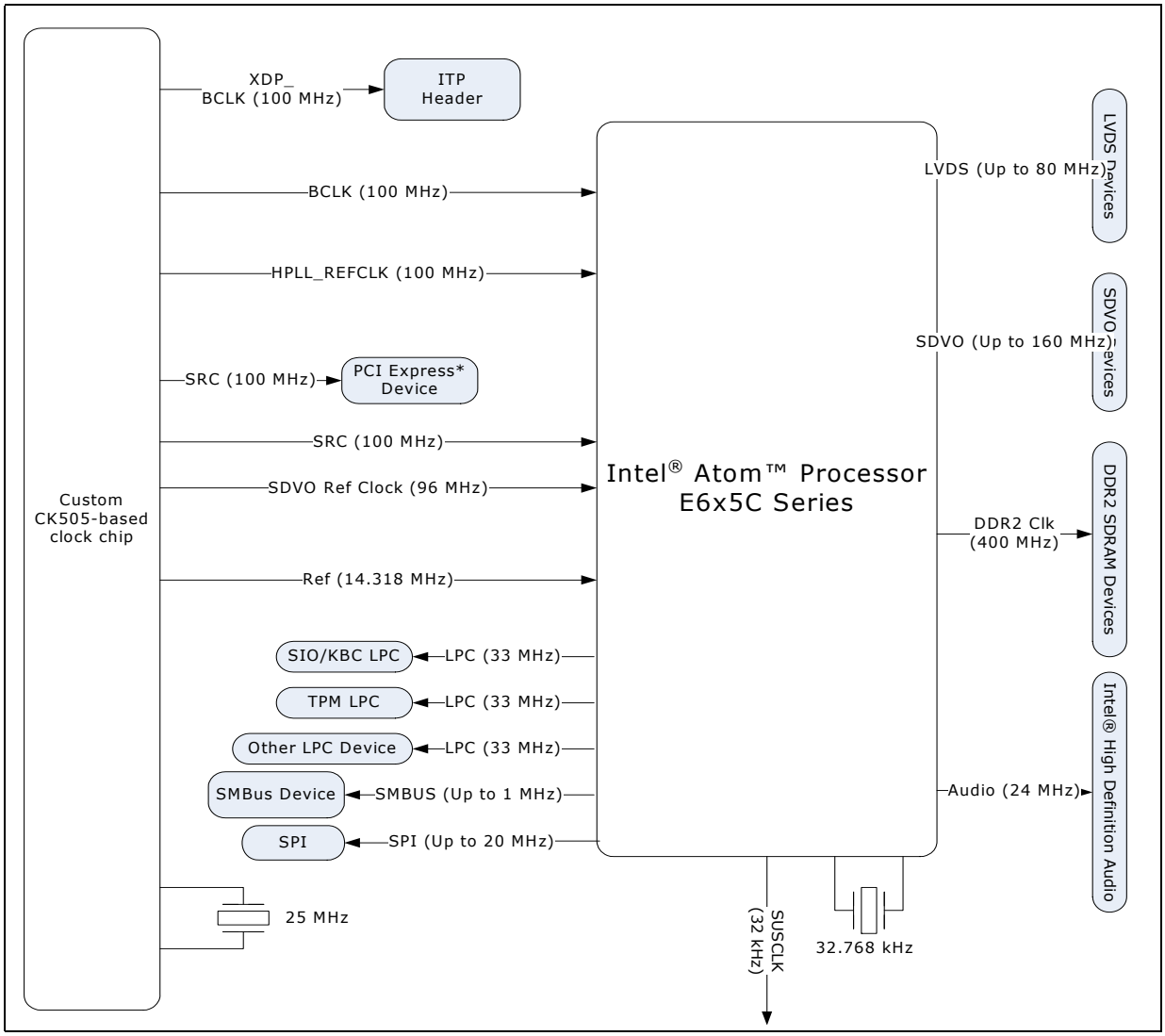
The system clock generator provides timing for all components in the system except for the real time clock. Table 23 shows the implementation of clocks for the Intel® Atom™ Processor E6x5C Series.

Note: For the Intel® Atom™ Processor E6x5C Series B0 stepping, the Host Clock for Premium, Mainstream, Entry and Ultra Low Power SKUs are running at 100 MHz.

Table 23. Chipset Clock Groups

Section	Group	Signal	Description
Section 6.3	Host Clocks	BCLK[P,N] HPLL_REFCLK[P,N] XDP_BCLK[P,N]	100 MHz clocks connect to the Intel® Atom™ Processor E6x5C Series - CPU core and GFX core, XDP debug port.
Section 6.4	SRC Clocks	PCIE_CLKIN[P,N]	A 100 MHz differential clock connects to the Intel® Atom™ Processor E6x5C Series - PCI Express* 100 MHz Input Clock.
Section 6.5	96 MHz Clock	SDVO_REFCLK[P,N]	A 96 MHz differential clock is used for the Intel® Atom™ Processor E6x5C Series - SDVO Display PLL Positive/ Negative Ref Clock.
Section 6.6	33 MHz Clocks	LPC_CLKOUT[2:0]	33 MHz clocks from the Intel® Atom™ Processor E6x5C Series to LPC devices
Section 6.7	14 MHz Clock	CLK14	A 14 MHz clock is used for the Intel® Atom™ Processor E6x5C Series 8254 timers and HPET.

Figure 20. Clock Distribution Diagram



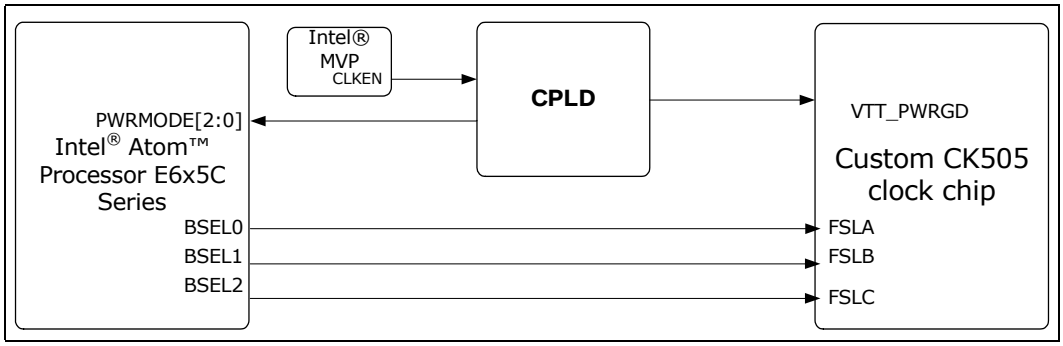
Notes:
1. The Host Clocks (XDP BCLK, BCLK and HPLL_REFCLK) are generated from CK505 CPU Clock outputs.
2. The SRC Clock is generated from CK505 PCIe* output.
3. Refer to third party clock chip vendors for more information on clock device features and compliance.

6.3 Host Clock Group

6.3.1 Host Clock Frequency Selection

The frequency of the host clock is determined by the BSEL outputs of the Intel® Atom™ Processor E6x5C Series. BSEL[2:0] pins are used by the Intel® Atom™ Processor E6x5C Series to indicate the host clock frequency. Connect the Intel® Atom™ Processor E6x5C Series BSEL[2:0] signals to the CK505 as shown in Figure 21.

Figure 21. Host Clock Frequency Selection



Notes:
1. Only 100 MHz Host Clock frequencies are supported. Other encodings on BSEL are reserved.

Table 24. Host Clock Frequency Select

BSEL0	BSEL1	BSEL2	Host Clock Frequency
Clock Chip Setting (Customer Reference Board)			
0	0	0	100 MHz
1	0	0	100 MHz
Intel® Atom™ Processor E6x5C Series Setting			
0	0	0	100 MHz
1	0	0	100 MHz

Notes:
1. If using the CK505 clock chip, special attention must be paid to the BSEL0 and BSEL2 signals due to the signal muxing by the clock chip.
2. The clock chip setting above might not the same for different clock chips. Please contact your clock chip vendors for the specification or datasheet.

6.3.2 Host Clock Trace Dimensions

Table 25. Host Clock Trace Geometry (Sheet 1 of 2)

Parameter[1]	Main Routing		Breakout Routing[2]	Units	Target Differential Impedance
	Microstrip	Stripline			
Mils					
Nominal Trace Width	3.51	3.76	3.76	mils	100 Ω ±15%
Nominal Trace Space[3]	6.99	6.24	6.24	mils	100 Ω ±15%
Bus-to-bus Spacing[4]	20	20	20	mils	

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Breakout trace dimensions apply to stripline routing at the processor.
3. Increased spacing to other differential pairs and single-ended signals helps to minimize crosstalk and increases margins. It is possible to offset decreases in pair-to-pair spacing by reducing maximum trace lengths. However, whenever trade-offs are made, the new topology must be simulated to ensure specification compliance.
4. Bus-to-bus spacing is the space between a host clock signal and any neighboring non-clock signal.
5. The trace parameter refers to Intel® Atom™ Processor E6x5C Series CRB design only.
6. Please consult your clock chip vendors for your clock chip design parameters.

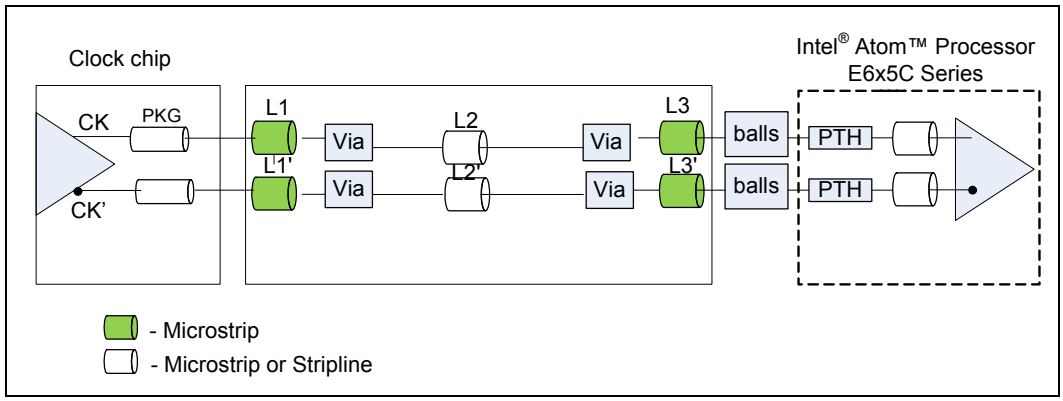
Table 25. Host Clock Trace Geometry (Sheet 2 of 2)

Parameter[1]	Main Routing		Breakout Routing[2]	Units	Target Differential Impedance
	Microstrip	Stripline			
Millimeters					
Nominal Trace Width	0.089	0.096	0.096	mm	100 Ω ±15%
Nominal Trace Space[3]	0.178	0.158	0.158	mm	100 Ω ±15%
Bus-to-bus Spacing[4]	0.508	0.508	0.508	mm	

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Breakout trace dimensions apply to stripline routing at the processor.
3. Increased spacing to other differential pairs and single-ended signals helps to minimize crosstalk and increases margins. It is possible to offset decreases in pair-to-pair spacing by reducing maximum trace lengths. However, whenever trade-offs are made, the new topology must be simulated to ensure specification compliance.
4. Bus-to-bus spacing is the space between a host clock signal and any neighboring non-clock signal.
5. The trace parameter refers to Intel® Atom™ Processor E6x5C Series CRB design only.
6. Please consult your clock chip vendors for your clock chip design parameters.

6.3.3 Host Clock Topology

Figure 22. Host Clock Topology



Notes:
1. Some clock chips have integrated series termination in their design, if not place a 33 Ω ±10% terminating resistor between L1 and L2.
2. Important Note: The total length matching between BCLK differential pair signals and HPLL_REFCLK differential pair signals is required.

Table 26. Host Clock Trace Length Example

Parameter	Description	Trace Length	Notes
L1, L1'	Clock Driver to Via	100 mils	
L2, L2'	Via to Via, Main Route	5000 mils	
L3, L3'	Via to Receiver, Breakin	100 mils	
TOTAL	Clock to Receiver L_{TOTAL} = L1 + L2 + L3 and L_{TOTAL} = L1' + L2' + L3'	5200 mils	

Notes:
1. The trace length is measured from the Intel® Atom™ Processor E6x5C Series CRB design.
2. Please consult your clock chip vendor for the max length specifications.

6.3.4 Host Clock General Routing Guidelines

The clock synthesizer provides three pairs of 100 MHz differential clock output. The differential clocks are driven to the Intel® Atom™ Processor E6x5C Series and the XDP debug port with the topology shown in Figure 22. For some CK505 and CK610 designs, both topologies implement a Source Serial Termination. CK540 and some CK505 do not need serial termination as it is internal to the chips. Host clock routing to the Intel® Atom™ Processor E6x5C Series should be done with the same topology type. Only the recommended topology (Figure 22) should be used for host clock routing.

- Host clock differential signals should be continuously referenced to ground and must not be split between different routing layers.
- If the clock chip without integrated series resistors is used, place the clock generator and series resistors on the same layer. (No resistor is needed for CK540, CK610 and some CK505.)
- If a layer transition on the trace is required, make sure that the skew induced by vias used to transition between routing layers is compensated in the traces to other agents. Reference plane stitching vias must be used in conjunction with high-speed signal layer transitions that include a reference plane change. Place at least one stitching via between the two reference planes for every four signals that transition. The stitching via should be placed within 100 mils of the signal transition via to improve signal integrity.
- Do not place vias between adjacent complementary clock traces and avoid differential vias. Vias, placed in one signal of a differential pair, must be matched by a via in the complement.

Table 27. Host Clock Routing Guidelines

Layout Guideline	Value	Notes
Host Clock Skew Between Agents	CPU Clock outputs cycle-to-cycle jitter is < 85 ps	1, 2, 3

Notes:
1. The skew budget does not include clock driver common mode.
2. The skew budget includes clock driver output pair to output pair jitter (differential jitter), clock skew due to interconnect process variation and static skew due to layout differences between clock to all bus agents.
3. Please refer to your clock chip vendor for the skew jitter specifications.

6.3.5 Host Clock Length Matching Requirements

- Each host signal segment must be within 10 mils (0.254 mm) of its complement
  - Example: L1 must be within 10 mils (0.254 mm) of L1’
- The host clock length matching requirements listed above are the only compensation that is needed. No additional routing or length compensation is required due to internal package trace lengths on the Intel® Atom™ Processor E6x5C Series.
- The skew between BCLK[P,N] and HPLL_REFCLK[P,N] must be set less than 100 ps including all variations and mismatches as measured at the processor.

6.3.6 Host Clock Via Placement on Intel® Atom™ Processor E6x5C Series

There are special requirements for BCLK and HPLL_REFCLK differential pair signals (Host Clock signals) via and stitching via routing. Please consult your clock vendor for specifications.

6.3.7 Host Clock Via Placement on the Motherboard

Vias are allowed on the BCLK and HPLL_REFCLK signals (Host clock signals) although limiting their use is a good design practice. The following guidelines concerning vias usage should be adhered to:

- Vias impact the overall loss and jitter budget and therefore should be carefully used as they may impact the signal quality of Host Clock signals.
- The number of vias for each signal within a differential pair must be matched because each signal within the differential pair must stay on the same layer. Vias on the differential pair should not only match in quantity but also in relative location. This is especially important for tightly coupled pairs where trace lengths before and after the via transition should be matched to within a 10 mil (0.254 mm) delta. It should also be noted that the overall trace route needs to conform to a total of a 10 mil (0.254 mm) delta between the P (+) and N (-) signals within the differential pair.

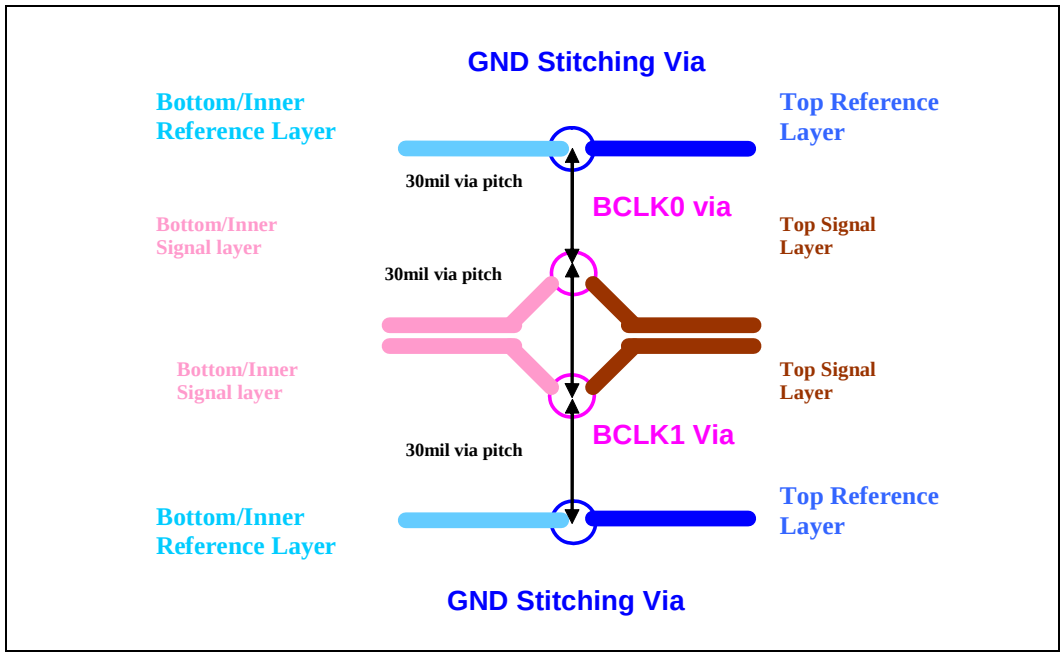
Note: For example, if a via is needed to escape one signal in a differential pair from the package then both signals in the differential pair must transition through vias at the package.

If there is a via transition in the middle of the trace, then both traces in the pair should have vias at the same location on the signal routing for tightly coupled pairs.

6.3.8 Host Clock Stitching Via Usage and Placement

Stitching vias must be used when signal traces change layers from top to internal layer and change to bottom layer (and vice versa). In these cases, the reference GND layer associated with the top signal layer has to be connected with GND reference layer associated with the bottom or internal signal layer using GND stitching via. Placing GND stitching via according to the your clock chip guidelines will maintain an optimal current return path and minimize crosstalk effect. Placement of additional stitching vias, where possible, is recommended.

Figure 23. MB GND Stitching Via Placement for BCLK Signal



6.4 SRC Clock Group

The clock chip synthesizer provides 100 MHz differential clock outputs for Serial Reference Clocks (SRC). These SRC pairs are used for PCI Express* devices placed on board or on a daughter card. The SRC clock can also be routed to the Intel® Atom™ Processor E6x5C Series for PCIE_CLKIN[P,N]. SRC1/SRC1# of the custom designed CK505 can be configured to output a 100 MHz spread spectrum clock with a 2.5% spread.

For the clock chip which is used on the CRB, by default, no spread spectrum is set. Need to use SMBUS access to configure the registers to get 0.5% down spread on all CPU/SRC/PCIe* clocks.

6.4.1 SRC Trace Dimensions

Table 28. SRC Trace Geometry

Parameter[1]	Main Routing		Breakout Routing[2]	Units	Notes	Target Differential Impedance
	Microstrip	Stripline				
Mils						
Nominal Trace Width	3.5	3.76	3.76	mils		100 Ω ±15%
Nominal Trace Space	6.99	6.24	6.24	mils	3	100 Ω ±15%
Bus-to-bus Spacing	20	20	20	mils	4	100 Ω ±15%
Millimeters						
Nominal Trace Width	0.089	0.096	0.096	mm		100 Ω ±15%
Nominal Trace Space	0.178	0.158	0.158	mm		100 Ω ±15%
Bus-to-bus Spacing	0.508	0.508	0.508	mm		100 Ω ±15%

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Breakout trace dimensions apply to stripline routing at the processor.
3. Increased spacing to other differential pairs and single-ended signals helps to minimize crosstalk and increases margins. It is possible to offset decreases in pair-to-pair spacing by reducing maximum trace lengths. However, whenever trade-offs are made, the new topology must be simulated to ensure specification compliance.
4. Bus-to-bus spacing is the space between an SRC signal and any neighboring non-SRC signal.
5. The trace parameter refers to the Intel® Atom™ Processor E6x5C Series CRB design.
6. Please consult your clock chip vendors for your clock chip design parameters.

6.4.2 SRC Routing Guidelines

- Nominal microstrip impedance is 100 Ω ± 15% and stripline impedance is 100 Ω ± 15%.
- Do not place vias between adjacent complementary clock traces, and when possible avoid layer transitions.
- Vias placed in one half of a differential pair must be matched by vias in the other half.
- The differences in length of every transmission line segment must match to within 25 mils (0.635 mm).
- The total length of each SRC clock signal must be within 25 mils (0.635 mm) of its complement, though no length matching is required between different source pairs.

6.4.3 SRC Topologies

The SRC clocks support a device down topology, which allows four differential transmission line segments and four vias, as shown in Figure 24.

The following assumptions apply to the device down topology:

- The breakout section is assumed to be on the same microstrip layer where the clock chip is placed. All other trace segments are assumed to be any microstrip or stripline layer.
- The breakin and breakout sections to the series resistor are not explicitly shown. They will be required for cases where the signal transitions to or from the other microstrip layer or a stripline layer. These breakin and breakout sections must each be kept to less than 100 mils (2.54 mm).

An example of the trace lengths is expressed for the device down topology in Table 29.

Figure 24. SRC Device Down Topology

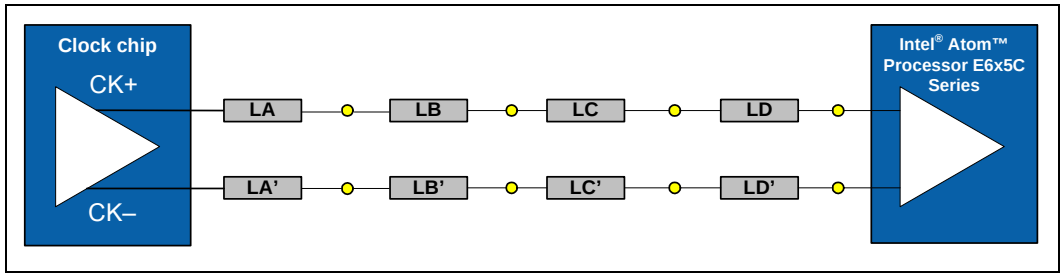


Table 29. SRC Trace Length Example

Parameter	Description	Trace Length	Notes
LA, LA'	Breakout (Microstrip)	200 mils	
LB, LB'	Breakout to Via (Microstrip or Stripline)	1000 mils	
LC, LC'	Via to Via (Microstrip or Stripline)	1500 mils	
LD, LD'	Breakin (Microstrip or Stripline)	100 mils	
Total	Clock to Receiver L_{TOTAL} = LA + LB + LC + LD and L_{TOTAL} = LA' + LB' + LC' + LD'	2800 mils	

Notes:
1. The trace length is measured from the Intel® Atom™ Processor E6x5C Series CRB design.
2. Please consult your clock chip vendor for the max length specifications.
3. Simulation is required if the differential impedance is mis-matched between carrier card and daughter card.

6.5 96 MHz Dot Clock Group (SDVO_REFCLKP / SDVO_REFCLKN)

The SDVO_REFCLK[P:N] signals that make up the dot clock signal group use the same trace dimensions, topologies, and routing guidelines as the SRC clock group. See Section 6.4.1 through Section 6.4.3.

Table 30 contains the trace length example from CRB design for this topology.

Note: It is important to generate the 96 MHz dot clock group (SDVO_REFCLK/ DSDVO_REFCLKN) and 100 MHz host clock group from the same clock chip to ensure

both clocks are aligned. This recommendation is part of the workaround for the SDVO image clipping issue.

Table 30. Dot Clock Trace Length Example

Parameter	Description	Trace Length	Notes
LA, LA'	Breakout (Microstrip)	200 mils	
LB, LB'	R_S to Via	3000 mils	
LC, LC'	Breakin	100 mils	
Total	Clock to Receiver L_{TOTAL} = LA + LB + LC and L_{TOTAL} = LA' + LB' + LC'	3300 mils	

Notes:
1. The trace length is measured from the Intel® Atom™ Processor E6x5C Series CRB design.
2. Please consult your clock chip vendor for the max length specifications.

6.6 33 MHz Clock Group (LPC_CLKOUT)

For the 33 MHz clock group, it is important to note that the Intel® Atom™ Processor E6x5C Series is driving the clocks (not the clock chip) to the LPC devices.

6.6.1 33 MHz Clock Trace Geometries

The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.

Table 31. LPC_CLKOUT Trace Geometry

Parameter	Main Routing		Breakout	Units	Target Single Ended Impedance
	Microstrip	Stripline			
Mils					
Nominal Trace Width	4.5	4.3	3.5	mils	50 Ω ±15%
Nominal Trace Space	10	10	5	mils	50 Ω ±15%
Millimeters					
Nominal Trace Width	0.114	0.102	0.089	mm	50 Ω ±15%
Nominal Trace Space	0.254	0.254	0.127	mm	50 Ω ±15%

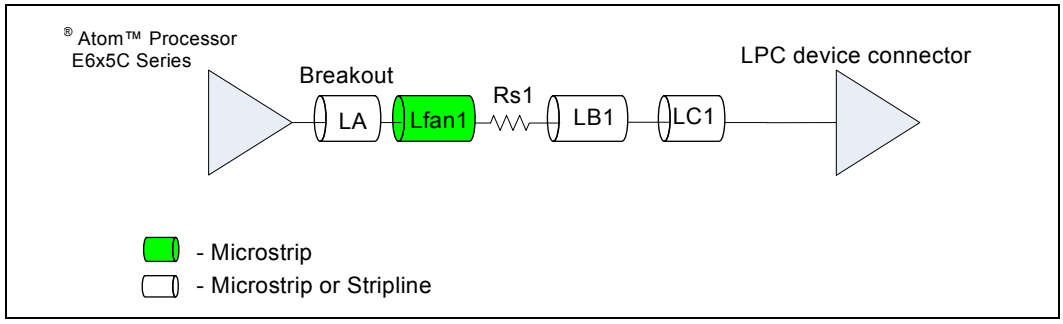
Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the single-ended impedance.
2. Breakout trace dimensions apply to both stripline or microstrip routing.
3. Increased spacing to other single-ended signals helps to minimize crosstalk and increases margins.

6.6.2 33 MHz Clock Topologies

Figure 25 and Figure 26 show the supported routing from the Intel® Atom™ Processor E6x5C Series to the 33 MHz input receivers. This guideline supports single and dual-load clock receivers (using a T topology for dual-load). Buffering the clock lines to drive additional loads is not supported.

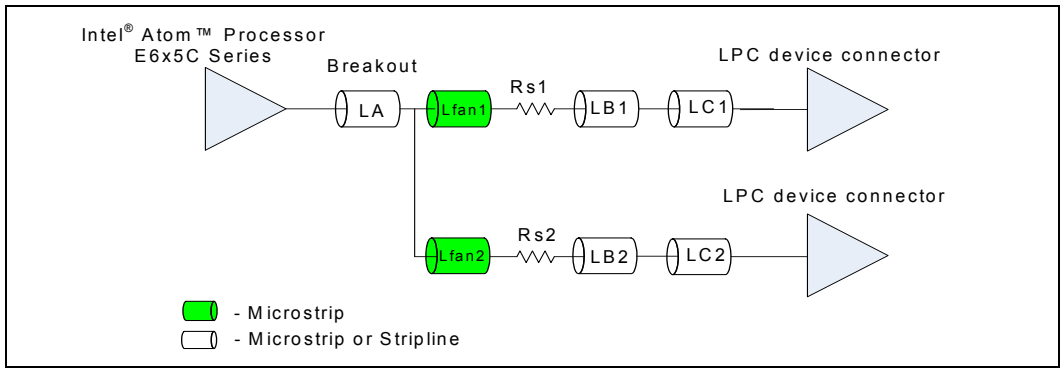
Signal breakin and breakout will be required when signals transit to or from the other microstrip layer or stripline layer. Each of the breakin and breakout sections must be kept to less than 100 mils (2.54 mm).

Figure 25. LPC_CLKOUT Single Load Topology to Socket



Notes:
1. Rs1 = 22 Ω ± 5%

Figure 26. LPC_CLKOUT Dual Load Topology to Socket



Notes:
1. Rs1, Rs2 = 22 Ω ± 5%

Table 32. LPC_CLKOUT Trace Lengths

Segment	Description	Trace Length	Notes
LA	Breakout	400 mils max	
Lfan1, Lfan2	Breakin to Rs	100 mils max	
LB1, LB2	Main Route	7200 mils max	
LC1, LC2	Main Route	7200 mils max	
Total	Total Trace Length • 1-load: LA+Lfan+LB+LC • 2-load: LA+Lfan1+LB1+LC1 / LA+Lfan2+LB2+LC2	9000 mils max	1

Notes:
1. The main route and breakin traces to each load (e.g., LB1+LC1) must be length matched to within 300 mils of the other trace (e.g., LB2+LC2).

6.7 14.31818 MHz Clock Group (REFCLK)

In cases where three loads are present customers should insure that they validate the signal integrity of their specific implementation.

Note: The exact frequency for REFCLK is 14.31818 MHz.

6.7.1 14.31818 MHz Clock Trace Geometries

Table 33. 14.31818 MHz Clock Trace Geometry

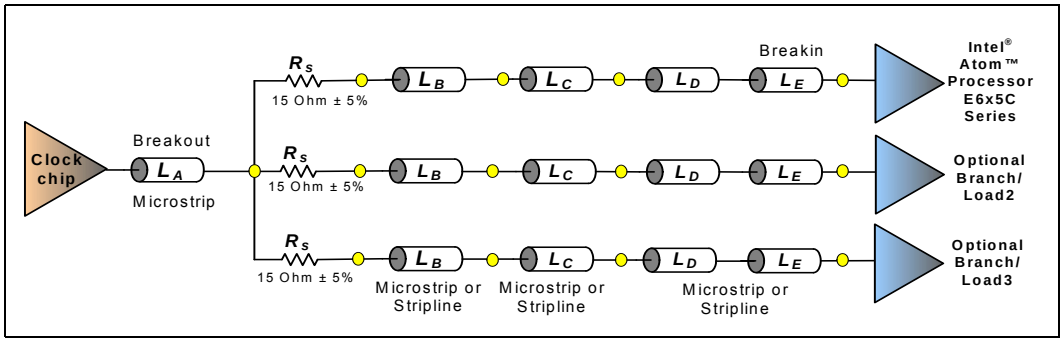
Parameter	Main Routing		Breakout	Units	Target Single-Ended Impedance
	Microstrip	Stripline			
Mils					
Nominal Trace Width	4.5	4.3	3.5	mils	50 Ω ±15%
Nominal Trace Space	20	20	5	mils	50 Ω ±15%
Millimeters					
Nominal Trace Width	0.114	0.109	0.089	mm	50 Ω ±15%
Nominal Trace Space	0.508	0.508	0.127	mm	50 Ω ±15%

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Breakout trace dimensions apply to both stripline or microstrip routing.
3. Increased spacing to other single-ended signals helps to minimize crosstalk and increases margins.

6.7.2 14.31818 MHz Clock Topology Description

Figure 27 shows the supported routing from the clock driver to the Intel® Atom™ Processor E6x5C Series input receiver and one or two optional receivers. This guideline supports a single, dual or triple load topology with a single breakout including via routed to one, two, or three branches each with a series termination. Each branch of the T includes three impedance discontinuities in four transmission line segments (including the breakin) and four vias. In addition there is a short stub allowed for the BSEL2 isolation resistor. The clock chip breakout section is assumed to be on the same microstrip layer as the clock chip, so only microstrip is supported. The breakin and breakout sections to the series resistor are not explicitly shown. They will be required for cases where the signal transitions to or from the other microstrip layer or a stripline layer. These breakin and breakout sections must each be kept to less than 100 mils (2.54 mm).

Figure 27. Topology for REFCLK



Note: In a one load topology, series resistors should equal 33 Ω ± 5%. In a two load topology, both series resistors, Rs should be 22 Ω ± 5%. In the case of a triple load topology, series resistor, Rs = 15 Ω ± 5% for each series resistor.

In cases where three loads are present customers should ensure they validate the signal integrity of their specific implementation.

Table 34. 14.31818 MHz Clock Trace Lengths

Segment	Routing Guideline	Maximum Trace Length	
		Inches	Millimeters
LA	Clock chip breakout to T	0.25	6.35
LB	Series resistor, Rs to LC	6	152.4
LC	LB to LD	6	152.4
LD	LC to LE	8	203.2
LE	LD breakin to Receiver	0.5	12.7
Total	Total Trace Length: LA + LB + LC + LD+ LE	13	330.2
LS	BSEL Stub Length	0.1	2.54

6.7.2.1 BSEL2 Isolation

No BSEL2 isolation is required for CK540 designs. Isolation is only required for CK505 designs where the 14 MHz reference clock is muxed with BSEL2 functionality. Refer to vendor clock chip specification for details.

6.8 Clock Enable

The CLKEN_B signal from the Intel® Mobile Voltage Positioning 6 (Intel® MVP-6) must be used to indicate the Intel® Atom™ Processor E6x5C Series power good to the System Microcontroller (SMC). The CLKEN_B signal will mux with PWRMODE[2:0] at SMC before routing to the clock chip.

6.9 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two signals of each differential clock pair.
- Route clocks on physical layer adjacent to the V_{SS} reference plane only.

6.10 Disabling Unused Clocks

Unused clock outputs should be disabled to limit EMI radiation and adverse signal quality effects. This can be done using the CK505, CK540 or CK610 clock synthesizer SMBus interface. Each clock output has an enable bit in the SMBus register space. Most applications turn off unused clock pairs through the SMBus shortly after power-on during the boot cycle.

6.11 Miscellaneous Clock Signal Guidelines

The following section is the schematic requirements for the signals on the CK505, CK540 and CK610 clock drivers. No special connections or termination are required on signals that are not specifically addressed-they should be connected directly to the appropriate destination pin (the Intel® Atom™ Processor E6x5C Series and connector) without the need for additional logic or passive components. Always consult your clock vendor for details of specifications.

§ §

7.0 I/O Subsystem

The following sections contain detailed design recommendations for the primary I/O interfaces of the Intel® Atom™ Processor E6x5C Series. A thorough understanding of the general design guidelines in Section 3.0 is highly recommended. This chapter does not discuss the functional aspects of any interface protocol or architecture. Nor does it discuss the layout guidelines for an add-in device.

The following interfaces are contained within this chapter:

Interface	Section
PCI Express*	Section 7.1
SPI	Section 7.2
Intel® High Definition Audioβ	Section 7.3
SMBus	Section 7.4
RTC	Section 7.5
LPC	Section 7.6
Intel® Atom™ Processor E6x5C Series Strapping	Section 7.7

Caution: If system designers do not follow the guidelines listed in this document, it is very important that they perform thorough signal integrity and timing simulations for each design.

7.1 PCI Express* Interface

The Intel® Atom™ Processor E6x5C Series contains four x1 PCI Express* expansion interfaces. It is a high-bandwidth, low pin-count serial interface ideal for I/O expansion.

7.1.1 PCI Express* Interface Signals

Table 35. PCI Express* Interface Signals

Signal Name	Direction/Type	Description
PCIE_PETp[3:0] PCIE_PETn[3:0]	O PCIE*	PCI Express* Transmit pair (P and N) signals.
PCIE_PERp[3:0] PCIE_PERn[3:0]	I PCIE*	PCI Express* Receive pair (P and N) signals.
PCIE_CLKINP PCIE_CLKINN	I/O A	PCI Express* Input Clock: 100 MHz differential clock signals.
PCIE_ICOMPO	I/O A	PCI Express* Compensation pin: Output compensation for both current and resistance.
PCIE_ICOMPI	I/O A	PCI Express* Compensation pin: Input compensation for current.
PCIE_RCOMPO	I/O A	PCI Express* Compensation pin: PCI Express* resistance compensation
PCIE_RBIAS	I/O A	PCI Express* Compensation pin: PCI Express* Bias control

7.1.2 PCI Express* Trace Dimensions

Table 36. PCI Express* Trace Geometry

Parameter[1]	Main Routing	Breakout Routing[2]	Units	Target Differential Impedance
Mils				
Trace Width - Microstrip	4.51	4.51	mils	85 Ω ±15%
Differential Pair Trace Spacing - Microstrip	4.49	4.49	mils	85 Ω ±15%
Trace Width - Stripline	5.01	5.01	mils	85 Ω ±15%
Differential Pair Trace Spacing - Stripline	4.99	4.99	mils	85 Ω ±15%
Minimum Differential Pair-to-pair Spacing[3]	20	20	mils	85 Ω ±15%
Minimum Bus-to-bus Spacing[4]	25	25	mils	85 Ω ±15%
Millimeters				
Trace Width - Microstrip	0.114	0.114	mm	85 Ω ±15%
Differential Pair Trace Spacing - Microstrip	0.114	0.114	mm	85 Ω ±15%
Trace Width - Stripline	0.127	0.127	mm	85 Ω ±15%
Differential Pair Trace Spacing - Stripline	0.126	0.126	mm	85 Ω ±15%
Minimum Differential Pair-to-pair Spacing[3]	0.508	0.508	mm	85 Ω ±15%
Minimum Bus-to-bus Spacing[4]	0.635	0.635	mm	85 Ω ±15%

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Breakout trace dimensions apply to both stripline or microstrip routing.
3. Increased spacing to other differential pairs and single-ended signals helps to minimize crosstalk and increases margins. It is possible to offset decreases in pair-to-pair spacing by reducing maximum trace lengths. However, whenever trade-offs are made, the new topology must be simulated to ensure specification compliance.
4. Bus-to-bus spacing is the space between a PCI Express* signal and any neighboring non-PCI Express* signal.

7.1.3 PCI Express* Routing Guidelines

- PCI Express* signals should be ground referenced.
- GND stitching vias are required next to signal vias if transitional layers are located between GND layers.
- Power referencing is acceptable if stitching caps are used.
- Interleaved routing is allowed for main motherboard routing or breakout routing (microstrip or stripline).
- Maintain routing symmetry between two signals of a differential pair. Failure to do so can introduce an AC common mode voltage.
- Increased spacing between differential pairs and single-ended signals minimizes crosstalk and increases margins. It is possible to offset decreases in pair-to-pair spacing by reducing maximum trace lengths. When trade-offs are made the new topology must be simulated to ensure specification compliance.
- A minimum distance must be maintained between the edge of a trace and its reference plane. This minimum distance ensures a proper return path for the trace's EM field.
- All major traces should be routed on internal layers.

7.1.4 Length Matching

The following are length matching guidelines for PCI Express* differential pairs:

- Length matching between pairs of a link is not generally required.
- Match the length of both nets within a differential pair is +/- 5 mils to series components and connectors.
- Maintain +/- 10 mils for PCI Express* signal from the Intel® Atom™ Processor E6x5C Series to COM Express* connector
- Match the length of pair-to-pair PCI Express* signals within 3000 mils from Intel® Atom™ Processor E6x5C Series to COM Express* connector lanes.

7.1.5 Via Usage and Placement

Vias are allowed on a PCI Express* interconnect, though their use should be limited. Current guidelines concerning vias are as follows:

- Vias impact the overall loss and jitter budget and therefore should be carefully used as they may impact the overall length of route that may be achievable.
- It is recommended that no more than 4 vias per TX pair and RX pair to be used on each net in a differential pair.

7.1.6 PCI Express* Topologies

Simulations of the PCI Express* interface were performed assuming the following usage models/topologies:

- PCI Express* to COM Express* connector
- COM Express* connector to PCIe* slot

The following sections describe the layout requirements for each of these options. Other topologies are possible, but simulations are required to verify solution space of such topologies.

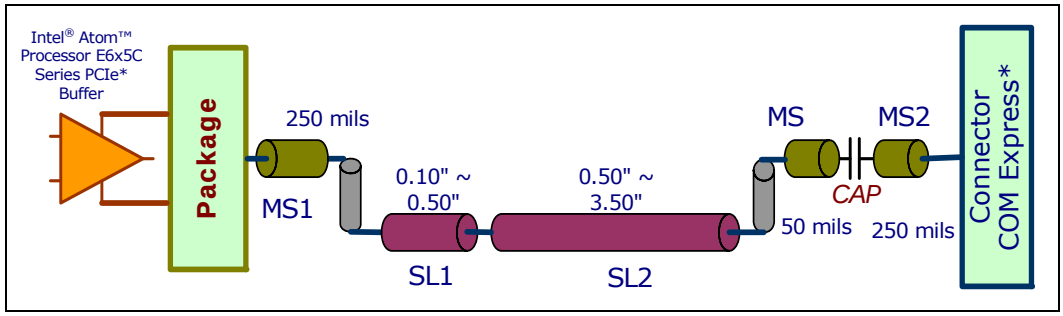
7.1.6.1 PCI Express* to COM Express* Connector Topology

This topology applies to the below PCI Express* signals:

- PCIE_PET[P, N] [3:0]
- PCIE_PER[P, N] [3:0]

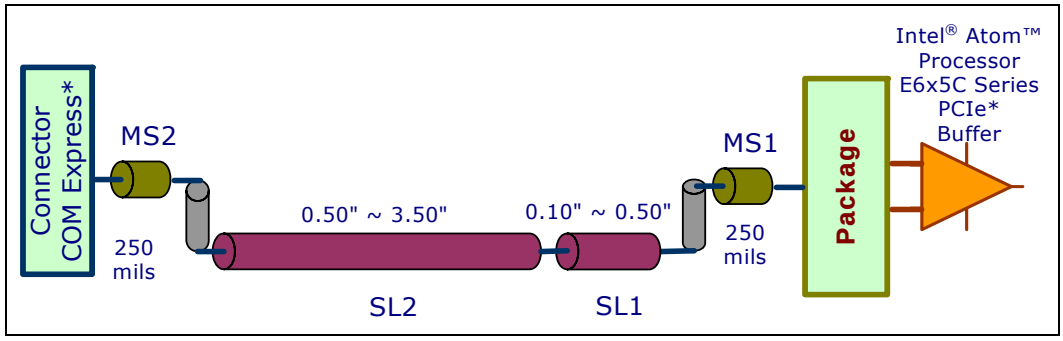
Figure 28, Figure 29 and Table 37 show the required geometry for routing of PCI Express* differential signals from the Intel® Atom™ Processor E6x5C Series to COM Express* Connector on the COM Express* board.

Figure 28. PCI Express* to COM Express* Connector Transmitter Topology Example



Notes:
1. Maximum number of vias allowed is 4 for COM Express* CPU Module.
2. Maximum number of vias allowed is 4 for Carrier board.
3. AC coupling capacitor value = 0.1 µF (+/- 2% of part tolerances).

Figure 29. PCI Express* to COM Express* Connector Receiver Topology Example



Notes:
1. Maximum number of vias allowed is 4 for COM Express* CPU Module.
2. Maximum number of vias allowed is 4 for Carrier board.
3. AC coupling capacitor value = 0.1 µF (+/- 2% of part tolerances).

Table 37. PCI Express* to COM Express* Connector Length Guidelines

Trace Length	Description	Max Trace Length	
		Inches	Mils
MS1	Breakout	< 0.25	< 250
SL1	Breakout	0.1 - 0.5	100 - 500
SL2	Main route	0.5 - 3.5	500 - 3500
MS	Stripline	< 0.05	< 50
MS2	Breakin to COM Express* connector	< 0.25	< 250
Total Length	Transmitter: MS1 + SL1 + SL2 + MS + MS2	< 4.55	< 4550
	Receiver: MS2 + SL2 + SL1 + MS1	< 4.55	< 4550

7.1.6.2 COM Express* to PCI Express* Slot Topology

This topology applies to below PCI Express* signals:

- PCIE_TX[3:0][P, N]

- PCIE_RX[3:0][P, N]

Figure 30 and Table 38 show the required geometry for routing of PCI Express* differential signals from COM Express* Connector to PCI Express* slot on the carrier board.

Figure 30. COM Express* Connector to PCI Express* Slot Transmitter/Receiver Topology

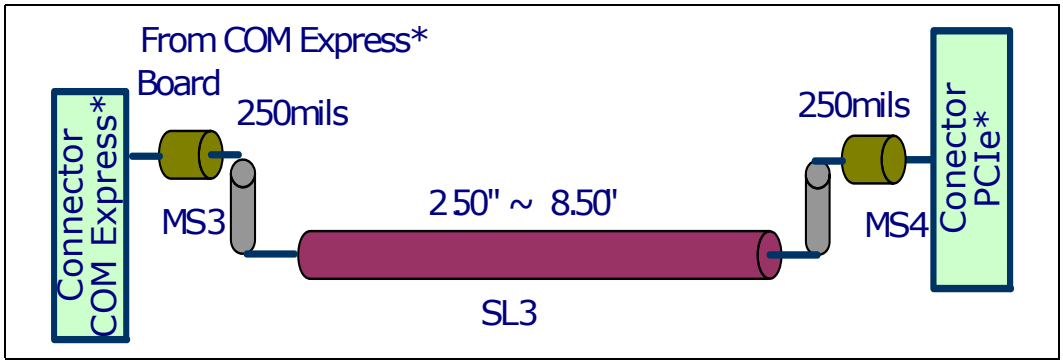


Table 38. PCI Express* to COM Express* Connector Length Guidelines

Trace Length	Description	Max Trace Length	
		Inches	Mils
MS3	Breakout	0.25	250
SL3	Main route	2.50 - 8.50	2500 - 8500
MS4	Break in to the PCIe* connector	0.25	250
Total Length	MS3 + SL3 + MS4	< 9.0	< 9000

7.1.6.3 PCI Express* Single Board Routing Topology

Figure 31 and Figure 32 show the topologies for single board routing. Trace geometries for the single board routing are the same as in Section 7.1.6.1 and Section 7.1.6.2. The length requirements are as shown in Figure 31 and Figure 32.

Figure 31. PCI Express* Topology for Transmit Signals

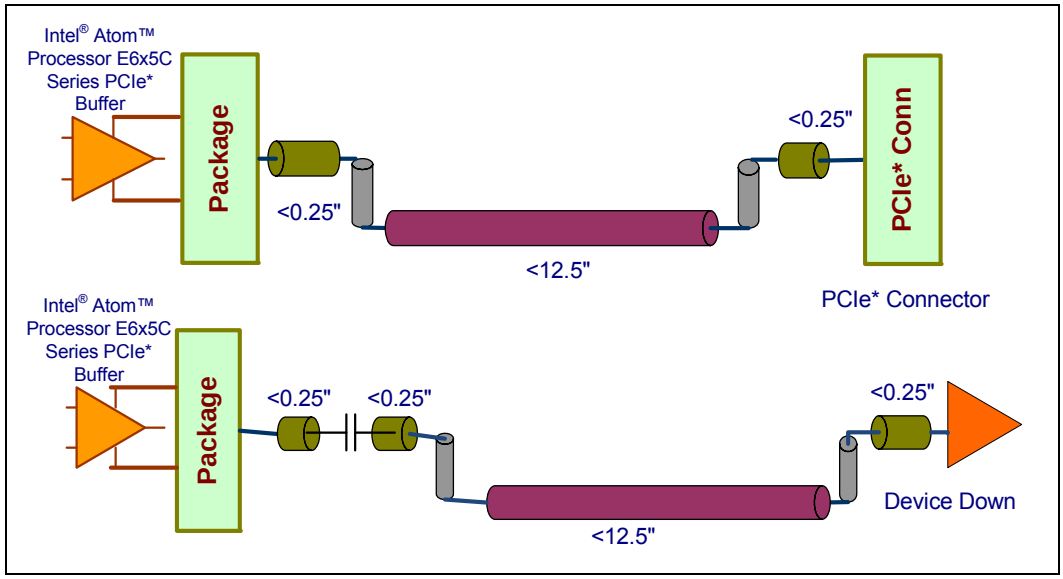
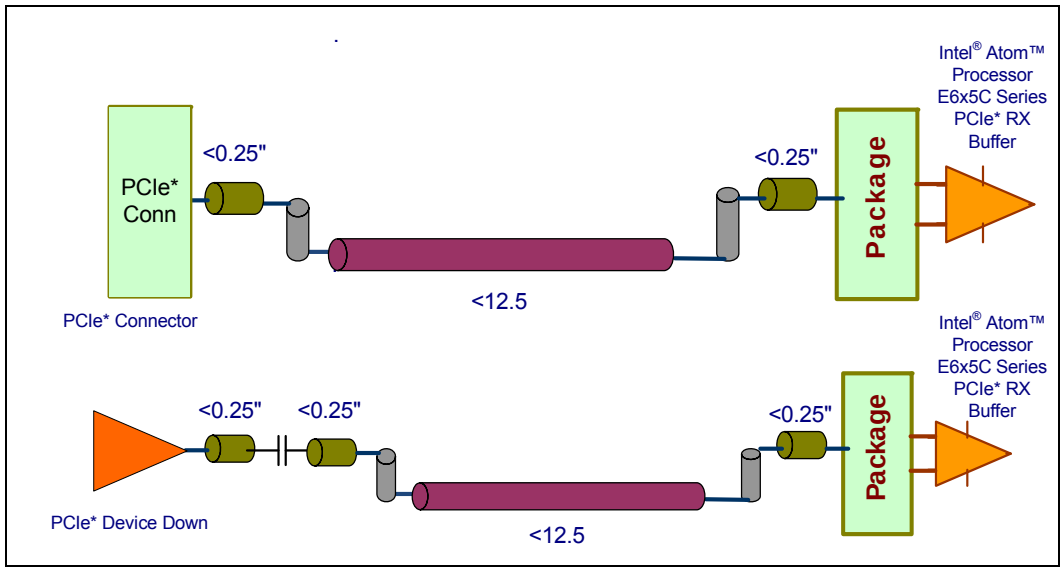


Figure 32. PCI Express* Topology for Receive Signals



7.1.7 AC Coupling Capacitors

The PCI Express* specification requires that each lane of a PCI Express* link be AC coupled between the driver and receiver. The specification allows for the actual AC coupling capacitors to be located either on or off the die. However, it is anticipated that in most cases the AC coupling will be separate from the die and in the form of discrete capacitors on the motherboard itself. Use the following guidelines for AC coupling capacitors:

- 0.1 µF capacitors are a good choice because they are a common value and generally present in a typical bill of materials.

- Locate capacitors at the same linear location along the signals of a given differential pair.
  - No more than a 5 mils (0.127 mm) delta should exist between the differential signals on the trace segments on either side of the AC coupling capacitor.
  - There is no requirement to length match the routing from the Intel® Atom™ Processor E6x5C Series to the AC coupling capacitors between the differential pairs.
- Place the capacitors as close to each other as possible per DFM rules for each differential pair.
- Size 0402 capacitors are strongly encouraged; they have lower series inductance and occupy less board space.
  - The same capacitor package size should be used for each signal in a differential pair.
- Do not use C-pack capacitors. VNA measurements have shown that the loss across the channel due to crosstalk is great and causes a severe decrease in margin. Also, layout studies show that less than 10% board area is saved when using a 0504, x2, C-pack versus discrete 0402 capacitors.
- The breakout into and out of the capacitors should be symmetrical for both signal lines in a differential pair. Minimize this trace route in order to maximize the amount of coupling between the signals within the pair.

7.1.8 Unused PCI Express* Port

For customers that choose not to implement PCI Express*, it is possible to disable the ports. To disable all PCI Express* ports, the following design recommendations should be followed:

- PCIE_TX[P:N] and PCIE_RX[P:N] signals should left as No Connects.
- WAKE# signal should be pulled-up to $V_{CC33SUS}$ with a 680 Ω to 1 kΩ resistor.
- Both clocks (PCIE_CLKINN and PCIE_CLKINP) should be grounded.
- The ports must be disabled via software.

7.1.9 PCI Express* Compensation Pin (PCIE_ICOMPO, PCIE_ICOMPI, PCIE_RCOMP0) Recommendations

PCIE_ICOMPO is the output compensation pin for both current and resistance. PCIE_ICOMPI is the input compensation pin for current and PCIE_RCOMP0 is resistance compensation for PCI Express*. One pull-down (49.9Ω ±1% to ground) is shared between these 3 signals.

7.2 Serial Peripheral Interface (SPI)

The Intel® Atom™ Processor E6x5C Series provides serial peripheral interface for use in the system. It is used to support a single SPI compatible flash device.

7.2.1 SPI Interface Signals Description

Table 39. SPI Interface Signals

Group	Signal Name	IO Type	Description
Data	SPI_MOSI	LVTTL, 3.3 V	SPI serial output data from the Intel® Atom™ Processor E6x5C Series to the SPI flash device
Data	SPI_MISO	LVTTL, 3.3 V	SPI serial input data from the SPI flash device to the Intel® Atom™ Processor E6x5C Series
Clock	SPI_SCK	LVTTL, 3.3 V	SPI Clock output from the Intel® Atom™ Processor E6x5C Series
Chip Select	SPI_CS#	LVTTL, 3.3 V	SPI chip select

7.2.2 SPI Routing Guideline

7.2.2.1 SPI General Routing Guideline

- Signals can be routed on an external or internal layer while referencing solid ground planes.
- If signal is routed on internal layers, it is recommended to reference the signals to ground planes, top and bottom of the signal layer.
- No external termination is needed on these signals.
- Signal trace spacing to width ratio is 2:1.

Layer assignment can be either microstrip or stripline.

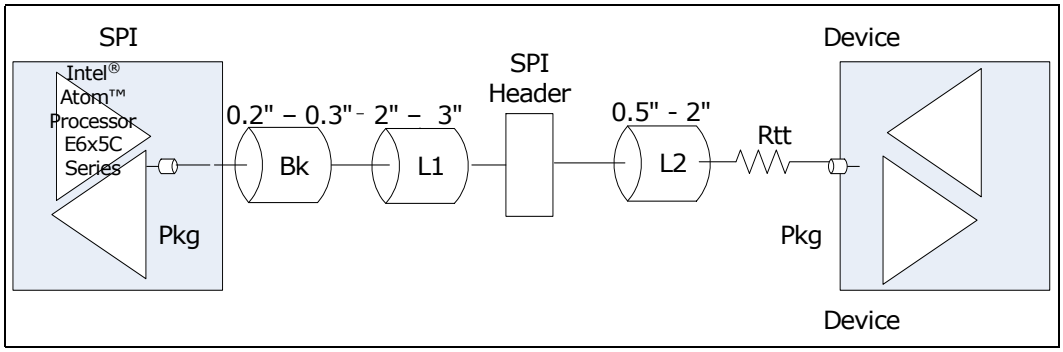
Table 40. SPI Trace Routing

Parameter[1]	Main Routing	Breakout Routing	Units	Target Single Ended Impedance
Mils				
Trace Width - Microstrip	4.5	4.5	mils	50 Ω ±15%
Trace Width - Stripline	4.3	4.3	mils	50 Ω ±15%
Minimum Bus-to-bus Spacing[2]	10	10	mils	50 Ω ±15%
Millimeters				
Trace Width - Microstrip	0.114	0.114	mm	50 Ω ±15%
Trace Width - Stripline	0.109	0.109	mm	50 Ω ±15%
Minimum Bus-to-bus Spacing[2]	0.254	0.254	mm	50 Ω ±15%

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Bus-to-bus spacing is the minimum spacing required between SPI Trace and neighboring non-SPI Trace signals.

7.2.2.2 SPI Signals Routing Topology

Figure 33. SPI Signals Routing Topology



Notes:
1. Layer assignment can be any—microstrip or stripline.
2. SPI signals require 50 Ω ±15% characteristic impedance.
3. Signals trace spacing to width ratio is 2:1.
4. The total trace length should < 5000mils (5” inch)
5. This topology requires the low R buffer if per device load is 15–40 pF.
6. Normal GPIO drive strength can be used for less than 15 pF.

Table 41. SPI Trace Length

Parameter	Description	Maximum Trace Length	
		Inches	Mils
BK	Breakout	0.3	300
L1	Breakout to SPI-header	3.0	3000
L2	SPI-header to device	2.0	2000

Notes:
1. Layer assignment can be any—microstrip or stripline.
2. SPI signals require 50 Ω ±15% characteristic impedance.
3. Signals trace spacing to width ratio is 2:1.
4. This topology requires the low R buffer if per device load is 15–40 pF.
5. Normal GPIO drive strength can be used for less than 15 pF
6. Rtt = 33 Ω ±5% near the load.

7.3 Intel® High Definition Audioβ

The architecture of the Intel® Atom™ Processor E6x5C Series - Intel® High Definition Audioβ (Intel® HD Audioβ) link allows a maximum of two CODECs to be connected. Intel® HD Audioβ clocking is provided from the Intel® Atom™ Processor E6x5C Series via HDA_CLK. HDA_CLK is a 24.000 MHz clock driven by the to any CODEC present on the link. HDA_CLK requires a 33 Ω ± 5% series termination resistor.

7.3.1 Intel® High Definition Audioβ Interface Signals

Table 42. Intel® High Definition Audioβ Interface Signals

Signal Name	Direction /Type	Description
HDA_RST_B	O CMOS_HDA	This signal is the reset to external codecs
HDA_SYNC	O CMOS_HDA	This is an 48-kHz fixed rate sample sync to the codec(s). It is also used to encode the stream number.
HDA_CLK	O CMOS_HDA	This is a 24.000MHz serial data clock generated by the Intel® HD Audioβ controller. This signal contains an integrated pull-down resistor so that it does not float when an Intel® HD Audioβ codec (or no codec) is connected.
HDA_SDO	O CMOS_HDA	This signal is a serial TDM data output to codec(s). The serial output is double-pumped for a bit rate of 48 MB/s for Intel® HD Audioβ.
HDA_SDI[1:0]	O CMOS_HDA	These serial inputs are single-pumped for a bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled.
HDA_DOCKEN_B	O CMOS_HDA	This active low signal controls the external Intel® HD Audioβ docking isolation logic. When deasserted, the external docking switch is in isolate mode. When asserted, the external docking switch electrically connects the Intel® HD Audioβ dock signals to the corresponding processor signals.
HDA_DOCKRST_B	O CMOS_HDA	This signal is a dedicated reset signal for the codec(s) in the docking station. It works similar to, but independent of, the normal HDA_RST_B signal.

7.3.2 Intel® High Definition Audioβ Layout Guidelines

Table 43. Intel® High Definition Audioβ Trace Routing

Parameter[1]	Main Routing	Breakout Routing	Units	Target Single Ended Impedance
Mils				
Trace Width - Microstrip	4.5	4.5	mils	50 Ω ±15%
Trace Width - Stripline	4.3	4.3	mils	50 Ω ±15%
Minimum Bus-to-bus Spacing[2]	10	10	mils	50 Ω ±15%
Millimeters				
Trace Width - Microstrip	0.114	0.114	mm	50 Ω ±15%
Trace Width - Stripline	0.109	0.109	mm	50 Ω ±15%
Minimum Bus-to-bus Spacing[2]	0.254	0.254	mm	50 Ω ±15%

Notes:
1. The geometry of the trace will impact the insertion loss, return loss, and the differential impedance.
2. Bus-to-bus spacing is the minimum spacing required between Intel® HD Audioβ Trace and neighboring non-Intel® HD Audioβ Trace signals.

Figure 34. Intel® High Definition Audioβ (Star Topology)

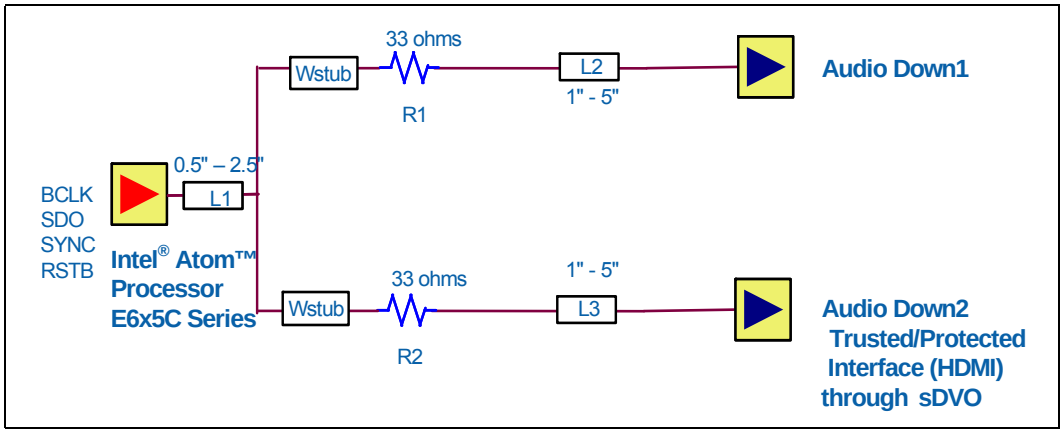


Table 44. Intel® High Definition Audioβ Segment Lengths (Star Topology)

Trace Length	Series Termination Resistance	Signal Length Matching
L1 = 0.5″ – 2.5″ (12.7 mm - 63.5 mm)	R1 = 33 Ω ±5% R2 = 33 Ω ±5%	N/A
L2 = 1″ – 5″ (25.4 mm - 127 mm)		
L3 = 1″ – 5″ (25.4 mm - 127 mm)		

Figure 35. Intel® High Definition Audioβ HDA_SDO (Device Down Topology)

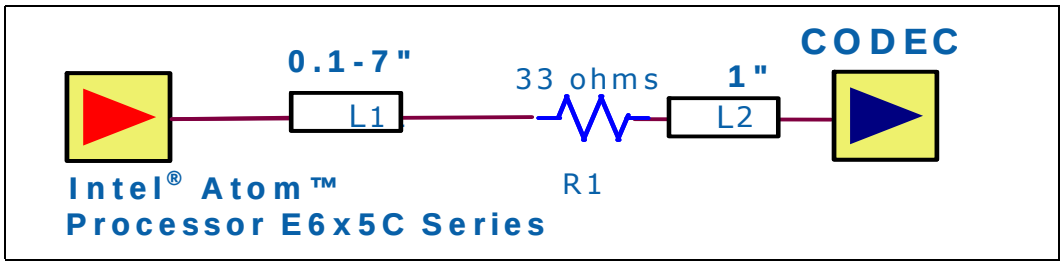
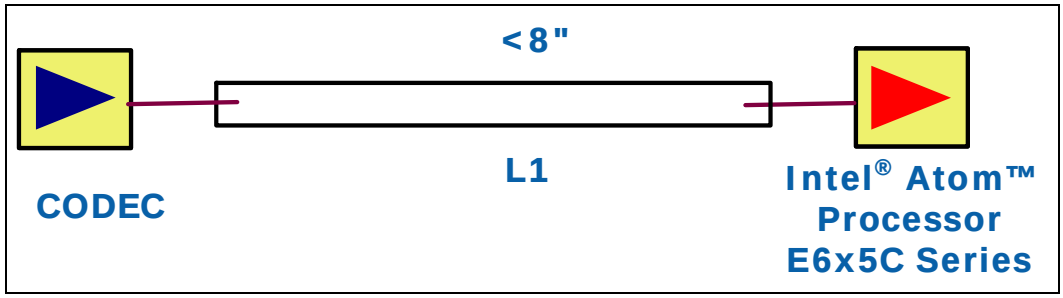


Table 45. Intel® High Definition Audioβ Segment Lengths (Device Down Topology)

Trace Length	Series Termination Resistance	Signal Length Matching
L1 = 0.1″ – 7″ (2.54 mm - 177.8 mm)	R1 = 33 Ω ±5%	N/A
L2 ≤ 1.0″ (25.4 mm)		

Figure 36. Intel® High Definition Audioβ HDA_SDI (Device Down Topology)



7.3.3 Audio Jack Connector Considerations

The audio jack connectors can be designed to support up to two analog audio jacks, each of which can signal user connection or disconnection to the operating system via sense resistors and a programmable GPIO signal.

7.3.3.1 Intel® High Definition Audioβ Reset (HDA_RST#)

HDA_RST# is the reset signal to external CODECs. This signal should have a series termination of 33 Ω ± 5%.

7.3.3.2 Intel® High Definition Audioβ Serial Data Out (HDA_SDO)

HDA_SDO is a serial TDM data output to the CODEC(s). The serial output is double-pumped for a bit rate of 48 Mb/s for Intel® HD Audioβ. This signal should have a series termination of 33 Ω ± 5%. It has a weak internal pull-down and should not be pulled high. However, a non-stuffed resistor site for a 1 kΩ ± 5% pull-up to 3.3 V should be provided.

7.3.3.3 Intel® High Definition Audioβ Serial Data In (HDA_SDI [1:0])

These signals are serial single-pumped input signals with bit rate of 24 MB/s. They have integrated pull-down resistors that are always enabled. Termination resistor is not necessary and these signals can be routed directly to the audio codec.

7.3.3.4 Intel® High Definition Audioβ Sync (HDA_Sync)

HDA_SYNC is a 48 kHz fixed rate sample sync to the CODEC(s). It is also used to encode the stream number. This signal should have a series termination of 33 Ω ± 5%. It has a weak internal pull-down and should not be pulled high.

7.3.3.5 Unused Intel® High Definition Audioβ Interface

HDI_SDI[1:0] can be left unconnected if Intel® High Definition Audioβ is not in use.

7.4 SMBus 1.0 Interface

The Intel® Atom™ Processor E6x5C Series integrates an SMBus 1.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on system memory (if implemented on the PCB), thermal sensors, etc. The slave interface allows an external microcontroller to access system resources.

The SMBus interface on the Intel® Atom™ Processor E6x5C Series uses two signals, SMB_CLK and SMB_DATA, to send and receive data from components residing on the bus. These signals are used by the SMBus host, SMBus slave, and TCO controllers. These controllers reside inside the Intel® Atom™ Processor E6x5C Series.

7.4.1 SMBus Design Considerations

No single SMBus design solution will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Any extra bus capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times. The primary considerations in the design process which device class is supported (high/low power). Most designs use primarily high power devices.

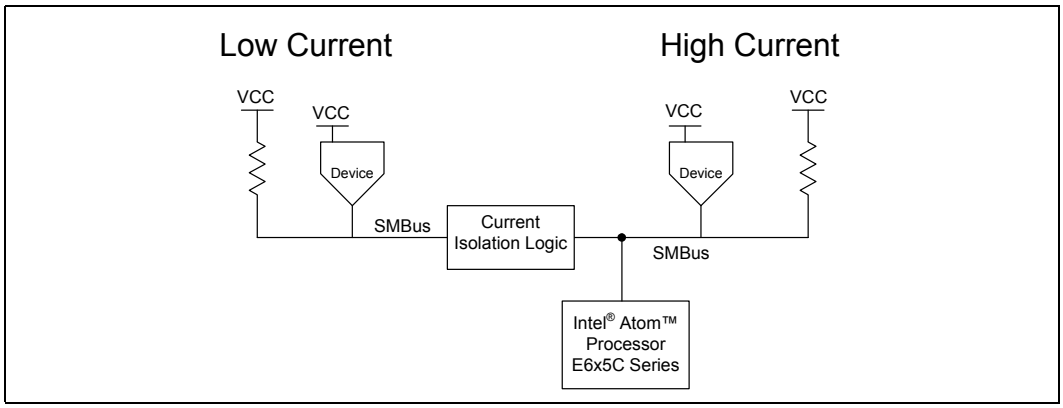
7.4.2 General SMBus Design Issues/Notes

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- It is recommended that I^2C* devices be powered by the V_{CC_CORE} supply. During an SMBus transaction in which the device is sending information to the Intel® Atom™ Processor E6x5C Series, the device may not release the SMBus if the Intel® Atom™ Processor E6x5C Series receives an asynchronous reset. V_{CC_CORE} is used to allow BIOS to reset the device if necessary. SMBus 2.0-compliant devices have a timeout capability which makes them insusceptible to this I^2C* issue, allowing flexibility in choosing a voltage supply.
- If SMBus is connected to PCI Express*, it must be connected to all PCI Express* slots.
- The SMBUS_ALERT# signal can be used to wake the system, generate an interrupt or generate an SMI#. This signal should be pulled-up to 3.3 V with 10 kΩ ± 10%.

7.4.3 High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices. The bus bridge can be a device like the Phillips PCA9518 (Refer to Figure 37.).

Figure 37. High Power/Low Power Mixed V_{CC} Architecture



7.4.4 Calculating the Physical Segment Pull-up Resistor

Table 46 and Table 47 are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, a bus bridge device must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 46. Bus Capacitance Reference Chart

Device	Number of Devices/ Trace Length	Capacitance Includes	Cap (pF)
Intel® Atom™ Processor E6x5C Series	1	Pin capacitance	12
CK505	1	Pin capacitance	5
Bus Trace Length in inches	24	2 pF per inch of trace length	48
	36		72

Table 47. Bus Capacitance/Pull-up Resistor Relationship

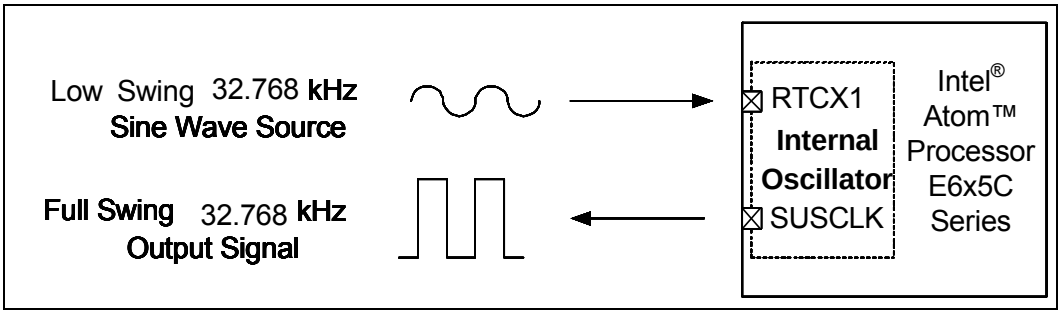
Physical Bus Segment Capacitance	Nominal Pull-up Value (for V_{CC} = 3.3 V)
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

7.5 RTC

The Intel® Atom™ Processor E6x5C Series contains a real time clock (RTC) with 256 bytes of battery-backed IO SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The Intel® Atom™ Processor E6x5C Series uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the Intel® Atom™ Processor E6x5C Series, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the Intel® Atom™ Processor E6x5C Series is called SUSCLK. This is illustrated in Figure 38.

Figure 38. RTCX1 and SUSCLK Relationship in Intel® Atom™ Processor E6x5C Series

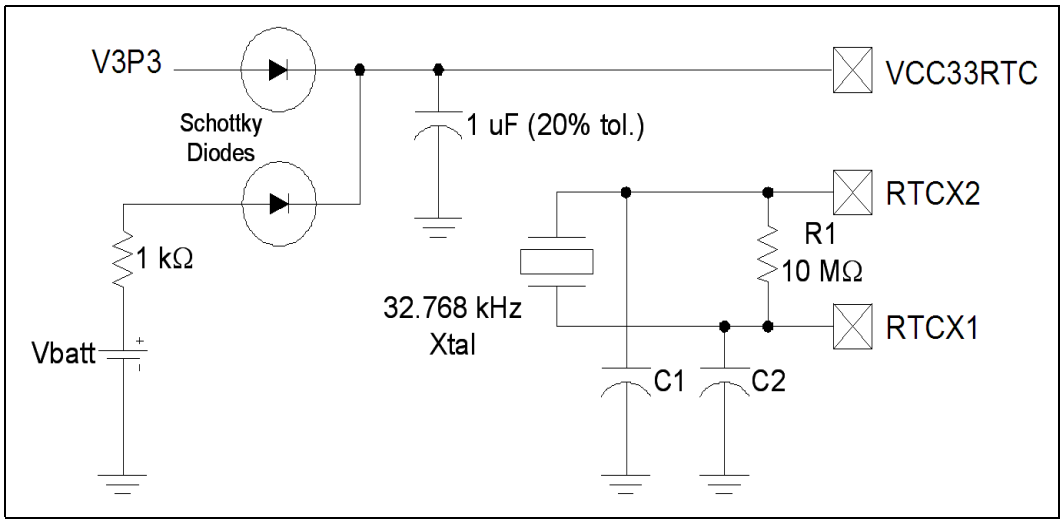


For further information on the RTC, consult Application Note *AP-728 ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for the Intel® Atom™ Processor E6x5C Series.

7.5.1 RTC Crystal

The Intel® Atom™ Processor E6x5C Series RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 39 documents the external circuitry that comprises the oscillator of the Intel® Atom™ Processor E6x5C Series RTC.

Figure 39. External Circuitry for Intel® Atom™ Processor E6x5C Series RTC



Notes:
1. The exact capacitor values for C1 and C2 must be based on the crystal maker recommendations. Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.
2. Reference designators are arbitrarily assigned.
3. V3P3 is active whenever the system is plugged in.
4. Vbatt is voltage provided by the battery.
5. $V_{CC33RTC}$, RTCX1, and RTCX2 are Intel® Atom™ Processor E6x5C Series pins.
6. $V_{CC33RTC}$ powers the Intel® Atom™ Processor E6x5C Series RTC well.
7. RTCX1 is the input to the internal oscillator.
8. RTCX2 is the feedback for the external crystal.

Table 48. RTC Routing Summary

RTC Routing Requirements	Maximum Trace Length to Crystal	Signal Length Matching	R1, R2, C1, and C2 Tolerances	Signal Referencing
5 mil trace width (results in ~2 pF per inch)	1 inch	NA	R1 = 10 M ±5% C1 = C2 = (NPO class) See Section 7.5.2 for calculating a specific capacitance value for C1 and C2.	Ground

7.5.2 External Capacitors

To maintain the RTC accuracy, the values for the external capacitors C_1 and C_2 in Figure 39 should be chosen to provide the manufacturer's specified load capacitance (C_{load}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1}) \times (C_2 + C_{in2} + C_{trace2})] / [(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- C_{load} = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- C_{in1}, C_{in2} = input capacitances at RTCX1, RTCX2 balls of the processor. These values can be obtained in the *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*.
- C_{trace1}, C_{trace2} = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. A typical value, based on a 5 mils wide trace and a ½ ounce copper pour, is approximately equal to: C_{trace} = trace length x 2 pF/inch
- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C_1, C_2 can be chosen such that $C_1 = C_2$. Using the equation of C_{load} above, the value of C_1, C_2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C_2 can be chosen such that $C_2 > C_1$. Then C_1 can be trimmed to obtain the 32.768 kHz.

In certain conditions, both C_1, C_2 values can be shifted away from the theoretical values (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C_1, C_2 values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values C_1, C_2 in the case that theoretical values cannot guarantee the accuracy of the RTC in low temperature condition.

Example 1.

According to a required 12 pF load capacitance of a typical crystal that is used with the Intel® Atom™ Processor E6x5C Series, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C_1, C_2 are chosen to be 6.8 pF instead of 10 pF, the RTC will oscillate at a higher frequency at room temperature (+23 ppm) but this configuration of C_1/C_2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and 2 is the practical value.

Note that the temperature dependency of crystal frequency is a parabolic relationship (ppm/degree square). The effect of changing the crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

7.5.3 RTC Layout Considerations

Since the RTC circuit is very sensitive and requires high accuracy oscillation, reasonable care must be taken during layout and routing of the RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. The Intel® Atom™ Processor E6x5C Series requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of the board's material. On FR-4, a 5 mil trace has approximately 2 pF per inch.
- Trace signal coupling must be limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2.
- Ground guard plane is highly recommended.
- The oscillator V_{CC} should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

7.5.4 RTC External Battery Connections

The RTC requires an external battery connection to maintain its functionality and its RAM while the Intel® Atom™ Processor E6x5C Series is not powered by the system.

Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 6 µA, the battery life will be at least:

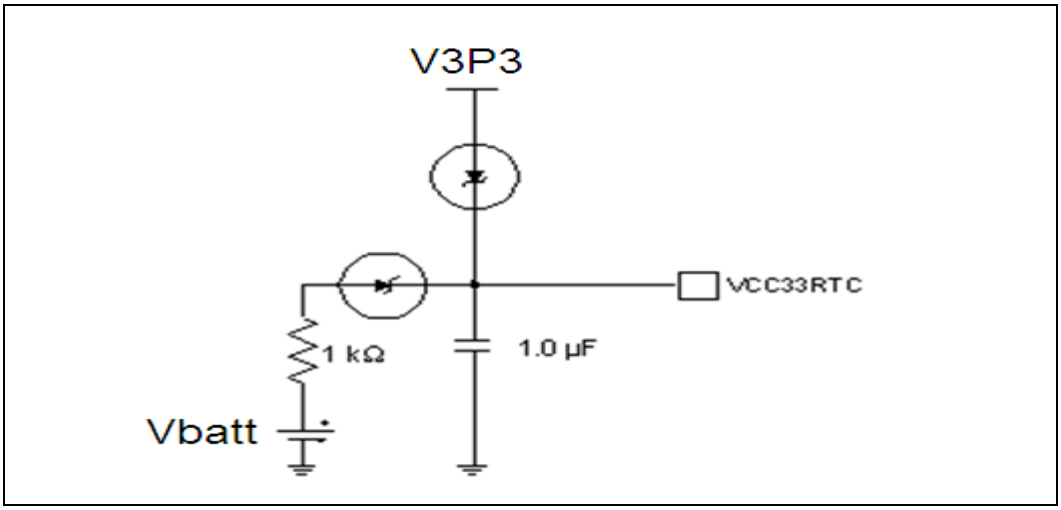
170,000 µAh / 6 µA = 28,333 h = 3.2 years

The above example is not applicable to the Intel® Atom™ Processor E6x5C Series because the average RTC current for the processor is between 33 µA and 36 µA.

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the Intel® Atom™ Processor E6x5C Series via a Schottky diode circuit for isolation. The Schottky diode circuit allows the Intel® Atom™ Processor E6x5C Series RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 40 is an example of a diode circuit that is used.

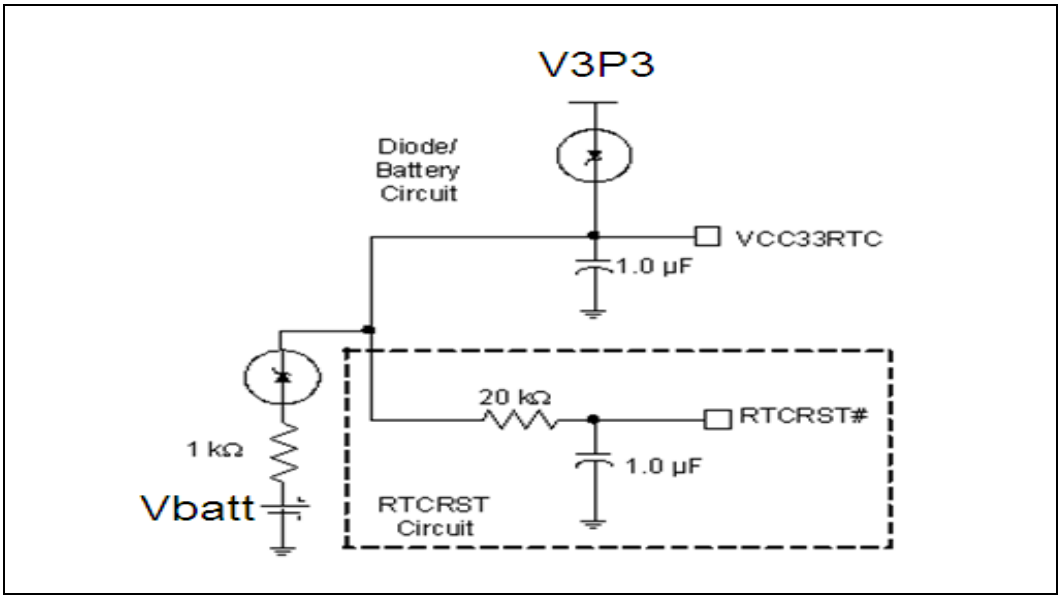
Figure 40. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a mobile system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

7.5.5 RTC External RTCRST# Circuit

Figure 41. RTCRST# External Circuit for Intel® Atom™ Processor E6x5C Series



Intel® Atom™ Processor E6x5C Series RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBATT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be 5 ms or longer. Any resistor and capacitor combination that yields the proper time constant is acceptable although it is recommended that 20 kΩ and 1.0 µF be used.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 40) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 41 is an example of this circuitry that is used in conjunction with the external diode circuit.

Note: Unlike many previous products,Intel® Atom™ Processor E6x5C Series does not use RTCRST# to clear CMOS. RTCRST# does not set a bit which BIOS can then read as a directive to clear CMOS.

Note: For the E6x5C B0 stepping device, a platform and BIOS based work-around is required to ensure the voltage supplied to the internal RTC does not violate the input specification. Please refer to document #463022 "Intel Atom E6xx series Erratum: Voltage supplied to Internal RTC Logic violates design specification" for detailed information.

7.5.6 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30% and 70%. If the SUSCLK duty cycle is beyond the 30% – 70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe) and it is an appropriate signal to check the RTC frequency to determine the accuracy of the Intel® Atom™ Processor E6x5C Series RTC Clock (see Application Note AP-728 for further details).

7.5.7 RTC-well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#) must be either pulled up to $V_{CC33RTC}$ or pulled-down to ground while in the G3 state. RTCRST# when configured as shown in Figure 41 meets this requirement. RSMRST# should have a weak external pull-down to ground. This will prevent this node from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. A weak (10 kΩ) external pull-down should also be used on the PWROK input.

7.6 LPC Guidelines

The following section details the schematic requirements for the signals on the LPC Interface.

7.6.1 Clock Run (LPC_CLKRUN#)

This signal gates the operation of the LPC_CLKOUTx. Once an interrupt sequence has started, LPC_CLKRUN# should remain asserted to allow the LPC_CLKOUTx to run. This signal should be pulled-up to 3.3 V with a 10 kΩ ± 1%.

7.6.2 Serial Interrupt Request (LPC_SERIRQ)

This signal conveys the serial interrupt protocol. This signal should be pulled-up to 3.3 V with a resistor sized between 8.2 kΩ ± 10% and 10 kΩ ± 1%.

7.6.3 Intel® Trusted Platform Module$^{\varepsilon}$ Guidelines

Intel® Trusted Platform Module$^{\varepsilon}$ (Intel® TPM$^{\varepsilon}$) functionality is a Trusted Computing Group (TCG) low cost security solution to increase confidence about system security. The Intel® TPM$^{\varepsilon}$ is a device that resides on the motherboard and is connected to the Intel® Atom™ Processor E6x5C Series using the low pin count (LPC) bus to communicate with the rest of the platform.

Today, most protection against computer viruses and unauthorized intrusions consists of adding and updating software that installs outer barriers and surveillance tools. The goal of safer computing is to go much deeper, integrating a level of trust into the actual hardware and pre-operating system environments. Applications intended for e-Business are based on trust in the communication partner and the reliability of the connection.

The objective of the Intel® TPM$^{\varepsilon}$ is to establish a baseline of platform integrity and enhance system security. Intel® TPM$^{\varepsilon}$s are available from several integrated circuit vendors in the form of a silicon component and accompanying software. When integrated into the platform, a Intel® TPM$^{\varepsilon}$ provides protected storage of platform data allowing for platform level authentication toward the goal of making data files, transactions and communication more trustworthy.

For more information on Intel® TPM$^{\varepsilon}$s and safer computing, refer to the TCG Web site: http://www.trustedcomputinggroup.org.

Table 49. Intel® Trusted Platform Module$^{\varepsilon}$ Signals

Group	Signal Name	Intel® Atom™ Processor E6x5C Series Signal Name	Description
Address Data	LAD[3:0]	LPC_AD[3:0]	Address/Data Lines
Clock	LCLK	LPC_CLKOUT[2:0]	Clock
Reset	LRESET#	RESET#	Reset
Control	LFRAME#	LPC_FRAME#	Cycle termination
	SERIRQ	LPC_SERIRQ	Serialized IRQ

7.6.3.1 Intel® Trusted Platform Module$^{\varepsilon}$ Design Considerations

Note: To properly reset Intel® TPM$^{\varepsilon}$ devices requiring a clock while reset is asserted, connect the RESET# going to Intel® Atom™ Processor E6x5C Series to Intel® TPM$^{\varepsilon}$ LRESET# pin. Intel® Atom™ Processor E6x5C Series will start driving the LPC clocks once it comes out of reset, so an appropriate delay between RESET# and LRESET# must be added (depending on the Intel® TPM$^{\varepsilon}$ device being used).

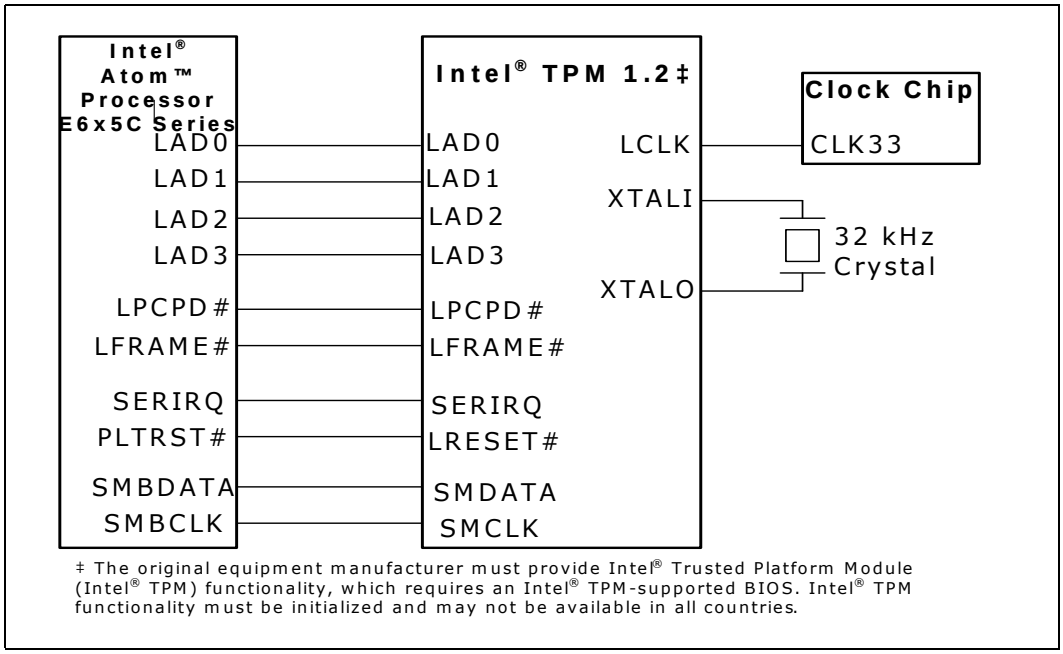
Routing requirements for the Intel® TPM$^{\varepsilon}$'s LPC interface are as follows:

- LAD[3:0] are shared with the Firmware Hub (FWH) component and the Super I/O (SIO) device
- LCLK should be connected to a 33 MHz clock
- LFRAME# is shared with FWH and the SIO
- SERIRQ is shared with the SIO

Figure 42 is a block diagram showing the Intel® TPM$^{\varepsilon}$ interconnect with Intel® Atom™ Processor E6x5C Series. Some of the LPC signals shown in the block diagram are shared with other LPC components that reside on the LPC interconnect such as the SIO and the FWH. It is important to note that Intel® TPM$^{\varepsilon}$ 1.2 devices are not pin compatible with previous generation Intel® TPM$^{\varepsilon}$ 1.1 devices.

Refer to the Intel® TPMε vendor documentation for additional Intel® TPMε specific design considerations.

Figure 42. Intel® Trusted Platform Moduleε 1.2/Intel® Atom™ Processor E6x5C Series Block Diagram



7.6.3.2 Motherboard Placement Considerations

Optimum routing can typically be achieved by placing the Intel® TPMε in proximity to the Intel® Atom™ Processor E6x5C Series or other LPC peripherals (e.g., Firmware Hub, Super I/O).

The Intel® TPMε is a security device that should be shielded as much as possible from physical access. In high security implementations, a number of mechanisms can be used to detect or prevent physical system intrusion, but such mechanisms are beyond the scope of this design guide.

7.7 Intel® Atom™ Processor E6x5C Series Strapping Requirements

Table 50. Intel® Atom™ Processor E6x5C Series Strapping Requirements

Pin Name	Strap Definition	Configuration	Notes
GPIO_SUS[0]	Strapping to define memory device width	0: x16 devices 1: x8 devices	Note 2
GPIO_SUS[6:5]	Strapping for memory device densities	00: 256 Mb 01: 512 Mb 10: 1 Gb 11: 2 Gb	Note 2
GPIO_SUS[8]	Strapping to memory define number of ranks	0: 2 Rank 1: 1 Rank	Note 2
GPIO[3:2]	Strapping for CMC base address	00: FFFB0000h 01: FFFC0000h 10: FFFE0000h 11: FFFD0000h	Note 1 and Note 2
GPIO[4]	LPC[0] Clock buffer strength control	0: 1 load driver strength 1: 2 load driver strength	Note 2

Notes:

1. A resistor is not required if the default CMC address is used (FFFD0000h). A resistor is only required if the default CMC address is to be overwritten. The signal must not be connected to an impedance of less than 100 kΩ before PWROK assertion, unless the default CMC address is being overridden.
2. Default internal pulled-up. To strap to a 0 value, it is recommended to use a 1 kΩ ± 1% pull-down to GND.

§ §

8.0 Platform Power Delivery and Power/Thermal Management

8.1 Chapter Contents

This chapter contains information about:

- Definitions
- Platform Power Architecture
- Intel® Atom™ Processor E6x5C Series Power Delivery, Decoupling, and Layout Guidelines
- Platform Power Sequencing Requirements
- Intel® Atom™ Processor E6x5C Series Thermal Management Interface Signals
- Miscellaneous Platform Power Management
- Information relating to the Power delivery for the E6x5C FPGA portion is discussed in chapter 11 “FPGA power supply design”.

8.2 Definitions

Table 51 defines power terminology used throughout this chapter. Table 52 defines the system power states supported by the platform.

Table 51. System State and Power Delivery Definitions

Term	Definition
Full-power Operation	During full-power operation, all components remain powered. Full-power operation is synonymous with the S0 state.
Suspend Operation	The platform supports a number of suspend states such as Suspend-to-RAM (S3), Suspend-to-disk (S4), and Soft-off (S5). During suspend operation, power is removed from some components on the motherboard.
Core Power Rail	A power rail that is only on during full-power operation.
Standby Power Rail	A power rail that is on during a suspend operation (S3, S4, or S5). The rail is also on during full-power operation.
Derived Power Rail	A derived power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, V3P3_A is usually derived (on the motherboard) from V5_A using a voltage regulator.

Table 52. Supported System Power States (S-states)

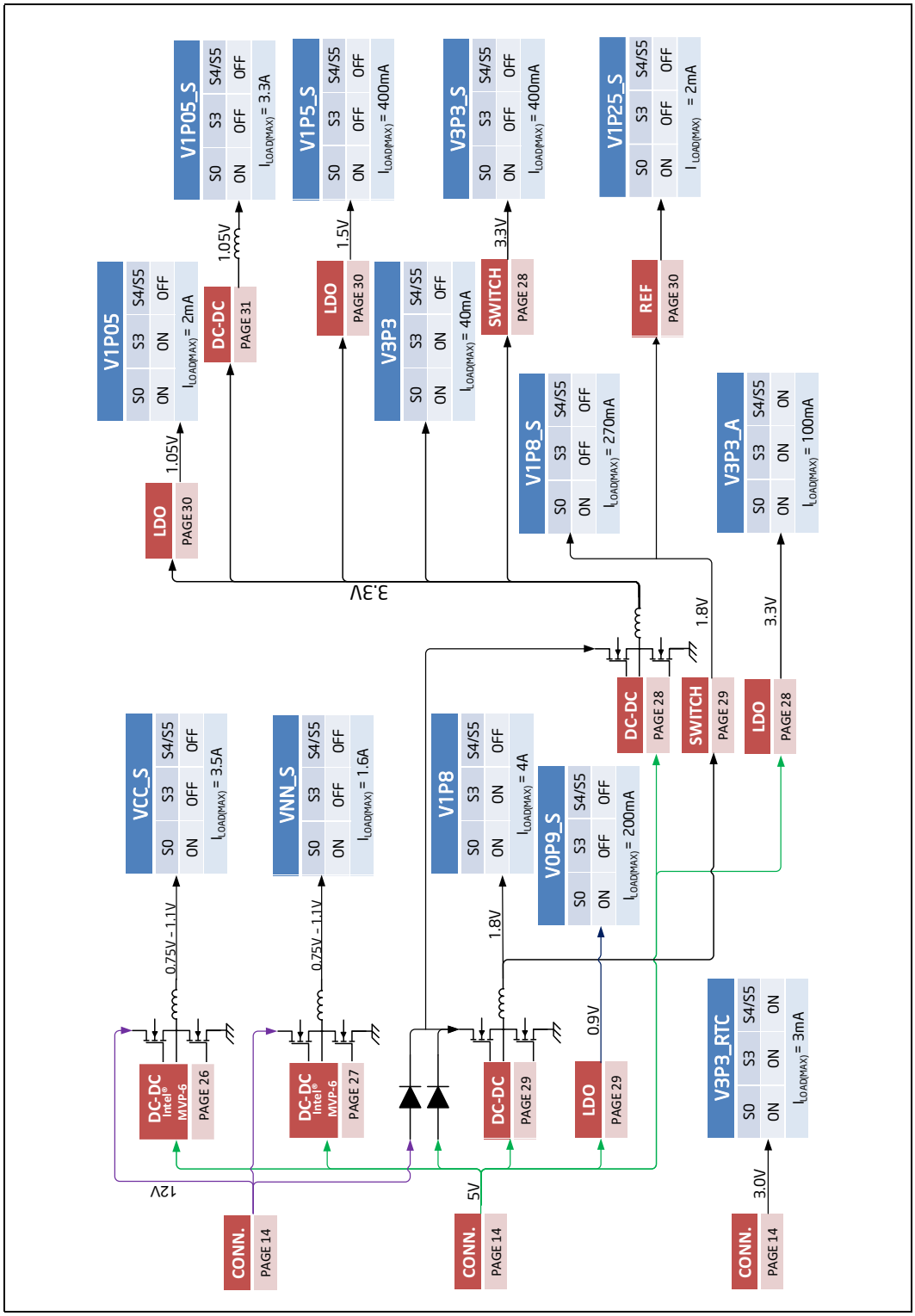
State Name	Description	Notes
S0 (Full on operation)	All components on the motherboard are powered and the system is fully functional.	
S3 (Suspend to RAM)	The system state/context is stored in main memory and all unnecessary system logic is turned off. Main memory and logic which are required to wake the system must remain powered. The SLP_S3_N signal should be used to remove power from any logic which is not required to wake the system from the S3 state.	
S4 (Suspend to Disk)	The system state/context is stored in non-volatile secondary storage (e.g., a hard disk drive) and all unnecessary system logic is turned off. Only logic which is required to wake the system remains powered.	
S5 (Soft-off)	The S5 state corresponds to the G2 global state. Restart is only possible with the power button.	

8.3 Platform Power Architecture

Figure 43 shows the power delivery architecture of Intel's Little Bay customer reference board (CRB) for an example platform. The solutions given in this document are only examples, as there are many power distribution methods that achieve similar results. Designers should work directly with their voltage regulator vendors of choice to ensure a robust power delivery solution for the platform.

The following power rails, as depicted below, are either standard platform rails or rails required by the Intel® Atom™ Processor E6x5C Series. Customer platforms may or may not have additional rails depending on system ingredients and architecture. Rail implementation can also vary depending on system configuration. This platform power architecture reflects usage of most of Intel® Atom™ Processor E6x5C Series features.

Figure 43. E6x5C CPU Power Delivery Map



Note: $I_{LOADMAX}$ refers to the maximum current for voltage regulators.

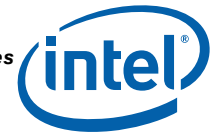


Table 53. Intel® Atom™ Processor E6x5C Series Maximum Design Power

Platform Power Planes	Voltage (V)	Current[1] (mA)	S4/S5	S3	S0	Description[2]
VCC_S	0.3 for C6, 0.75 to 1.15 depending on AVID	3500	Off	Off	On	CPU Core. Intel® MVP-6 compliant. ±3%[3]
VNN_S	0.75 to 0.9875 depending on AVID	1600	Off	Off	On	North Cluster and GFX Core. Intel® MVP-6 compliant. ±5%[3]
V0P9_S	0.9	200	Off	Off	On	DDR2 Termination. ±2%[3]
V1P05	1.05	100	Off	On	On	Legacy Core Suspend Well, CPU C6 SRAM, Fuses. ±2%[3]
V1P05_S	1.05	3300	Off	Off	On	CPU VTT, Legacy Core. ±2%[3]
V1P25_S	1.25	2	Off	Off	On	LVDS bandgap. ±2%[3]
V1P5_S	1.5	400	Off	Off	On	CPU PLL, HPLL, Thermal Sensors, SDVO, PCIe* digital, analog and PLL. ±2%[3]
V1P8_S	1.8	570	Off	Off	On	LVDS analog and digital, DDR core. ±5%[3]
V1P8	1.8	4000	Off	On	On	DDR core self-refresh, DDR DRAM main and self-refresh. ±5%[3]
V3P3_S	3.3	400	Off	Off	On	3.3 V Legacy IO, 3.3 V PCIe* bandgap, SPI Flash. ±5%[3]
V3P3	3.3	40	Off	On	On	3.3 V Legacy IO sustain. ±5%[3]
V3P3_RTC	3.3	3	On	On	On	RTC Well.

Notes:
1. Currents are I_{CC_MAX} for common system components. Large general use platform rails will vary depending on system load.
2. Describes larger loads on each rail and may vary depending on system configuration. The table above covers the Intel® Atom™ Processor E6x5C Series requirement only.
3. Tolerance should be taken at the load component motherboard pad. The ±% is DC and AC up to 1 MHz.
4. V3P3_A power plane is required by Platform System Management Controller and CK505.

8.3.1 Platform Power Rails

8.3.1.1 Core Rails (VCC_S, VNN_S)

The Core supplies are an output of the Intel® MVP-6 compliant voltage regulators and supply power to the core rails of the Intel® Atom™ Processor E6x5C Series.

8.3.1.2 1.05 V Rail (V1P05, V1P05_S)

The 1.05 V rail supplies many core parts of the Intel® Atom™ Processor E6x5C Series. It is also used for the processor signals of the ITP-XDP debug port (if used). Because of the 3.3A max loading, a switching regulator is recommended. The controller also should have light load features to optimize efficiency during sleep states.

8.3.1.3 1.25 V Rail (V1P25_S)

The 1.25 V rail supplies the Intel® Atom™ Processor E6x5C Series LVDS external voltage reference. A light load linear regulator is recommended to optimize efficiency during sleep states.

8.3.1.4 1.5 V Rail (V1P5_S)

This power source (known as V_{CCA}) is required to power the PLL clock generators on the silicon. The Intel® Atom™ Processor E6x5C Series has a 1.5 V internal voltage regulator to feed the resume well during suspend, so the main 1.5 V VR need only supply the V1P5_S rail on these platforms.

The loading on the 1.5 V VR is moderate on this platform, so a linear voltage regulator is recommended. The controller used should also have light load features to optimize efficiency during sleep states. Output decoupling should be sized appropriately so that the rails remain within its 2% tolerance at the load.

8.3.1.5 DDR Rails (V1P8, V0P9)

The Intel® Atom™ Processor E6x5C Series supports DDR2 memory technology, which requires 1.8 V for V1P8 and 0.9 V for V0P9 ($V_{REF)}$. Tolerance on V1P8 is ±5% and V0P9 or V_{REF} is V1P8/2 ±2%.

Because the V1P8 loading requirements can be quite large depending on the maximum memory populated in the system, a switching voltage regulator must be used. $V_{REF,}$ as recommended in the JEDEC spec, should be driven with a buffer. Many DDR voltage regulator solutions have a buffered V_{REF} output integrated into the controller. The controller used should also have light load features to optimize efficiency during low power or sleep states. Output decoupling should be sized appropriately so that the rails remain within tolerance at the load during periods of maximum AC transients.

8.3.1.6 3.3 V Rails (V3P3, V3P3_A, V3P3_S)

The 3.3 V rail is the most prolific rail on the platform. Most circuits on the platform use it, including the Intel® Atom™ Processor E6x5C Series. There are three versions of the 3.3 V rail that are generated by the voltage regulator: the main rail (V3P3), an Always version (V3P3A), and a Sleep version (V3P3S).

Because of the significant loading requirements on the 3.3 V regulator, a switching regulator should be used. The controller used should also have light load features to optimize efficiency during sleep states. In addition, the FETs used for the sleep rail generation should be chosen with a low R_{DSon} to minimize conduction losses. Output decoupling should be sized appropriately so that the rails remain within its 5% tolerance at the load.

8.3.1.7 5 V Rails (V5_A, V5_S)

There are two version of 5 V rails. The V5_A rail, an Always version is supplied by carrier board through COM Express* connector. This rail can be used to generate 3.3 V and DDR rails. The Sleep version rail, V5_S is a switched rail and is enabled in S0 only.

8.3.1.8 12 V Rail (V12_S)

The 12 V rail is supplied by external AC/DC adaptor. Most of the power rails can be derived from V12_S using on board voltage regulator.

8.3.2 S-state Management

Table 54 describes which supply rails are powered in each of the different power management states.

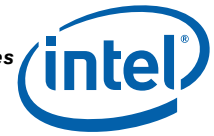


Table 54. Power Management State vs. Power Rail State

State	Signal/Voltage Rail					
	SMC S3_B Signal	SMC S4_B/S5_B Signal	V*P*_A	V*	V*P*_S	Clocks
S0	High	High	On	On	On	On
S3	Low	High	On	On	Off	Off
S4/S5	Low	Low	On	Off	Off	Off

Note: V12_S is an exceptional case for voltage rail type V*P*_S. V12_S voltage rail is always ON.

Power management transitions are handled by a System Management Controller (SMC) and on the platform. The SMC interfaces with the Intel® Atom™ Processor E6x5C Series via the SLPMODE, SLPRDY_B and RSTRDY_B signals on the Intel® Atom™ Processor E6x5C Series to determine Intel® Atom™ Processor E6x5C Series driven power transitions. The Intel® Atom™ Processor E6x5C Series must implement inputs for the SLPMODE, SLPRDY_B and RSTRDY_B signals for proper S-state power management. The Intel® Atom™ Processor E6x5C Series notifies the SMC of the type of S-state transition (e.g., S0 to S3) via the SLPMODE signal. The Intel® Atom™ Processor E6x5C Series then notifies the SMC that the Intel® Atom™ Processor E6x5C Series is ready to for the SMC to begin shutting down or powering on the system VRMs. Detailed timing diagrams can be found in the *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*.

8.4 Intel® MVP-6 Power Delivery, Decoupling, and Layout Guidelines

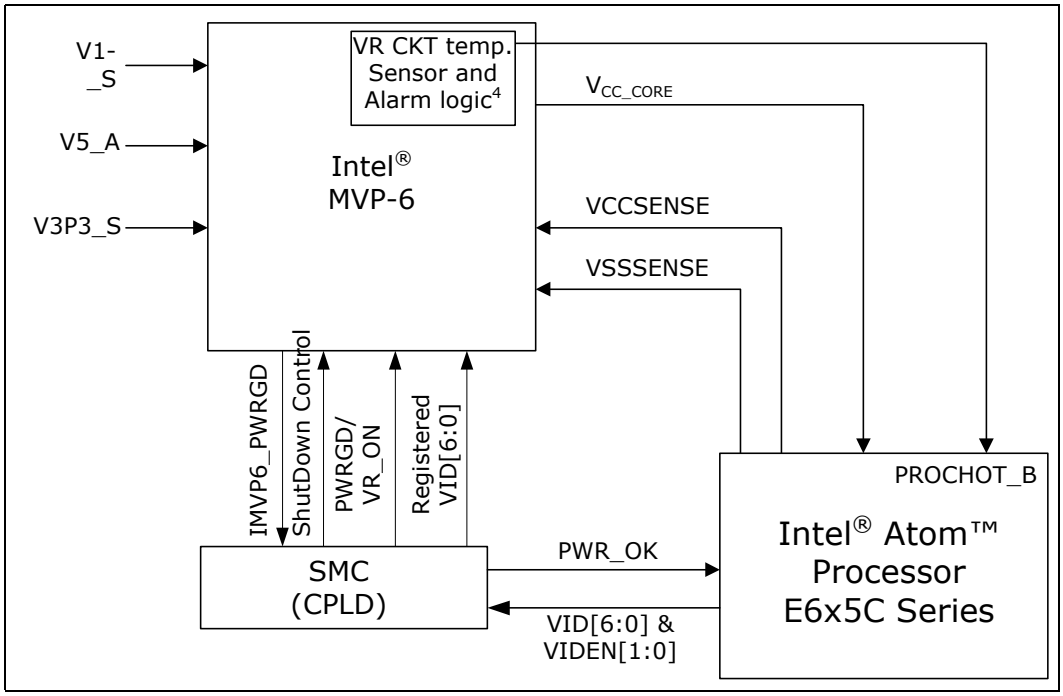
8.4.1 Power Delivery Architecture

An Intel® Mobile Voltage Positioning-6 (Intel® MVP-6) voltage regulator (VR) is used to regulate power to the core of the Intel® Atom™ Processor E6x5C Series. The Intel® Atom™ Processor E6x5C Series supports Enhanced Intel SpeedStep® Technology$^{\theta}$ which enables dynamic selection of different performance modes by dynamically changing the core operating voltage without resetting the system.

As shown in Figure 44, the Intel® MVP-6 receives three input power rails: V12_S, V5_A, and V3P3_S.

- V12_S is one of the main power input from ATX Power Supply.
- V5_A also is the 5 V Standby power input from ATX Power Supply. This rail is typically used to provide drive power to the MOSFET gate driver.
- V3P3_S is the output rail of the 3.3 V VR. This is typically used to provide power to VR controller and miscellaneous logic and pull-ups.

Figure 44. Intel® MVP-6 Voltage Regulator Block Diagram



Notes:

1. DPRSLPVR (Deep Sleep Voltage Regulator) is not supported by the Intel® Atom™ Processor E6x5C Series and should be tied to ground at the Intel® MVP-6 controller.
2. VID[6:0] and VIDEN[1:0] are used to control the VCC (CPU core) and VNN (Graphics core) voltage.
3. When VIDEN[0] is asserted, VID is valid for VCC; when VIDEN[1] is asserted, VID is valid for VNN
4. When VIDEN is asserted, VID signals need to be latched/registered and continue to be driven to the controller.
5. Thermal throttling may alternately be implemented using an external, discrete thermal sensor.

Some important points to note in this block diagram are as follows:

- The platform relies on a system management controller (SMC) to monitor the platform power good including IMVP6_PWRGD.
- VR_ON is generated by the logic AND of V_{CCP} and the system power good indicator. This may be implemented through glue logic or controlled by the SMC directly.
- As defined in the Intel® MVP-6 specification, the PSI_B signal is used for improved efficiency under light loads. This processor does not directly drive PSI_B to the voltage regulator. Designers should work directly with their Intel® MVP-6 vendor of their choice to ensure their power delivery solution is enabled for light load mode support.

8.4.1.1 V_{CC} Power Delivery

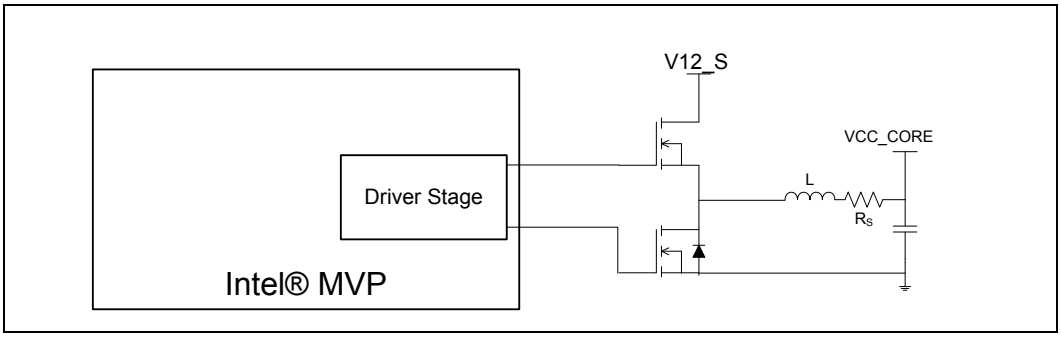
The Intel® MVP-6 mobile processor core regulator supplies the required voltage and current to the processor. Details on the load line specification and implementation features can be found in the *Intel® Mobile Voltage Positioning (Intel® MVP), 6 Voltage Regulation – Product Specification*.

The Intel® MVP-6 controller has been designed to control a minimum of one phase. In a single-phase topology, the duty cycle of the control (top) MOSFET is roughly the ratio of the output voltage and the input voltage. Due to the small ratio between V_{CC} and V12_S, the duty cycle of the Control MOSFET is very small. The main power loss in the Control MOSFET is therefore due to the transition or switching loss as it switches on

and off. To minimize the transition loss in the Control MOSFET, its transition time must be minimized. This is usually accomplished with the use of a small-size MOSFET. Or similarly, the duty cycle of the Synchronous MOSFET is very large; hence, to minimize the DC loss of the Synchronous MOSFET, its R_{DS-ON} must be small. This is usually accomplished with the use of a large-size MOSFET or several small-size MOSFETs connected in parallel. Care must be taken with this solution to properly minimize the effect of the Gate-glitch phenomenon in the synchronous MOSFET, as it can lead to shoot-through current due to C_{GD} charge coupling effect.

Refer to Figure 45 for a block diagram of a single-phase topology.

Figure 45. Intel® MVP-6 Single-phase Topology Example

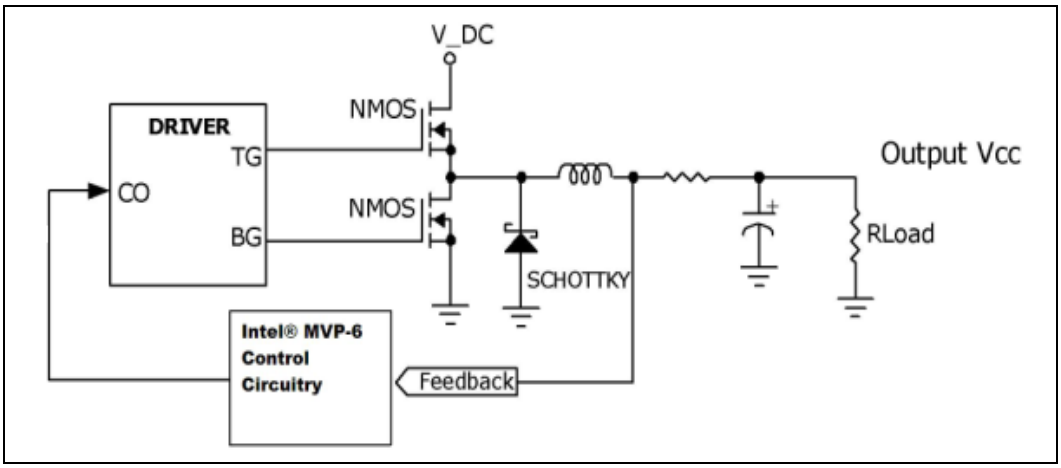


Notes:
1. Some solutions will use sense resistors (R_S above), others will use DCR current sensing of output inductor L.
2. Driver stage may be integrated into the Intel® MVP-6 depending on supplier implementation.

8.4.1.2 $V_{CC-CORE}$ Voltage Regulator Design Recommendations

Figure 46 shows a traditional Buck VR topology.

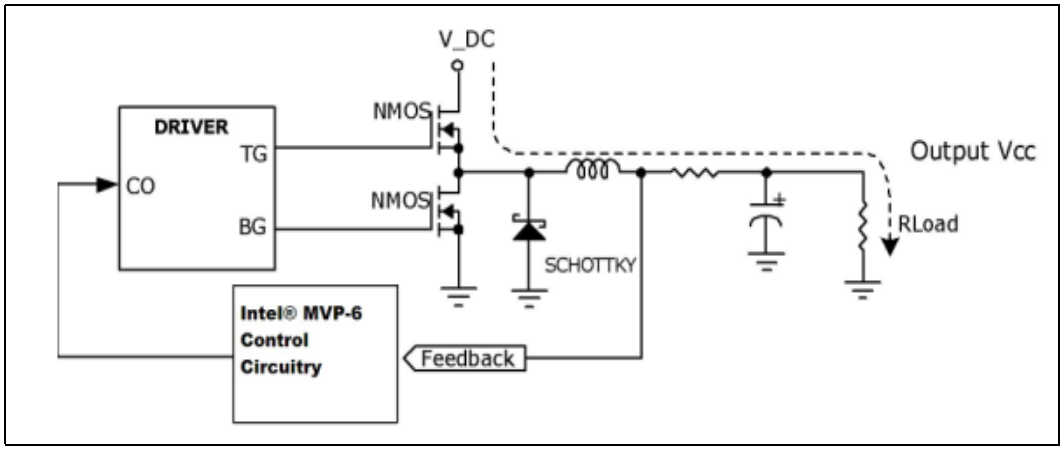
Figure 46. Buck Voltage Regulator Example



8.4.1.2.1 High-current Path, Top MOSFET Turned ON

The dashed-arrow line in the figure below indicates the high-current path when the top MOSFET is ON. Current flows from the V_DC or V12_S power source, through the top MOSFET (There may be more than one of these), through the inductor and sense resistor, and finally through the processor, RLoad, to ground. The components and current paths shown must be able to not only carry the high current through the processor, but the power source and ground must also be adequate.

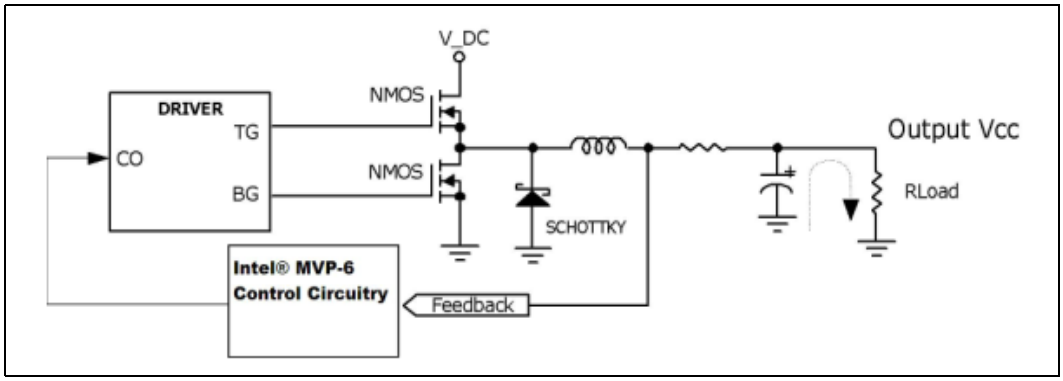
Figure 47. High Current Path with Top MOSFET Turned On



8.4.1.2.2 High-current Paths during Abrupt Load Current Changes

During abrupt changes in the load current, the bulk and decoupling capacitors must supply current for the brief period before the regulator circuit can respond. The dashed-arrow line in Figure 48 illustrates this current path. Stray inductance and resistance become a major concern and if they are not minimized, they can compromise the effectiveness of the capacitors. Bulk capacitors for V_{CC} should be located at the highest current density points. These high-density points are located along the shortest route between the processor core and the sense resistor. Using short, fat traces or planes can minimize both stray inductance and resistance.

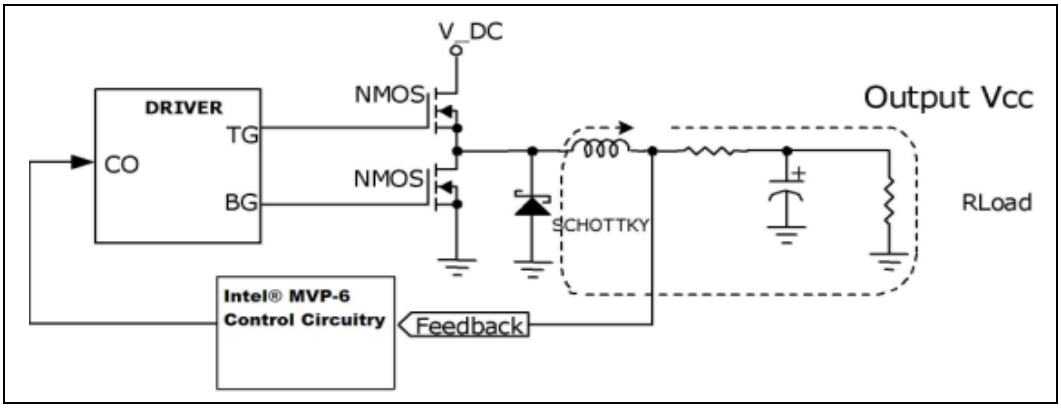
Figure 48. High Current Path During Abrupt Load Current Changes



8.4.1.2.3 High-current Paths during Switching Dead Time

When the top MOSFET turns OFF and before the bottom MOSFET (again, there may be more than one of these) is turned ON, the pattern of current flow changes. The inductor that is no longer being supplied current through the top MOSFET starts to collapse its magnetic field. The inductor literally becomes a generator at this point. The dashed-arrow line in the figure below shows the current path during the time that both top and bottom MOSFETs are OFF. This is termed "dead time." During dead time there is a high-current flow through the inductor, processor, ground, and the Schottky diode. The diode and its traces must be laid out in such as to minimize both stray inductance and resistance with short, fat traces or planes.

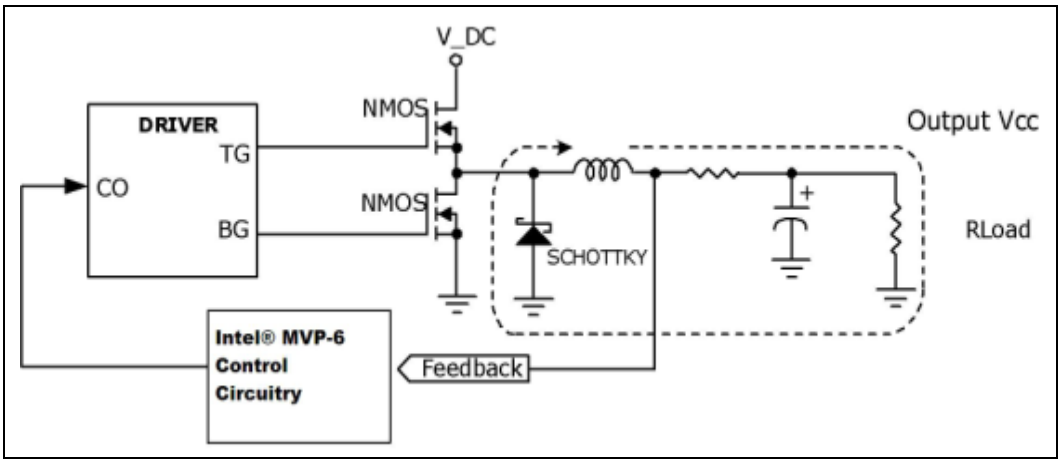
Figure 49. High-current Path with Top and Bottom MOSFETs Turned Off (Dead Time)



8.4.1.2.4 High-current Path with Bottom MOSFET(s) Turned ON

A few nanoseconds after the top MOSFET is turned OFF, the bottom MOSFET(s) is turned ON. The high-current path now switches from the Schottky diode to the bottom MOSFET(s), the current path shown by the dashed-arrow line in the figure below. Minimize stray inductance and resistance with short, fat traces, or planes.

Figure 50. High Current Path with Bottom MOSFET(s) Turned On

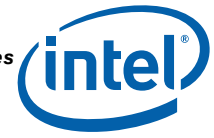


8.4.1.3 Intel® Atom™ Processor E6x5C Series Voltage Identification (VID)

The VID voltage is determined by the 7-bit VID code provided by the processor's voltage identification pins to the voltage regulator. The nominal VID value (as shown in Table 55) indicates the reference point that the VID provides for the static and ripple voltage. Due to voltage regulator tolerances, PCB parasitic and current draw variations, the average voltage seen at the processor may be slightly higher or lower than the reference value. However, voltage regulator designers must meet the entire range of processor load and processor static and ripple tolerance limits. $V_{CC\text{-}CORE}$ must meet the specifications of the processor as measured differentially at VCCSENSE/ VCC_VSSSENSE catch resistors on the motherboard.

Table 55. VID vs. $V_{CC-CORE}$ Voltage

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core
0	0	0	0	0	0	0	1.5000V	1	0	0	0	0	0	0	0.7000V
0	0	0	0	0	0	1	1.4875V	1	0	0	0	0	0	1	0.6875V
0	0	0	0	0	1	0	1.4750V	1	0	0	0	0	1	0	0.6750V
0	0	0	0	0	1	1	1.4625V	1	0	0	0	0	1	1	0.6625V
0	0	0	0	1	0	0	1.4500V	1	0	0	0	1	0	0	0.6500V
0	0	0	0	1	0	1	1.4375V	1	0	0	0	1	0	1	0.6375V
0	0	0	0	1	1	0	1.4250V	1	0	0	0	1	1	0	0.6250V
0	0	0	0	1	1	1	1.4125V	1	0	0	0	1	1	1	0.6125V
0	0	0	1	0	0	0	1.4000V	1	0	0	1	0	0	0	0.6000V
0	0	0	1	0	0	1	1.3875V	1	0	0	1	0	0	1	0.5875V
0	0	0	1	0	1	0	1.3750V	1	0	0	1	0	1	0	0.5750V
0	0	0	1	0	1	1	1.3625V	1	0	0	1	0	1	1	0.5625V
0	0	0	1	1	0	0	1.3500V	1	0	0	1	1	0	0	0.5500V
0	0	0	1	1	0	1	1.3375V	1	0	0	1	1	0	1	0.5375V
0	0	0	1	1	1	0	1.3250V	1	0	0	1	1	1	0	0.5250V
0	0	0	1	1	1	1	1.3125V	1	0	0	1	1	1	1	0.5125V
0	0	1	0	0	0	0	1.3000V	1	0	1	0	0	0	0	0.5000V
0	0	1	0	0	0	1	1.2875V	1	0	1	0	0	0	1	0.4875V
0	0	1	0	0	1	0	1.2750V	1	0	1	0	0	1	0	0.4750V
0	0	1	0	0	1	1	1.2625V	1	0	1	0	0	1	1	0.4625V
0	0	1	0	1	0	0	1.2500V	1	0	1	0	1	0	0	0.4500V
0	0	1	0	1	0	1	1.2375V	1	0	1	0	1	0	1	0.4375V
0	0	1	0	1	1	0	1.2250V	1	0	1	0	1	1	0	0.4250V
0	0	1	0	1	1	1	1.2125V	1	0	1	0	1	1	1	0.4125V
0	0	1	1	0	0	0	1.2000V	1	0	1	1	0	0	0	0.4000V
0	0	1	1	0	0	1	1.1875V	1	0	1	1	0	0	1	0.3875V
0	0	1	1	0	1	0	1.1750V	1	0	1	1	0	1	0	0.3750V
0	0	1	1	0	1	1	1.1625V	1	0	1	1	0	1	1	0.3625V
0	0	1	1	1	0	0	1.1500V	1	0	1	1	1	0	0	0.3500V
0	0	1	1	1	0	1	1.1375V	1	0	1	1	1	0	1	0.3375V
0	0	1	1	1	1	0	1.1250V	1	0	1	1	1	1	0	0.3250V
0	0	1	1	1	1	1	1.1125V	1	0	1	1	1	1	1	0.3125V
0	1	0	0	0	0	0	1.1000V	1	1	0	0	0	0	0	0.3000V
0	1	0	0	0	0	1	1.0875V	1	1	0	0	0	0	1	0.2875V
0	1	0	0	0	1	0	1.0750V	1	1	0	0	0	1	0	0.2750V
0	1	0	0	0	1	1	1.0625V	1	1	0	0	0	1	1	0.2625V
0	1	0	0	1	0	0	1.0500V	1	1	0	0	1	0	0	0.2500V
0	1	0	0	1	0	1	1.0375V	1	1	0	0	1	0	1	0.2375V
0	1	0	0	1	1	0	1.0250V	1	1	0	0	1	1	0	0.2250V
0	1	0	0	1	1	1	1.0125V	1	1	0	0	1	1	1	0.2125V
0	1	0	1	0	0	0	1.0000V	1	1	0	1	0	0	0	0.2000V
0	1	0	1	0	0	1	0.9875V	1	1	0	1	0	0	1	0.1875V
0	1	0	1	0	1	0	0.9750V	1	1	0	1	0	1	0	0.1750V
0	1	0	1	0	1	1	0.9625V	1	1	0	1	0	1	1	0.1625V
0	1	0	1	1	0	0	0.9500V	1	1	0	1	1	0	0	0.1500V
0	1	0	1	1	0	1	0.9375V	1	1	0	1	1	0	1	0.1375V
0	1	0	1	1	1	0	0.9250V	1	1	0	1	1	1	0	0.1250V
0	1	0	1	1	1	1	0.9125V	1	1	0	1	1	1	1	0.1125V
0	1	1	0	0	0	0	0.9000V	1	1	1	0	0	0	0	0.1000V
0	1	1	0	0	0	1	0.8875V	1	1	1	0	0	0	1	0.0875V
0	1	1	0	0	1	0	0.8750V	1	1	1	0	0	1	0	0.0750V
0	1	1	0	0	1	1	0.8625V	1	1	1	0	0	1	1	0.0625V
0	1	1	0	1	0	0	0.8500V	1	1	1	0	1	0	0	0.0500V
0	1	1	0	1	0	1	0.8375V	1	1	1	0	1	0	1	0.0375V
0	1	1	0	1	1	0	0.8250V	1	1	1	0	1	1	0	0.0250V
0	1	1	0	1	1	1	0.8125V	1	1	1	0	1	1	1	0.0125V
0	1	1	1	0	0	0	0.8000V	1	1	1	1	0	0	0	0.0000V
0	1	1	1	0	0	1	0.7875V	1	1	1	1	0	0	1	0.0000V
0	1	1	1	0	1	0	0.7750V	1	1	1	1	0	1	0	0.0000V
0	1	1	1	0	1	1	0.7625V	1	1	1	1	0	1	1	0.0000V
0	1	1	1	1	0	0	0.7500V	1	1	1	1	1	0	0	0.0000V
0	1	1	1	1	0	1	0.7375V	1	1	1	1	1	0	1	0.0000V



The VID[6:0] signals are 1.05 V CMOS level outputs. Intel recommends that 1:2 spacing and routing with a trace impedance of 50 Ω ±15% be used. No external termination is required for VID[6:0]. To ensure good signal quality, a point-to-point routing between the Intel® Atom™ Processor E6x5C Series and the VRM should be used.

8.4.1.3.1 Initial Boot Voltage

The V_{CC} output voltage rail level is initially defined by V_{BOOT}. When VR_ON is initially pulled high, V_{CC} ramps up to V_{BOOT} regardless of the VID code. V_{CC} must remain at V_{BOOT} for a period of t_{BOOT}, and then it must be regulated to its final value according to the VID code. The transition time between V_{BOOT} and VID is defined as $t_{BOOT\_VID\_TR}$. For more details, refer to the *Intel® Mobile Voltage Positioning (Intel® MVP), 6 Voltage Regulation – Product Specification*.

8.5 Intel® Atom™ Processor E6x5C Series Power Delivery, Decoupling, and Layout Guidelines

Guidelines in the following sections should be followed when laying out the Intel® MVP-6 processor power delivery circuit using a traditional Buck VR on a printed circuit board.

8.5.1 General Voltage Regulator Layout Recommendations

Ensure proper planning for the voltage regulator layout. Often the allocated area is too small with poor location. All the components in the high current paths dissipate some power, i.e., they get warm when current runs through them. To minimize temperature rise and facilitate thermal spreading, large copper fill areas connecting the high current components is imperative. For example, the MOSFET manufacturers recommend that each MOSFET be mounted on one square inch of 2 oz. copper. While this may not be possible in the small form factors environment, this recommendation serves to illustrate the importance of thermal considerations in the switching regulator layout.

- Bulk capacitors for V_{CC} need three or more vias per pad and vias should not be shared. Clusters of bulk and bypass capacitors may be clustered along the high current paths between the sense resistor and the processor. Clusters may have copper fill areas between capacitors. This provides additional opportunities for vias – do not stop at three. However, avoid clustering vias of the same polarity too close to each other. 50 mil spacing between vias of the same polarity is recommended to avoid severe perforation of alternate polarity planes.
- Some controllers sense the load on V_{CC} by monitoring the voltage drop across the sense resistor with a Kelvin connection. The two feedback traces do not handle a high current, but must be of equal lengths to get an accurate load measurement. Connect the feedback signal traces as close as possible to both ends of the sense resistor. While the feedback traces do not handle high current, they are high impedance and susceptible to interference from electrical and magnetic noise. Avoid routing these traces near the power inductor and avoid routing through vias.
- The sense resistor is to be placed as close to the inductor as possible, followed by the first two bulk capacitors.
- The lead frame in the power MOSFETs is used to dissipate heat. To do this each of the power MOSFETs requires 1 square inch of copper.
- Avoid ground loops as they pick up noise. Use star or single point grounding. The source of the lower (synchronous bottom MOSFET) is an ideal point where the input and output ground planes can be connected.
- Keep the inductor-switching node small by placing the output inductor; switching top MOSFET and synchronous bottom MOSFETs close together on the same copper fill.

- The MOSFET enable/gate traces to the driver must be as short (less than 1 inch), straight, and wide as possible (20 to 25 mils). Ideally, the driver has to be placed right next to the MOSFETs. Circuits using multiple top or bottom MOSFETs need to have the gate traces serpentined so the all the traces going to the top MOSFETs gates and most especially the bottom MOSFETs gates are the same length.
- Use a minimum of 3 vias per connection on each bulk capacitor, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
- Place the top MOSFET drains as close to the VDC-input capacitors as possible.
- The sense resistor has to be wide enough to carry the full load current. A minimum of 1 via per Amp to the V_{CC} plane should be used. Use more if space permits.
- Use solid 2 oz. copper fill under Drain and Source connections of the top and bottom MOSFETs.

8.5.2 VCC and VNN Core Decoupling and Layout Recommendations

System motherboards should include high frequency, mid frequency and bulk decoupling capacitors as close to the Intel® Atom™ Processor E6x5C Series power and ground pins as possible. Decoupling should be arranged such that the lowest ESL (effective series inductance) high-frequency ceramic decoupling capacitors are closest to the processor power pins followed by bulk electrolytic capacitors (organic covered tantalum or aluminum covered capacitors). Table 56 lists the recommended decoupling solution for VCC Core and VNN Core.

To reduce the resistance and lower inductance, VCC Core and VNN Core are fed from the VRM by means of multiple power planes between the voltage regulator, decoupling capacitors, and processor VCC and VNN core pins. To meet the VCC and VNN Core transient tolerance specifications for the worst-case stimulus, the maximum equivalent series resistance (ESR) of the bulk decoupling solution should be as low as possible. The contribution of the motherboard and the processor package contribute an additional 1.2 mΩ, so the effective load line as fed back to the VR from the processor VCCSENSE/VCC_VSSSENSE signals is 3 mΩ (Kelvin point measurements).

Table 56. VCC Core Decoupling Guidelines

Intel® Atom™ Processor E6xx Series Stepping	Description[1, 2]	Value	Qty	ESR	ESL
Intel® Atom™ Processor E6xx Series - B0 Stepping (Little Bay Fab D)	Low-frequency (Bulk) Decoupling (Polymer Covered Aluminum - SP Cap, AO Cap)	220 µF ± 20%	1	15 mΩ	
	Mid-frequency Decoupling (0402 MLCC, X7R, 16 V or better)	47 µF ± 10%	1	7.7 mΩ	1 pH
	High-frequency Decoupling (0402 MLCC, X5R, 6.3 V or better)	1 µF ± 10%	6	30 mΩ	400 pH
Intel® Atom™ Processor E6xx Series - B1 Stepping (Little Bay Fab E)	Low-frequency (Bulk) Decoupling (Polymer Covered Aluminum - SP Cap, AO Cap)	220 µF ± 20%	1	15 mΩ	
	Mid-frequency Decoupling (0402 MLCC, X7R, 16 V or better)	47 µF ± 10%	1	7.7 mΩ	1 pH
	High-frequency Decoupling (0402 MLCC, X5R, 6.3 V or better)	1 µF ± 10%	6	30 mΩ	400 pH
	High-frequency Decoupling (0204 Monolithic Ceramic Capacitor, X6S, 6.3 V)	0.22 µF ± 20%	4		250pH

Notes:
1. The High-frequency decoupling are required to be placed directly under the Intel® Atom™ Processor E6x5C Series package.
2. The component quantity above does not include an additional decap footprint. It is recommended to add at least one unstuffed decap footprint as a Defensive Design. It is shown in the CRB design.

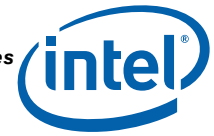


Table 57. VNN Core Decoupling Guidelines

Intel® Atom™ Processor E6xx Series Stepping	Description[1, 2]	Value	Qty	ESR	ESL
Intel® Atom™ Processor E6xx Series - B0 Stepping (Little Bay Fab D)	Low-frequency (Bulk) Decoupling (Polymer Covered Aluminum - SP Cap, AO Cap)	220 µF ± 20%	1	15 mΩ	
	Mid-frequency Decoupling (0402 MLCC, X7R, 16 V or better)	47 µF ± 10%	1	7.7 mΩ	1 pH
	High-frequency Decoupling (0402 MLCC, X5R, 6.3 V or better)	1 µF ± 10%	6	30 mΩ	400 pH
Intel® Atom™ Processor E6xx Series - B1 Stepping (Little Bay Fab E)	Low-frequency (Bulk) Decoupling (Polymer Covered Aluminum - SP Cap, AO Cap)	220 µF ± 20%	1	15 mΩ	
	Mid-frequency Decoupling (0402 MLCC, X7R, 16 V or better)	47 µF ± 10%	1	7.7 mΩ	1 pH
	High-frequency Decoupling (0402 MLCC, X5R, 6.3 V or better)	1 µF ± 10%	6	30 mΩ	400 pH
	High-frequency Decoupling (0204 Monolithic Ceramic Capacitor, X6S, 6.3 V)	0.22 µF ± 20%	4		250pH

Notes:
1. The High-frequency decoupling are required to be placed directly under the Intel® Atom™ Processor E6x5C Series package.
2. The component quantity above does not include an additional decap footprint. It is recommended to add at least one unstuffed decap footprint as a Defensive Design. It is shown in the CRB design.

8.5.2.1 VCC Core and VNN Core Power Delivery Layout for the Processor

The VCC Core and VNN Core power delivery corridor pins concentrated in the middle of the processor package. Since access to the VCC and VNN Core power pins are blocked on the top layer by I/O signals, power to the processor needs to come in on the bottom and inner layers. High-frequency decoupling capacitors should be placed directly under the Intel® Atom™ Processor E6x5C Series such that they reside as close as possible to the processor die. Mid-frequency decoupling should be placed at the edge of the processor package, between the Intel® MVP-6 voltage regulator and the processor. This will increase decoupling effectiveness and avoid voltage droop problems. All the VCC and VNN Core and ground vias of the processor pin-map should have vias that are connected to both internal and external power planes. Sharing of vias between several VCC and VNN Core pins or ground pins is not allowed.

8.5.2.2 Important Notes for VCC and VNN Power Delivery Layout Recommendations

It is important to use large power planes for VCC and VNN in order to have sufficient copper flooding with no restrictions to current flow. The system needs to respond to instantaneous changes in current flow to the device without adding noise to VCC and Vnn power planes. Figure 51 shows an example of a recommended power plane design versus the not recommended power plane design. Figure 52 shows an example of a recommended ground plane design versus the not recommended ground plane design.

Ideally the Vcc and Vnn power planes should be implemented on seperate power layers in order to provide the best power delivery scheme to each voltage rail. Pairing the Vcc and Vnn rail with an adjacent ground plane will provide additional intrinsic decoupling and minimize loop inductance. Due to the high current requirements of the Vcc rail, it should take priority over the Vnn in the power delivery implementation.

Figure 51. Comparison Between Recommended and Not Recommended Power Plane Designs

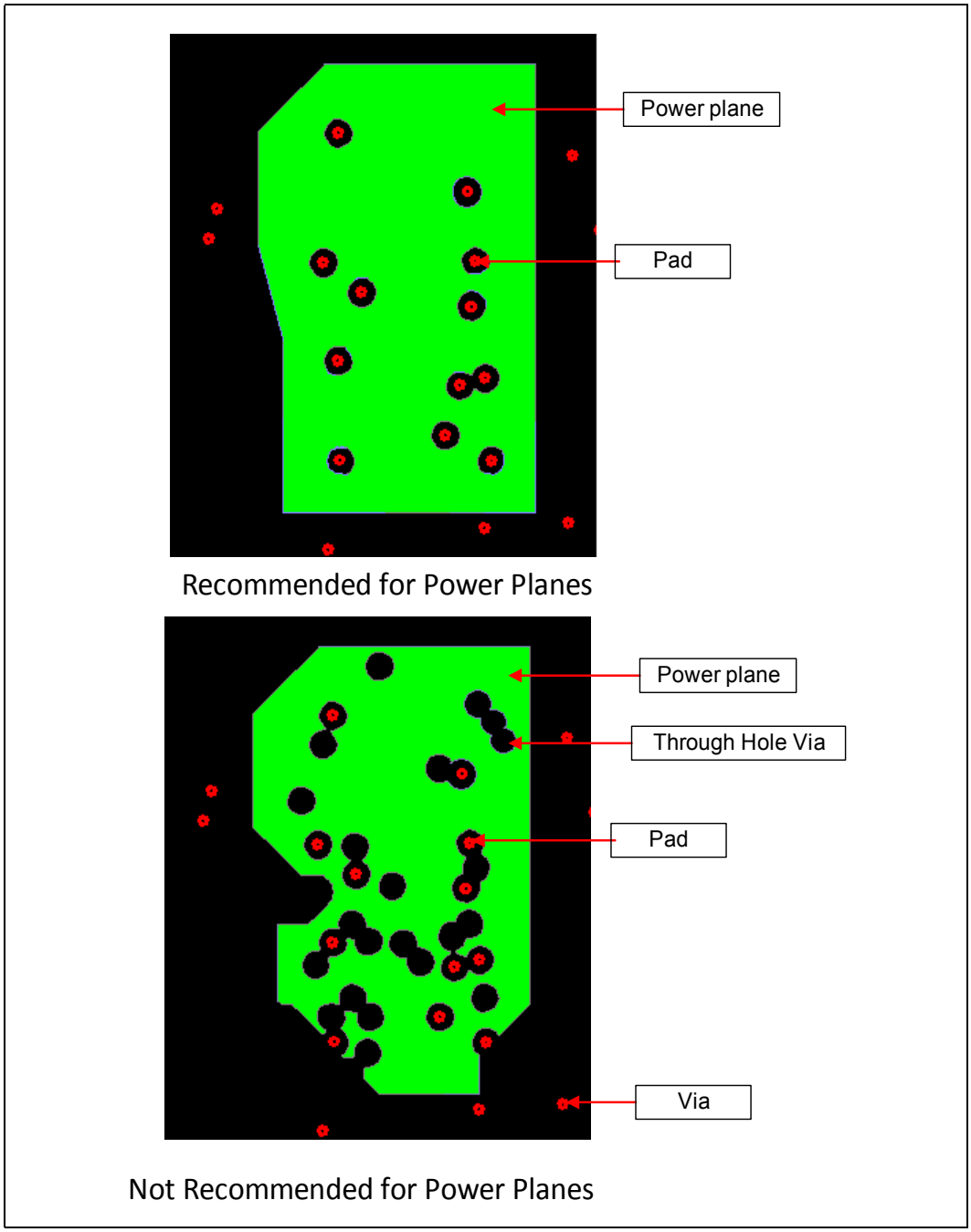
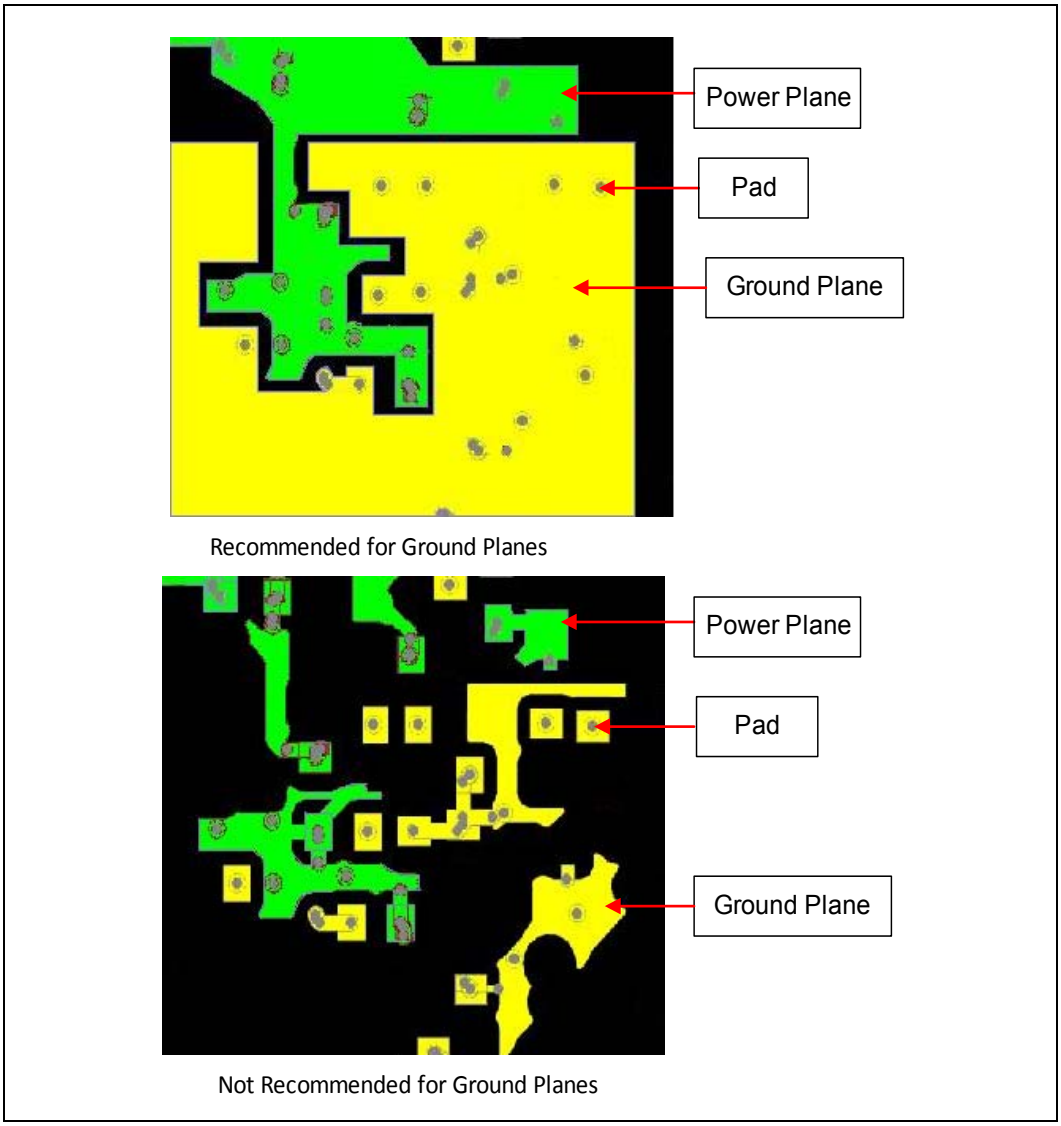


Figure 52. Comparison Between Recommended and Not Recommended Ground Plane Designs



Note: The bulk-decoupling 220 µF capacitor is placed on the VCC and VNN Core power delivery corridor near the voltage regulator. Add several VCC and ground vias (minimum of 3 vias each) on both sides of the capacitors in order to reduce the inductance of the capacitor connection as illustrated in the current flow loop area in Figure 48. If the voltage regulator feed is on the negative side of the capacitor then both VCC and GND stitching vias will be needed on both the positive and negative terminals of the capacitor to reduce the effective inductance of the capacitor.

Note: The high-frequency decoupling capacitors should be evenly spread out under the Intel® Atom™ Processor E6x5C Series shadow.

Note: Primary side layer (top-layer) and secondary side layer (bottom layer) are used for VCC and VNN current feeding while referencing ground planes with a thin dielectric. These layers are solid ground planes in the areas under the processor package outline

and where the decoupling capacitors are placed. This results in a reduction in effective loop inductance.

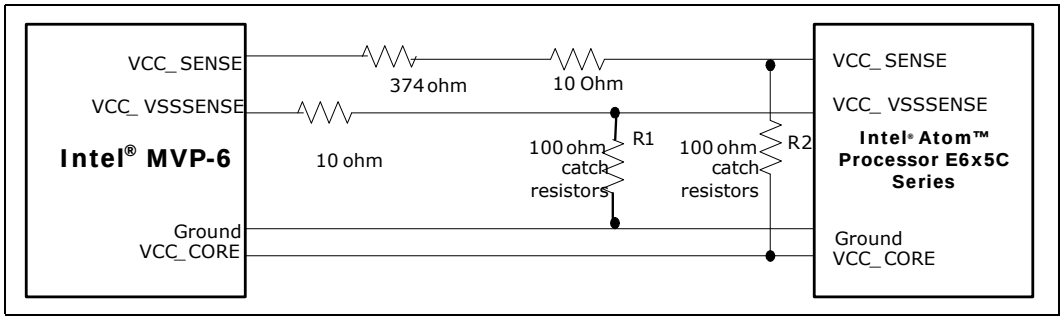
8.5.2.3 VCCSENSE/VCC_VSSSENSE Die Sensing

Embedded designs frequently are subject to severe layout area constraints that could significantly compromise the robustness of VR placement on the motherboard and its connection to Intel® Atom™ Processor E6x5C Series VCC and VNN Core pins. To ensure the impedance profile stays below the maximum target of 3 mΩ for frequencies ranging above the voltage regulator bandwidth of ~50 to 60 kHz, there is no layout compromise that can be made in the robustness of placement and connection of the recommended decoupling capacitor guidelines. However, at the low frequency range which the VR provides the current to the processor, less optimized VR layout placement could be compensated using negative feedback techniques to the VR by sensing the voltage at the die through VCCSENSE/VCC_VSSSENSE signals and feeding them back to the VR controller. This may allow more flexibility and compromises in the VR placement.

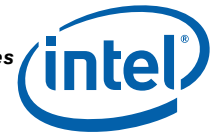
The Intel® Atom™ Processor E6x5C Series implements the concept of die sensing. For this purpose the VCC Core, VNN Core and VSS bumps are routed in "Kelvin" fashion to 2 pairs of VCCSENSE/VCC_VSSSENSE pins of the Intel® Atom™ Processor E6x5C Series package and fed back to the VR as a negative feedback. This implementation allows for the VR controller to adjust its output voltage in order to achieve accurate control of the 3 mΩ load line at the die VCCSENSE/VCC_VSSSENSE connection to VCC and VSS bumps. The conceptual implementation of VCCSENSE/VCC_VSSSENSE die sensing for the Intel® Atom™ Processor E6x5C Series is illustrated in Figure 53.

For debug and clean measurement of power delivery quality capabilities, it is suggested to route the VCCSENSE/VCC_VSSSENSE lines differentially between the Intel® Atom™ Processor E6x5C Series and VR, with a trace width of 8 mils (0.2032 mm), 7 mil (0.178 mm) spacing, and trace impedance of 27.4 Ω. The VCCSENSE/VCC_VSSSENSE should be length matched to within 25 mils (0.635 mm). To minimize any stray noise pickup to the VCCSENSE/VCC_VSSSENSE lines, these traces should reference to solid ground plane, avoid crossing over plane splits and maintain a 25 mils (0.635 mm) separation distance away from any other signals.

Figure 53. Intel® Atom™ Processor E6x5C Series VCCSENSE/VCC_VSSSENSE Die Sensing



If the Intel® Atom™ Processor E6x5C Series is not present on the motherboard (during board checkout, for example), the VR will not get the negative feedback it needs for its correct operation. This may potentially damage MB components like the bulk decoupling capacitors. In response, the R2 = 100 Ω catch resistor are added on the mother board that will "bypass" the VCCSENSE/VCC_VSSSENSE connection through the processor and provide the necessary negative feedback to the VR in the case when the processor is not present (refer to Figure 53). During normal operation, the processor VCCSENSE/VCC_VSSSENSE package trace connection shunts the R1, R2



catch resistors. To minimize the potential error the catch resistors could introduce due to VCCSENSE/VCC_VSSSENSE lines resistance, R1, R2 should be placed within 1 inch of the processor and should be routed such that stubs are avoided.

For convenience of die load line measurement capabilities, it is recommended to include VCCSENSE/VCC_VSSSENSE and GND test points next to the VR VCCSENSE/ VCC_VSSSENSE input pins. Place the test points within 100 mil (2.54 mm) of each other for testability.

Terminate the VCCSENSE signal using 384 Ω ±1% resistor and VCC_VSSSENSE signal using 10 Ω ±1% resistor placed as close as possible to the Intel® MVP-6 VCCSENSE/ VCC_VSSSENSE signals.

8.5.3 Miscellaneous Cores Filtering and Decoupling Guidelines

It is recommended that developers use the amount of decoupling capacitors specified in the following sections to ensure the component maintains stable supply voltages. The capacitors should be placed as close to the package pins as possible (100 mils nominal). It is recommended that additional pads for extra power plane decoupling capacitors be included if possible.

Note: It is important to note that adhering to the following decoupling and filtering requirements is critical to achieving stable power delivery to the numerous high-speed interfaces and ensuring proper interface performance.

Note: For all high-frequency, ceramic capacitors, careful selection of the dielectric (i.e., X5R, X7R, etc.) should be done to ensure it matches the thermal characteristics of the system motherboard. For all bulk decoupling capacitors, the specified ESR target should be adhered to.

Note: For the inductors and capacitors used in filter circuits, pay attention to the DC resistance values of these components since they are series components. Do not use inductors and capacitors with resistance ratings that deviate from the recommended target as they can lead to large IR drops that may affect electrical performance. When calculating the target ESR, maximum current and minimum voltage for the power supply pins of interest are used. In addition, components should have proper max voltage and current ratings that align with the voltage and current tolerances on the different power supply pins. For filter component placement, the inductor and capacitor in any circuit should be placed close together and should be placed close to the Intel® Atom™ Processor E6x5C Series.

8.5.3.1 Intel® Atom™ Processor E6x5C Series IO Core Power Supply Guidelines

Table 58 below lists the power supply filtering and decoupling requirements for the IO Core.

Table 58. IO Core Power Supply Filtering/Decoupling

Signal	Component (Quantity)	Value	Tolerance	ESR (Ω)/ESL (nH)	Type/Size	Component Placement
VCCD (1.05 V)	C1 (9)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place three under Intel® Atom™ Processor E6x5C Series VCCD pins and seven further away under the Intel® Atom™ Processor E6x5C Series.
VCCQ (1.05 V)	C1 (6)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCQ pins.
VCCP[1] (1.05 V)	C1 (6)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCP pins.
VCCPA[1] (1.05 V)	C1 (4)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCPA pins.
VCCA[1] (1.5 V)	C1 (4)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCA pins.
VCCA (1.5 V)	L1 (1)	1.0 µH, 0.22 A	N/A	N/A	N/A	Place near the edge of Intel® Atom™ Processor E6x5C Series VCCA pins.
VCCP33[1] (3.3 V)	C1 (4)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCP33 pins.
VCCP33SUS, VCCPSUS[1] (3.3 V)	C1 (2)[1]	0.1 µF, 16 V	± 10%	30 mΩ/400 pH	X7R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCP33SUS and VCCPSUS pins.
VCCRTCEXT (1.05 V)	C1 (1)	0.1 µF, 16 V	± 10%	30 m Ω/400 pH	X7R/0402	Place near the edge of the Intel® Atom™ Processor E6x5C Series VCCRTCEXT pin.
VCC33RTC	C1 (1)	0.1 µF, 16 V	± 10%	30 m Ω/400 pH	X7R/0402	Place above COM Express* connector.
	C2 (1)	1 µF, 16 V	± 10%	30 m Ω/400 pH	X7R/0402	
VCCD_DPL (1.05 V)	C1 (1)	1 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place near the edge of the Intel® Atom™ Processor E6x5C Series VCCD_DPL pin.
	FB (1)	120, 0.5 A	N/A	N/A	N/A	
VCCQHPLL (1.05 V)	C1 (1)	0.1 µF, 16 V	± 10%	30 mΩ/400 pH	X7R/0402	Place near the edge of the Intel® Atom™ Processor E6x5C Series VCCQHPLL pin.
	C2 (1)	22 µF, 6.3 V	± 20%	Low ESR and ESL	X5R/0805	
	FB (1)	120, 0.5 A	N/A	N/A	N/A	

Notes:
1. The component quantity above does not include an additional decap footprint. It is recommended to add at least one unstuffed decap footprint as a Defensive Design as shown in the CRB design.

8.5.3.2 Intel® Atom™ Processor E6x5C Series Memory Controller Power Supply Guidelines

Table 59 lists the power supply decoupling requirements for the Intel® Atom™ Processor E6x5C Series memory controller interface.

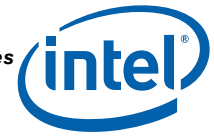


Table 59. Memory Controller Power Supply Decoupling Requirements

Signal	Component (Quantity)	Value	Tolerance	ESR (Ω)/ESL (nH)	Type/Size	Notes
VCCPDDR[1] (1.05 V)	C1 (1)[1]	47.0 pF	± 5%	N/A	COG/0402	Place under Intel® Atom™ Processor E6x5C Series VCCPDDR pins.
VCC180	C1 (3)	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCC180 pins.
VCC180SR[1] (1.8 V)	C1 (1)	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCC180SR pins.
VCCD180 (1.8 V)	C1 (2)	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under Intel® Atom™ Processor E6x5C Series VCCD180 pins.
VCCA180 (1.8 V)	C1 (1)	10 µF, 6.3 V	± 20%	N/A	X5R/0603	Place near the edge of Intel® Atom™ Processor E6x5C Series VCCA180 pins.
	L1 (1)	1.8 µH, 0.05 A	N/A	N/A	N/A	
VCCSFRDPLL (1.8 V)	C1 (1)	0.1 µF, 16 V	± 10%	N/A	X7R/0402	Place near the edge of Intel® Atom™ Processor E6x5C Series VCCSFRDPLL pins.
	FB (1)	120, 0.5 A	N/A	N/A	N/A	
VCCSFR_EXP and VCCSFRHPLL (1.8 V)	C1 (1)	0.1 µF, 16 V	± 10%	30 mΩ/400 pH	X7R/0402	Place near the edge of Intel® Atom™ Processor E6x5C Series VCCSFR_EXP and VCCSFRHPLL pins.
	C2 (1)	1 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	
	C3 (1)	22 µF	± 20%	N/A	X5R/0805	
	FB	N/A	N/A	N/A	N/A	

Notes:
1. The component quantity above does not include an additional decap footprint. It is recommended to add at least one unstuffed decap footprint as a Defensive Design as shown in the CRB design.

8.5.3.3 Intel® Atom™ Processor E6x5C Series PCI Express*, SDVO, and LVDS Power Supply Guidelines

Table 60 lists the power supply filtering and decoupling requirements for the PCI Express*, SDVO, and LVDS interfaces.

Table 60. PCI Express*/SDVO/LVDS Power Supply Filtering/Decoupling

Signal	Component (Quantity)	Value	Tolerance	ESR (Ω)/ESL (nH)	Type/Size	Notes
VCCA_PEG (1.05 V)	C1 (6)[1]	1.0 µF, 6.3 V	± 10%	30 mΩ/400 pH	X5R/0402	Place under the Intel® Atom™ Processor E6x5C Series VCCA_PEG pins.

Notes:
1. The component quantity above does not include an additional decap footprint. It is recommended to add at least one unstuffed decap footprint as a Defensive Design as shown in the CRB design.

8.6 Platform Power Sequencing Requirements

The Power-up sequencing for the Intel® Atom™ Processor E6x5C Series platform is controlled by SMC (System Management Controller).

Due to the independent power supplies to the E6x5C CPU and the Arria FPGA, together with AC PCIe coupled interface, there is NOT a tight power sequencing relationship between the CPU & FPGA. Please refer to Figure-67 in chapter-11 that illustrates the power sequencing relationship between the devices.

During the system power-up sequence, the recommended sequencing of the rails powering up is listed below in order of earliest to latest:

- RTC Power Well
- Suspend/Resume Power Wells
- Core Power Wells

The sequence is reversed when powering down.

The Intel® Atom™ Processor E6x5C Series RTC power sequencing order is
V3P3_RTC (3.3 V)

The Intel® Atom™ Processor E6x5C Series suspend well power sequencing order is
V3P3 (3.3 V) -> V1P8 (1.8V) -> V1P05 (1.05 V)

The Intel® Atom™ Processor E6x5C Series core power sequencing order is
V3P3_S (3.3 V) -> V1P5_S (1.50 V) -> V1P05_S (1.05 V) & VNN_S -> V1P8_S (1.8 V) -> V1P25_S -> VCC_S

Note: V1P05_S and VNN must ramp at the same time. Timing requirements are dependent on voltage regulators being used. The timing gap should be as small as possible to minimize current leakage from the V1P05_S power rail.

At no time should a lower voltage rail be 0.7 V higher than a higher voltage rail. For instance, a V1P8 suspend rail should not ramp more than 0.7 V in difference beyond a V3P3 suspend rail. This rule must be followed in order to ensure the proper functionality of the Intel® Atom™ Processor E6x5C Series. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the violating rails. This can be controlled via voltage follower circuits or having logic such as the SMC (System Management Controller) directly control the enabling of the individual regulators.

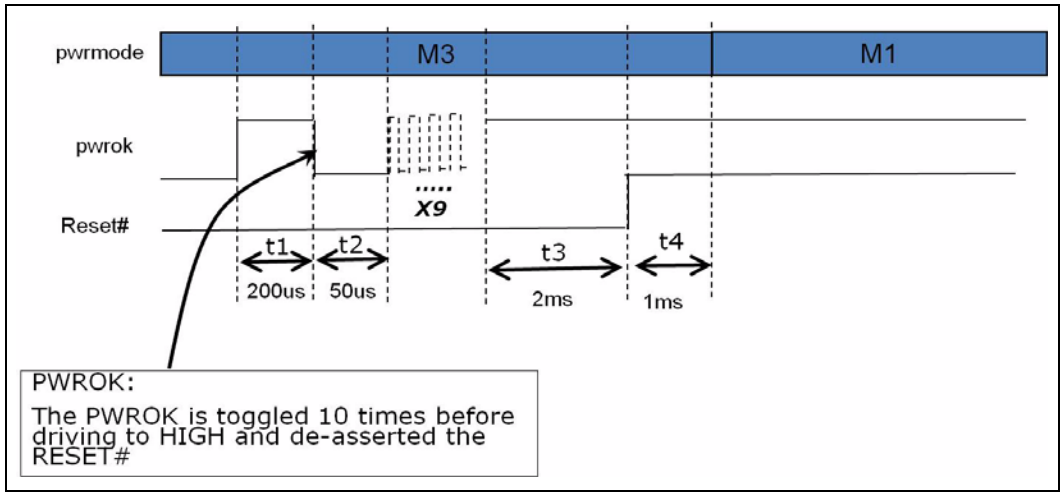
However, the above rule has exceptions that apply to V1P05_S, VNN_S and VNN_S -> V1P8_S during processor core power sequencing:

V3P3_S (3.3 V) -> V1P5_S (1.50 V) -> V1P05_S (1.05 V) & VNN_S - must not be higher than 0.7V

V1P8_S (1.8 V) -> V1P25_S -> VCC_S - must not be higher than 0.7V

The Intel® Atom™ Processor E6x5C Series PWROK pin must be asserted after all Intel® Atom™ Processor E6x5C Series core power supplies are stable. On the CRB, PWROK pin is toggled for 10 times before driving to HIGH and de-asserted the RESET#. The number of toggling PWROK is calculated based on SMC clock. For CRB, 10 times of toggling PWROK is based on 5 MHz and 7.56 MHz SMC clock. Different SMC clock frequency would require different number of times for toggling PWROK. PWROK toggling must also follow a specific timing requirement as shown in Figure 54.

Figure 54. Timing Requirement to Toggle PWROK



PWROK toggling must be implemented during S3, S4 and S5. It is recommended to drive the PWROK pin with the DELAYED POWER GOOD out of the Intel® MVP controller (either directly or qualified by SMC).

Refer to the *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for relationship dependencies, timing requirements and full power sequencing diagrams.

8.6.1 Intel® Atom™ Processor E6x5C Series Thermal Management Interface Signals

The THRM_B signal of the Intel® Atom™ Processor E6x5C Series is active low input generated by external hardware, typically thermal sensor. System thermals can be monitored and subsequently issue an SMI#/SCI message via this pin. The Power Management software will take corrective action accordingly. The sensors are usually used to monitor the skin temperature near the DDR2 memory devices, CPU and other high power areas in the system for a possible thermal condition.

Current third party vendor product offerings that may be suitable for THRM_B pin applications include ambient temperature thermal sensors and remote diode thermal sensors. Also, thermal sensors that implement an open-drain output for signaling a thermal event would provide the most flexibility from an electrical and layout design perspective.

8.6.1.1 THRM_B Signal

8.6.1.1.1 THRM_B Usage Model

The THRM_B signal of the Intel® Atom™ Processor E6x5C Series can be connected directly to an external controller or hardware logic monitoring the thermal state of the Intel® Atom™ Processor E6x5C Series and DDR2 SDRAM where the desired effect is to start the hardware H_STPCLK_B based throttling mode through the generation of an SCI or SMI# routine.

The thermal sensors targeted for application with the Intel® Atom™ Processor E6x5C Series are planned to be capable of measuring the ambient temperature only and should be able to assert THRM_B if the pre-programmed thermal limits/conditions are met or exceeded.

Factors such as thermal sensor placement, airflow within the chassis, adjacent components, thermal sensor sensitivity, and thermal sensor response time should be comprehended for THRM_B to effectively control skin temperatures. THRM_B should not be used for measuring or controlling the T_J or T_{CASE} parameters of DDR2 SDRAM devices since they cannot respond quickly enough to dynamic changes in DRAM power.

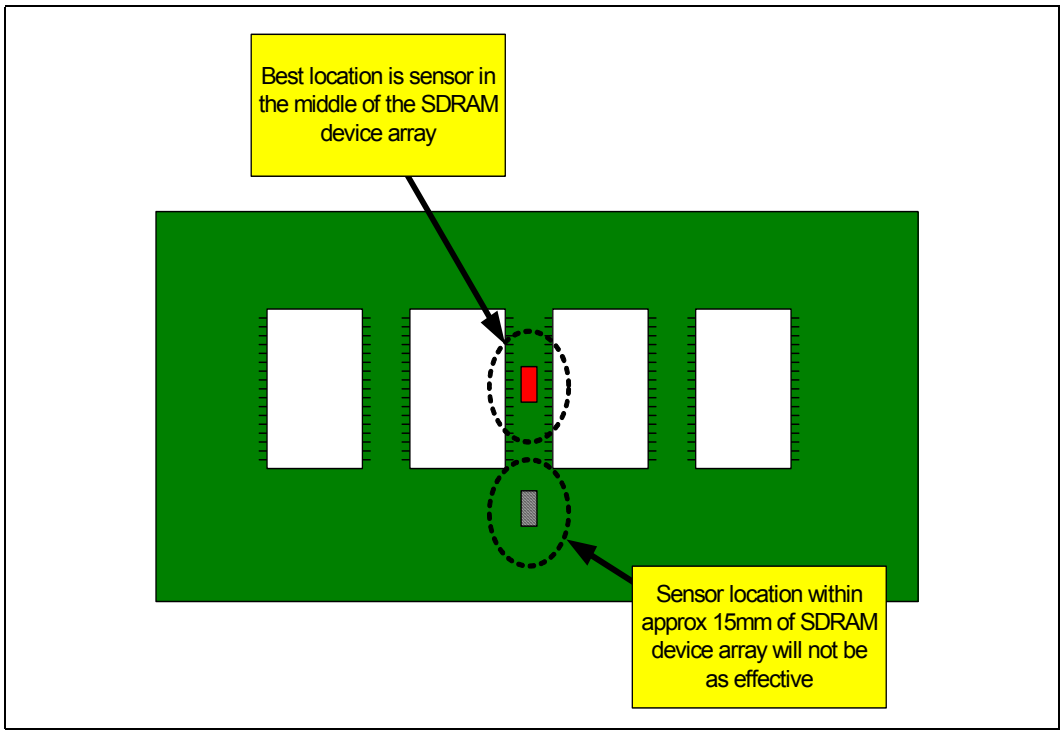
8.6.1.1.2 THRM_B Design and Placement Guidelines

Ideally, the thermal sensor should implement an open drain type output buffer to drive THRM_B. As implemented in the Intel® Atom™ Processor E6x5C Series, THRM_B is active low signal and is required external 8.2 kΩ to 10 kΩ pull-up resistors to 3.3 V on the board since it does not have integrated pull-up.

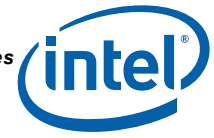
A system is expected to have one thermal sensor for the memory down on the motherboard. Design considerations will vary by thermal sensor type and supplier, so consult with the manufacturer for appropriate layout guidelines. The thermal sensor should be placed near the memory down in a system and in an area where airflow and conduction from adjacent components are minimized. This allows for the best correlation of thermal sensor temperature to chassis or system surface temperature. Refer to Figure 55 below for details.

Assuming airflow is negligible within a system, the optimal placement of the thermal sensor is on the surface of the motherboard in the middle of the SDRAM device array, centered longitudinally and laterally in relation to the outline of the overall device array. If placement within the outline of the SDRAM device array is not possible, then the next best option is to locate it within approximately 15 mm (0.6 inch) of the SDRAM device array.

Figure 55. DDR2 Memory Thermal Sensor Placement



Note: Current SDRAM sensor implementation on CRB is placed further away from SDRAM due to board area constraint, therefore the sensor will not be used.



8.6.1.1.3 THRM_B Disable Guidelines

If THRM_B functionality is not implemented, the THRM_B signal must be properly terminated with an external 8.2 kΩ to 10 kΩ pull-up resistor to 3.3 V.

8.6.1.2 THERMTRIP_B Signal

If the Intel® Atom™ Processor E6x5C Series has reached an operating temperature that may damage the part, the platform should immediately cut power to the Intel® Atom™ Processor E6x5C Series via this pin.

If THERMTRIP_B is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the Intel® Atom™ Processor E6x5C Series and to meet input thresholds for the external logic.

8.6.1.3 PROCHOT_B Signal

The Intel® Atom™ Processor E6x5C Series can drive PROCHOT_B when it is throttling due to temperature. PROCHOT_B can be input signal to cause the Intel® Atom™ Processor E6x5C Series to throttle. A series resistor of 22.1 Ω ± 1% and a pulled-up resistor of 60.4 Ω ± 1% to 1.05 V should be added.

The following are PROCHOT_B routing and implementation recommendation:

- The routing guidelines allow the signal to be routed as either a microstrip or stripline.
- Recommended to route this signal with trace impedance of 50 Ω, trace width of 4.5mils (microstrip) and 4.3mils (stripline), and trace space of 10 mils.
- Minimum of 2:1 trace spacing ratio is allowed as long as the same ground reference plane is kept all the way from the Intel® Atom™ Processor E6x5C Series to the Intel® MVP-6 mobile processor core regulator.
- Changing reference plane is not recommended and may cause signal integrity degradation.
- Any necessary voltage translation logic should be used as PROCHOT_B is a 1.05-V tolerant signal.
- If PROCHOT_B is not used, then it must be terminated with a 62 Ω pull-up resistor to VCC.

8.6.1.4 THRMDA and THRMDC Signals

The Intel® Atom™ Processor E6x5C Series incorporates an on-die thermal diode. THRMDA (diode anode) and THRMDC (diode cathode) pins on the Intel® Atom™ Processor E6x5C Series can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Intel® Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Intel® Thermal Monitor. Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to the THRMDA and THRMDC pins. It can be approximately 4 to 8 inches away as long as the noise sources such as clock generators, data buses and address busses, etc. are avoided.
- Route the THRMDA and THRMDC lines in parallel.
- Use wide traces to reduce inductance and noise pickup that may be introduced by narrow traces in the system. A width of 10 mils, and spacing of 10 mils, is recommended.

8.7 Miscellaneous Platform Power Management

8.7.1 RESET_B Usage Model

The system Reset signal has been redefined for the platform. The platform uses a SMC (System Management Controller) to signal a Reset event to the rest of the platform. The SYS_RESET_B of the SMC can be connected directly to a reset button or any other equivalent driver in the system where the desired effect is to immediately put the system into reset. If a processor ITP-XDP debug port is implemented on the system, it is recommended that the DBR_B signal of the ITP interface be connected to SYS_RESET_B as well. If SYS_RESET_B is implemented, a weak pull-up resistor pulled-up to the 3.3 V standby rail ($V_{CC33SUS}$) may be required to ensure that no potential floating inputs to RESET_B cause a system reset. It is expected that the SMC will drive a separate signal (RSTWARN_B) to the Intel® Atom™ Processor E6x5C Series input before resetting the system. The Intel® Atom™ Processor E6x5C Series will respond to the SMC with assertion of RSTRDY_B shortly after receiving the RSTWARN assertion. This handshake will allow the Intel® Atom™ Processor E6x5C Series to shut down critical interfaces in an orderly manner prior to PLTRST_B assertion.

Note: The PWROK or VRMPWRGD signal should not be used to implement reset.

8.7.2 PWRBTN_B Usage Model

The Power Button signal has been redefined for the platform. The platform uses a SMC (System Management Controller) to signal a Power Button event to the rest of the platform. The Power Button signal (PWRBTN_B) of the SMC can be connected directly to a power button or any other equivalent driver (e.g., power management controller) where the desired effect is to indicate a system request to go to a sleep state (if in a normal operating mode) or to cause a wake event (if in a sleep state already).

8.7.3 PLTRST_B/PCIRST_B Usage Model

The Platform Reset signal (PLTRST_B) should be connected to all devices on the motherboard that require a reset. If no PCI Express* devices are present in the system, then there must be a minimum of 20 µs delay from PWROK assertion and 100 µs delay from RSTWARN assertion to PLTRST_B deassertion to ensure Intel® Atom™ Processor E6x5C Series PLLs are stable. The delay from PWROK assertion to PLTRST_B deassertion increases to 100 ms when PCI Express* devices are present in the system in order to meet PCI Express* specification requirements.

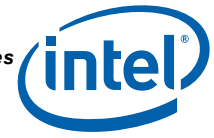
8.7.4 Intel® Display Power Saving Technology (Intel® DPST)

Intel® Display Power Saving Technology (Intel® DPST) maintains apparent visual experience by managing display image brightness and contrast while dynamically dimming the backlight. As a result, the display backlight power can be reduced by up to 25% with minimal visual impact depending on Intel® DPST settings and system use.

To support Intel® DPST with the LVDS display interface, one of two available options for Backlight Control mechanism (BLC) must be implemented: using GPIOSUS[4:0] pins which support Pulse Width Modulation (PWM), or GMBus.

8.7.4.1 GPIOSUS[4:0] Pins Which Support PWM Configuration

The GPIOSUS[4:0] pins output from the Intel® Atom™ Processor E6x5C Series must be routed to the LVDS display's PWM-based backlight inverter module with a point-to-point topology. For the best visual experience, it is recommended that the PWM- based backlight inverter module is capable of on input granularity of 0.1%. That is, the



inverter should be able to respond to a 0.1% change in duty cycle. For example, the change from 20% duty cycle to 20.1% duty cycle should be within the capabilities of the PWM-based inverter.

8.7.4.2 GMBus Configuration

The GMBus signals must be routed to the LVDS display's two-wire serial bus interface. The GMBus acts as a master on this interface and it does not support multi-master mode, hence no other master device should be connected on this interface. It is recommended that the GPIO output pins which emulate LCTLCLKA and LCTLCLKB will be routed from the Intel® Atom™ Processor E6x5C Series to the LVDS display's two-wire serial bus compatible inverter. For the Intel® Atom™ Processor E6x5C Series best visual experience, it is recommended that the SMBus-based backlight inverter module is capable of at least 256 discrete backlight output levels (an equivalent of 0.4% granularity).

For more information, please refer to the *Intel® Display Power Saving Technology 5.0 and Intel® Automatic Display Brightness – Application Notes / Briefs*.

8.7.5 Intel® Automatic Display Brightness

Intel® Automatic Display Brightness allows the system to change the backlight brightness in response to changing environment lighting. An ambient light sensor device should be able to provide an interrupt to the Intel® Atom™ Processor E6x5C Series to notify it of any changes in the environment lighting. The suggested method of implementation is to connect the ambient light sensor device to the embedded controller. The embedded controller is then programmed to detect changes in the ambient light and generates an ACPI-visible interrupt (EC_SCI). The backlight should be controlled through Backlight Control mechanism (BLC) of the Intel® Atom™ Processor E6x5C Series. The backlight inverter module can be PWM or GMBus-based as discussed in Section 8.7.4.

For more information, please refer to the *Intel® Display Power Saving Technology 5.0 and Intel® Automatic Display Brightness – Application Notes / Briefs*.

8.8 Errata BI38 Clarification: Processor May Not Recognize Signal PWROK on Its Inital Assertion

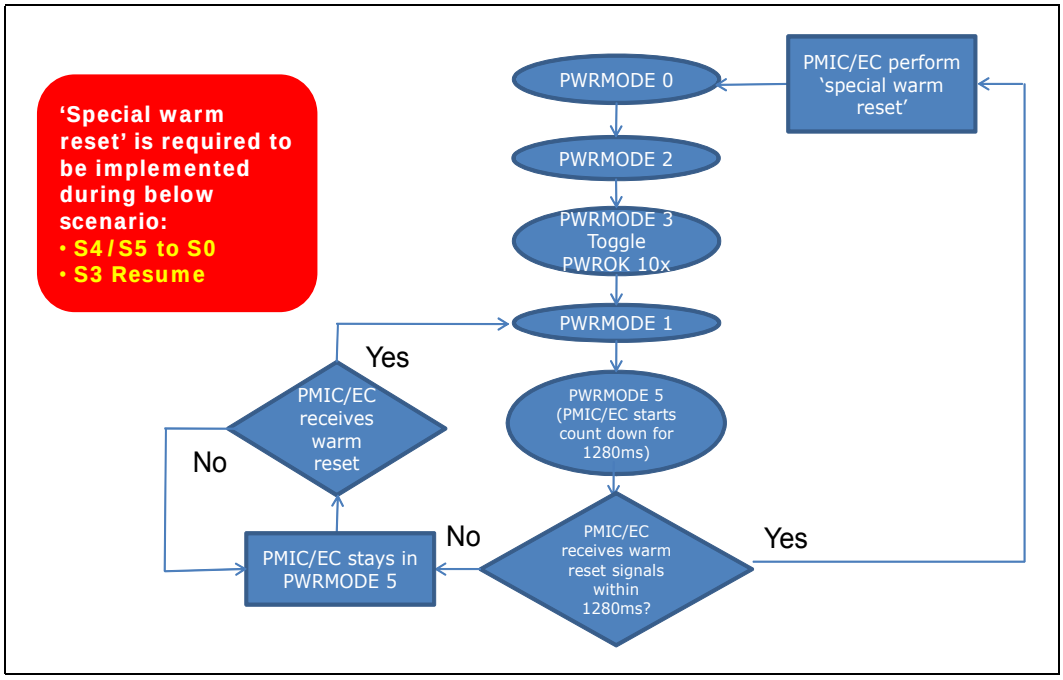
Due to errata BI38, customers must toggle the PWROK signal for 10x, as mentioned in section 8.6, "Platform Power Sequencing Requirements". In addition, the Intel® Atom™ Processor E6x5C Series has implemented a special warm reset based on an internal counter of 1280ms. Table 61 shows the differences between the special warm reset and normal warm reset implemented in the Intel® Atom™ Processor E6x5C Series.

Table 61. Differences Between Special Warm Reset and Normal Warm Reset

Special Warm Reset	Normal Warm Reset
Sent out before 1280ms	Sent out after 1280ms
RSMRST_N maintain high (de-asserted)	RSMRST_N maintain high (de-asserted)
Input and SUS clock maintain valid	Input and SUS clock maintain valid
VCC Core and VCC SUS power maintain valid	VCC Core and VCC SUS power maintain valid
PMIC/CPLD reset to powermode M0	PMIC/CPLD reset to powermode M1

Figure 56 explains how the special warm reset works in the Intel® Atom™ Processor E6x5C Series.

Figure 56. Implementation of Special Warm Reset



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9.0 JTAG

This chapter contains information about:

- JTAG overview
- JTAG pins connection
- Unused JTAG pins

9.1 Overview

The Intel® Atom™ Processor E6x5C Series device is a Multi-chip package (MCP) consisting of the Intel® Atom™ Processor E6x5C Series CPU and an Altera FPGA. From a JTAG perspective the CPU and the FPGA can be treated as independent devices. Each has its own external independent JTAG port. The FPGA JTAG port functions identically to JTAG ports on discrete ArriaII Gx devices.

The processor supports a JTAG/IEEE1149.1 Test Access Port which supports public instructions (EXTEST, SAMPLE/PRELOAD, CLAMP, HIGHZ, IDCODE, BYPASS).

- The JTAG interface is accessible only after PWROK is asserted.
- 6 TAP controllers, 4 TAP for the CPU core and 2 TAP for IO

Refer to the *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for more information.

For more detailed information on the Intel® Atom™ Processor E6x5C Series FPGA JTAG port, and associated routing guidelines please refer to Altera JTAG literature for ArriaII Gx devices.

9.2 JTAG Pins

The Intel® Atom™ Processor E6x5C Series requires four JTAG input pins and one output pin for each CPU, IO core and North Complex. The pins are:

- TRST_N, IO_TRST_N and NCTRST_N (Test Reset)
- TCK, IO_TCK and NCTCK (Test Clock)
- TMS, IO_TMS and NCTMS (Test Mode Select)
- TDI, IO_TDI and NCTDI (Serial Test Data In)
- TDO, IO_TDO and NCTDO (Serial Test Data Out)

It is recommended to use daisy-chained between XDP for the Intel® Atom™ Processor E6x5C Series and XDP for the IO debug port. For more information, please refer to the Intel® Atom™ Processor E6x5C Series – *Debug Port Design Guide* for more information.

The Intel® Atom™ Processor E6x5C SeriesFPGA JTAG pins are

- 8C_TIO_Config_TCK
- 8C_TIO_Config_TMS
- 8C_TIO_Config_TDI
- 8C_TIO_Config_TDO

The Intel® Atom™ Processor E6x5C Series FPGA JTAGcan be used for device configuration and for devixe debug using Altera SignalTap. It is strongly recommended to route this JTAG port to a header to support these capabilities.

9.2.1 JTAG Pins Connection

If XDP is used, it is recommended to:

- Pull TDI and TMS pins to V1P05 with 56.2 Ω to 60.2 Ω, 1%, 0402 resistors; and close to XDP debug port
- Pull TDO pins to V1P05 with 56.2 Ω to 60.2 Ω, 1%, 0402 resistors; and close to Intel® Atom™ Processor E6x5C Series
- Pull TRST_N pin to ground with 49.9 Ω to 60.2 Ω, 1%, 0402 resistor; and close to XDP debug port
- Pull TCK pin to ground with 56.2 Ω to 60.2 Ω, 1%, 0402 resistor; and close to XDP debug port

9.2.2 Unused JTAG Pins

If boundary scan is not implemented on the system board, TMS and TDI must be independently bused and pulled up, each with ~10 kΩ, 5%, 0402 resistors, and TRST_N and TCK must be independently bused and pulled down, each with ~1 kΩ, 1%, 0402 resistors. TDO must be left open.

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10.0 System Management Controller

This chapter contains information about the System Management Controller (SMC) function implemented in an FPGA or CPLD. This chapter will refer to the device as CPLD, as this is the most likely device used for this function.

10.1 Overview

The Intel® Atom™ Processor E6x5C Series CRB platform power management transitions are handled by Altera* Cyclone FPGA. (Since the FoxBrook CRB was initially developed as a validation platform this FPGA also included validation features not required for standard designs.

The device is optimized for multi-voltage system power up and system reset. The CPLD is always powered up first and then manages the start sequences for other devices.

The CPLD interfaces with the Intel® Atom™ Processor E6x5C Series via the SLPMODE, SLPRDY_B, RSTRDY_B and RSTWARN signals to determine Intel® Atom™ Processor E6x5C Series driven power transitions and M-state of the processor. Refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for more information.

Other uses of the SMC FPGA (other than power sequencing) are:

- VID multiplexing
- Control the THERMTRIP LED indicators
- Programming E6x5C FPGA Image from SPI PROM

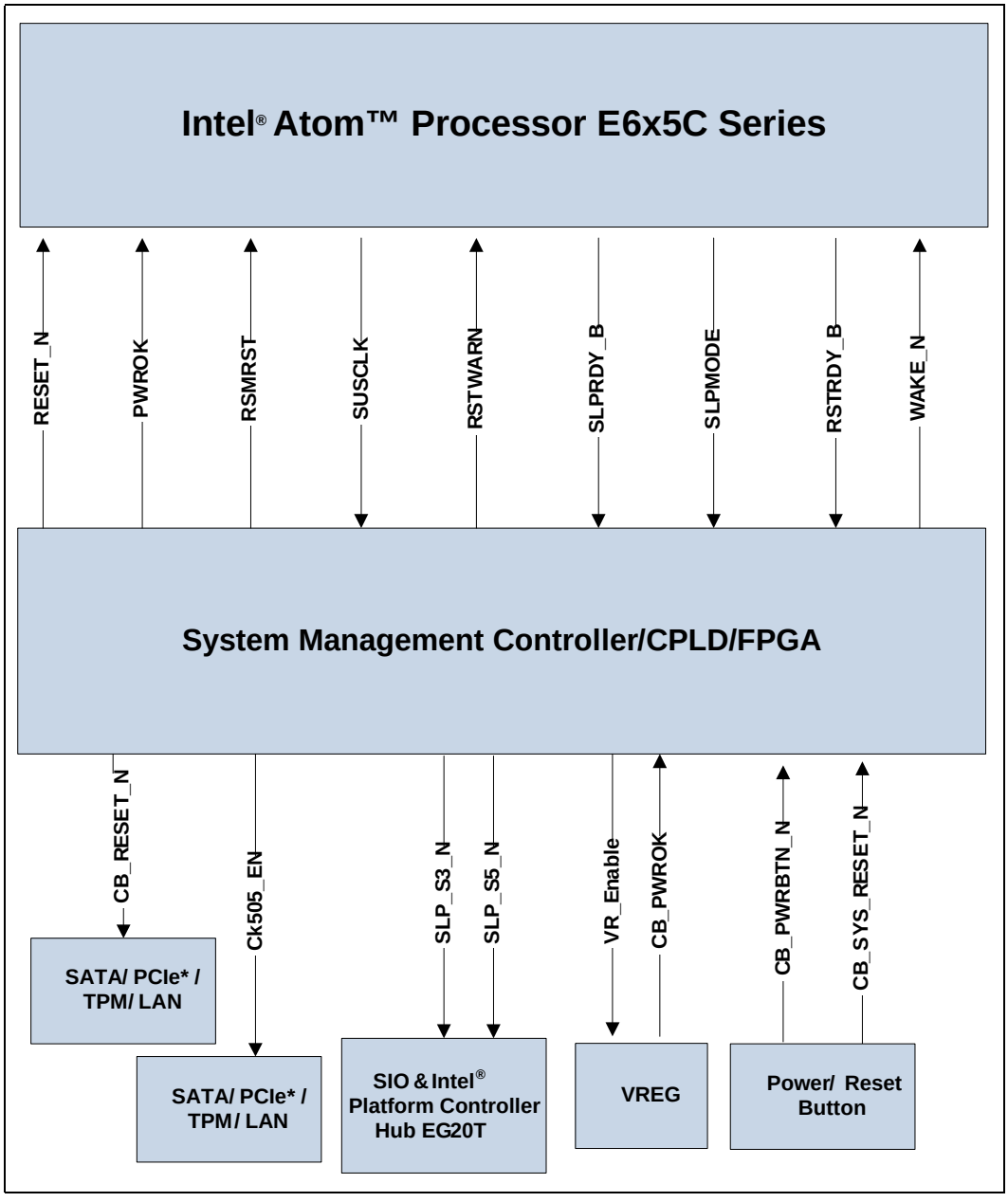
Please refer to your vendor web site for more information about their CPLD board design requirements.

You may use a microcontroller or Power Management IC solution from Dialog* and ROHM* to achieve the same purpose as stated above. Please consult with Rohm & Dialog on how best to use their produtcs with the E6x5C device.

The source code of the FoxBrook SMC FPGA may be attained following a license agreement approval from Intel. Please contact you Intel representitive for details.The code is provided for reference only and it is the users responsibility to ensure it meets the timing and logic requirements of the Intel® Atom™ Processor E6x5C Series device.

Figure 57 shows the general overview of CPLD signals that are connected to the processor and other devices on the CRB.

Figure 57. System Management Controller — CPLD



The processor supports the S0, S3, S4 and S5 platform states. These states are defined in *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* (refer to Chapter 11 in the EDS for timing diagrams implemented in the CPLD code).

Table 63 defines the transitions supported in the CPLD code and the reference timing diagram from the *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*.

Table 62. Transition Supported in the CPLD

Transition	EDS Chapter	Description
S0 to S3 to S4/S5	11.8.3	Initiated by BIOS and O/S.
S4/S5 to S0	11.8.2	Power button initiates S4/S5 transition to S0.
S3 to S0	11.8.5	Can be internal triggered wake event or external triggered wake event. When the Intel® Atom™ Processor E6x5C Series detects wake event, it deasserts SLPRDY_B to the CPLD.
Cold Reset	11.10.1	
Warm Reset	11.10.2	Support Internal and External events
Catastrophic Shutdown	11.10.5	Power Button initiates the shutdown when the system is in S0. External events, e.g. Thermal

Table 64 shows the Intel® Atom™ Processor E6x5C Series and the CPLD power management handshaking signals.

Table 63. Intel® Atom™ Processor E6x5C Series and CPLD Power Management Handshaking Signals

Signal	Direction	Descriptions
SLPMODE	Output from the Intel® Atom™ Processor E6x5C Series to CPLD	**SLEEP MODE.** It determines which sleep state is entered. When SLPMODE is HIGH -> S3 is chosen. When SLPMODE is LOW -> S4/S5 is chosen.
SLPRDY_N	Output from the Intel® Atom™ Processor E6x5C Series to CPLD	**SLEEP READY.** Intel® Atom™ Processor E6x5C Series drives the signal LOW to indicate to the CPLD that the processor is awake and able to be placed into a sleep state. De-assertion of this signal indicates that a wake is being requested from a system device.
RSTRDY_N	Output from the Intel® Atom™ Processor E6x5C Series to CPLD	**RESET READY**. Assertion of this signal indicates to the CPLD that it is ready to be placed into a LOW power state. During a transition from S0 to S3/S4/S5 sleep states, the Intel® Atom™ Processor E6x5C Series asserts RSTRDY_N after detecting assertion of the RSTWARN signal from the CPLD.
RTSWARN	Input to the Intel® Atom™ Processor E6x5C Series from CPLD	**RESET WARNING.** Assertion of the RSTWARN signal tells the Intel® Atom™ Processor E6x5C Series to enter a sleep state or begin to power down. A CPLD might do so after an external event, such as pressing of the power button or occurrence of a thermal event.

Table 65 shows the CPLD Input Control Signals for System Power Management.

Table 64. The CPLD Input Control Signals for System Power Management

Signal	Direction	Descriptions
CB_RST_BTN_N	RESET Button to CPLD	**Connected to system reset signal button.** Whole platform will be reset when the RESET button is pressed. Only valid during S0.
CB_PWR_BTN_N	PWR Button to CPLD	**Connected to system power signal button.** Platform can be power on/down or woke up from S3 by pressing this PWR button. Valid in S0, S3 and S5. 4s assertion during S0 will trigger to power OFF. 1ms assertion triggers wake event if the system is in S3 or Power Up if the system is in S0.
CB_PWROK (From CRB Carrier Board)	PWROK from discrete components to CPLD	The PWROK signals are from miscellaneous discrete components like ATX Power Supply and voltage regulators. It is an indication to the CPLD that the power is stable.
VR PWRGD signals (From CRB Little Bay)	PWRGD from various VR	It is an indication of each Little Bay voltage regulators of VCC, VNN, 3.3V, 1.8V, 1.5V, 1.05V and 0.9V that the power is stable.
PWRMODE[2:0]	PWRMODE[] from Intel® Atom™ Processor E6x5C Series to CPLD	CPLD is expected to sequence the processor through various states using the PWRMODE[] pins to facilitate cold reset and warm reset.

Table 66 below shows the CPLD Output Control Signals for System Power Management.

Table 65. The CPLD Output Control Signals for System Power Management

Signal	Direction	Descriptions
SLP_S5_N	Output from CPLD to Intel® Atom™ Processor E6x5C Series	**Sleep S5.** When driven to LOW, all the power rails except the RTC power rails are turned OFF.
SLP_S3_N	Output from CPLD to Intel® Atom™ Processor E6x5C Series	**Sleep S3.** When driven LOW, the power planes required for S0 are OFF. Only the power planes required for S3/S4/S5 are ON.
CK505_EN	Output from CPLD to clock chip	**Clock Enable Signal.** When driven LOW, the CK505 is OFF. when driven HIGH, the CK505 is ON.
PWROK	Output from CPLD to Intel® Atom™ Processor E6x5C Series	**Power OK.** When asserted, PWROK is an indication to the Intel® Atom™ Processor E6x5C Series that core power is stable. PWROK can be driven asynchronously. PWROK signal must be toggle for 10x.
RSMRST_N	Output from CPLD to Intel® Atom™ Processor E6x5C Series	**Resume Well Reset.** It is used for resetting the resume well. An external RC circuit is required to ensure that the resume well power is valid prior to RSMRST# going high.

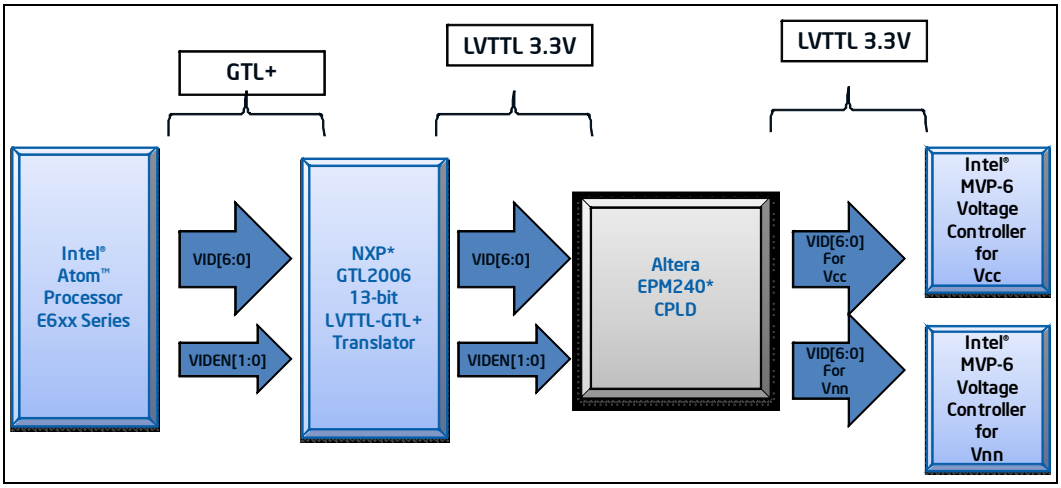
Table 65. The CPLD Output Control Signals for System Power Management

Signal	Direction	Descriptions
CPU_RST_N	Output from CPLD to Intel® Atom™ Processor E6x5C Series	**Force a reset** to Intel® Atom™ Processor E6x5C Series.
CB_RESET_N	Output from CPLD to other devices	**Force a reset** to other discrete components like PCIe* to PCI bridge.
VR Enable Control Signals	Output from CPLD to other voltage regulators	It is used to enable or disable the voltage regulators of VCC, VNN, 3.3V, 1.8V, 1.5V, 1.05V and 0.9V.

10.2 The Hardware Implementation

The VID[6:0], VIDEN[1:0], PWRMODE[2:0] and THERMTRIP signals of Intel® Atom™ Processor E6x5C Series are CMOS 1.05V IO standard. A set of voltage translator circuitry is required if the CPLD solution is not supporting the CMOS 1.05V standard. This was not required on the FoxBrook CRB since the FPGA I/O was configurable. If SMC functionality were implemented in a CPLD then this additional translation circuitry is required. Figure 58 shows the implementation.

Figure 58. The LVTTL to GTL+ Translation



Note: The illustration shows VID and VIDEN implementation only

10.3 The Current Code and Testing Status

The code is written with Verilog* language and compiled with Altera* Quartus* program. Although the code was successfully tested in hardware, the code has not been optimized for timing reduction.

10.4 The Hierarchy Files of CPLD Code

top.v

- **Top Level module**; it describes the modules that we have and includes the definition of inputs, outputs and registers.

max_osc.v

- Altera* MAX* II oscillator megafunction wizard; it describes the internal oscillator.

cru.v

- **Clock Unit Module**; it describes the clock unit which time the state machine, delays and counters.

pwr_mgt.v

- **Power management module**.

vr_seqcr.v

- **Voltage rails sequencer module**.

vid_demux.v

- Demuxing of VID values from Intel® Atom™ Processor E6x5C Series.

SPI2Arria_Config

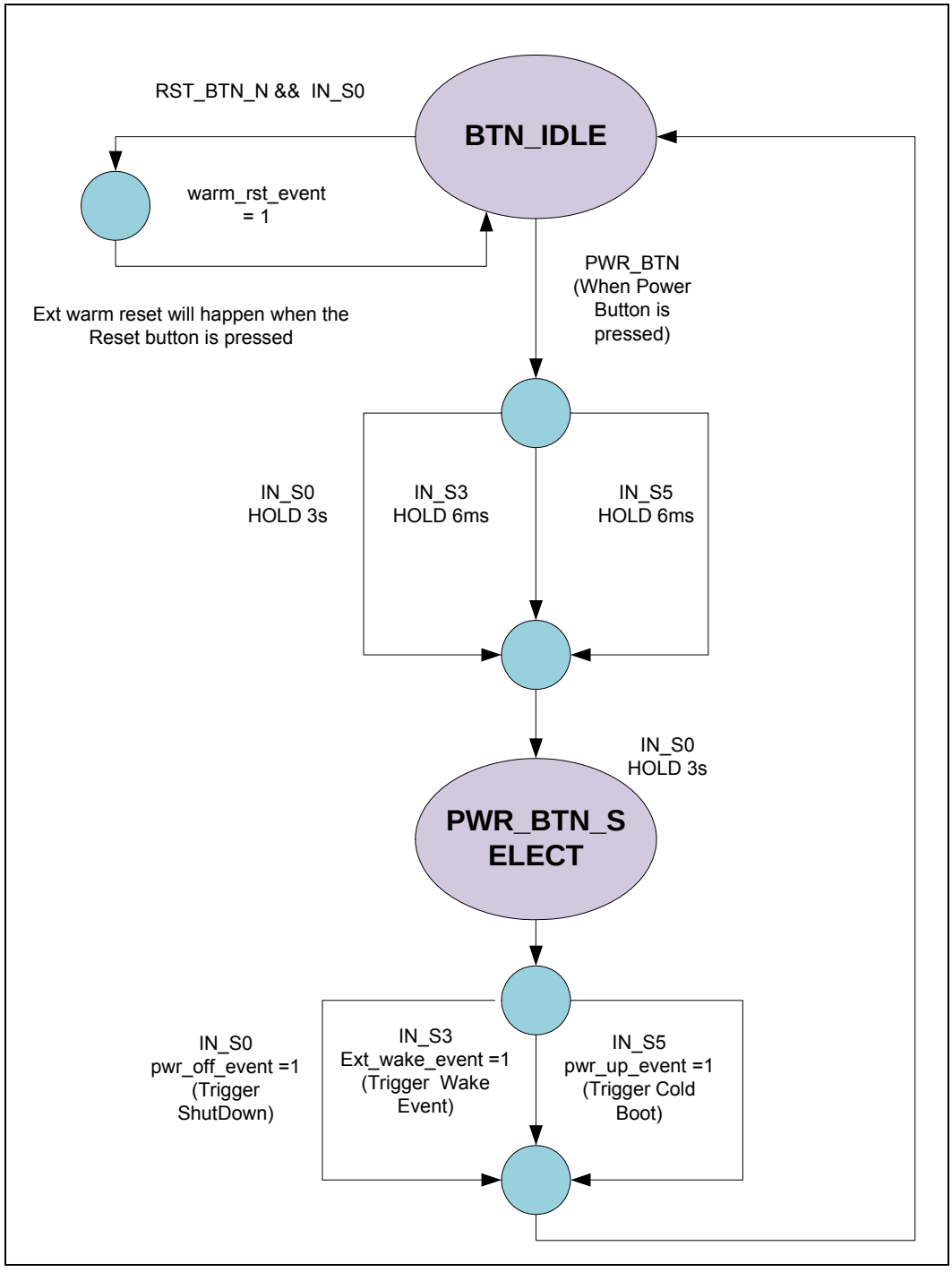
- Configuring the E6x5C FPGA from the SPI PROM device.

10.5 Power Management Design Overview

10.5.1 External Trigger Events

The CPLD is designed and triggered with 2 external switches, Power and Reset buttons. The buttons are designed with latches to get clean debounce without a delay limitation. The debounce is accomplished by a 25-bit down counter. Figure 59 shows the overview of external trigger events and for more detail refer to pwr_mgt.v Verilog* file.

Figure 59. Overview Of External Trigger Events



10.5.2 Platform Power Up Sequence (S4/S5 to S3 to S0 Sequence)

A 25-bit counter is used in the design to control timing of the output control signals. A state machine consisting of 10 states (COLD_BOOT) and 1 state (WAIT_FOR_BSEL) is designed in the pwr_mgt.v Verilog* files.

The sequence occurs whenever the system is in the S4 or S5 state and the CPLD initiates the exit sequence from S4/S5 to S0. Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*, section 11.8.2 for timing details.

1. The CPLD detects an event (i.e., power button) to initiate transition from S4/S5 to S0.
2. The CPLD enables the Vcc_Sus power rails according to the sequence requirements outlined in *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* and drives the PWRMODE to the M0 state.
3. The CPLD de-asserts RSMRST_B after the Vcc_Sus rails becomes stable.
4. Vcc_Core, Vcc and Vnn may be enabled after the initiation of the S4/S5 to S0 event. The Vcc and Vnn voltage rails must be driven to the default value (Vcc = 1.1V & Vnn = 0.9V).
5. Once the voltage rails are stable, the CPLD transitions PWRMODE to the M2 state, followed by M3 state.
6. During M3 state,
   a. The processor will drive a valid VID to the Vnn voltage regulator. The Vnn voltage regulator must be stabilized to the new Vnn voltage as soon as possible.
   b. The processor will drive a valid BSEL signal. The input clocks to the processor must be stable after receiving the valid BSEL signal.
   c. Once the clocks are stable, the CPLD will asserts PWROK to the processor, followed by driving RSTWARN to LOW.
   d. The CPLD will de-assert RESET_B to the processor after PWROK is stable.
   e. The CPLD must ensure the processor resides in the M3 for a certain period of time. Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for the timing.
7. After RESET_N is stable, the CPLD will drive the PWRMODE to the M1 state.
8. During M1 state, the Intel® Atom™ Processor E6x5C Series will drive a valid VID[6:0] for the Vcc voltage regulator. The VID[6:0] value is based on the fusing of the processor.
9. The CPLD will drive the PWRMODE to M5 state after the Vcc has stabilized to the fused value.
10. The processor will begin fetching code from SPI interface after entering the M5 PWRMODE state.

Figure 60 and Figure 61 explain the Intel® Atom™ Processor E6x5C Series platform power up sequence which is implemented in the CPLD.

Figure 60. Platform Power Up Sequence State Machine (1)

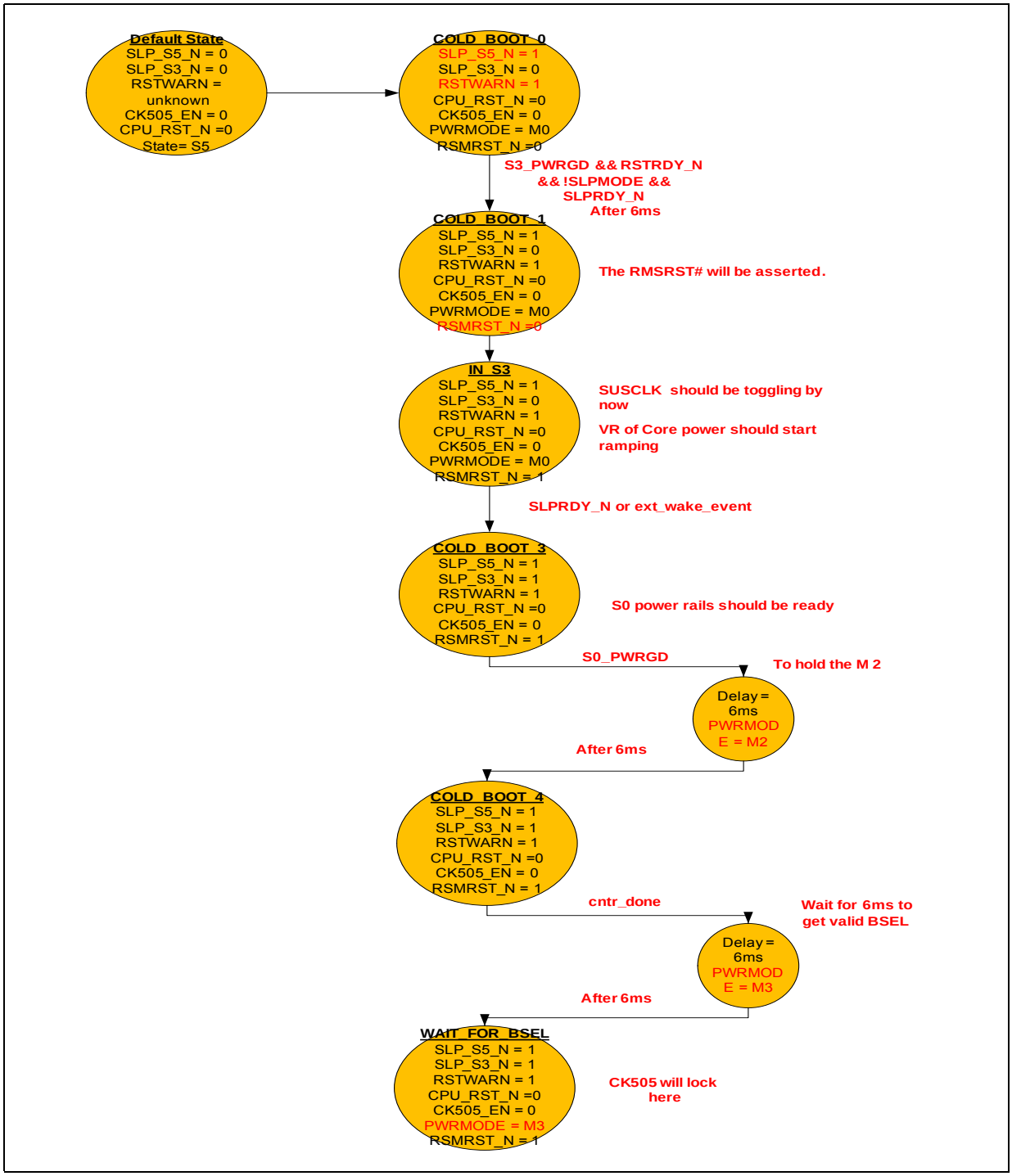
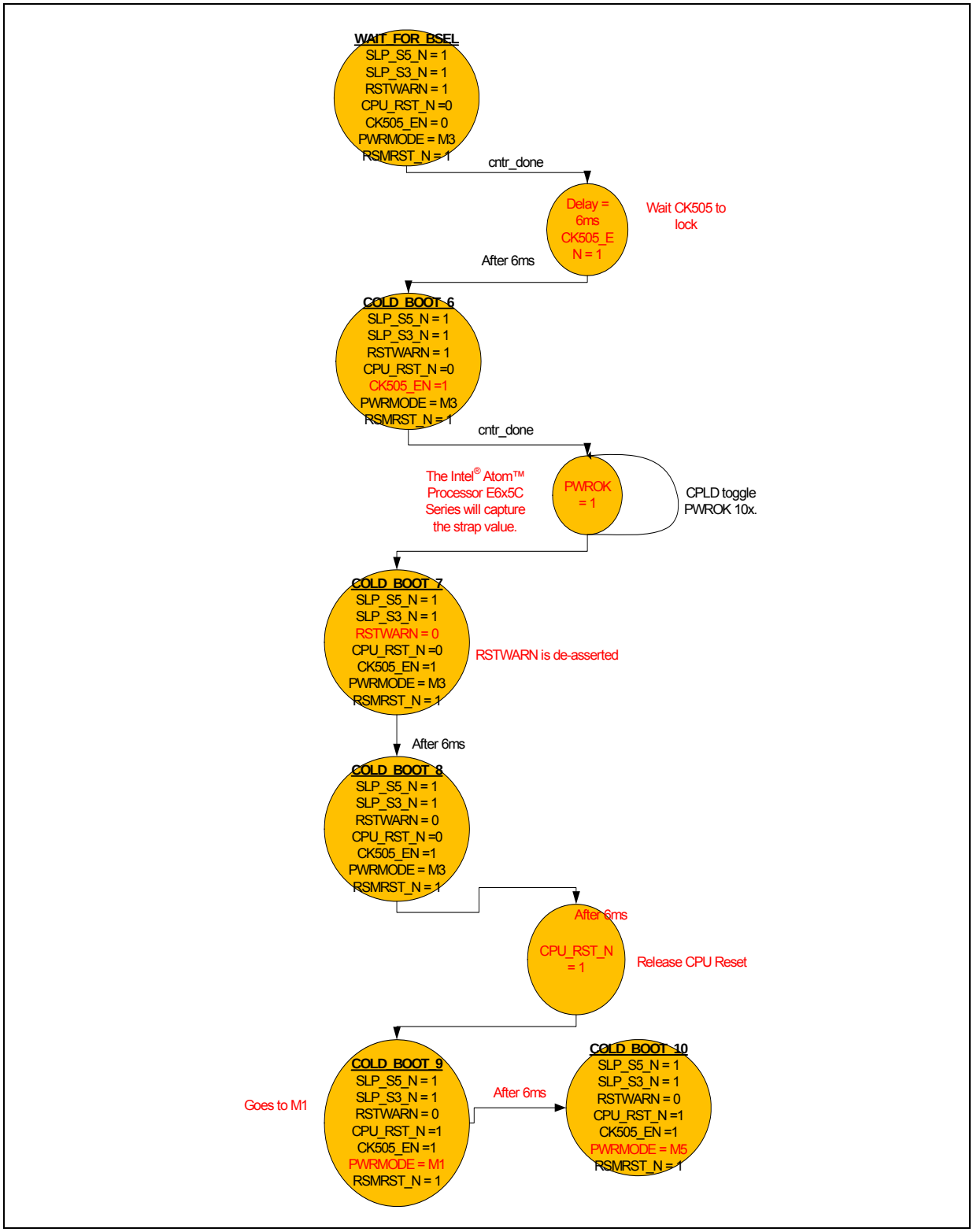


Figure 61. Platform Power Up Sequence State Machine (2)



10.5.3 Power Down Sequence (S0 to S3 to S4/S5 Sequence)

The sequence occurs whenever the system is in the S0 state and the Intel® Atom™ Processor E6x5C Series initiates the exit sequence from S0 to S3 or S4/S5. Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*, section 11.8.3 for timing details.

1. The Intel® Atom™ Processor E6x5C Series drives the SLPMODE pin to signal the desired sleep state. For S3, SLPMODE pin is driven HIGH, for S4/S5 the SLPMODE pin is driven LOW.
2. After SLPMODE has been driven to the desired sleep state, the processor drives the SLPRDY_B signal LOW.
3. Once the CPLD detects the sleep request from the processor, it must respond by driving RSTWARN HIGH.
4. Upon detecting RSTWARN HIGH, the processor asserts RSTRDY_B to indicate to the CPLD that it is ready to placed into the programmed sleep state.
5. After detecting the assertion of RSTRDY_B, the CPLD asserts RESET_B to the processor. The CPLD must also place the processor in the M1 PWRMODE state.
6. After the CPLD asserts the RESET_B, the CPLD will de-assert the PWROK signal and transition the processor into the M0 PWRMODE state.
7. After de-assertion of PWROK signal, the CPLD can disable all Vcc_core wells (including Vcc and Vnn) according to the rules listed in *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*.

This completes the entry to S3. If SLPMODE was LOW (indicating S4/S4 was the desired state) the CPLD takes the additional actions:

8. The CPLD asserts RSMRST_B. This causes SUSCLK to be disabled and SLPRDY_B, RSTRDY_B, and SLPMODE to return to their reset states.
9. After RSMRST_B is asserted, the CPLD may disable the Vcc_Sus wells and the system is now in the S4/S5 state.

Figure 62 explains the Intel® Atom™ Processor E6x5C Series platform power down sequence which implemented in CPLD.

10.5.4 Cold Rest Sequence

The sequence occurs whenever the system is in the S0 state and the processor initiates the Cold Reset Sequence. Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*, section 11.10.1 for timing details.

1. The processor drives SLPMODE = 0, SLPRDY_B = 1 and RSTRDY_B = 0 signaling to the CPLD to execute a cold reset.
2. Once the CPLD detects the cold reset sequence from the processor, the CPLD must respond by driving RSTWARN HIGH.
3. After asserting RSTWARN, the CPLD will assert RESET_B to the processor, followed by transitioning the processorprocessor to the M1 PWRMODE state.
4. After asserting RESET_B, the CPLD de-asserts the PWROK signal and transitions the processor into the M0 PWRMODE state.
5. After de-asserting PWROK signal, the CPLD can disable all Vcc_core wells including Vcc and Vnn.
6. After Vcc_core wells are disabled, the CPLD asserts RSMRST_B and this causes the SUSCLK to be disabled; SLPRDY_B, RSTRDY_B and SLPMODE return to their reset states.

7. After RSMRST_B is asserted, the CPLD may disable the Vcc_Sus wells and the system now is in the S4/S5 state.

8. The CPLD returns the system to S0 after a duration not more than 5s.

Figure 62 explains the Intel® Atom™ Processor E6x5C Series platform Cold Reset sequence which is implemented in the CPLD.

10.5.5 Warm Rest Sequence (Internal)

The sequence occurs whenever the system is in the S0 state and the processor initiates the Warm Reset Sequence (Internal). Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*, section 11.10.2 for timing details.

1. The processor drives SLPMODE = 1, SLPRDY_B = 1, RSTRDY_B = 0, signaling to the CPLD to execute a warm reset.
2. Once the CPLD detects the warm reset request from the processor, it must respond by driving RSTWARN HIGH.
3. After asserting the RSTWARN, the CPLD asserts RESET_B to the processor. The CPLD must also place the processor in the M1 PWRMODE state. The PWRMODE must not be driven to M0 when performing a warm reset.
4. The CPLD de-asserts RESET_B and drives RSTWARN LOW after ***"t"*** timing. Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for the timing.
5. RSTRDY_B and SLPMODE return to their S0 values.
6. The CPLD skips the M0, M2, M3 PWRMODE and returns the system to the M5 PWRMODE.

Figure 62 explains the Intel® Atom™ Processor E6x5C Series platform Warm Reset sequence (internal), which is implemented in CPLD.

10.5.6 Warm Rest Sequence (External)

The sequence occurs whenever the system is in the S0 state and the processor initiates the Warm Reset Sequence (External). Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)*, section 11.10.3 for timing details.

1. The CPLD detects a press of the "reset" button and asserts the RSTWARN signal to the processor.
2. The processor drives SLPMODE = 1, SLPRDY_B = 1, RSTRDY_B = 0, signaling to the CPLD to execute a warm reset.
3. The CPLD asserts RESET_B to the processor. The CPLD must also place the processor in the M1 PWRMODE state. The PWRMODE must not be driven to M0 when performing a warm reset.
4. The CPLD de-asserts RESET_B and drives RSTWARN LOW after ***"t"*** timing. Please refer to *Intel® Atom™ Processor E6x5C Series – External Design Specification (EDS)* for the timing.
5. RSTRDY_B and SLPMODE returns to their S0 values.
6. The CPLD skips the M0, M2, M3 PWRMODE and returns the system to the M5 PWRMODE.

Figure 62 explains the Intel® Atom™ Processor E6x5C Series platform Warm Reset sequence (external), which is implemented in CPLD.

10.5.7 Catastrophic Shutdown

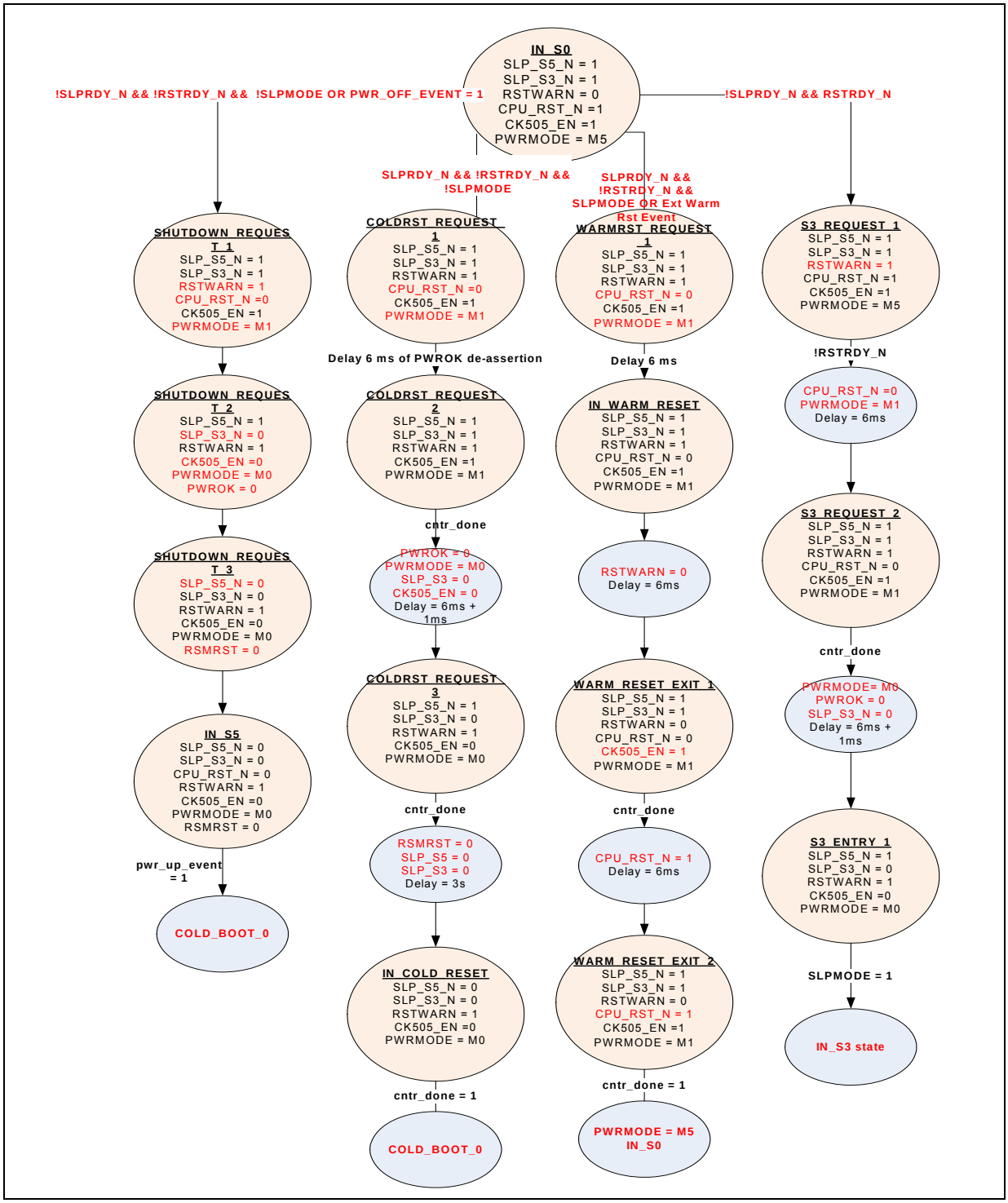
The catastrophic shutdown sequence is asynchronous to all handshakes. This sequence request can occur at any time, including in the middle of another sleep or reset sequence. Therefore, the CPLD should be able to handle this request at any time.

The shutdown is initiated by the processor driving SLPMODE, SLPRDY_B and RSTRDY_B to all 0's at the same time.

The CPLD, upon seeing this condition, should perform the shutdown of all power wells (except RTC) in the proper order, but should forsake any handshakes or delay insertion.

The Figure 62 explains the Intel® Atom™ Processor E6x5C Series platform Catastrophic Shutdown which is implemented in the CPLD.

Figure 62. Shutdown, Cold, Warm Reset and Catastrophic Sequences State Machine



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11.0 FPGA Power Supply Design

11.1 Introduction

This chapter explains the power supply requirements for the FPGA part of the Intel® Atom™ Processor E6x5C Series. There is no special sequencing requirement for the FPGA portion as long as all the power supplies are ramped up within the T-ramp period. This chapter also discusses the relation between reset signals and power sequencing.

Table 66. Power Supply Names and Description

Supply Name (Name In Altera FPGA documents)	Nominal Voltage	Description
ARRIA_VCC (VCC)	0.9 V	Supplies power to the core, periphery, I/O registers, PCI Express®(PCIe®) hard Intellectual Property (hard IP) block, and transceiver physical coding sub-layer (PCS)
X_TC_L_VCCD1, X_TC_R_VCCD2, X_BC_R_VCCD3, X_BC_L_VCCD4 (VCCD_PLL)	0.9V	Supplies power to the digital portions of the phase-locked loop (PLL)
X_TC_L_VCCA1, X_TC_R_VCCA2, X_BC_R_VCCA3, X_BC_L_VCCA4 (VCCA_PLL)	2.5V	Supplies power to the analog portions of the PLL and device-wide power management circuitry
ARRIA_VCCR (VCCCB)	1.5V	Supplies power to the configuration RAM bits
X_LC_T_VCCBAT (VCCBAT)	1.2V -3.3V	Battery back-up power supply for the design security volatile key register
ARRIA_VCCE (VCCL_GXB)	1.1V	Supplies power to the transceiver PMA TX, PMA RX, and clocking
ARRIA_VCCEHT (VCCH_GXB)	1.5V	Supplies power to the transceiver PMA output (TX) buffer
ARRIA_VCCEH (VCCA)	2.5V	Supplies power to the transceiver physical medium attachment (PMA) regulator
3A_BIO1_VREF3A, 4A_BIO6_VREF4A, 5A_RIO1_VREF5A, 6A_RIO8_VREF6A, 7A_TIO6_VREF7A, 8A_TIO1_VREF8A (VREF)	0.6 V, 0.75 V, 0.9 V, 1.25 V	Reference voltage for the voltage-referenced I/O standards
VCCN*A (VCCIO)	1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V	Supplies power to the I/O banks
VCCPD*A (VCCPD)	2.5 V, 3.0 V, 3.3 V	Supplies power to the I/O pre-drivers, differential input buffers

11.2 Power-On Reset Circuitry

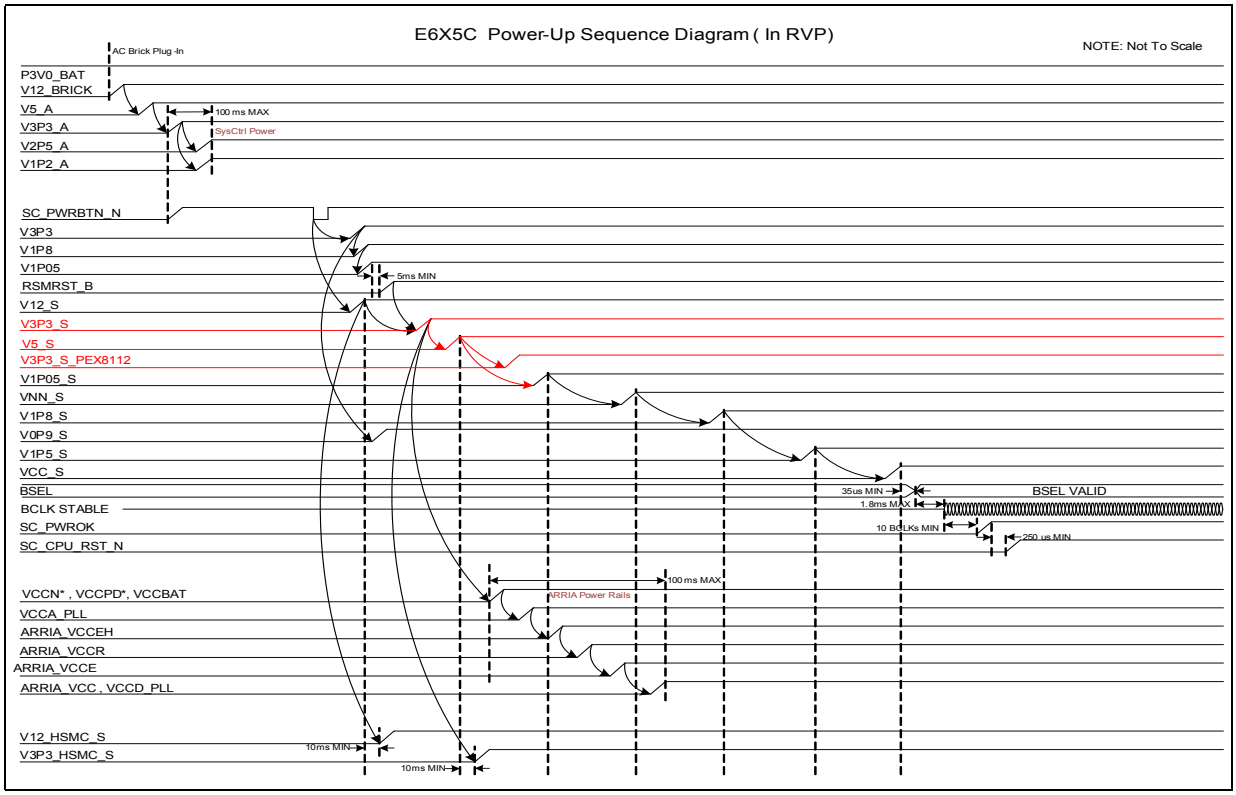
The FPGA power-on reset (POR) circuitry generates a POR signal to keep the device in the reset state until the power supply's voltage levels have stabilized during power-up. The POR circuitry monitors Arria_VCC, X_TC_L_VCCA1, X_TC_R_VCCA2, X_BC_R_VCCA3, X_BC_L_VCCA4, X_LC_T_VCCBAT and supplies for I/O banks 3C and 8C (VCCPD3C, VCCPD8C and VCCN3C, VCCN8C) in the FPGA, where the configuration pins are located. The POR circuitry tri-states all user I/O pins until the power supplies reach the recommended operating levels. These power supplies are required to monotonically reach their full-rail values without plateaus and within the maximum power supply ramp time (tRAMP). The POR circuitry de-asserts the POR signal after the power supplies reach their full-rail values to release the device from the reset state.

POR circuitry is important to ensure that all the circuits in the FPGA are at certain known states during power up. You can select the POR signal pulse width between fast POR time and standard POR time using the MSEL pin settings. For fast POR time, the POR signal pulse width is set to 4 ms for the power supplies to ramp up to full rail. For standard POR time, the POR signal pulse width is set to 100 ms for the power supplies to ramp up to full rail. In both cases, you can extend the POR time with an external component to assert the nSTATUS pin low. This is recommended sharing power supplies with other components on the board necessitates a need for longer ramp time.

11.3 Power Sequencing Requirements

There is no specific requirement for sequencing the power supply to FPGA other than meeting the ramp time of 100ms from the ramp of first power supply to the ramp of the last power supply for FPGA. The diagram below shows the sequencing and ramp requirement for all the power supplies in the Intel® Atom™ Processor E6x5C Series and their relation to the reset signals.

Figure 63. Power-up Sequence Diagram (in RVP)



11.4 Additional Resources

Altera has a power distribution network tool that customers can use to design their power distribution. This tool can be downloaded from the Altera web site and Device-Specific Power Delivery Network (PDN) Tool User Guide explains how to use the tool. The PDN printed circuit design methodology is described in detail in the Application note AN 574: Printed Circuit Board (PCB) Power Delivery Network (PDN) Design Methodology a (PDF). It also describes the role of Feffective in designing an efficient system delivery solution. Step by step procedure to design the power supply has a checklist that can be used by the board designer. Pin connection guide lines discuss Power supply sharing guidelines.

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12.0 FPGA Design and Configuration

12.1 Introduction

The FPGA portion of the Intel® Atom™ Processor E6x5C Series can be designed using QuartusII subscription edition software version 10.1 or higher. This chapter explains the design flow and configuration options for the FPGA. Additional documentation is available on the Altera Web site.

12.2 Creating Design Specifications

Before creating the logic design or completing the system design, prepare detailed FPGA design specifications. The specifications define what the system should do and should specify:

- the I/O interfaces for the FPGA
- how the IP communicates with the interfaces and the Intel® Atom™ core
- how to configure the PCIe* link to the Intel® Atom™ core (for more details please refer to PCIe* chapter of the design)
- a block diagram of basic design functions

Taking the time to create these specifications will help improve design efficiency.

Creating an FPGA test plan at this phase can also help design for testability and manufacturability. For example, do you want to perform any built-in self-test functions to drive interfaces? Do you need to have loop back capabilities to test interfaces?

12.3 Device Selection

Once the specification part is complete you need to choose FPGA device in the Intel® Atom™ Processor E6x5C Series. This can be done by selecting EP2AGXE6XXFPGA from the device selection menu in Quartus design tool.

12.4 Design Flow

12.4.1 Design Entry

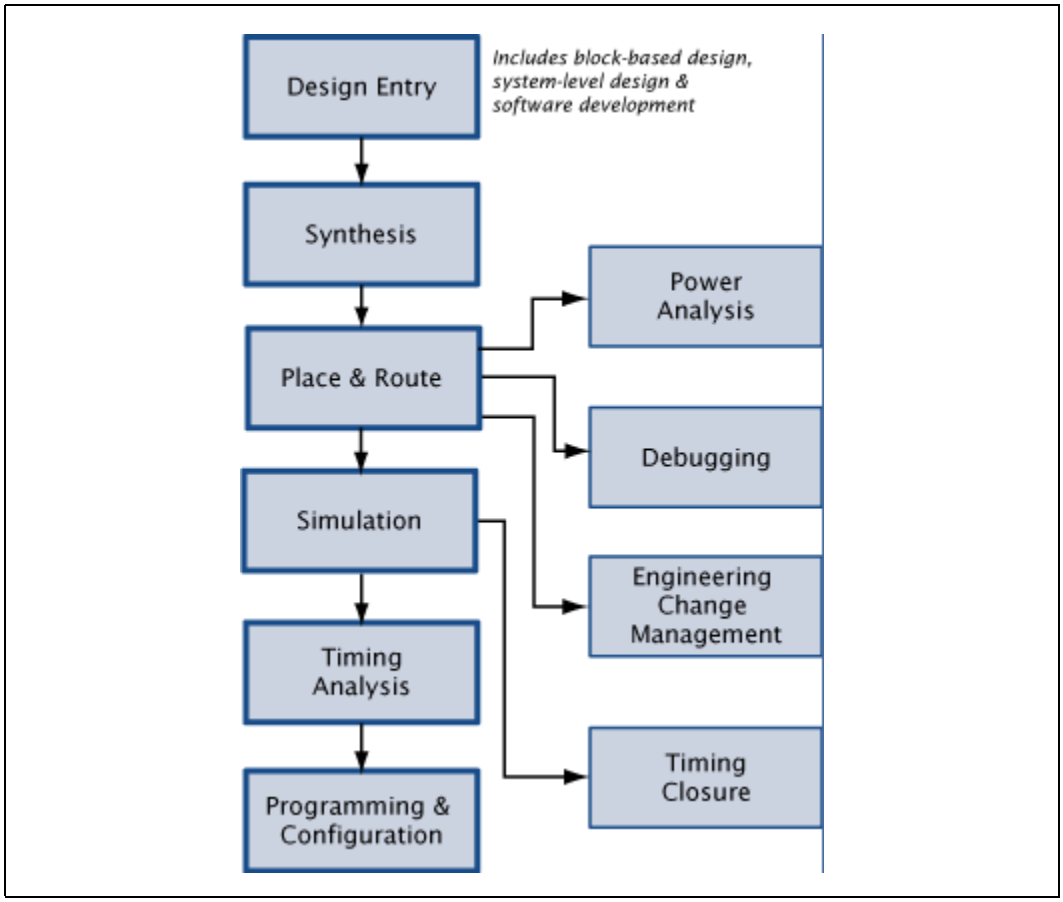
You can use the Quartus II Block Editor, Text Editor, MegaWizard Plug-In Manager, and EDA design entry tools to create the design files in a project. You can create schematic or block designs with the Block Editor, or you can create AHDL, VHDL, or Verilog HDL designs with the Text Editor. The MegaWizard Plug-In Manager helps you to create design files for customized megafunctions. The Quartus II software also supports EDIF Input Files (.edf) or Verilog Quartus Mapping Files (.vqm) generated by EDA design entry and synthesis tools. The following sections contain more information about design entry methods.

The Block Editor allows you to enter and edit graphic design information in the form of schematics and block diagrams. The Block Editor reads and edits Block Design Files (.bdf).

You can create Block Design Files that contain blocks and symbols that represent logic in the design. The Block Editor incorporates the design logic represented by each block diagram, schematic, or symbol into the project. You can create new design files from the blocks in a Block Design File, update the design files when you modify the blocks and the symbols, and generate Block Symbol Files (.bsf),AHDL Include Files (.inc), and HDL files from Block Design Files. You can also analyze the Block Design Files for errors before compilation.

The Block Editor also provides a set of tools that help you connect blocks and primitives together, including bus and node connections and signal name mapping. You can change the Block Editor to display options, such as guidelines and grid spacing, rubberbanding, colors and screen elements, zoom, and different block and primitive properties to suit your preferences.

Figure 64. FPGA Implementation Flow



The Quartus II Text Editor is a flexible tool for entering text-based designs in the AHDL, VHDL, Verilog HDL, and Tcl script languages. You can also use the Text Editor to edit other ASCII text files, including internal files created by the Quartus II software. You can use the Quartus II Text Editor to create text design files and combine them with other types of design files in a hierarchical design. Verilog Design Files and VHDL

Design Files can contain any combination of Quartus II–supported constructs, as well as Altera-provided logic functions, including primitives, megafunctions, and user-defined logic functions.

The Text Editor also provides templates for AHDL statements, Tcl commands, and supported VHDL or Verilog HDL constructs. AHDL, VHDL, and Verilog HDL templates provide an easy way for you to enter HDL syntax, increasing the speed and accuracy of design entry. You can get context-sensitive help on all AHDL elements, keywords, and statements, as well as on megafunctions and primitives.

You use the Create/Update command to create a Block Symbol File from a Verilog HDL or VHDL design file and then incorporate it into a Block Design File. Similarly, you can create an AHDL Include File that represents a Verilog HDL or VHDL design file and incorporate it into a Text Design File or another Verilog HDL or VHDL design file. For VHDL designs, you can specify the name of a VHDL library for a design in the Properties dialog box that is available from the Files page of the Settings dialog box or from the Files tab of the Project Navigator.

Altera megafunctions are high-level building blocks that can be used together with gate and flipflop primitives in Quartus II design files. The parameterizable megafunctions and LPM functions provided by Altera are optimized for Altera device architectures. You must use megafunctions to access some Altera device-specific features, such as memory, DSP blocks, LVDS drivers, PLLs, and SERDES and DDIO circuitry. You can use the **MegaWizard Plug-In Manager** to create Altera megafunctions, LPM functions, and IP functions for use in designs in the Quartus II software and EDA design entry and synthesis tools.

The **MegaWizard Plug-In Manager** helps you create or modify design files that contain custom megafunction variations, which you can then instantiate in a design file. These custom megafunction variations are based on Altera provided megafunctions, including LPM, MegaCore, and AMPP functions. The **MegaWizard Plug-In Manager** runs a wizard that helps you easily specify options for the custom megafunction variations. The wizard allows you to set values for parameters and optional ports. You can open the **MegaWizard Plug-In Manager** from the Tools menu or from within a Block Design File, or you can run it as a stand-alone utility.

12.4.2 I/O Assignment Validation

The Intel® Atom™ Processor E6x5C Series FPGA I/O assignment is different that that for discrete FPGA devices. The QuartusII software does not have the Intel® Atom™ Processor E6x5C Series pin-out within its libraries. The QuartusII software uses the Altera sub-package pin-out for the Intel® Atom™ Processor E6x5C Series. Therefore the pin-out translation the Microsoft Excel* file or tcl script must be used to translate the Quartus FPGA I/O to the physical pin-number of the Intel® Atom™ Processor E6x5C Series package. Detailed information on this process can be found in document #465465 “Mapping Altera* FPGA Pins to Intel® Atom™ Processor E6x5C Series Pins Application Note”. The Microsoft Excel* file is document #464895 “E6x5C to EP2AGXE6XXFPGA Pin Mapping” and the Tcl script is document #469824 “E6x5C Pin Mapping Tcl Script”.

Due to the multiple functions that many of the FPGA I/O pins possess and various limitations associated with certain functions, it is recommended to perform a complete I/O validation of the FPGA I/O prior to finalizing the schematics to ensure the schematic supports the FPGA implementation.

12.4.3 Synthesis

You can use the Analysis & Synthesis module of the Compiler to analyze and synthesize design files and create the project database. Analysis & Synthesis performs logic synthesis to minimize the logic usage of the design, and performs technology mapping

to implement the design logic using device resources such as logic elements. Finally, Analysis & Synthesis generates a single project database integrating all the design files in a design.

Analysis & Synthesis uses Quartus II Integrated Synthesis to synthesize your Verilog Design Files (.v) or VHDL Design Files (.vhd). You may use other EDA synthesis tools to synthesize your Verilog Design Files or VHDL Design Files, and then generate an EDIF netlist file (.edf) or a Verilog Quartus Mapping File (.vqm) that you can use with the Quartus II software.

You can start a full compilation, which includes the Analysis & Synthesis module, or you can start Analysis & Synthesis with the Start Analysis & Synthesis command for a design. The Quartus II software also allows you to perform an Analysis & Elaboration to check design files for syntax and semantic errors, or use the Analyze Current File command to check a single design file for syntax errors. These commands do not perform logic synthesis or technology mapping on the design logic.

Analysis & Synthesis considers specific logic as it generates the database and performs logic synthesis and optimizes the design.

As it generates the database, Analysis & Synthesis examines the logical completeness and consistency of the project, and checks for boundary connectivity and syntax errors (for example, mistyped keywords in Verilog or VHDL, or incorrect port names in entity instantiations).

As it generates the database, Analysis & Synthesis also synthesizes and optimizes your design. For example, it infers flipflops, latches and state machines from "behavioral" languages, such as Verilog HDL and VHDL. In addition, the module replaces operators, such as + or -, with modules from the Altera library of parameterized modules (LPM) functions, which are optimized for Altera devices.

Analysis & Synthesis performs logic synthesis using several algorithms to minimize gate count, remove redundant logic, and use the device architecture as efficiently as possible. The module also applies logic synthesis techniques to help implement timing requirements for a project, As part of the logic minimization and optimization process, logic and nodes in the project may be changed or removed.

Analysis & Synthesis also creates state assignments for state machines and makes choices that will minimize the number of resources used.

Analysis & Synthesis then performs technology mapping to group register and combinational resources into individual logic cell-sized units. In addition, in device architectures with shareable expander product terms, the number of logic cells and expander product terms is balanced to use resources efficiently.

12.4.4 Place and Route

The Quartus II Fitter, which is also known as the PowerFit Fitter, performs place and route, also referred to as "fitting" in the Quartus II software. Using the database that has been created by Analysis & Synthesis, the Fitter matches the logic and timing requirements of the project with the available resources of a device. The Fitter assigns each logic function to the best logic cell location for routing and timing, and selects appropriate interconnection paths and pin assignments.

If you have made resource assignments in your design, the Fitter attempts to match those resource assignments with the resources on the devices, tries to meet any other constraints you may have set, and then attempts to optimize the remaining logic in the design. If you have not set any constraints on the design, the Fitter automatically optimizes it. If it cannot find a fit, the Fitter terminates compilation and issues an error message.

You can start a full compilation in the Quartus II software, which includes the Fitter module, or you can start the Fitter separately. You must run Analysis & Synthesis successfully before starting the Fitter separately.

12.4.5 Timing Analysis

The TimeQuest Timing Analyzer provides a method of analyzing, debugging, and validating the performance of a design. Timing analysis measures the delay along the various timing paths and verifies performance and operation. You can specify constraints that help the design meet timing requirements by causing the Quartus II Fitter to optimize the placement of logic in the device in order to meet those constraints. The TimeQuest Timing Analyzer is a powerful ASIC-style timing analysis tool that uses industry standard constraint, analysis, and reporting methodologies. You can use the TimeQuest analyzer's GUI or command-line interface to constrain, run, and view results for all timing paths in the design.

Before running the TimeQuest analyzer, you must specify initial timing constraints that describe the clock characteristics, timing exceptions, and external signal arrival and required times. You can make initial timing constraints for your design using the TimeQuest Timing Analyzer Wizard. You can specify or modify timing constraints in the Synopsys Design Constraints (SDC) format using the TimeQuest Timing Analyzer GUI, the Quartus II Text Editor, or the command-line interface. The Quartus II Fitter optimizes the placement of logic in the device to meet your specified constraints.

Early in the design cycle, before final device fitting is completed, you can check preliminary timing data by running an early timing estimate with the Start Early Timing Estimate command. When your design is complete, you can run a full timing analysis following compilation.

During timing analysis, the TimeQuest analyzer analyzes the timing paths in the design, calculates the propagation delay along each path, checks for timing constraint violations, and reports timing results as slack in the Report pane and in the Console. If the TimeQuest analyzer reports timing violations, you can customize the reports to view precise timing information about specific paths. You can then determine whether the design requires additional timing constraints or exceptions, or if the design requires logic changes or place and route constraints.

12.4.6 Programming and Configuration

The Intel® Atom™ Processor E6x5C Series FPGA supports all of the configuration options that are supported by discrete ArriaIIGX FPGAs. Please refer to the Altera Literature “AGX52011 Configuring ArriaGX Devices” available from the Altera* website. This document describes the schematics configuration required for the various standard configuration modes.

Intel also implemented a scheme in which the Intel® Atom™ Processor E6x5C Series FPGA image and the Intel® Atom™ BIOS are stored in the same SPI Flash devices. The FPGA based SMC is used to access the SPI Flash device and emulates the SPI BIOS device for the Intel® Atom™ core and the configuration device for the Intel® Atom™ Processor E6x5C Series FPGA.

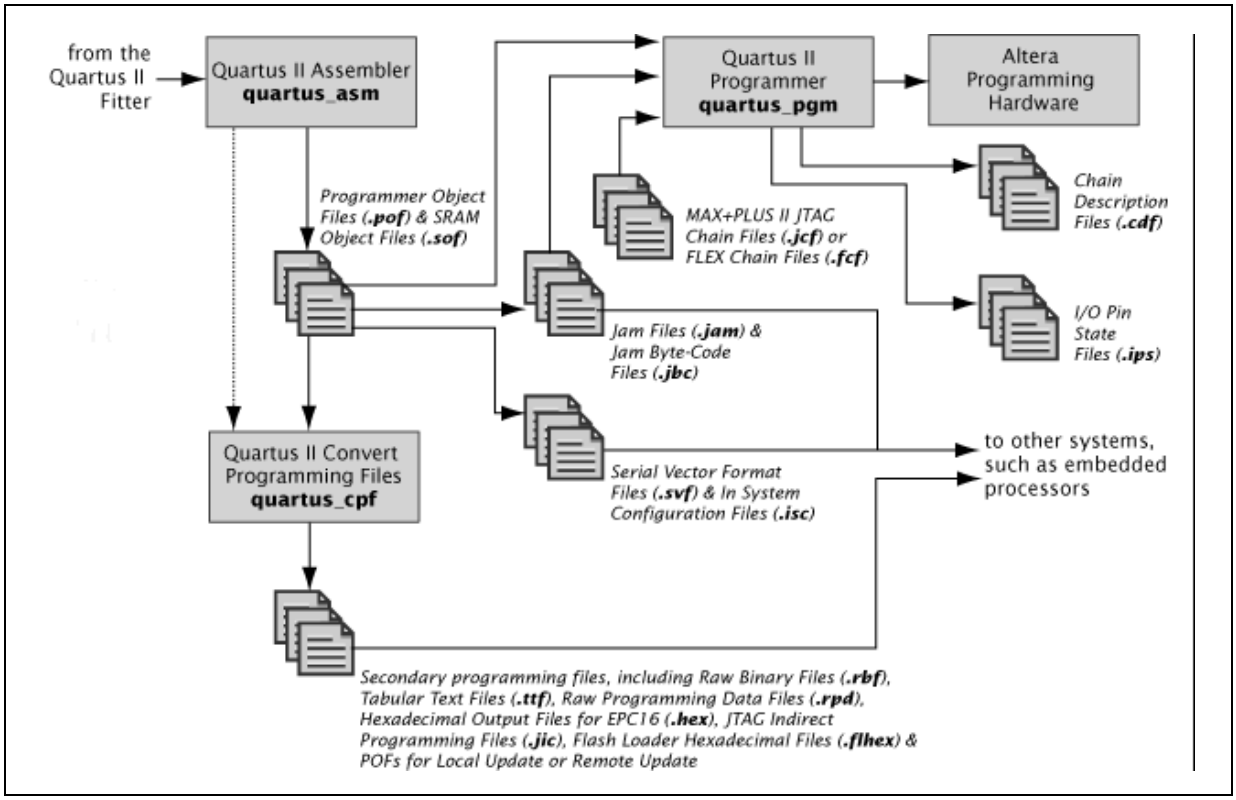
The BIOS and FPGA image is merged into one file using Intel developed software tools and saved to the SPI Flash device using FTDI. The Intel configuration tools package is document #447774 “E6x5c Series Tools Package”.

The Quartus Programmer allows programming or configuring all Altera devices supported by the Quartus II software with files generated by the Compiler. The Assembler module of the Quartus II Compiler generates programming files that the

Programmer can use to program or configure a device with Altera programming hardware. A stand-alone version of the Programmer can be used to program and configure devices.

During compilation, the Compiler automatically generates an SRAM Object File (.sof) SRAM Object Files can be used to configure EP2AGXE6XXFPGA devices. Other programming files can be generated with the Device and Pin Options dialog box.

Figure 65. FPGA Programming Image Files



The Programmer has four programming modes:

- In Passive Serial programming mode, you can select which SRAM Object Files (.sof) to include in the device chain. You can program an SRAM device with Raw Binary File (.rbf) data via the Passive Serial configuration scheme. You cannot add Programmer Object Files to Chain Description Files (.cdf), or select Programmer Object Files to replace programming files in a Chain Description File, when using Passive Serial programming mode.
- In JTAG programming mode, you can add specific devices to the device chain; add a Jam File (.jam) or Jam Byte Code File (.jbc) to the File list; add SRAM Object Files or Programmer Object Files to the Files list; and select between several programming options for each device and programming file in the chain. This mode also allows you to program a parallel configuration device with Programmer Object File (.pof) data via the Parallel Flash Loader and the JTAG interface. Additionally, you can choose to display the checksum without usercode in JTAG programming mode or to initiate configuration of attached devices after programming a configuration device by changing Programmer options. In JTAG programming mode, you can define or edit user-defined devices and add them to the device chain. You can also import or export user-defined devices. You can only program PFLs in JTAG programming mode.

- In Active Serial programming mode, you can program a single serial configuration device with a Programmer Object File for supported device families. All the programming options available for devices in JTAG programming mode, except Security Bit, are also available when using Active Serial Programming mode. The Active Serial programming mode allows you to program a single serial configuration device using the download cable
- In In-Socket programming mode, you can program a single configuration device with a Programmer Object File, Jam File, or Jam Byte Code File. The programming options available for devices in JTAG programming mode are also available when using In-Socket programming mode. Additionally, you can choose to display the checksum without usercode in In-Socket programming mode or to initiate configuration of attached devices after programming a configuration device by changing Programmer options. In addition, you can turn on the Erase option if you wish to erase the contents of CPLD devices. The In-Socket programming mode allows you to program a single device with a Chain Description File and the Altera Programming Unit (APU). You can also add remote JTAG servers so that you can use programming hardware that is not available on your computer, and configure local JTAG server settings so remote users can connect to your local JTAG server.

Both Passive Serial and JTAG programming modes allow programming single or multiple devices with a Chain Description File and the download cable. The download cable options can be modified by changing the hardware setup for each Chain Description File that is opened in Passive Serial or JTAG mode in the Programmer.

Once the system setup is complete, the FPGA device in the Intel® Atom™ Processor E6x5C Series appears in the selection as an EP2AGXE6XXFPGA device. If more than one device appears, delete the device and re-setup.

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13.0 Platform PCIe Implementation Requirements

The Intel® Atom™ Processor E6x5C Series MCP device comprises of two internal PCIe x1 lanes between the FPGA and the CPU. In order to ensure this internal interface operates correctly there are some mandadory requirements on the platform design and mandatory requirements on the FPGA implementation.

The first sub-section discusses the requirements of the Stellarton platform.

13.1 Power Delivery Requirements

Intel strongly recommends that all power pins are connected to their correct voltage levels irrespective of the underlying functionality being utilised in the FPGA.

Arria_VCCE (VCCL_GXB)

These pins supply power to the Transceiver Transmit & Receive PMA blocks. These pins must be connected to a 1.1V linear regulator or switching power supply. This plane should be isolated from all other power supplies.

Arria_VccEHT (VCCH_GXB)

These pins provide power to the analog Transmit buffers. These pins must be connected to a 1.5V supply with a maximum voltage ripple of _+/- 5mV. This voltage can be sourced from the same regulator as the Arria _VccR (VCCB) voltage with a proper isolation filter.

Place one high frequency decoupling cap (X7R 0402) for each pin directly under the pin on the secondary side of the PCB.

Arria_VccEH (VccA)

These pins supply power to the Transceiver PMA regulator. They must be connected to a 2.5V linear regulator or switching power supply with a maximum ripple voltage of +/- 5mV. These pins may share the same regulator as VCCA_PLL with a proper isolation filter.

Place one high frequency decoupling cap (X7R 0402) on each of the two pins directly under the pin on the secondary side of the PCB.

13.2 Clocking Implementation for PCIe

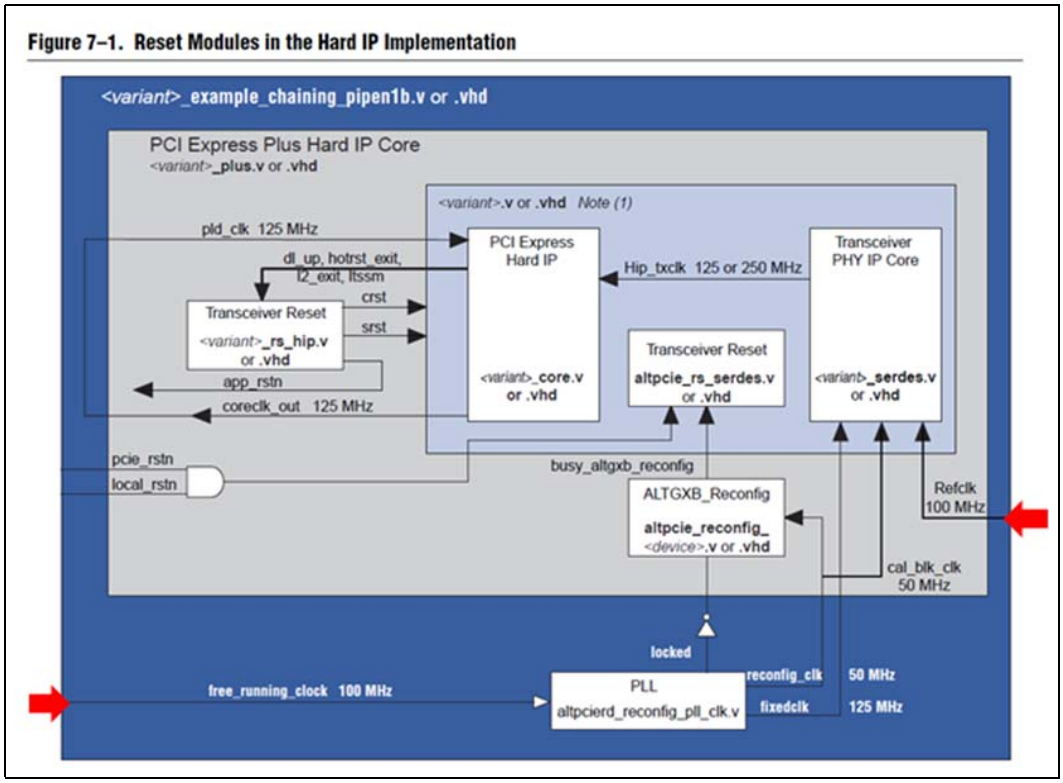
The following clocks are required to support the PCIe endpoint functionality in the FPGA. Each shall be discussed in more detail in the following sections.

- 100MHz refclk
- Fixed clock
- Calibration clock (or reconfig clock)

These clocks will be required irrespective of a soft IP or Hard IP PCIe implementation as they are required for the Transceiver block. The following diagram indicates how these clocks relate to the PCIe implementation in the FPGA.

Users implementing third-party PCIe soft IP may require additional clocking schemes. This is beyond the scope of this document and users must be familar with the clocking requirements of the IP to ensure their platorm meets the requirements.

Figure 66. Reset Modules in the Hard IP Implementation



13.2.1 PCIe Refclk

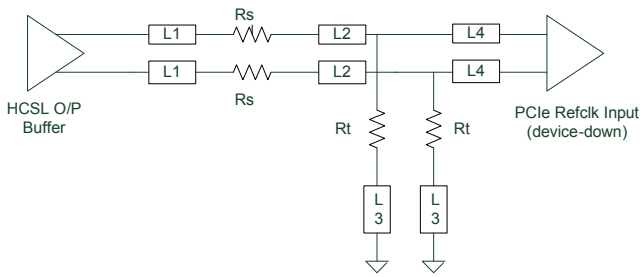
This is the PCIe reference clock used to clock the high-speed rx and tx signals of the PCIe lane.This is an external clock to the FPGA and it is used to drive the transceiver only. The clock frequency is 100MHz.

This differential clock must be input to the QL0_CMU0_REFCLK_REFCLK0QL0P/N pins of the E6x5c device. Since this clock is multiplied internally in the FPGA to generate the 2.5Gb/s data rate, care must be taken to ensure a quality clock at the FPGA inputs. This clock utilises a HCSL buffer in the FPGA implementation and must be externally terminated on the PCB.

Note: In version 10.1 of the QuartusII tools the HCSL buffer incorrectly defaults to being internally terminated. Users must manually disable the internal termination for sucessful operation.

The PCIe Refclk differential signals should be DC coupled and routed with a 100-ohm +/- 10% differential impedance. Observe all high speed differential routing recommendations when routing this clock to the FPGA input pins.

Figure 67. PCIe* Refclk to FPGA Input



PCIe Reference clock to E6x5C FPGA input			
Routing Recommendations	**Min Value**	**Max Value**	**Unit**
L1 length, routed as non-coupled 50-ohm trace		350	mils
L2 length, routed as non-coupled 50-ohm trace		200	mils
L3 length, routed as non-coupled 50-ohm trace		200	mils
L4 length, routed as 100-ohm coupled stripline	2	12	inches
Rs	33		ohms
Rt	49.9		ohms

Users must also consult the PCIe clock device/driver datasheet to ensure the termination scheme is compatibe with their output buffer characterestics.

13.2.2 Free_running_sys_clock

This clock may be used as the system clock for the FPGA logic. It must be input to one of the four internal PLLs. Its frequency must be such that it is possible to generate a 125 MHz Fixed clock and the calibration clock on the PLL outputs. This clock must not be derived from the PCIe REFCLK. A typical frequency for this clock is 125 MHz.

13.2.3 Fixed_CLK

This clock must be 125 MHz clock. This clock is generated internally in the FPGA from the Free running sys clock as shown in the diagram above.

13.2.4 PCIe Calibration CLK

There is a calibration block within the PCIe transceiver, which requires its own clock. This clock is also generated internally in the FPGA using the same PLL that generated Fixed clock. This clock can range in frequency between 10 MHz and 125 MHz and it must be free-running with respect to the PCIe Refclk. A typical frequency for this clock is 50 MHz.

13.3 PCIe Reset Signals

There is no mandatory requirement to provide an external reset signal to the FPGA. However the PLL locked signal should be used to gate the release of reset to the re-configuration block and the PCIe Hard-IP core. This ensures all clocks are stable prior to logic being released from reset.

The following are the Reset inputs generated by the Altera PCI Express compiler Mega-wizard.

Reset Input	Description	Comment
gxb_powerdown	Active high signal to Transceiver	Wire to the inverted PLL locked output
pll_powerdown	Active high signal to the internal RefCLK PLL in the PCIe core.	Wire to the inverted PLL locked output
pcie_rstn_pcie_compiler	Active low reset input.	wire to logic '1' or connect to active low reset signal.

13.4 FPGA Implementation Requirements

The PCIe lanes between the processor CPU and the FPGA are implemented on the Intel® Atom™ Processor E6x5C Series package. Intel have validated the link with the optimal FPGA Transceiver settings to ensure a robust link under all supported operating environments.

Intel® Atom™ Processor E6x5C Series users should ensure that the PCIe Transceivers are configured as shown in Table 67.

Table 67. PCIe Transceiver Configuration (Sheet 1 of 2)

Protocol:	PCIe Gen-1 x1
Number of Channels	1
Effective Data Rate:	2500Mbps
Inclk Frequency	100MHz
GXB Tx PLL BW mode:	High
Rx Vom	0.82V
Receiver DC Gain	1
Signal detect Treshold	4
External Receiver Termination	No
VCCHTX	Auto
Tx Vcm	0.65V
External Transmitter Termination	No
Vod Control Setting	4
Pre-emph pre-tap	0
Pre-emph first post-tap	0
Pre-emph second post-tap	0
Self Test Mode	None
Word Alignment	Sync State Machine
Word Alignment Width	10
Word Alignment pattern	17C
8b/10b mode	Normal

Table 67. PCIe Transceiver Configuration (Sheet 2 of 2)

Rate Match FIFO mode	Normal
Rate Match Pattern1	D0E83
Rate Match Pattern2	2F17C

Screen captures of the Mega-Wizard dialog boxes can be found in the package titled "478218 - PCI Express Transceiver Implementation Settings for Intel® Atom™ Processor E6x5C Series."

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14.0 FPGA Schematic Checklist

This sections provides recommendations on how the Intel® Atom™ Processor E6x5C Series FPGA pins should be connected for successful operation.

This section is divided into the following sub-sections

- FPGA Power-supply pins
- FPGA Configuration pins
- FPGA Transceiver pins
- User I/O

Due to the flexibility of the I/O and the various configuration options available the user must ensure the validity of the design.

There are many reports available for use after a successful Quartus compilation or I/O analysis. For example, you can use the "All Package Pins" and "I/O Bank Usage" reports within the Compilation – Fitter – Resource Section to see all of the I/O standards and I/O configurable options that are assigned to all of the pins in your design, as well as view the required VCCIO for each I/O bank. These reports must match your schematic pin connections.

14.1 E6x5C FPGA Power Supply Connections

Intel recommend that all Power supply pins on the FPGA are connected to valid voltages irrespective of whether the particular function within the FPGA is being utilised. (e.g. If I/O bank 3A is not being used then Intel recommend that the user connect valid voltage levels to the VCCN3A pins.)

Intel recommend that all power on ground pins have a dedicated PCB Via to ensure optimum power delivery and return current paths. In HDI PCB stack-up structures ensure that all ground planes are adequately stitched together with burried Vias.

Table 68. E6x5C FPGA Power Supply (Sheet 1 of 3)

E6x5C Signal Name	Quartus Signal Name	Connection Guidelines
Arria_VCC	VCC	All Arria_VCC pins require a 0.9V supply. Place three 0.1UF 0402 X7R caps for every four Arria VCC pins directly under the BGA device. Place three 0.47uF 0402 caps under the BGA at the Arria VCC pins. Place three 0.1uF 0402 caps under the BGA at the Arria VCC pins. Place one 10uF 0603 cap for every two Arria VCC pins. Distribute on both sides of the PCB. Refer to the power delivery application note for recommended decoupling requirements. Decoupling for these pins depends on the design decoupling requirements of the specific board.
Arria_VCCR	VCCCB	Connect to a filtered 1.5V supply. These pins may be sourced from the same regulator as VCCH_GXB with a proper isolation filter. Ensure maximum voltage ripple on this filtered supply is within ±5mV. Place one 0.1uF 0402 X7R cap directly under each pin of the BGA device. Place one 10UF and one 2.2UF 0603 cap on this filtered supply.
Arria_VCCEHT 6-pins	VCCH_GXB	Connect these pins to the V1P5 supply. Place one 0.1uF 0402 X7R cap directly under each pin of the BGA device.
X_TC_L_VCCD[1:4]	VCCD_PLL_[1:4]	Connect these pins to a filtered 0.9V supply. With a proper isolation filter these pins may be sourced from the same regulator as Arria_VCC. These pins must be connected to 0.9V even if the PLL is not used. PLLs that are guaranteed not to be used in the implementation may be connected directly to the 0.9V VCC supply. Place one 0.1uF 0402 X7R cap directly under each pin of the BGA device. Place one 10UF 0603 cap on the filtered PLL supply.

Table 68. E6x5C FPGA Power Supply (Sheet 2 of 3)

ARRIA_VCCEH	VCCA	Supplies power to the transceiver PMA regulator. Connect VCCA to a 2.5V linear regulator or switching power supply with ±5mV maximum voltage ripple. These pins may be sourced from the same linear regulator as VCCA_PLL with a proper isolation filter. Decoupling depends on the design decoupling requirements of the specific board design.
ARRIA_VCCEHT	VCCH_GXB	Analog power, block level (PMA output)TX buffers. These pins may be sourced from the same regulator as VCCCB with a proper isolation filter. Connect these pins to the V1P5 supply. Place one 0.1uF 0402 X7R cap directly under each pin of the BGA device.
VCCL_GXB	VCCL_GXB	Analog power to the transceiver PMA TX, PMA RX and clocking. Connect VCCL_GXB to a 1.1V linear regulator or switching power supply. For better jitter performance at high data rates this plane should be isolated from all other power supplies. For the best jitter performance, provide each quad its own power source. Decoupling for these pins depends on the design decoupling requirements of the specific board design.
X_TC_L_VCCA[1:4]	VCCA_PLL_[1:4]	Connect these pins to a filtered 2.5V supply. Ensure a ±5mV maximum voltage ripple on the filtered supply. It is advised to keep this pin isolated from other VCC for better jitter performance. Connect these pins to 2.5V, even if the PLL is not used. PLLs that are guaranteed not to be used in the implementation may be connected directly to the 2.5V VCCA supply. Place one 0.1uF 0402 X7R cap directly under each pin of the BGA device. Place one 10UF and one 2.2uF 0603 cap on this filtered PLL supply.

Table 68. E6x5C FPGA Power Supply (Sheet 3 of 3)

Arria_VCCN[3:8][A]	VCCIO[3:8][A]	Connect these pin to 1.2V, 1.5V, 1.8V, 2.5V, 3.0V or 3.3V supplies, depending on the I/O standard implemented onthe specified bank. These pins may be tied to the same regulator as VCCPD, but only if each of these supplies require the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board.
Arria_VCCN[3:8][C]	VCCIO[3,8]C	Connect these pin to 1.5V, 1.8V, 2.5V, 3.0V or 3.3V supplies, depending on the I/O standard connected to the specified bank. When using configuration schemes that require external configuration devices, the voltage level of these pins must match that of the configuration device. These pins may be tied to the same regulator as VCCPD, but only if each of these supplies require the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board.
VCCPD[3:8][A,B], VCCPD[3,8]C	VCCPD[3:8][A,B], VCCPD[3,8]C	The VCCPD pins require 2.5V, 3.0V or 3.3V and must ramp-up from 0 V to 2.5V, 3.0V or 3.3V within 100ms to ensure successful configuration. When these pins require 2.5V, 3.0V or 3.3V they may be tied to the same regulator as VCCIO, but only if each of these supplies require the same voltage level. VCCPD voltage connection depends on the VCCIO voltage of the bank. VCCPD is 3.3V for 3.3V VCCIO. VCCPD is 3.0V for 3.0V VCCIO. VCCPD is 2.5V for 2.5V/1.8-V/1.5V/1.2V VCCIO. Decoupling for these pins depends on the design decoupling requirements of the specific board.
X_LC_T_VCCBAT	VCCBAT	Connect this pin to a Non-volatile battery power source in the range of 1.2V - 3.3V when using design security volatile key. 3.0V is the typical power selected for this supply. When not using the volatile key tie this pin to a 3.0V supply or GND. Do not share this source with other FPGA power supplies.
VREF[3:8]A	VREF[3:8][A]	Input reference voltage for each I/O bank. If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. These pins cannot be used as regular I/Os. Decoupling depends on the design decoupling requirements of the specific board.
GND	GND	All ground pins must be connected to the board ground plane.

14.2 E6x5C FPGA Configuration pins

The E6x5C device supports all of the FPGA configuration options that are available on standard ArriaII GX devices from Altera. For details on the various configuration options available please refer to the ***Configuration, Design Security, and Remote system upgrades in Arria II GX devices*** chapter in the Arria II GX devices handbook that can be downloaded from Altera website.

Table 69. E6x5C FPGA Configuration Pins (Sheet 1 of 3)

E6x5C Signal Name	Quartus Signal Name	Connection Guidelines
3C_Config_nIOPULLUP	nIO_PULLUP	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual purpose I/O pins (nCSO, ASDO, DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5V, 1.8V, 2.5V,or 3.0V) turns off the weak pull-up, while a logic low turns them on. The nIO-PULLUP can be tied directly to VCCIO_3C, use a 1-kΩ pull-up resistor or tied directly to GND depending on the use desired for the device.
3C_Config_MSEL[0:3]	MSEL[0:3]	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPD3C or GND either directly or through 0-Ω resistors. Refer to the ***Configuration, Design Security, and Remote System Upgrades*** chapter in the Arria II GX Handbook.
3C_Config_nCE	nCE	This pin should be connected directly to GND assuming multi FPGA configuration is not being implemented.
3C_Config_nCONFIG	nCONFIG	If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCIO3C.
3C_Config_CONF_DONE	CONF_DONE	Connect this pin to a 10-kΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin.
3A_BIO1_LVDS_RD_B2P	nCEO	This pin is required for multi-device configuration. This pin can be used as a regular IO on E6x5C. When not using this pin as regular IO, you can leave it unconnected.

Table 69. E6x5C FPGA Configuration Pins (Sheet 2 of 3)

3C_Config_nSTATUS	nSTATUS	Connect this pin to a 10-kΩ pull-up resistor to an acceptable voltage which satisfies the input voltage of the receiving device. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up should not be used on these pins. When not using external configuration devices, connect this pin to an external 10-kΩ pull-up resistor to VCCIO3C.
8C_Config_TCK	TCK	JTAG Clock input. Connect this pin to a 1-kΩ pull-down resistor to GND. Treat this signal like a clock and follow typical JTAG clock routing guidelines.
8C_Config_TMS	TMS	JTAG TMS Connect this pin through a pull up resistor with a value between 1-kΩ and 10-kΩ to VCCPD8C. 1-kΩ pull-up to VCCPD8C is required if the JTAG circuitry is not being utilized.
8C_Config_TDI	TDI	Connect this pin through a pull up resistor with a value between 1-kΩ and 10-kΩ to VCCPD8C. A 1-kΩ pull-up to VCCPD8C is required if the JTAG circuitry is not being utilized.
8C_Config_TDO	TDO	JTAG TDO TDO can be left unconnected if JTAG circuitry is not being utilized.
Optional Dual Purpose Configuration Pins		
8C_Config_nCSO	nCSO	This pin is used for programming the device in Active Serial (AS) mode. Otherwise it is not used and it is recommended to leave the pin unconnected.
8C_Config_ASDO	ASDO	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
8C_Config_DCLK	DCLK	Dedicated configuration clock pin. In Passive Serial (PS) and FPP configuration, DCLK is an input used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface. Do not leave this pin floating. Drive this pin either high or low.
8A_TIO1_LVDS_RD_T28P	CRC_ERROR	This pin is used as a regular IO on E6x5C. When not using this pin, it can be left floating.

Table 69. E6x5C FPGA Configuration Pins (Sheet 3 of 3)

6A_RIO8_LVDS_TX_R32P	DEV_CLRn	This pin is used as a regular IO on E6x5C. This pin is optional and allows you to override all clears on all device registers. When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. **???**
6A_RIO8_LVDS_RD_R31P	DEV_OE	This pin is used as a regular IO on E6x5C. This pin is optional and allows you to override all tri-states on the device. When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
8C_Config_DATA0	DATA0	Data0 of the parallel configuration bus. When the dedicated input for DATA[0] is not used then it is recommended to tie this pin to GND.
DATA[1:7]	DATA[1:7]	Data[1:7] of the parallel configuration bus. If parallel configuration is not implemented these pins can be used as regular IO. When the dedicated inputs for DATA[1:7] are not used and these pins are not used as an I/O then connect them as defined in Quartus II software.
3A_BIO1_LVDS_RD_B1P	INIT_DONE	This pin is used as a regular IO on E6x5C. When using this pin as INIT_DONE connect it to an external 10-kΩ pull-up resistor to an acceptable voltage which satisfies the input voltage of the receiving device. When not using this pin, it can be left floating or tied to GND.
6A_RIO8_LVDS_RD_R30P	CLKUSR	This pin is used as a regular IO on E6x5C. If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground.
	JTAG Header	Connect pin 4 of the USB-Blaster cable to the VCCIO supply of I/O bank 8C of the device. The ByteBlaster II and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the ByteBlaster II Download Cable User Guide and the USB-Blaster Download Cable User Guide.

14.3 E6x5C FPGA Transceiver

Table 70. E6x5C FPGA Transceiver Pins (Sheet 1 of 2)

E6x5C Signal Name	Quartus Signal Name	Connection Guidelines
QL0_CMU0_REFCLK_REFCLK0QL0P QL0_CMU0_REFCLK_REFCLK0QL0N	REFCLK0_P REFCLK0_N	These pins provide the reference clock for the PCIe interface between the Arria FPGA and the Atom CPU. Connect this pin to a 100MHz differential reference clock. These pins should be DC-coupled and utilize an HCSL buffer in the FPGA implementation. The clock must be terminated internally. (HSCL – High speed Current steering Logic) Use best practices for Layout routing of this clock signal to ensure minimum signal integrity distortion and minimum clock Jitter at the clock input buffer. This clock should NOT be the source of the system reference clock within the FPGA implementation.
QL0_CMU0_REFCLK_REFCLK1QL0P/N QL1_CMU1_REFCLK_REFCLK0QL1P/N QL1_CMU1_REFCLK_REFCLK1QL1P/N	REFCLK[1:3]p/n	High speed differential reference clock. These pins should be AC-coupled when used as reference clocks for all applications, except for PCIe HCSL clocks. Connect all unused REFCLK[1..3]p/n pins either individually to GND through a 10k-Ω resistor or tie all unused pins together through a single 10k-Ω resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible.

Table 70. E6x5C FPGA Transceiver Pins (Sheet 2 of 2)

QL20_AUX1_RREFQL20	RREF[0]	Reference resistor for transceiver. This pin must be connected to its own individual 2.00k-Ω +/- 1% resistor to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
QL0_CH_RX[2:3]p/n QL0_CH_RX[4:7]p/n	GXB_RX[2..7]p/n	Transceiver High speed differential receiver channels. These pins may be AC-coupled or DC-coupled when used. Connect all unused GXB_RXp pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible.
QL0_CH_TX[2:3]p/n QL0_CH_TX[4:7]p/n	GXB_TX[2..7]p/n	Transceiver High speed differential transmitter channels. Leave all unused GXB_TX_[L,R]p/n pins floating.

14.4 E6x5C FPGA User I/O

The LVDS bank utilization limits the percentage of pins used based on the current setting and I/O standard. For the best jitter performance, adhere to the following guidelines:

- 100% of the pins in the bank can be used when using 2.5V LVTTL 4 mA, 50 Ω or 25 Ω, SSTL2.5V ClassI 8 mA and 12 mA
- 90% of the pins in the bank can be used when using 2.5V LVTTL 8 mA
- 60% of the pins in the bank can be used when using 2.5V LVTTL 12 mA
- 50% of the pins in the bank can be used when using 2.5V LVTTL 16 mA
- 60% of the pins in the bank can be used when using SSTL2.5V ClassII 16 mA

Table 71. FPGA User I/O (Sheet 1 of 2)

E6x5C Signal Name	Quartus Signal Name	Connection Guidelines
General for unused FPGA I/O		On unused I/O pins ensure there are no conflicts between the Quartus II software device wide default configuration for unused I/Os and the board level connection. It is recommended to set unused I/O pins on a project wide basis to behave as inputs tri-state with weak pull up resistor enabled. Individual unused pins can be reserved with specific behavior such as output driving ground or as output driving VCC to comply with the PCB level connection.
3A_CLKIN_LVDSCLK_p/n 4A_CLKIN_LVDSCLK_p/n 5A_CLKIN_LVDSCLK_p/n 6A_CLKIN_LVDSCLK_p/n 7A_CLKIN_LVDSCLK_p/n 8A_CLKIN_LVDSCLK_p/n	CLK[4:15]	Single ended clock input pin or clock input pin pair for differential clock input. When not used for clock inputs, these pins can be used as data inputs. Use these dedicated clock pins to drive clocks into the device. These pins can connect to the device PLLs. Output operation is not supported. OCT Rd is not supported. Programmable weak pull up resistor / bus hold is not supported. Connect unused pins to GND.
8A_TIO_PLL2_L_PLL1_CLKOUT_1N 8A_TIO_PLL2_L_PLL1_CLKOUT_1P 7A_TIO_PLL2_R_PLL2_CLKOUT_1N 7A_TIO_PLL2_R_PLL2_CLKOUT_1P 4A_BIO_PLL2_R_PLL3_CLKOUT_1N 4A_BIO_PLL2_R_PLL3_CLKOUT_1P 3A_BIO_PLL2_L_PLL4_CLKOUT_1N 3A_BIO_PLL2_L_PLL4_CLKOUT_1P	PLL1_CLKOUT1n PLL1_CLKOUT1p PLL2_CLKOUT1n PLL2_CLKOUT1p PLL3_CLKOUT1n PLL3_CLKOUT1p PLL4_CLKOUT1n PLL4_CLKOUT1p	When not using this pin as a clock output, this pin may be used as a user I/O. Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
3A_BIO_PLL2_L_RUP0 7A_TIO_PLL2_R_RUP1 8A_TIO_PLL2_L_RUP2	RUP0 RUP1 RUP2	Reference pins for I/O banks. When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to the VCCIO of the bank in which the RUP pin resides or GND. When using OCT Rs tie these pins to the VCCIO of the required bank(s) through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard. The pull up voltage must match the VCCIO of the bank which the RUP pin is located.

Table 71. FPGA User I/O (Sheet 2 of 2)

3A_BIO_PLL2_L_RDN0 7A_TIO_PLL2_R_RDN1 8A_TIO_PLL2_L_RDN2	RDN0 RDN1 RDN2	Reference pins for I/O banks. When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT Rs tie these pins to GND through either a 25-Ω or 50-Ω resistor, depending on the desired I/O standard.
LVDS_RX_[T,B,R] [##]p, LVDS_RX_[T,B,R] [##]n T => Top B => Bottom R => Right Note This references locations on the die, rather than the E6x5C package.	DIFFIO_RX_[T,B,R] [##]p, DIFFIO_RX_[T,B,R] [##]n	These are true LVDS receiver channels with OCT Rd support. Pins with a "p" suffix carry the positive signal, pins with an "n' suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as single ended user I/O pins. Note there is no 'Hard' Serdes available to the Top/Bottom LVDS pins.
LVDS_TX_[T,B,R] [##]p, LVDS_TX_[T,B,R] [##]n	DIFFIO_TX_[T,B,R] [##]p, DIFFIO_TX_[T,B,R] [##]n	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as single ended user I/O pins. Note there is no 'Hard' Serdes available to the Top/Bottom LVDS pins.

14.5 External Memory Interfaces

If implementing external memory interfaces on the E6x5C FPGA I/O please refer to the Altera literature relating to external memory interfaces for Altera II GX devices and the specific schematic checklists.

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