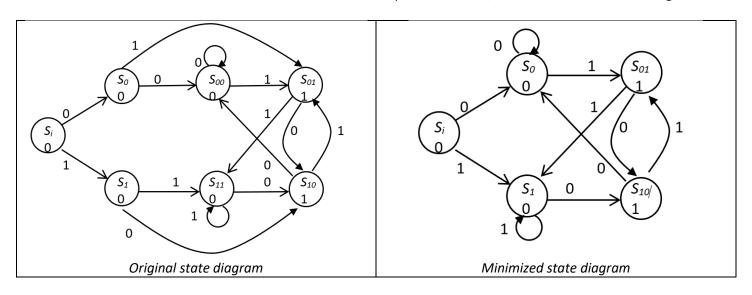
1. From the last lecture

- a. Was working on the Moore model edge detector FSM
- b. Used Partition Minimization Procedure to minimize the original state diagram
 - i. $P_3 = (S_i)(S_1, S_{11})(S_0, S_{00})(S_{01})(S_{10})$
- c. Now use this to create minimized state diagram
 - i. K-successors are the same for the multiple-state blocks, use that to combine them together



2. Implementing the minimized FSM

a. From our minimized, equivalent FSM we get the following state table

Present State	Next	Output		
Present State	<i>x</i> = 0	x = 1	Z	
i	0	1	0	
0	00	01	0	
1	10	11	0	
00	00	01	0	
01	10	01	1	
10	00	01	1	
11	10	11	0	

Original	state	table

Present State	Next	State	Output
rieseiil State	<i>x</i> = 0	x = 1	Z
i	0	1	0
0	0	01	0
1	10	1	0
01	10	1	1
10	0	01	1

Minimized state table

- b. Next, assign binary codes
 - i. Will need 3 flip flops to represent 5 states, call these A, B, and C

Present State	Binary	Pres	ent S	tate	Input	Ne	xt St	Output	
Present State	Code	Α	В	С	X	A'	B'	C'	z
i	000	0	0	0	0	0	0	1	0
i	000	0	0	0	0 1		1	0	0
0	001	0	0 1 0		0	0	1	0	
0	001	0	0	1	1	0	1	1	0
1	010	0	1	0	0	1	0	0	0
1	010	0	1	0	1	0	1	0	0
01	011	0	1	1	0	1	0	0	1
01	011	0	1	1	1	0	1	0	1
10	100	1	0	0	0	0	0	1	1
10	100	1	0	0	1	0	1	1	1

- c. Create K-maps for each flip flop based on input and present state
 - i. States that weren't assigned form don't cares

A'		AB					B'	' AB						C'	AB					
		00	01	11	10				00	01	11	10				00	01	11	10	
	00	0	1	d	0			00	0	0	d	0			00	1)	0	d		
Сх	01	0	0	d	0			01	1	1	d	1		Сх	01	0	0	d	1	
CA	11	0	0	d	d		Сх	11	1	1	d	d		C 2.	11	1	0	d	d	
	10	0	1	d	d			10	0	0	d	d			10	7	0	d		
	$A' = B\bar{x}$ $B' = x$									С	'= A ·	$+\overline{Bx}$	$+ \overline{B}$	Ċ						

- d. Use derivations from these K-maps to design initial combinational circuit
- e. Create a K-Map based on flip-flops to determine the output combinational circuit
 - i. Assign don't cares for the same reason as above

