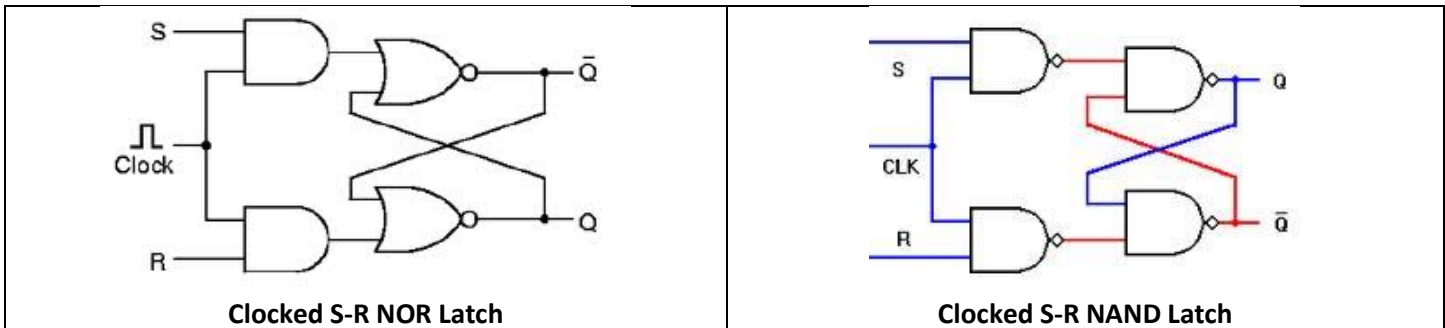
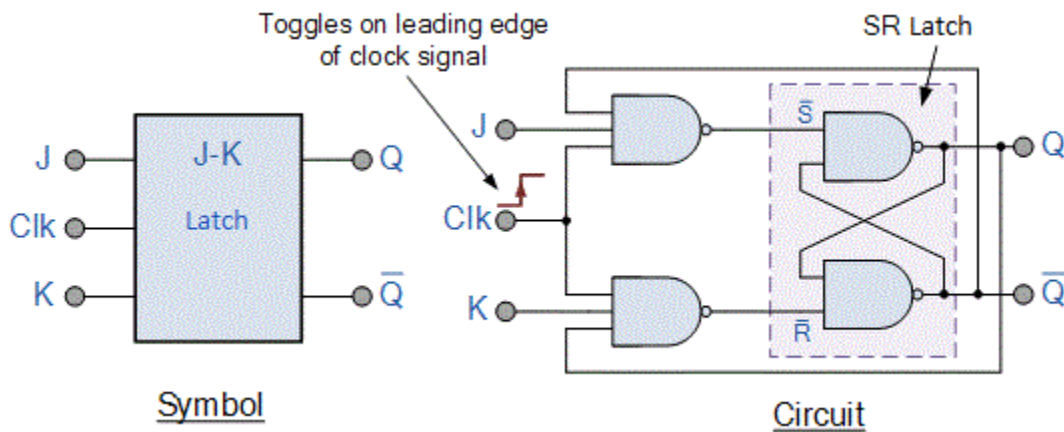


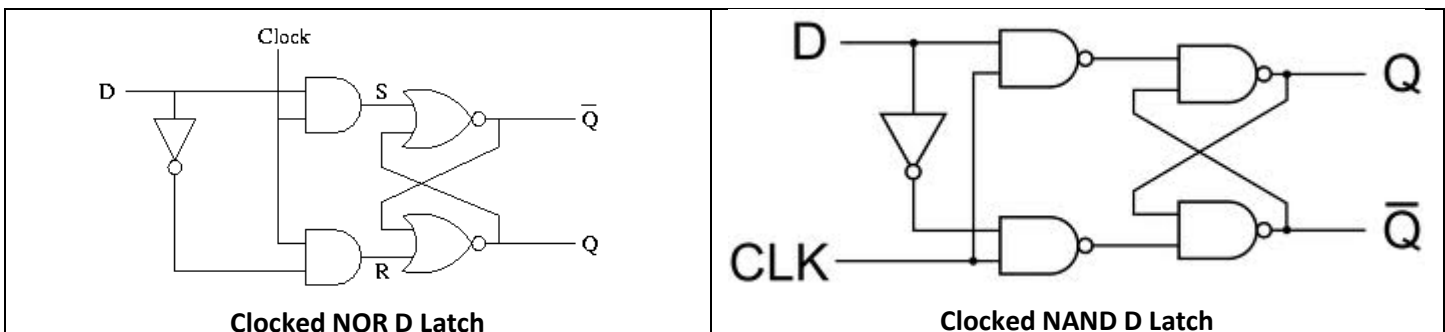
1. More on latches
 - a. Clocking the latches
 - i. Prevent the latch from changing, except at specific times as determined by the clock



2. Clocked J-K latch
 - a. Like a S-R latch, except that passing in $(S, R) = (1, 1)$ toggles/inverts Q instead of leading to undefined behavior
 - b. Uses feedback from outputs to do so



3. Clocked D latch
 - a. Only takes one input, ensures that inputs that cause unpredictable states don't occur
 - b. Output of latch is equal to the most recent value applied to the input
 - i. When clock is 1, sample the current value of D
 - ii. Store that value in the latch
 - iii. Can retrieve the value at output Q



4. Flip-flops

a. Circuit terminology

- i. Level sensitive – output controlled by the level of the clock input
- ii. Edge triggered – output changes only when the clock changes from one value to the other
 1. Positive / rising edge – when clock “rises” from 0 to 1
 2. Negative / falling edge – when clock “falls” from 1 to 0

b. Back to flip-flops

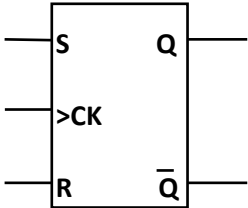
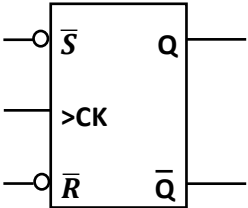
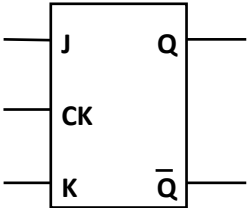
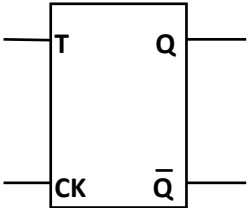
- i. Clocked (gated) latches are level sensitive
- ii. Unlike latches, flip flops are edge-triggered
- iii. Named so because they flip and flop from one stable state (0) to another (1)

c. Advantages

- i. Signal on input pin captured as soon as the clock changes
- ii. Subsequent changes of the input are ignored until clock changes again
- iii. Better timing control on complex circuits

d. Types of flip flops

<p>Positive D Latch</p> <p>Can change when the clock is high.</p>	<p>Negative D Latch</p> <p>Can change when the clock is low.</p>	<p>Rising Edge D Flip-Flop</p> <p>Can change when clock goes from 0 to 1.</p>	<p>Falling Edge D Flip-Flop</p> <p>Can change when clock goes from 1 to 0.</p>
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 <p>S-R Flip-Flop (NOR)</p> <table><tr><th>S</th><th>R</th><th>$Q(t + 1)$</th></tr><tr><td>0</td><td>0</td><td>$Q(t)$</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>Undefined</td></tr></table>	S	R	$Q(t + 1)$	0	0	$Q(t)$	0	1	0	1	0	1	1	1	Undefined	 <p>S-R Flip-Flop (NAND)</p> <table><tr><th>S</th><th>R</th><th>$Q(t + 1)$</th></tr><tr><td>0</td><td>0</td><td>Undefined</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>$Q(t)$</td></tr></table>	S	R	$Q(t + 1)$	0	0	Undefined	0	1	1	1	0	0	1	1	$Q(t)$	 <p>J-K Flip-Flop</p> <table><tr><th>J</th><th>K</th><th>$Q(t + 1)$</th></tr><tr><td>0</td><td>0</td><td>$Q(t)$</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>$\bar{Q}(t)$</td></tr></table>	J	K	$Q(t + 1)$	0	0	$Q(t)$	0	1	0	1	0	1	1	1	$\bar{Q}(t)$	 <p>T Flip-Flop</p> <table><tr><th>T</th><th>$Q(t + 1)$</th></tr><tr><td>0</td><td>$Q(t)$</td></tr><tr><td>1</td><td>$\bar{Q}(t)$</td></tr></table>	T	$Q(t + 1)$	0	$Q(t)$	1	$\bar{Q}(t)$
S	R	$Q(t + 1)$																																																				
0	0	$Q(t)$																																																				
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1	0	1																																																				
1	1	Undefined																																																				
S	R	$Q(t + 1)$																																																				
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1	1	$\bar{Q}(t)$																																																				
T	$Q(t + 1)$																																																					
0	$Q(t)$																																																					
1	$\bar{Q}(t)$																																																					

e. Named flip flops work similarly to their latch counterparts

- i. One new addition – T flip flop
- ii. When T is high, on next clock the output is “toggled” and is inverted
- iii. Same as (1, 1) input on J-K flip flop and latch

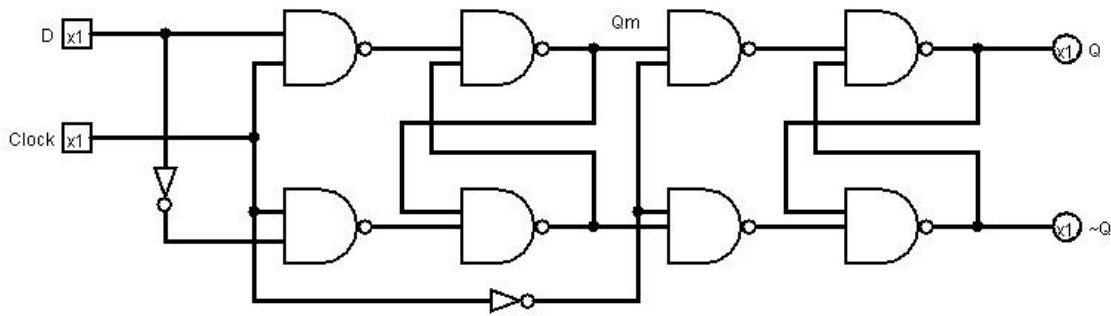
5. Flip flop timing

- a. Setup time t_{su} – minimum time before clock arrives that inputs must be stable and unchanging to ensure first latch in flip flop is stable

- b. Hold time t_h – minimum time after clock arrives that inputs must remain stable and unchanging to ensure first latch clock NAND is off
 - i. Not important for this course, but exists

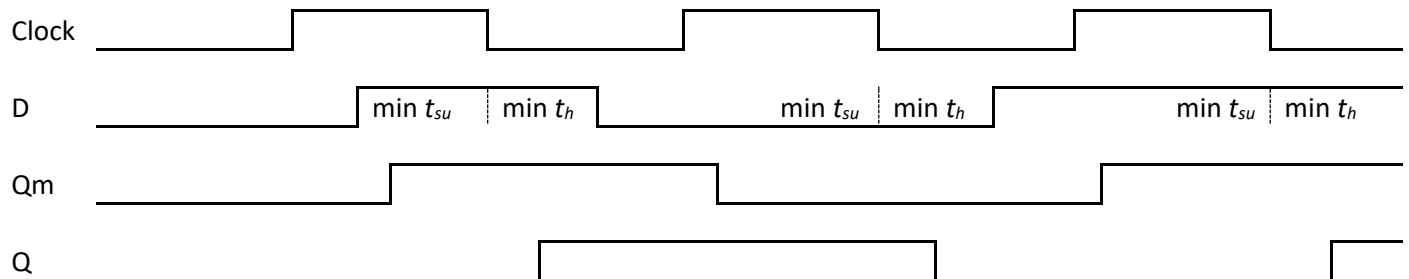
6. Falling-edge Triggered Master-Slave D flip-flop

- a. Master latch in front controls slave latch's output in back
- b. Q_m is the output of the master latch



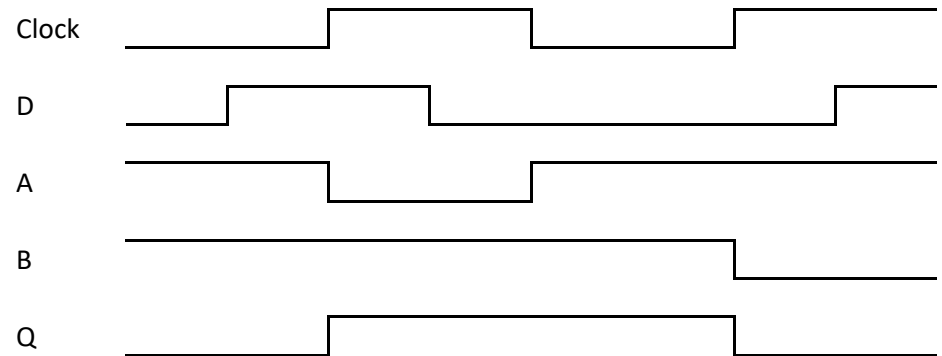
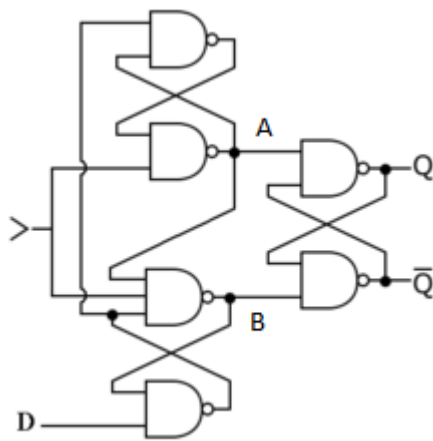
c. Timing diagram

- i. Remember that this flip flop is falling edge triggered
- ii. In general, will stick to rising edge
- iii. Input needs to stay constant before the falling edge for time t_{su}
- iv. Input needs to stay constant after the falling edge for time t_h



7. Rising-edge triggered D flip-flop

- a. Here, t_h and t_{su} not specified explicitly but you can still see the impact on signal D



- b. The second stage can be thought of as an S-R latch made of NANDs