C-V profiling of Schottky diode and other semiconductor devices using LabVIEW

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This study explores capacitance-voltage (C-V) profiling of a Schottky diode using a cost-effective approach. A low-cost op-amp circuit and LabVIEW-based instrumentation replace traditional lock-in amplifiers and phase shifter circuits. The investigation aims to determine impurity dopant density and the built-in electric potential of the semiconductor layer. Results demonstrate consistency with anticipated values, endorsing the efficiency of the cost-effective methodology. The methodology is extended to C-V profiling of other devices, including an LED and a MOSFET, yielding results in accordance with theoretical expectations. This study suggests the viability of the proposed method for accurate and economical semiconductor device characterization.

I. THEORY

A. Schottky Diode

Schottky diodes (shown in Figure 2) are semiconductor devices with distinct electrical properties due to the metal-semiconductor junction they form. Schottky diodes differ from ordinary p-n junction diodes by having a metal-semiconductor junction. These diodes have a lower forward voltage drop and faster switching speed than p-n junction diodes, making them suitable for rectification, power supply protection, and high-frequency circuits.

To establish a rectifying contact, allowing current flow in one direction, it is essential for the metal's work function (W_m) to exceed that of the semiconductor (W_s). Upon contact, to maintain a constant Fermi level (E_F), electrons migrate from the semiconductor's conduction band to the metal, inducing band structure deformation. This deformation persists until the semiconductor's chemical potential aligns with the metal's Fermi level. As electrons move from the semiconductor to the metal, a slight negative charge accumulates on the metal, hindering further electron flow. The modified band structure, characterized by an upward bending of the bands (see Figure 2), creates a potential barrier near the contact area, resulting in the formation of a depleted region within the semiconductor. This depleted region lacks charge carriers, and the metal's contribution to it is minimal due to the surplus of electrons present in the metal.

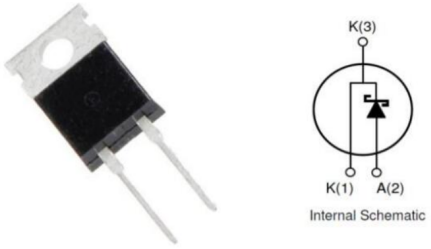

FIG. 1: Schottky diode [1]

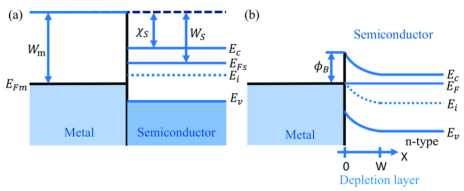

FIG. 2: Before and after contact the metal semiconductor contact is made in Schottky diode [2]

1. *Reverse-biased Schottky Barrier*

In the reverse bias scenario, the metal is connected to the negative terminal, while the semiconductor is connected to the positive terminal of the battery. Electrons within the semiconductor migrate towards the positive battery terminal, resulting in an increase in both the height and width of the potential barrier in the depletion region, while maintaining Φ_B constant. The application of reverse bias reduces the significance of diffusion current due to the substantial potential barrier, giving prominence to a minor drift current. The region between the two extremes of the depletion region acts as a capacitor, devoid of free charge carriers, with the boundaries carrying opposite charges.

The Schottky diode can be envisioned as a parallel arrangement of a capacitor (C) and a resistor (R_L, representing leakage) along with a resistor (R_S, resembling the neutral bulk region beyond the depletion layer) connected in series to them. In the case of high-quality diodes, characterized by significant doping density, the impedance generated by R_L and C is sufficiently large in comparison to the impedance produced by the series resistor RS. Consequently, $R_S \approx 0$ and can be disregarded.

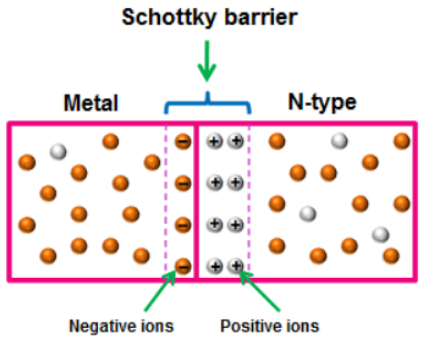

FIG. 3: Reverse biased Schottky diode [3]

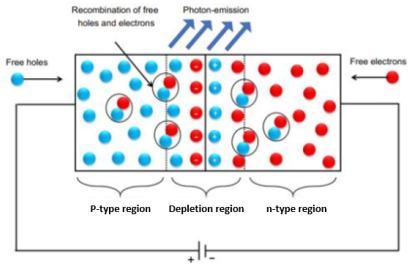

FIG. 4: Schematic showing recombination of electrons and holes in LEDs [4]

B. Light Emitting Diode(LED)

Light Emitting Diodes (LEDs) operate as p-n junction diodes, converting electrical energy into light energy. Electrons within the semiconductor recombine with holes, releasing energy in the form of photons through radiative emission. LEDs have become the preferred choice over incandescent lamps and CFL tubes in lighting applications due to their energy efficiency and longer lifespan. In contemporary applications, Organic LEDs (OLEDs) are designed using organic electroluminescent materials, serving various purposes such as displays in TVs, laptops, mobile phones, and other electronic devices.

Despite the generally favorable characteristics of LEDs, drawbacks include restrictions on electrical input to low voltage, typically limited to DC (not AC) power. LEDs face challenges in delivering consistent illumination from a pulsating DC or AC electrical supply source. Additionally, they exhibit lower maximum operating and storage temperatures.

C. Mosfet

Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are widely used in electrical circuits as switches or amplifiers. In this work, we investigated an N-channeled 2N7000 MOSFET with three pins: source, gate, and drain. The gate voltage controls the current

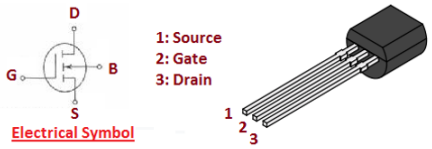

FIG. 5: N-channel Enhancement MOSFET 2N7000 [5]

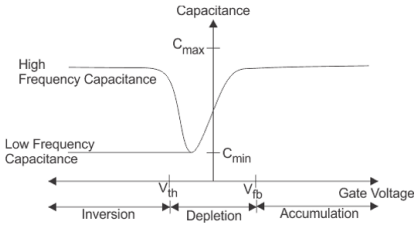

FIG. 6: Three modes of MOSFETs

flow between the source and the drain. To establish the Capacitance-Voltage (C-V) profile, we supplied an AC voltage to the gate terminal and measured the capacitance between it and the source or drain terminals.

The MOSFET operates in three fundamental modes: accumulation, depletion, and inversion. These modes characterize the behavior of charge carriers within the semiconductor material of the transistor.

- **Accumulation:** When we put a voltage on the metal gate, electrons from the semiconductor gather near the metal-semiconductor interface, forming a layer that improves the flow of electricity between the source and drain.
- **Depletion:** Without any voltage or with a small positive voltage on the gate, a region near the surface of the semiconductor gets depleted of charge carriers, making it less conductive.
- **Inversion:** Applying a strong positive voltage to the gate attracts electrons from the semiconductor to the surface, forming a conductive channel between the source and drain. This process, called "inversion," changes the semiconductor's type from p-type to n-type.

D. Capacitance of the Schottkey Diode

To analyze the capacitance-voltage profile, we apply a reverse DC bias to the diode along with a small AC signal. This setup allows the AC signal to pass through, as a capacitor offers infinite resistance to a DC signal. If the angular frequency of the AC signal in the circuit is denoted as ω, the resulting output current is expressed as:

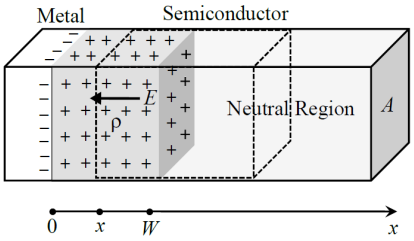

FIG. 7: Depletion region of a Schottky diode along with a chosen rectangular Gaussian surface [6]

$$I = \frac{V_{ac}}{Z} = V_{ac}\left(\frac{1}{R_L} + i\omega C\right) \tag{1}$$

So, we get two components of the output current, I_x being proportional to $1/R_L$ which is in-phase with the input signal to the diode, and I_y is proportional to ωC which is 90° out-of-phase with respect to the input signal. Corresponding voltages, V_x is called the in-phase component, and V_y is called the quadrature component of the output voltage.

We take a capacitor of known capacitance (C_0) as a reference. By measuring the corresponding voltage (V_0) of this capacitor, we can determine the capacitance of the diode by using the expression:

$$C = C_0\frac{V}{V_0} \tag{2}$$

Accounting for the small phase shifts from the amplifiers and cables, the above equation gets modified as:

$$C_{diode} = \frac{(V_x V_{x_0} + V_y V_{y_0})}{(V_{x_0}^2 + V_{y_0}^2)} C_{ref} \tag{3}$$

E. Capacitance-Voltage Profiling Of Schottky Diode

Consider a Schottky barrier with a cross-sectional area A and an x-axis, aligned along the length of the diode, where the origin is the metal-semiconductor interface (see Fig. 9). Assuming that positively charged dopant atoms are incorporated into the semiconductor lattice in a position-dependent manner, the doping density $\rho(x)$ becomes a function of the distance from the metal-semiconductor interface.

If an external reverse bias voltage $-V_R$ is applied, then the total potential at the barrier will be:

$$V_0 = -(V_R + V_{bi})$$

and the total charge stored in the metal surface will be $-Q$ (since reverse bias). Let the width of the depletion region be W , beyond which the semiconductor is neutral.

Taking a rectangular Gaussian surface as shown in Figure 8 and using Gauss' law:

$$\epsilon EA = \frac{e\rho(x)A(W-x)}{\epsilon_0} \tag{4}$$

For electric potential $V(x)$, we get two boundary conditions:

$$V(0) = -(V_R + V_{bi}), \qquad V(W) = 0$$

Thus, from $V(W) - V(0) = -\int_W^0 E\dot{d}x$, we get:

$$V_R + V_{bi} = \frac{e}{\epsilon\epsilon_0}\int_w^0 x\rho(x)dx \tag{5}$$

If the bias voltage is increased by a small amount dV_R, the depletion width increases by dW along with creating extra space charge of $dQ = e\rho(W)AdW$, where $\rho(W)$ is the doping density at the edge of the depletion region. So,

$$dV_R = \frac{e}{\epsilon\epsilon_0}W\rho(W)dW \tag{6}$$

Thus, the capacitive response is given by:

$$C \equiv \frac{dQ}{dV_R} = \frac{e\rho(W)AdW}{\frac{e}{\epsilon\epsilon_0}W\rho(W)dW} = \frac{\epsilon\epsilon_0 A}{W} \tag{7}$$

If we plot C vs V, we can see that the capacitance is inversely proportional to the square root of the applied V_R. So, plotting $1/C^2$ vs V should be linear in nature. So:

$$\frac{d}{dV_R}\left(\frac{1}{C^2}\right) = \frac{1}{(\epsilon\epsilon_0 A)^2}2W\frac{dW}{dV_R} \tag{8}$$

$$\frac{d}{dV_R}\left(\frac{1}{C^2}\right) = \frac{2}{(\epsilon\epsilon_0 A)^2\rho(W)} \tag{9}$$

This is the Profiler's equation, used to characterize the spacial distance of dopants in the semiconductor.

For a constant doping density ($\rho(x) = \rho$), the width of the depletion region W, corresponding to V_R, is given by $W = \epsilon\epsilon_0 A/C$ and the doping density as W is

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m} \tag{10}$$

where m is the slope of the linear plot of $1/C^2$ vs V. Let b be the y-intercept of the plot, then the build-in potential can be calculated as:

$$V_{bi} = \frac{b}{m} \tag{11}$$

II. LOCK-IN AMPLIFIER

A Lock-in Amplifier is a tool designed for measuring AC signals accompanied by noise. It finds applications in engineering, particularly when the signal of interest is weak, comparable to the accompanying noise that needs extraction. This amplifier works by multiplying the input signal, denoted as ω_s, with a reference signal of frequency ω_r.

$$V_S = V_{0_s} \sin \omega_s t \tag{12}$$
$$V_S = V_{0_r} \sin \omega_r t \tag{13}$$

If $V_{0_r} = 2$ (amplitude of the reference signal), then the product of the two becomes

$$2V_{0_s} \sin \omega_s t \sin \omega_r t = V_{0_s}[\cos(\omega_s t - \omega_r t) - \cos(\omega_s t + \omega_r t)] \tag{14}$$

As a result, the product involves two frequencies: one is the sum, and the other is the difference of ω_s and ω_r. When $\omega_s = \omega_r$, the difference-frequency sinusoid becomes a DC voltage with amplitude V_0. Utilizing a low-pass filter allows us to obtain the final DC value. Consequently, this approach enables the determination of the amplitude of the sinusoidal component within the experimental waveform, where its frequency matches that of the reference, effectively filtering out higher frequency noise.

III. LAB-VIEW PROGRAM

In lieu of a commercial Lock-in amplifier, our approach utilizes a LabVIEW code for DC signal amplitude extraction. The code encompasses reference signal generation, phase-sensitive detection (PSD), and low-pass filtering. The MFR-2230M function generator, controlled by a LabVIEW driver, varies the DC offset voltage incrementally. Software triggering generates the reference signal, synchronized with the output signal from the function generator. This signal triggers the DAQ device for measurements.

To calculate capacitance, both in-phase and quadrature components of potential are required. Two reference signals with a 90° phase difference feed into separate PSDs, followed by low-pass filters. The Fast Fourier Transform is employed for low-pass filtering, extracting the DC component's amplitude. The LabVIEW code records voltage values corresponding to reverse bias voltage in an Excel sheet.

IV. PROCEDURE

We varied the reverse bias of the device from $0\,V$ to $4\,V$ in increments of $0.05\,V$. The AC signal's amplitude remained at $30\,mV$, and its frequency was set to $1\,kHz$. We sampled data at a rate of $32,000\,samples/sec$, collecting a total of $16,384$ samples.

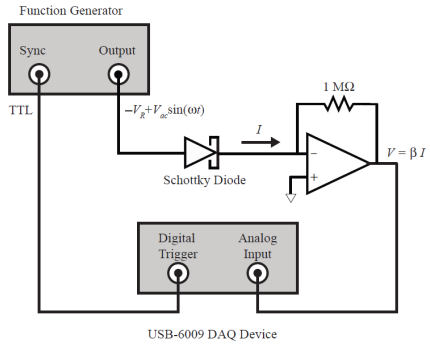

FIG. 8: Circuit diagram for low-cost implementation of capacitance profiling using USB-60009 DAQ device

To use the auto-phasing technique, we initially recorded in-phase and quadrature voltage values after replacing the device with a calibration capacitor having $C_0 = 1\,nF$. These values were then plugged into Eq 3 to find the device's capacitance, and a graph of C versus V was created.

Subsequently, we plotted $1/C^2$ against V_R. The resulting straight line suggests that the diode's doping density remains constant over the spatial profile. Using Eq 10 and Eq 11 we calculated the doping density and the diode's built-in potential.

V. APPARATUS

- **Semiconductor Device (DUT):** These are the devices under test, and their C-V properties will be evaluated. Our primary DUT is the Schottky diode (STPS 20120D), which has a metal-semiconductor junction that forms a depletion area that functions as a capacitor. Similarly, we can determine the C-V profile of other semiconductor devices with a depletion area, such as LEDs and MOSFETs.

- **Function Generator:** We use the GW Instek MFG-2000 Series Multi-Channel Function Generator to produce the bias voltage. This is important because we need a DC bias voltage with a low amplitude AC voltage to measure capacitance without changing the DC bias.

- **Preamplifier Circuit:** We use an OpAmp LF411, a $1M\Omega$ feedback resistor, and wires on a breadboard to create a cost-effective preamplifier circuit.

- **Data Acquisition Device (DAQ):** We use the NI USB-6003 DAQ, an affordable data collection device, to collect data from the preamplifier circuit. The function generator uses hardware to trigger the DAQ.

FIG. 9: NI USB-6003 DAQ [7]

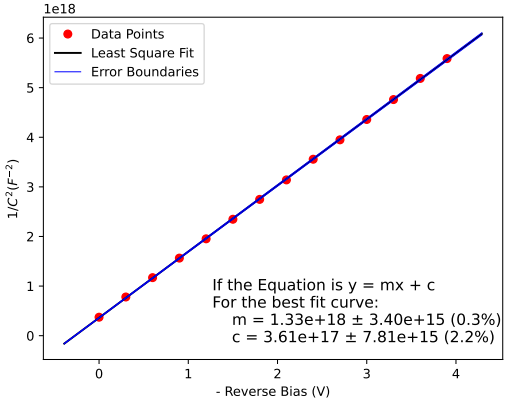

FIG. 10: Schottky diode graph (500 Hz)

- **PC with LabVIEW Software:** Our LabVIEW code handles all data gathering and processing, including the automation of the function generator, production of hardware-triggered reference signals, phase-sensitive detection, low-pass filtering, and data recording.

- **Reference Capacitor:** A $1nF$ capacitor acts as a reference. The in-phase and quadrature voltages of this capacitor are required to calculate and determine the capacitance of the device under test (DUT).

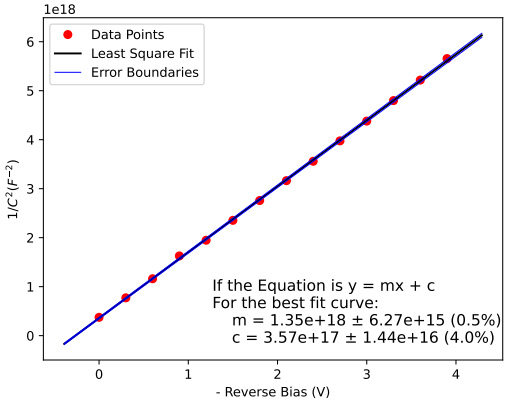

FIG. 11: Schottky diode graph (750 Hz)

VI. OBSERVATIONS, CALCULATIONS AND ERROR ANALYSIS

Here I have used python to automatically load data from the CSV file, do calculations, plot graph and generate required latex code. The data can be found here: `https://github.com/PeithonKing/OpenLabUpdates/tree/main/cv_profiling/data/`. Moreover, the code used to do all these can be found here: `https://github.com/PeithonKing/OpenLabUpdates/blob/main/cv_profiling/a.ipynb`.

If you visit the URL provided above, you would get the data for LED too. We had done that experiment also, but the data didn't come good, so we discarded the experiment altogether.

Reference Capacitor $(C_0) = 1.67nF$

A. For Schottky Diode

Dielectric constant for silicon $(\epsilon) = 11.7$

Area of cross-section $(A) = 5.38 \times 10^{-6} m^2$

1. 500Hz

In Figure 10, the slope (m) $= 1.33 \times 10^{18} \pm 3.40 \times 10^{15} (0.3\%)$ and the intercept, (c) $= 3.61 \times 10^{17} \pm 7.81 \times 10^{15} (2.2\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

$$V_{bi} = \frac{1.33 \times 10^{18} \pm 3.40 \times 10^{15}}{3.61 \times 10^{17} \pm 7.81 \times 10^{15}} = 0.27 \pm 0.01V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m}$$
$$= 3.13 \times 10^{21} \pm 7.98 \times 10^{18} Dopants/m^3$$

2. 750Hz

In Figure 11, the slope (m) $= 1.35 \times 10^{18} \pm 6.27 \times 10^{15} (0.5\%)$ and the intercept, (c) $= 3.57 \times 10^{17} \pm 1.44 \times 10^{16} (4.0\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

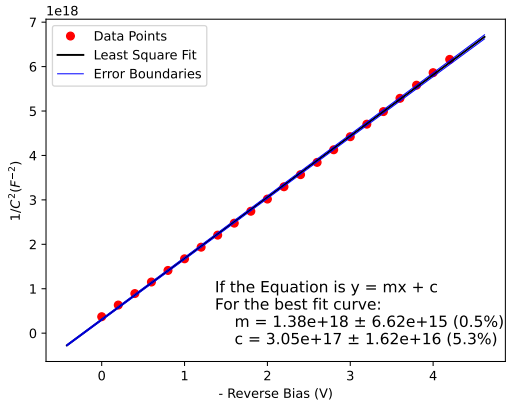

FIG. 12: Schottky diode graph (1000 Hz)

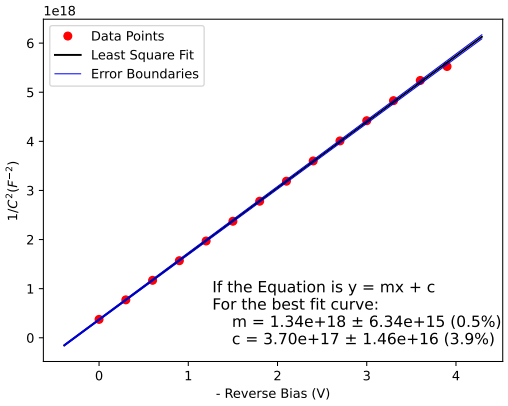

FIG. 13: Schottky diode graph (1250 Hz)

$$V_{bi} = \frac{1.35 \times 10^{18} \pm 6.27 \times 10^{15}}{3.57 \times 10^{17} \pm 1.44 \times 10^{16}} = 0.27 \pm 0.01V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m}$$
$$= 3.10 \times 10^{21} \pm 1.44 \times 10^{19} Dopants/m^3$$

3. 1000Hz

In Figure 12, the slope (m) $= 1.38 \times 10^{18} \pm 6.62 \times 10^{15}(0.5\%)$ and the intercept, (c) $= 3.05 \times 10^{17} \pm 1.62 \times 10^{16}(5.3\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

$$V_{bi} = \frac{1.38 \times 10^{18} \pm 6.62 \times 10^{15}}{3.05 \times 10^{17} \pm 1.62 \times 10^{16}} = 0.22 \pm 0.01V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m}$$
$$= 3.03 \times 10^{21} \pm 1.45 \times 10^{19} Dopants/m^3$$

4. 1250Hz

In Figure 13, the slope (m) $= 1.34 \times 10^{18} \pm 6.34 \times 10^{15}(0.5\%)$ and the intercept, (c) $= 3.70 \times 10^{17} \pm 1.46 \times 10^{16}(3.9\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

$$V_{bi} = \frac{1.34 \times 10^{18} \pm 6.34 \times 10^{15}}{3.70 \times 10^{17} \pm 1.46 \times 10^{16}} = 0.28 \pm 0.01V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m}$$
$$= 3.11 \times 10^{21} \pm 1.47 \times 10^{19} Dopants/m^3$$

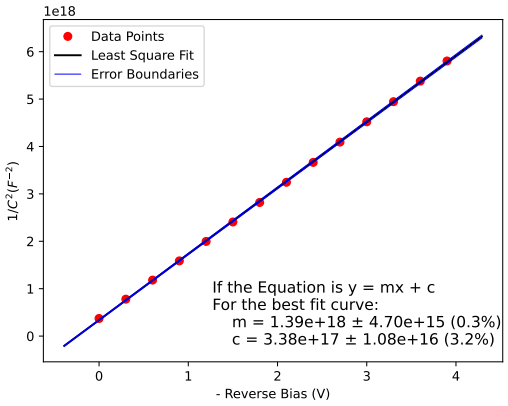

FIG. 14: Schottky diode graph (1500 Hz)

5. 1500Hz

In Figure 14, the slope (m) $= 1.39 \times 10^{18} \pm 4.70 \times 10^{15}(0.3\%)$ and the intercept, (c) $= 3.38 \times 10^{17} \pm 1.08 \times 10^{16}(3.2\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

$$V_{bi} = \frac{1.39 \times 10^{18} \pm 4.70 \times 10^{15}}{3.38 \times 10^{17} \pm 1.08 \times 10^{16}} = 0.24 \pm 0.01V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m}$$
$$= 2.99 \times 10^{21} \pm 1.01 \times 10^{19} Dopants/m^3$$

B. For Solar Panel

Dielectric constant for silicon $(\epsilon) = 11.7$
Area of cross-section $(A) = 3.7 \times 10^{-4} m^2$

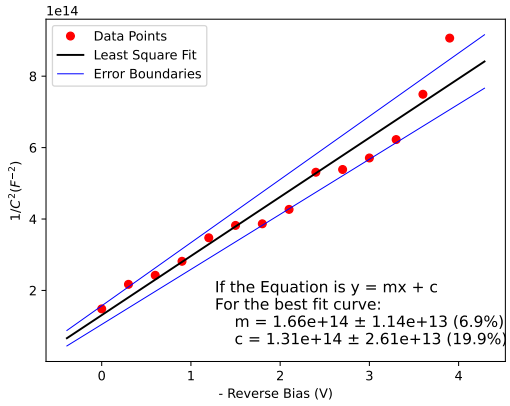

FIG. 15: Solar Panel graph (500 Hz)

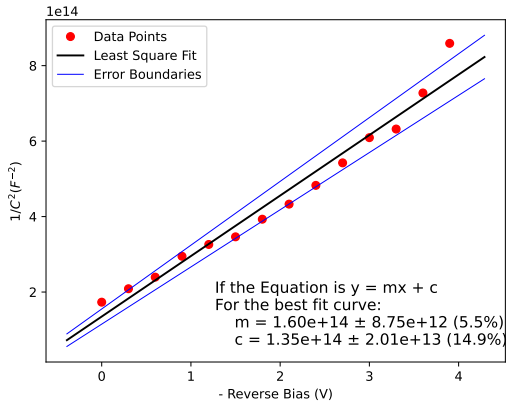

FIG. 16: Solar Panel graph (1000 Hz)

1. 500Hz

In Figure 15, the slope (m) $= 1.66 \times 10^{14} \pm 1.14 \times 10^{13}(6.9\%)$ and the intercept, (c) $= 1.31 \times 10^{14} \pm 2.61 \times 10^{13}(19.9\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

$$V_{bi} = \frac{1.66 \times 10^{14} \pm 1.14 \times 10^{13}}{1.31 \times 10^{14} \pm 2.61 \times 10^{13}} = 0.79 \pm 0.21V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m} = 5.33 \times 10^{21} \pm 3.65 \times 10^{20} Dopants/m^3$$

2. 1000Hz

In Figure 16, the slope (m) $= 1.60 \times 10^{14} \pm 8.75 \times 10^{12}(5.5\%)$ and the intercept, (c) $= 1.35 \times 10^{14} \pm 2.01 \times 10^{13}(14.9\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

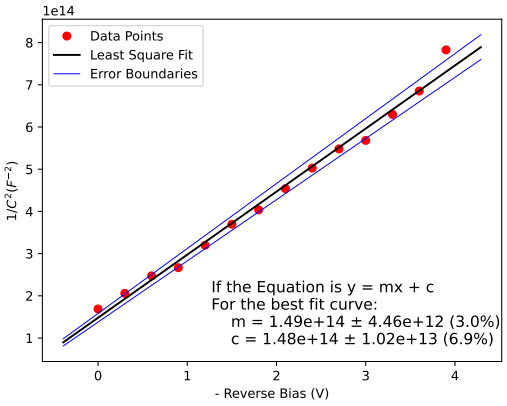

FIG. 17: Solar Panel graph (1500 Hz)

$$V_{bi} = \frac{1.60 \times 10^{14} \pm 8.75 \times 10^{12}}{1.35 \times 10^{14} \pm 2.01 \times 10^{13}} = 0.84 \pm 0.17V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m} = 5.50 \times 10^{21} \pm 3.00 \times 10^{20} Dopants/m^3$$

3. 1500Hz

In Figure 17, the slope (m) $= 1.49 \times 10^{14} \pm 4.46 \times 10^{12}(3.0\%)$ and the intercept, (c) $= 1.48 \times 10^{14} \pm 1.02 \times 10^{13}(6.9\%)$. Following Eq 11 and 10, the builtin voltage and doping density are:

$$V_{bi} = \frac{1.49 \times 10^{14} \pm 4.46 \times 10^{12}}{1.48 \times 10^{14} \pm 1.02 \times 10^{13}} = 0.99 \pm 0.10V$$

$$\rho = \frac{2}{e\epsilon\epsilon_0 A^2 m} = 5.90 \times 10^{21} \pm 1.76 \times 10^{20} Dopants/m^3$$

VII. CONCLUSION

In the experiment, we successfully got the C-V characteristics and the $1/C^2 - V$ plot for the Schottky diode and solar cell. The acquired values have narrow error margins, and the resultant plots closely match the theoretical expectations. This achievement demonstrates the usefulness of our low-cost system for C-V profiling in semiconductor devices.

The calculated doping densities (ρ) are as follows:

- Schottky diode: $3.07 \times 10^{21} \pm 1.23 \times 10^{19}$ $Dopants/m^3$

- Solar Panel: $5.58 \times 10^{21} \pm 2.81 \times 10^{20}$ $Dopants/m^3$

Similarly, the built-in potentials (V_{bi}) are determined to be:

- Schottky diode: 0.25 ± 0.01 V
- Solar Panel: 0.87 ± 0.16 V

The C-V plot exhibits variation proportional to the square root of the reverse bias voltage. The $1/C^2$ vs V_R linearly increases with an increasing reverse bias voltage, indicating that an increase in V_R leads to an increase in the width of the depletion region, resulting in decreased capacitance. While the plots for the Schottky diode closely resembled the expected pattern, a slight deviation was observed in the case of the Solar panel.

A. Sampling Rate of DAQ

The sampling rate must be set in accordance with the applied frequency of the AC signal. We observed that altering the frequency of the AC signal without adjusting the sampling rate results in fluctuating values of V_{rms}, particularly when the sampling rate is low, leading to a more noisy signal. For instance, when the AC frequency was 1kHz, we maintained the sampling rate at 32,000 samples/sec. However, when the AC frequency was changed to 2kHz, we had to adjust the sampling rate to 64,000 samples/sec to ensure accurate data acquisition.

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