ADC and DAC with Sample and Hold (ADC-DAC-2)

Aritra Mukhopadhyay
National Institute of Science Education and Research
Bhubaneswar, Odisha 751005, India
3rd year, Integrated M.Sc. Physics
Roll No.: 2011030
(Dated: March 14, 2023)

This experiment involved the construction and analysis of digital-to-analog converter (DAC) and analog-to-digital converter (ADC) circuits using integrated circuits. By sampling an input AC signal and passing it through a series of ADC and DAC, we were able to observe and verify that the output analog voltage is approximately equal to the input signal. We also studied the working and pin diagram of the ICs, and discussed the importance of sampling in these circuits. Overall, the experiment provided valuable insights into the operation and applications of DAC and ADC circuits.

I. THEORY

The Analog to Digital Converter (ADC) converts analog signals to digital signals while the Digital to Analog Converter (DAC) converts digital signals to analog signals. In this experiment, we will construct and study the working of an ADC and a DAC using dedicated Integrated Circuits (ICs) instead of using basic electronic components. This circuit diagram is shown in **Figure 1**.

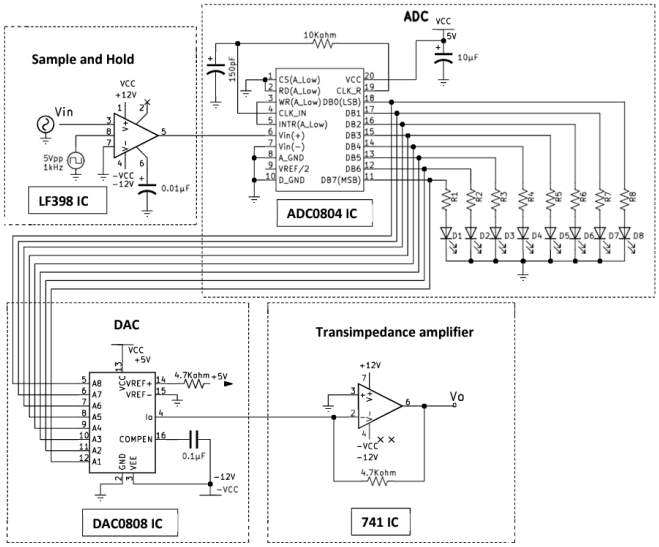


FIG. 1: Circuit for ADC-DAC with sample and Hold

Compared to the previous circuit, this circuit is much simpler and does not require a priority encoder, while also working with a larger number of bits. The circuit diagram for the experiment is shown below.

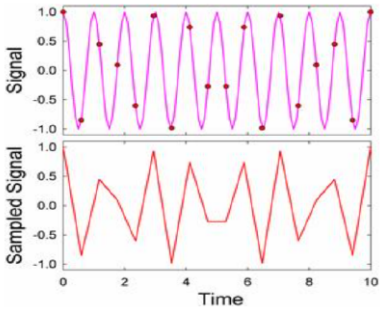


FIG. 2: Aliased Sampled output for sampling rate violating Nyquist theorem

A. Nyquist Frequency

The Nyquist frequency is the minimum sampling rate required for accurate representation of an analog signal in digital form. If the signal is sampled at a rate below the Nyquist frequency, the resulting digital signal will not accurately represent the original analog signal. The Nyquist frequency is defined as half the sampling rate.

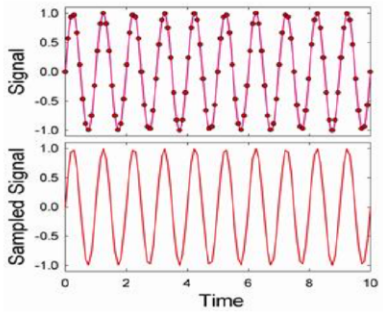


FIG. 3: Sampled output that is a good approximation of the input signal

As shown in **Figure 2**, violating Nyquist's theorem can

result in aliasing, which is when signals at higher frequencies get shifted down to lower frequencies. On the other hand, **Figure 3** demonstrates a good approximation of the input signal using a properly sampled output.

B. Sample and Hold Circuit

The sample and hold circuit is shown in Figure 1 and is constructed with the LF398 IC. The purpose of this circuit is to sample the input signal and hold it until it is converted to digital format. The sample and hold circuit discretizes a continuous input AC signal by capturing the signal at an instant of time and holding it via hold mode (using capacitors).

It requires an external clock signal for its operation which is supplied using a function generator. Approximation accuracy depends on the sampling rate and resolution. The sampling frequency (f_z) should be more than twice the maximum frequency present in the signal, also known as the Nyquist frequency. If we violate Nyquist's theorem we get aliasing; signals at higher frequencies get shifted down to lower frequencies as shown in Figure 2.

The output digital signal from the sample and hold circuit is fed to an 8-bit ADC IC, which then outputs a digital signal. This digital signal is then fed to an 8-bit DAC IC for digital to analog conversion. Sampling and holding is important for proper conversion of analog signals, which we encounter every day in the lab. All multichannel analyzers also use ADC.

C. Analog to Digital Converter (ADC)

The ADC circuit is constructed with an ADC0804 IC, which is an 8-bit successive approximation ADC converter. The circuit involves a sample and hold component for sampling the input AC signal and feeding it to the ADC IC. The sample and hold circuit is constructed using an LF398 IC, which discretizes a continuous input AC signal by capturing the signal at an instant of time and holding it via hold mode (using capacitors). The ADC IC also utilizes an internal clock to give clock pulse to the sample and hold circuit, but it is not used in this experiment due to noise in the clock pulse signal.

D. Digital to Analog Converter (DAC)

The DAC circuit is constructed using a DAC0808 IC, which is an 8-bit DAC chip with an R-2R ladder. For this experiment, we are using a dual in-line package. The output of this IC is given by the equation:

$$I_0 = K\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \frac{A_4}{2^4} + \dots\right) \tag{1}$$

where $K = \frac{V_{Ref}}{R}$, $K_{ref} = 5V$, and $R = 4.7k\Omega$.

E. Transimpedance Amplifier

A transimpedance amplifier is an electronic circuit that converts current to voltage. It is a current-to-voltage converter that is constructed using an operational amplifier such as the 741 IC. Compared to other methods of current-to-voltage conversion, the transimpedance amplifier has superior impedance characteristics due to its low input impedance and high output impedance. This results in a higher gain, making it a much better method of current-to-voltage conversion than using an ordinary resistor. The transimpedance amplifier is commonly used in a variety of applications, such as in photodiodes, where it converts the current generated by the diode to a voltage signal.

II. OBSERVATION, CALCULATION

Sl. No.	V_{in} (V)	Binary Output	Equivalent Voltage
1	0.1	00000101	0.10
2	0.5	00011001	0.49
3	1.0	00110011	1.00
4	1.5	01001100	1.49
5	2.0	01100110	2.00
6	2.5	01111111	2.49
7	3.0	10011001	3.00
8	3.5	10110010	3.49
9	4.0	11001100	4.00
10	4.5	11100101	4.49
11	5.0	11111111	5.00

TABLE I: ADC-DAC Observation

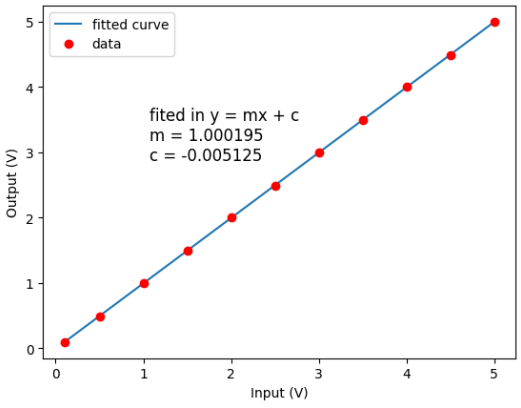
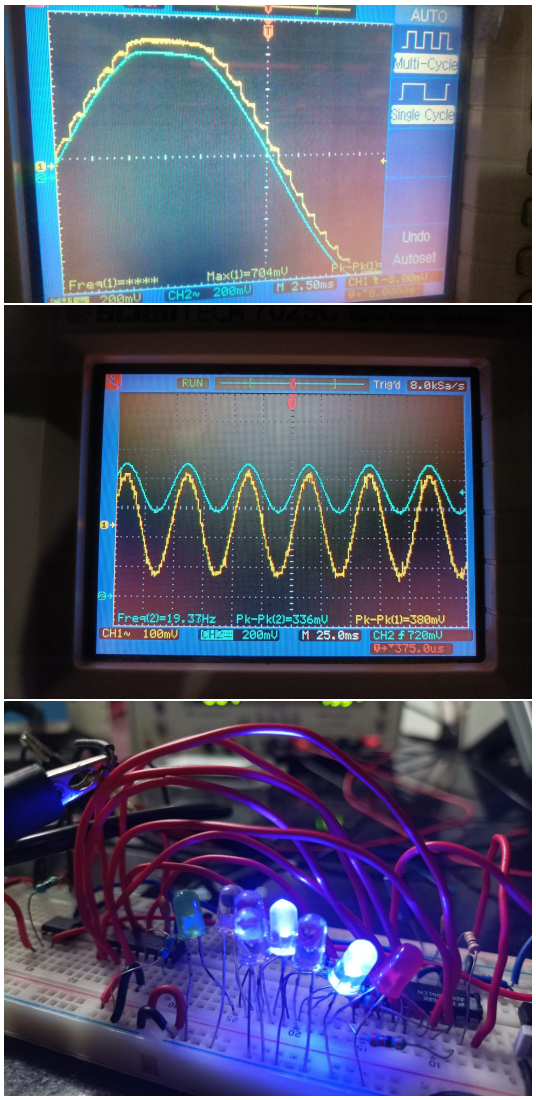


FIG. 4: ADC graph

We fit the input and the output using a straight line. Theoretically they should be equal, so the expected slope is 1. From the Figure 4 we can see that the slope is 1.000195, with a very minor offset along the y axis of -0.005125



III. ERROR

The expected slope is 1, but the slope of the graph is 1.000195. So the formula for error will be:

$$\Delta s = \frac{|observed - expected|}{expected} = \frac{|1.000195 - 1|}{1} = 0.000195$$

This comes out to be around 0.0195% error. This is a very small error, and can be attributed to the fact that the resistors used in the circuit are not very accurate. The error can be reduced by using more accurate resistors.

The sampling process was performed at various clock frequencies to determine the optimal frequency for sampling the signal. The oscilloscope was used to obtain readings for each frequency tested. The results were consistent with the Nyquist theorem: as the sampling frequency approaches the frequency of the input signal (100Hz), the resulting signal becomes more aliased.

A. Suspected Sources of Error

1. The circuit diagram must be followed correctly, and the junctions should be represented using bold points to make proper connections.

2. The connections between ADC and DAC on the circuit diagram are incorrect. The input pins of DAC should be flipped, i.e., output pin 18 of ADC should be connected to A1 of DAC, and pin 11 to A8.

3. All circuit components should be checked for defects before conducting the experiment.

4. Resistances should be added before each LED to prevent them from fusing.

5. The biasing voltage must not exceed 15V, and the input voltage for the digital signal must not exceed 5V.

IV. CONCLUSION

In this experiment, we studied the working of Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) using integrated circuits. By considering the different parameters that define the performance of a converter, we calculated the linearity error in the slope of the ADC and DAC plot between theoretical and experimental values. The low error confirms the validity of the experiment.

A. Sample and Hold Circuit Parameters

During the experiment, we also encountered certain terms related to the Sample and Hold circuit. The **Acquisition Time** (t_{ac}) is the time it takes for the charge in the holding capacitor to reach a level close to the input voltage. It depends on the RC time constant, OPAMP's slew rate, and output current. As the capacitance (C) increases, the acquisition time also increases.

The **Droop Rate** is the rate at which voltage droop develops when the leakage current drops the voltage across the holding capacitor. For higher capacitance, the leakage is smaller since the capacitor has more capacity to store charges, hence the droop rate decreases.

In conclusion, this experiment provided hands-on experience with ADC and DAC using ICs and helped in understanding the significance of the different parameters of Sample and Hold circuit.

[1] SPS, Lab manual, Website (2022), https://www.niser.ac.in/sps/sites/default/files/basic_page/p341_2023/Study_and_construction_of_ADC_and_DAC_circuit.pdf.