VLSI LAB REPORT

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EXPERIMENT-1

NMOS TRANSISTOR CHARACTERISTICS

Aim: Studying the characteristics of NMOS transistor and their dependencies on L, W and lmd.

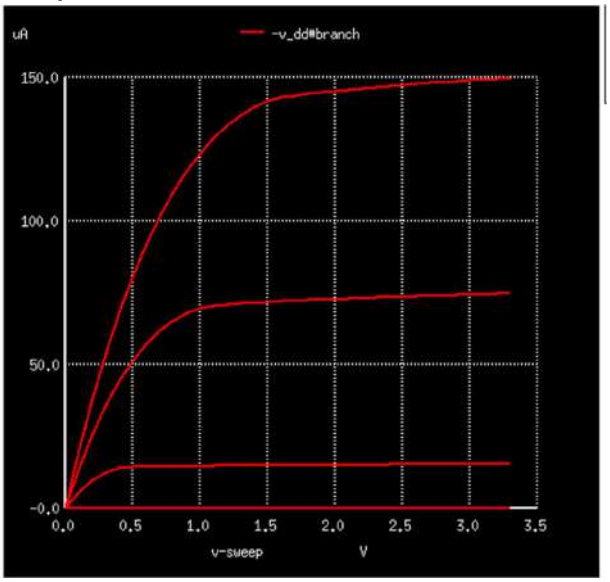
Procedure:

Finding IV characteristics for a given L,W:

Netlist:

```
* nmos characteristics
* include the model files
.include ./cmos_include.txt
m1 vdd in 0 0 cmosn l=1u w=0.5u
v_dd vdd 0 3.3
v_in in 0 3.3
.control
dc v_dd 0 3.3 0.1 v_in 0 3.3  1
run
setplot dc2
plot -v_dd#branch
.endc
.end
```

Graphs:



X-axis sweeps vdd from 0 to 3.3 with a step of 0.1 and Y-axis contains current through the transistor. 4different graphs for 4 different gate voltages.

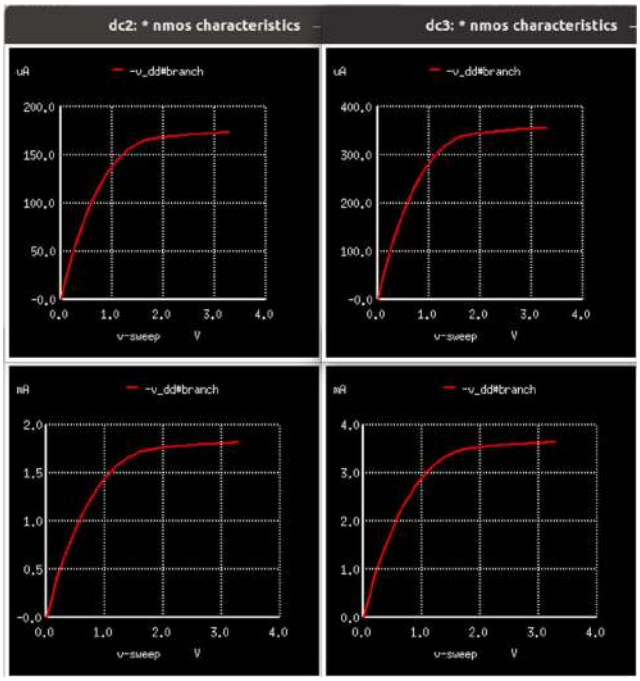
Observation: Current increases as gate voltage increases.

Varying width from 0.5u to 10u

Netlist:

```
      * nmos characteristics

* include the model files
.include ./cmos_include.txt
m1 vdd in 0 0 cmosn l=1u w=0.5u
v_dd vdd 0 3.3
v_in in 0 3.3
.control
    foreach wid in 0.5u 1u 5u 10u
        alter m1 w=$wid
        dc v_dd 0 3.3 0.1
    end
.endc
.control
    foreach it in 1 2 3 4
        setplot dc$it
        plot -v_dd#branch
    end
.endc

.end
```

Graphs:



X-axis represent VDS

Y-axis represents current through transistor.

(where VGS = 3.3V)

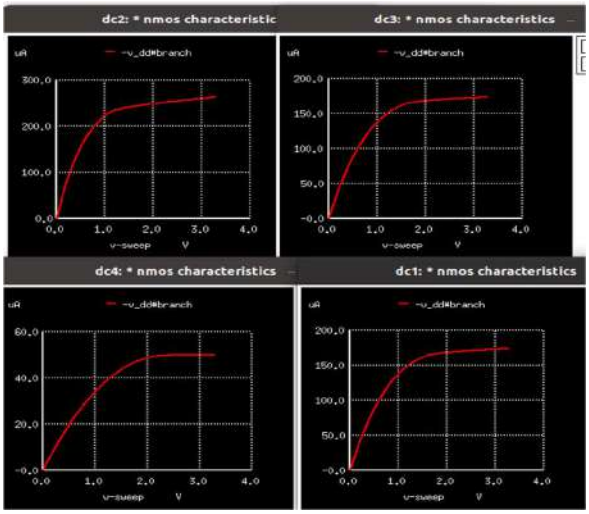
Observation: As the width of the transistor increases the current through the transistor also increases this shows that the resistance is inversely proportional to the width of the transistor.

Varying Length:

Netlist:

```
* nmos characteristics
* include the model files
.include ./cmos_include.txt
m1 vdd in 0 0 cmosn l=1u w=0.5u
v_dd vdd 0 3.3
v_in in 0 3.3
.control
    foreach wid in 0.5u 1u 5u 10u
        alter m1 l=$wid
        dc v_dd 0 3.3 0.1
    end
.endc
.control
    foreach it in 1 2 3 4
        setplot dc$it
        plot -v_dd#branch
    end
.endc

.end
```

Graph:



X-axis represent VDS

Y-axis represents current through transistor.

(where VGS = 3.3V)

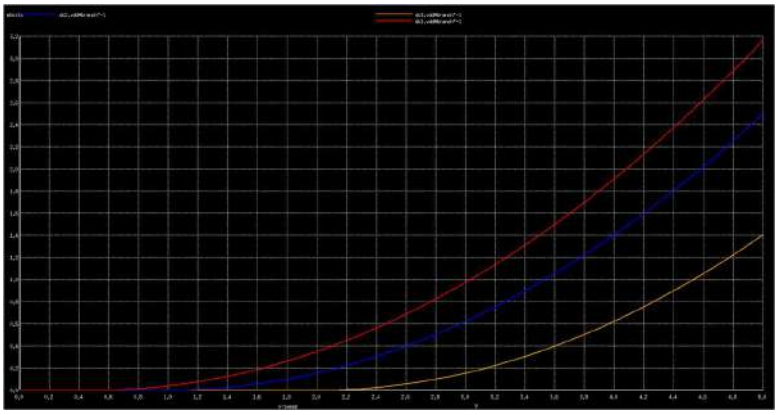
Observation: As the length of transistor increases from dc2 to dc5 the current through the transistor is reduced. So the resistance of transistor is inversely proportional to the length.

Varying VT of the transistor:

Spice Code:

```
.MODEL cmosn NMOS ( LEVEL = 1
+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.4317311
+ PHI = 0.7 VTO = 0.4238252 DELTA = 0
+ UO = 425.6466519 ETA = 0 THETA = 0.1754054
+ KP = 2.501048E-4 VMAX = 8.287851E4 KAPPA = 0.1686779
+ RSH = 4.062439E-3 NFS = 1E12 TPG = 1
+ XJ = 3E-7 LD = 3.162278E-11 WD = 1.232881E-8
+ CGDO = 6.2E-10 CGSO = 6.2E-10 CGBO = 1E-10
+ CJ = 1.81211E-3 PB = 0.5 MJ = 0.3282553
+ CJSW = 5.341337E-10 MJSW = 0.5
+ LAMBDA = 0.05 )
m drain in source 0 cmosn l=1u w=1u
Vss source 0 0
Vdd drain 0 5
Vin in 0 5
.dc Vin 0 5 0.1
.control
foreach res 0.5 1 2
altermod m VTO=$res
run
end
plot dc1.Vdd#branch*-1 dc2.Vdd#branch*-1 dc3.Vdd#branch*-1
.endc
.end
```

Graphs:



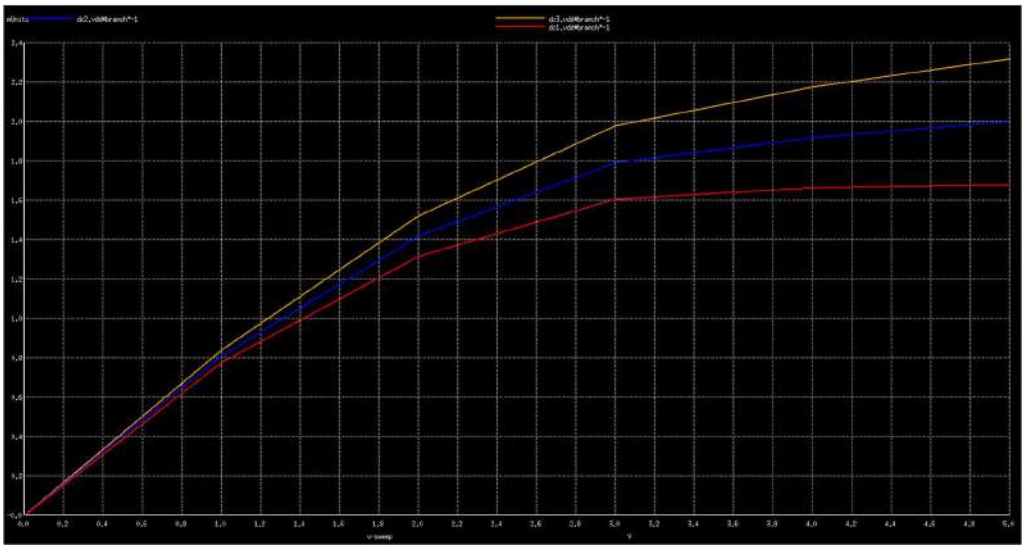
From above graph we can see that as Vt increases current through the transistor decreases.

Varying LAMDA:

Spice Code:

```
*varying lamda
.MODEL cmosn NMOS ( LEVEL = 1
+ TOX = 5.7E-9 NSUB = 1E17 GAMMA = 0.4317311
+ PHI = 0.7 VTO = 0.4238252 DELTA = 0
+ UO = 425.6466519 ETA = 0 THETA = 0.1754054
+ KP = 2.501048E-4 VMAX = 8.287851E4 KAPPA = 0.1686779
+ RSH = 4.062439E-3 NFS = 1E12 TPG = 1
+ XJ = 3E-7 LD = 3.162278E-11 WD = 1.232881E-8
+ CGDO = 6.2E-10 CGSO = 6.2E-10 CGBO = 1E-10
+ CJ = 1.81211E-3 PB = 0.5 MJ = 0.3282553
+ CJSW = 5.341337E-10 MJSW = 0.5
+ LAMBDA = 0.01 )
m vdd vg 0 0 cmosn L=1u w=1u
Vdd vdd 0 5
Vgs vg 0 4
.dc Vdd 0 5 1
.control
    foreach lmda .01 .05 .09
    altermod m LAMBDA=$lmda
    run
end
plot dc1.Vdd#branch*-1 dc2.Vdd#branch*-1 dc3.Vdd#branch*-1
.endc
.end
```

Result:



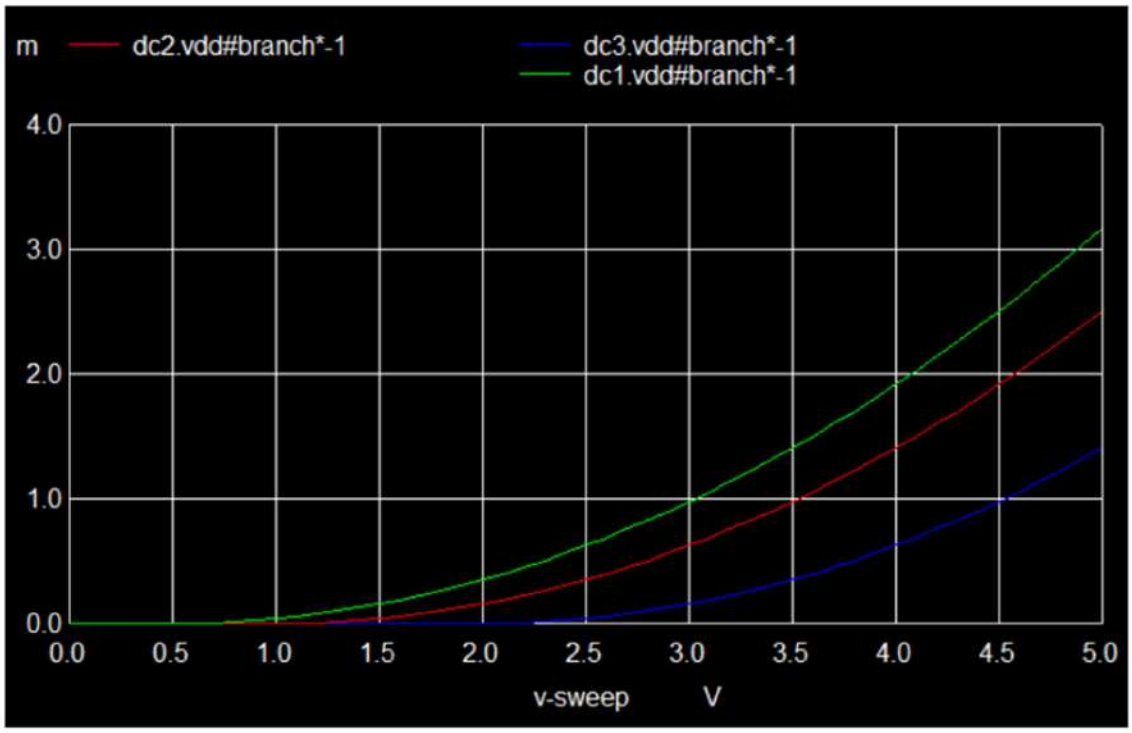
From the graph we can observe that as LAMDA increases the current in linear region has no effect but in non-linear region there is increase in current due to increase in LAMDA.

Varying VSB in reasonable range:

Spice Code:

```
*nmos characteristics
.include ./cmos_include.txt
m out in Vss 0 cmosn l=1u w=0.5u
Vss Vss 0 3
Vdd out 0 6
Vin in 0 6
.control
dc Vin 0 5 0.1 Vss 0 3 1
run
end
plot dc1.Vdd#branch*-1 dc2.Vdd#branch*-1 dc3.Vdd#branch*-1
.endc
.end
```

Result:



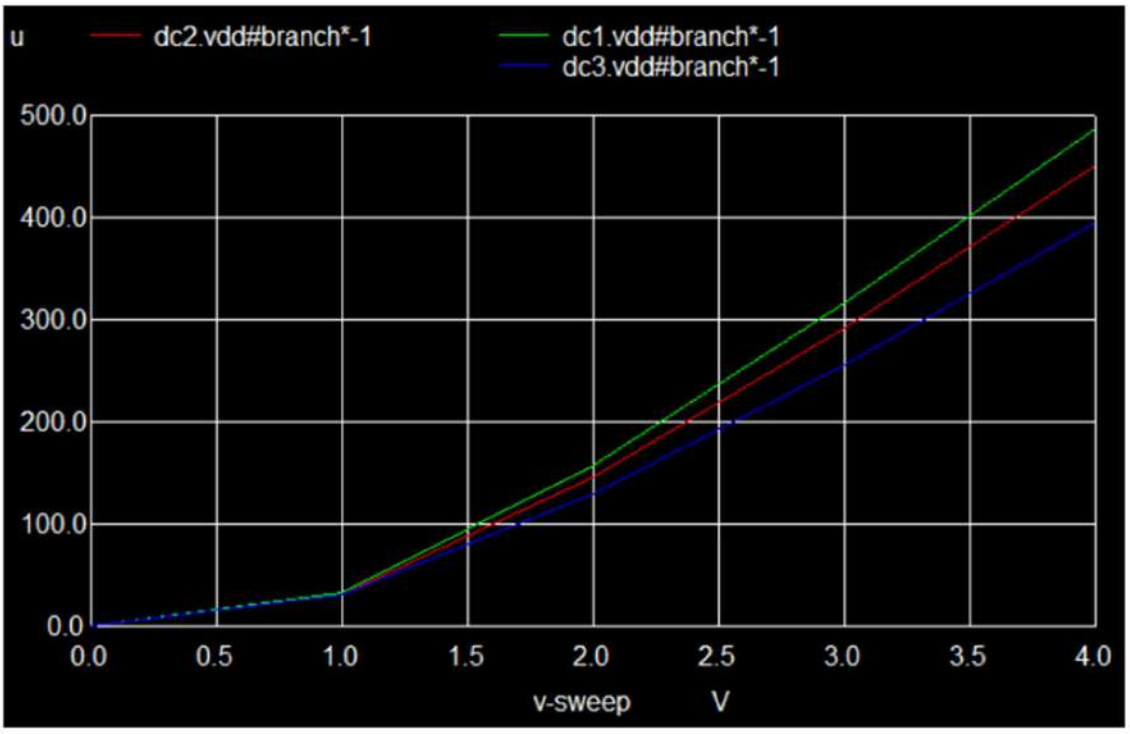
From the graph it is clear that as the VSB increases the current is reduced, this can verified by the statement that as VSB increased VT also increases resulting in the decrease in the current.

Varying Temperature:

Spice Code:

```
*mos chracteristics for varying temperature
.include ./t14y_tsmc_025_level3.txt
m Vdd Vg 0 0 cmosn l=1u w=1u
Vdd Vdd 0 5
Vgs Vg 0 4
.control
foreach t 27 60 120
alter m TEMP=$t
dc Vgs 0 4 1
run
end
plot dc1.Vdd#branch*-1 dc2.Vdd#branch*-1 dc3.Vdd#branch*-1
.endc
```

Graphs:



From the graph as the temperature increases the current through the mosfet is decreased.

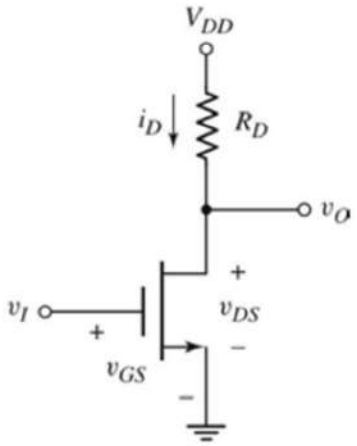
Conclusion: As L increases, Id decreases. As W increases ,Id increases. As VT o increases, Id decreases. As Lambda increases, Id increases As VSB increases, Id decreases (As VT increases) As temperature increases, Id decreases

EXPERIMENT-2

STUDY OF MOS-INVERTER WITH RESISTIVE LOAD

Objective: Study the transfer function, Noise margin, effect on risetime, fall time, propagation delay, power and energy consumed of a MOS Inverter for various L, W, Load Capacitance, and rise/fall time of input.

Circuit Diagram:

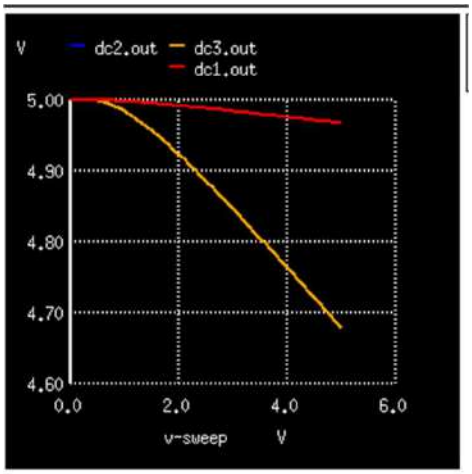


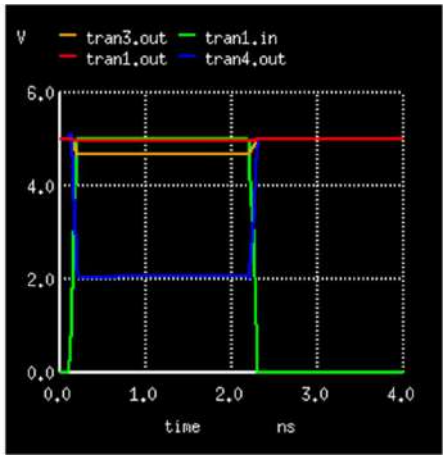
Spice Code:

```
      *resistive load chracteristics

.include ./cmos_include.txt

m1 out in 0 0 cmosn l=1u w=0.5u
r0 vdd out 100

Vdd vdd 0 5
V_in in 0 pulse(0 5 0.1n 0.1n 0.1n 2n 4n)

.dc V_in 0 5 0.1
.tran 0.1n 4n

.control
    foreach res in 100 1k 10k
    alter r0=$res
    run
    end
.endc
```

```
.control
    plot dc1.out dc2.out dc3.out
    plot dc1.Vdd#branch*-1 dc3.Vdd#branch*-1 dc3.Vdd#branch*-1
    plot tran1.out tran2.out tran3.out tran1.in
    plot tran1.Vdd#branch*-1 tran2.Vdd#branch*-1 tran3.Vdd#branch*-1
.endc

.end
```

Results:





The picture on left represents dc analysis and left represent transient analysis

As we can see that as the resistance of the load increases the out put is settling to zero when the input is 1, this shows that as R increase VOL decreases

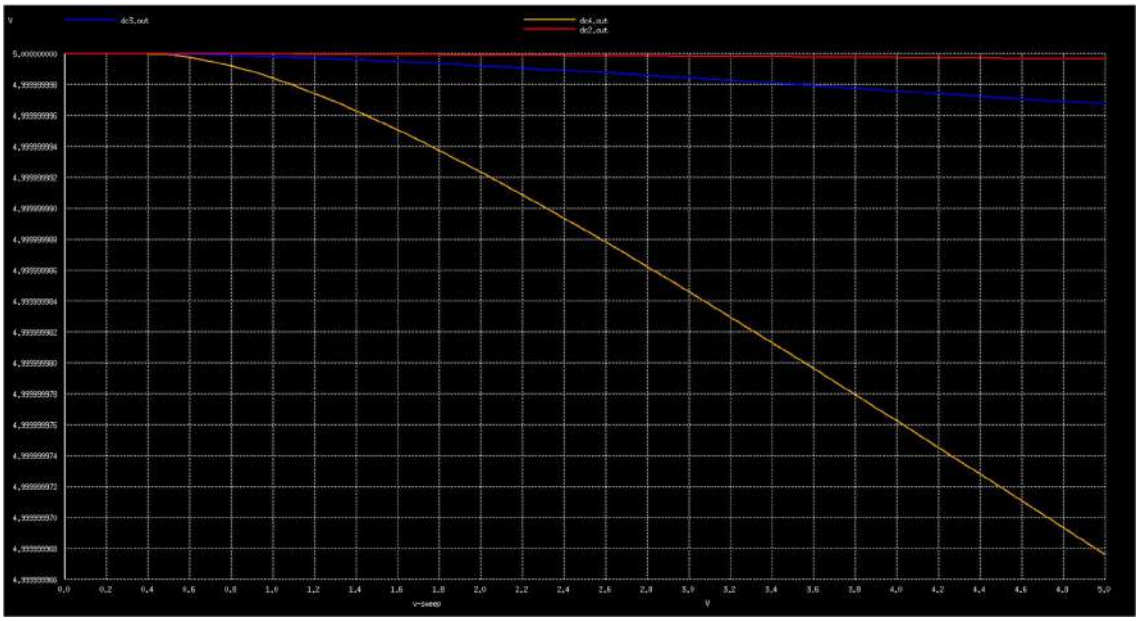
Characteristic variation wrt W/L:

Spice Code:

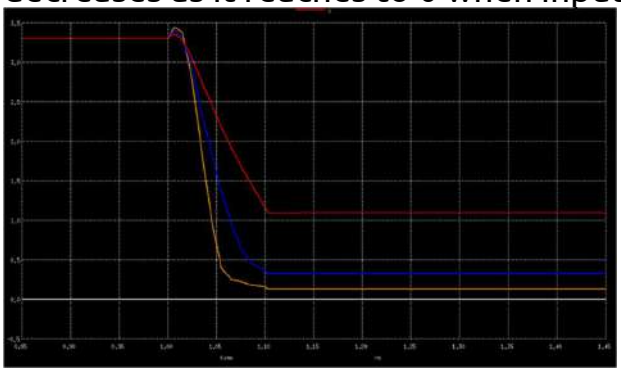
```
      *resistive load chracteristics

.include ./cmos_include.txt

m1 out in 0 0 cmosn l=1u w=0.5u
r0 vdd out 100

Vdd vdd 0 5
V_in in 0 pulse(0 5 0.1n 0.1n 0.1n 2n 4n)

.dc V_in 0 5 0.1
.tran 0.1n 4n
```

```
.control
    foreach res in 1u 10u 100u
    alter r0=$res
    run
    end
.endc

.control
    plot dc2.out dc3.out dc4.out
    plot dc2.Vdd#branch*-1
    plot dc3.Vdd#branch*-1
    plot dc4.Vdd#branch*-1
    plot tran1.out tran4.out tran3.out tran1.in
    plot tran1.Vdd#branch*-1 tran2.Vdd#branch*-1 tran3.Vdd#branch*-1
.endc

.end
```

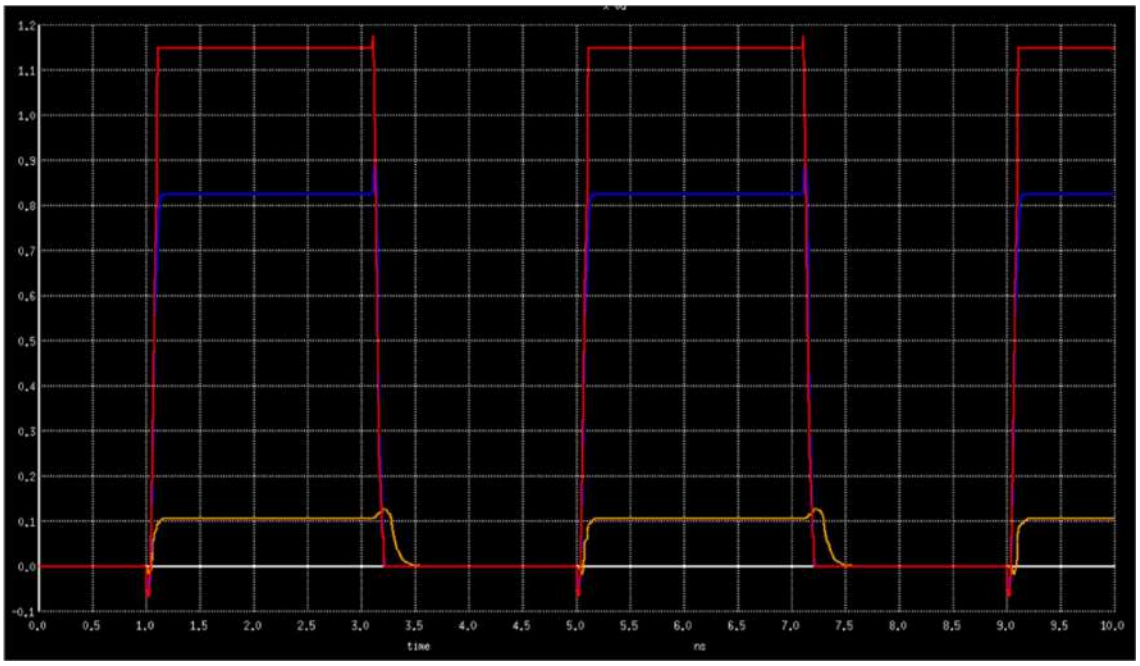
Result:



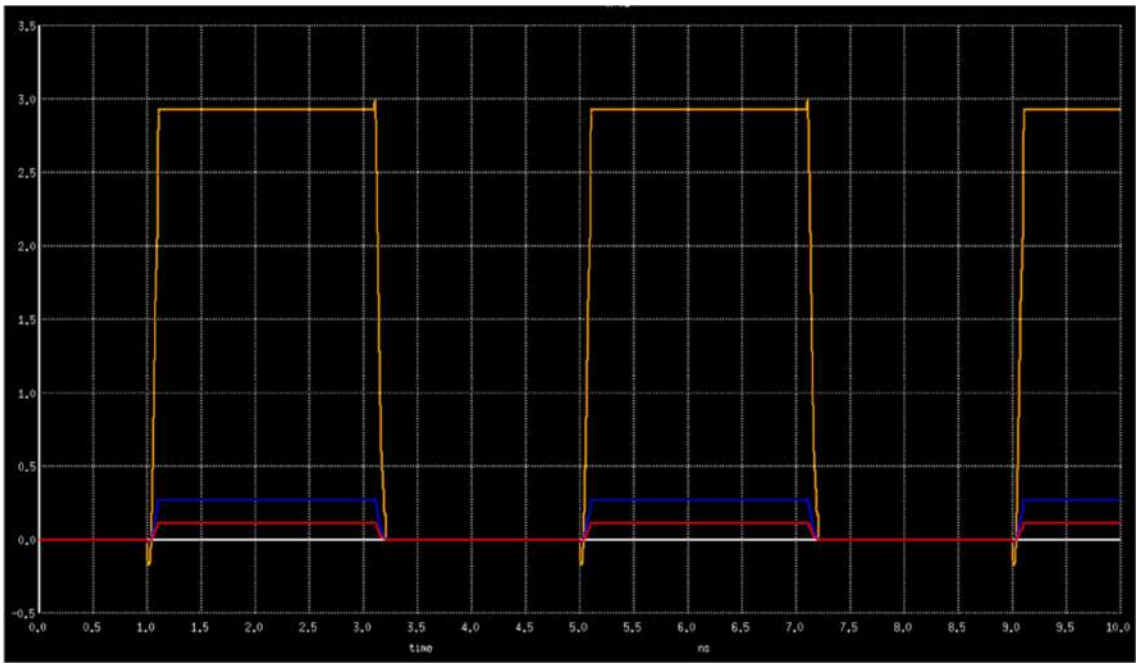
From the graph it is clear that as the W/L ratio increase the VOL decreases as it reaches to 0 when input is 1.



This shows the effect of W/L on tfall., there is no effect on trise.



The above graph shows the effect on due to resistance variation, as resistance(load) increases power decreases.



This shows effect on power due to varying W/L, this shows that as W/L increases power increases.

Conclusion:

As Load Resistance increases

- VTC shifts towards left
- The gain of the transition region in the VTC increases
- VOL decreases as R becomes larger than Resistance offered by nmos.
- Rise time and fall time of transient response decreases.
- Power consumption decreases.

As W/L ratio increases:

- VTC shifts towards left
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- the gain of the transition region in the VTC increases
- VOL decreases as Resistance offered by nmos decreases.
- Rise time and fall time of transient response decreases.
- Static and Dynamic Power consumption increases as resistance decreases.

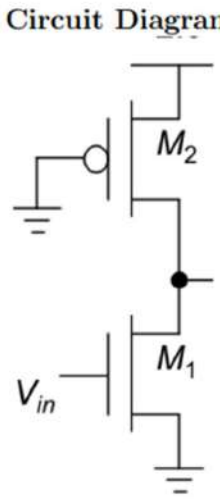
EXPERIMENT-3

MOS-INVERTER CHARACTERISTICS WITH ACTIVE LOAD NMOS AND PMOS

(PSEUDO NMOS LOAD)

Objective: For a MOS inverter with active load NMOS and PMOS (pseudo NMOS load), Study the transfer function, noise margin, effect on rise time, fall time, propagation delay, power and energy consumed by a NMOS inverter with NMOS, PMOS load for various L,W of the pull-up and pulldown transistors and to determine the power and energy consumed with non-ideal step input.

PMOS Load Circuit Diagram:

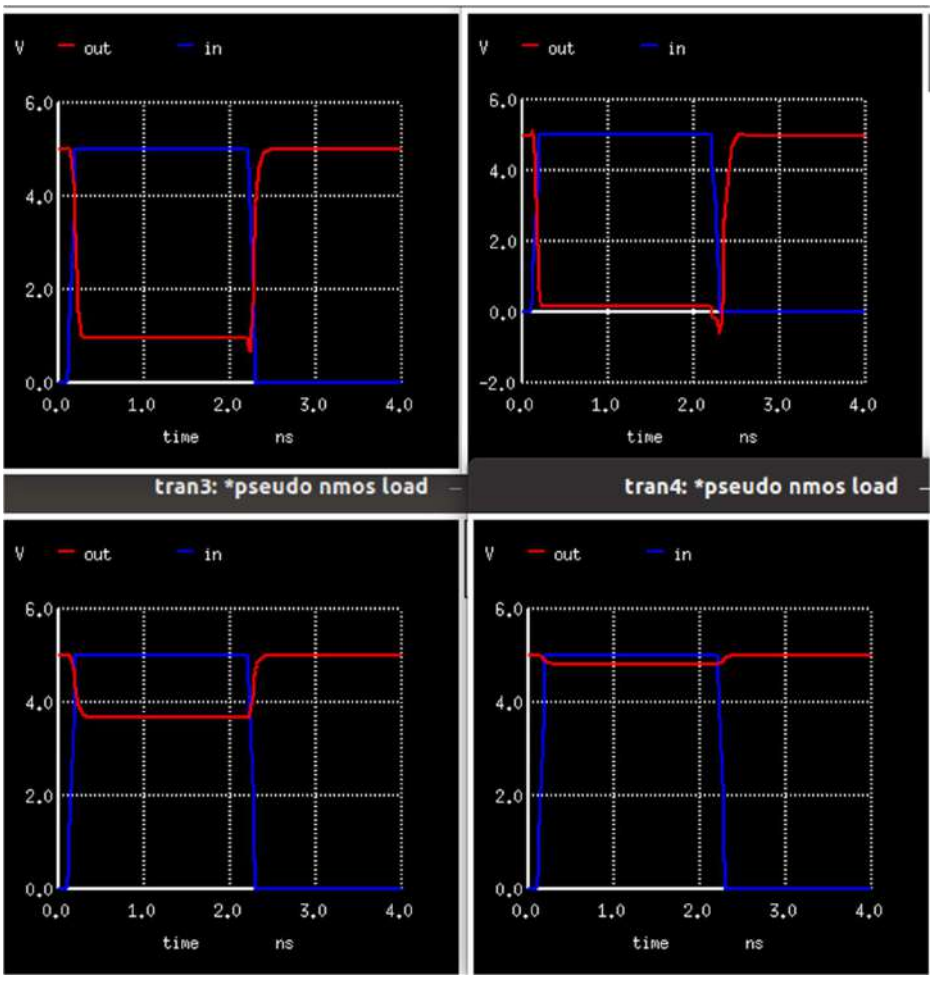


Spice Code:

```
*pseudo nmos load
.include ./cmos_include.txt

m2 out 0 vdd vdd cmosp l=1u w=4u
m1 out in 0 0 cmosn l=1u w=2u

Vdd vdd 0 5
V_in in 0 pulse(0 5 0.1n 0.1n 0.1n 2n 4n)

.dc V_in 0 5 0.1
.tran 0.1n 4n
```

```
.control
    foreach wid in 1u 10u 100u
    alter @m2 w=$wid
    run
    plot out in
    end
.endc

.end
```

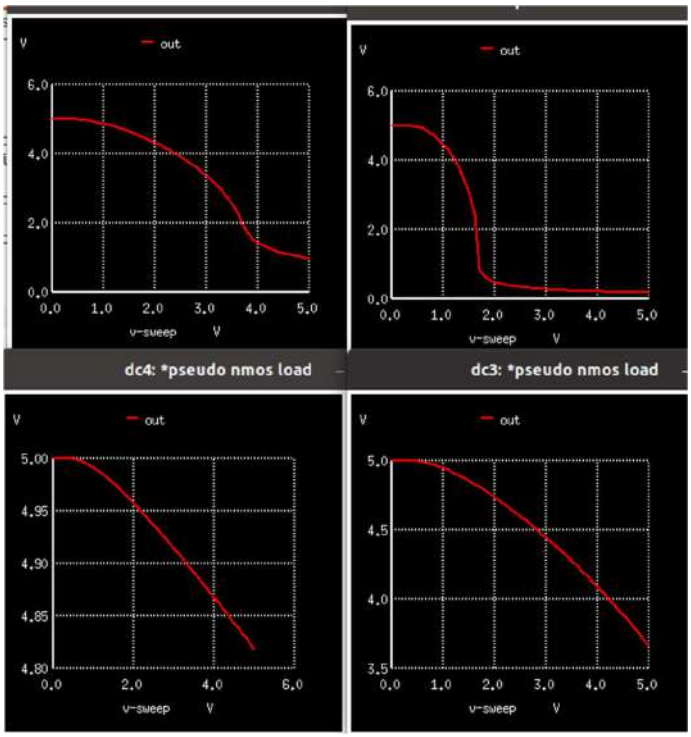
Result:



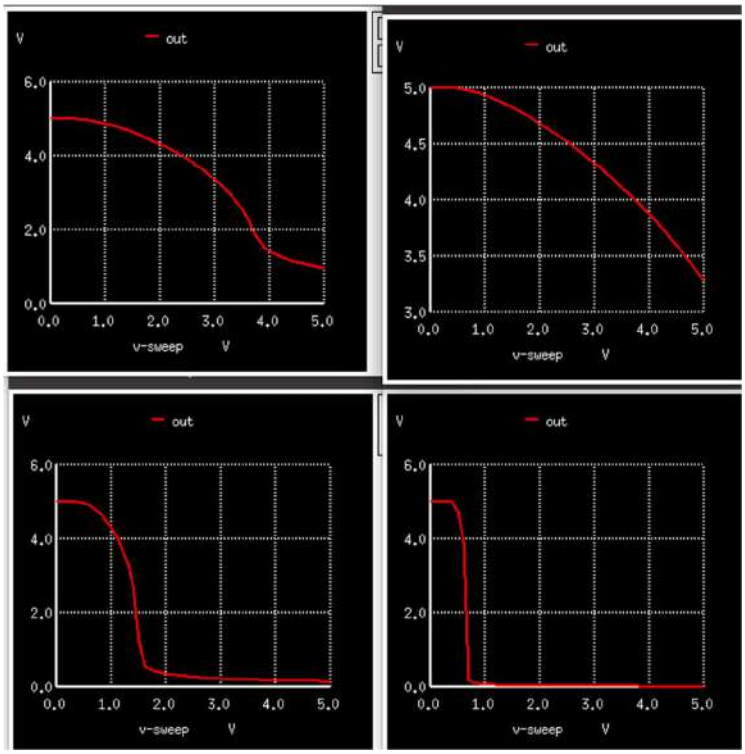
From the above graphs it is clear that as W/L ratio of pmos increases the output doesn't reaches zero, this shows that the VOL is increased.

Transfer Characteristics:

To plat transfer characteristics we use dc analysis the graphs are shown below.



From the graph as W/L ratio of pmos increases the transfer characteristics move towards right.



From the graphs as W/L ratio of nmos increases the transfer characteristics moves towards left.

Conclusion:

As W/L of NMOS increases

- VTC shifts towards left
- The gain of the transition region in the VTC increases.
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as R becomes smaller than Resistance offered by pmos.
- Power Dissipation Increases as R is smaller and also energy consumed per transition increases.
- Rise/Fall time reduces.

As W/L of PMOS LOAD decreases

- VTC shifts towards left
- the gain of the transition region in the VTC increases
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as Resistance offered by pmos increases.
- Static and Dynamic Power Dissipation decreases as R is larger and also energy consumed per

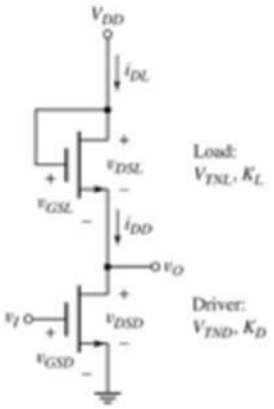
  transition decreases.
- Rise/Fall time reduces.

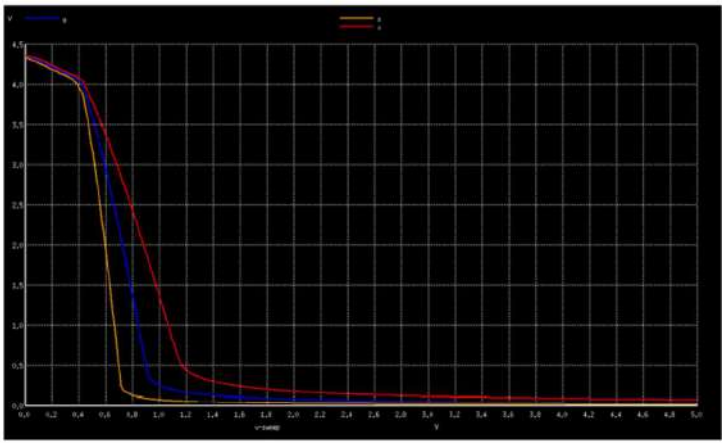
As Load Capacitance increases, Rise/Fall time of output increases and Energy consumed per

transition increases.

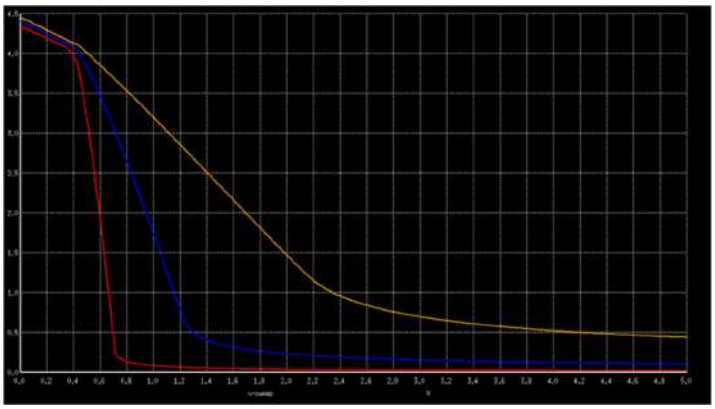
Also, Static power increases. As input rise time and fall time increases TPHL and TPLH increases.

NMOS load Circuit Diagram:

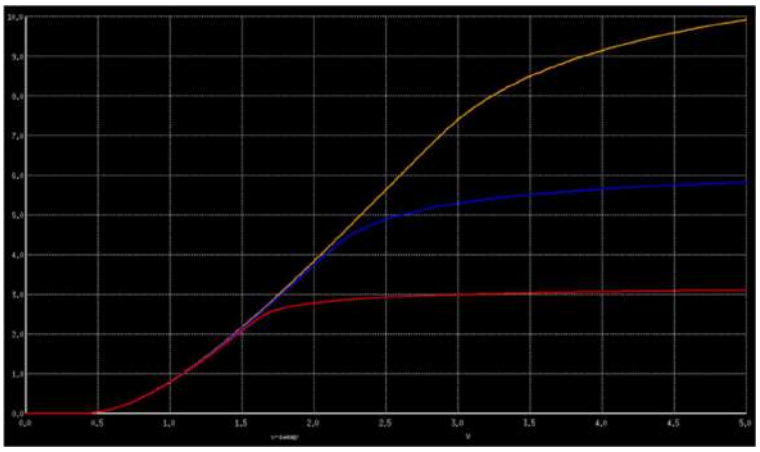




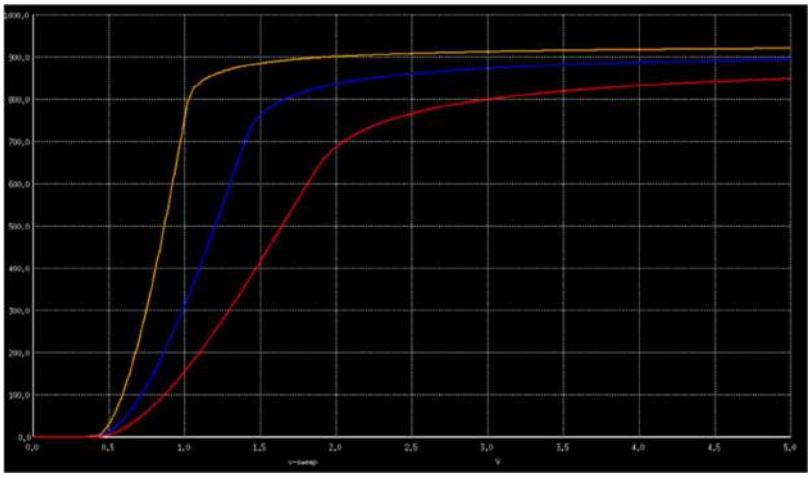
Transfer due to varying the width of driver



Transient Characteristics due to varying the Width of load- nmos



Static power wrt variation in load width(W/L)



Static power wrt variation in driver width(W/L)

Conclusion: VOH can never be equal to VDD as NMOS can pull up to only VDD-VT.

As W/L of NMOS LOAD decreases

- VTC Shifts towards left
- The gain of the transition region in the VTC increases
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as Resistance offered by nmos increases.
- Power Dissipation decreases as R is larger and also energy consumed per transition decreases.
- Rise/Fall time of output reduces.

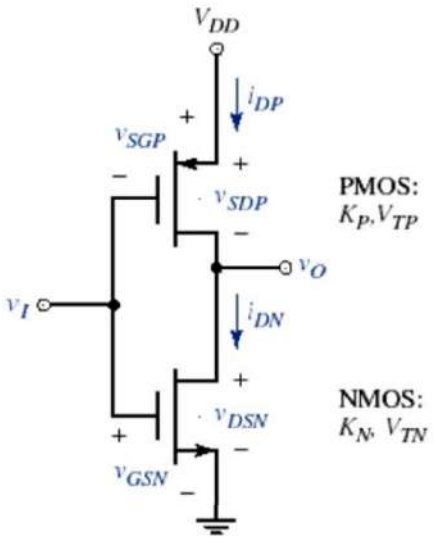
As W/L of NMOS increases

- VTC Shifts towards left
- the gain of the transition region in the VTC increases.
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as R becomes smaller than Resistance offered by pmos.
- Power Dissipation Increases as R is smaller and also energy consumed per transition increases.
- Rise/Fall time reduces

EXPERIMENT-4

STUDY OF CMOS INVERTER

Circuit Diagram:

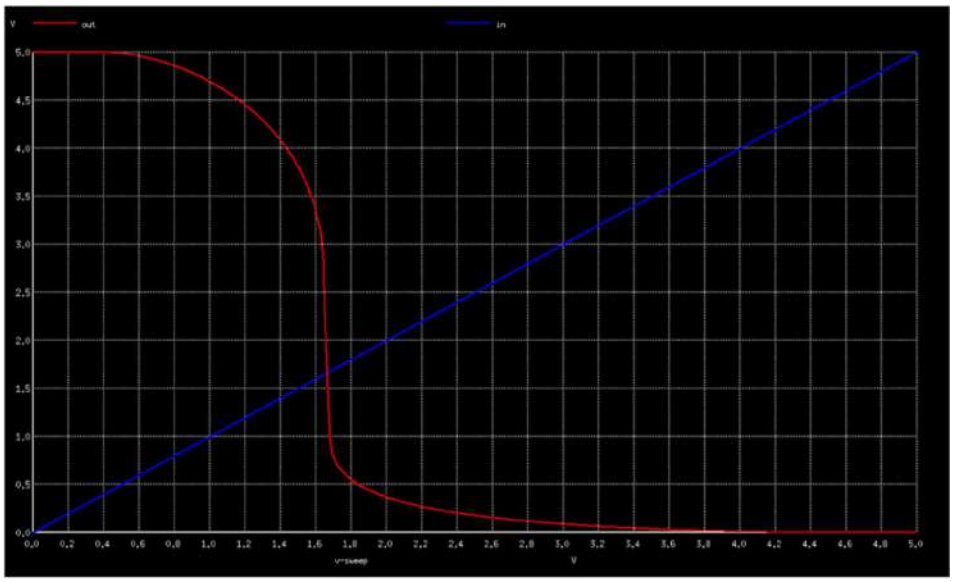


Spice Code Used:

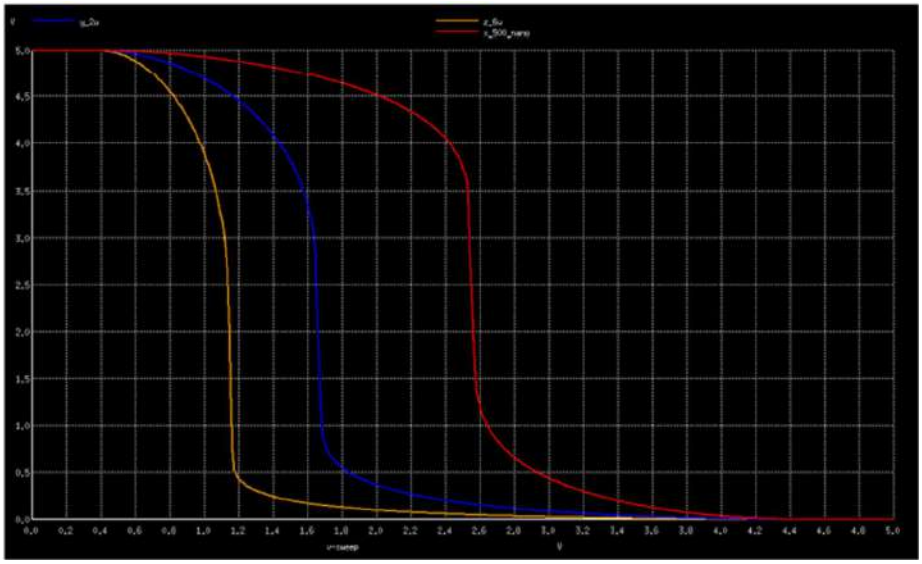
```
      * cmos inverter characteristics

.include ./t14y_tsmc_025_level3.txt
m1 out in 0 0 cmosn l=1u w=1u
m2 out in vdd vdd cmosp l=1u w=15u
v_dd vdd 0 5
v_in in 0 dc 2.5 pulse(5 0 0 0.05n 0.05n 1n 2n)
.control
    tran 0.01n 2n
    meas tran t1 when v(out)=0
    meas tran t2 when v(out)=5
    meas tran power INTEG i(v_dd) from=0 to=t2
    print power*2.5
    print t2-t1
    setplot tran1
    plot in out
    plot -v_dd#branch
    dc v_in 0 5 0.1
    setplot dc1
    plot in out
```

```
    plot -v_dd#branch
.endc

.end
```

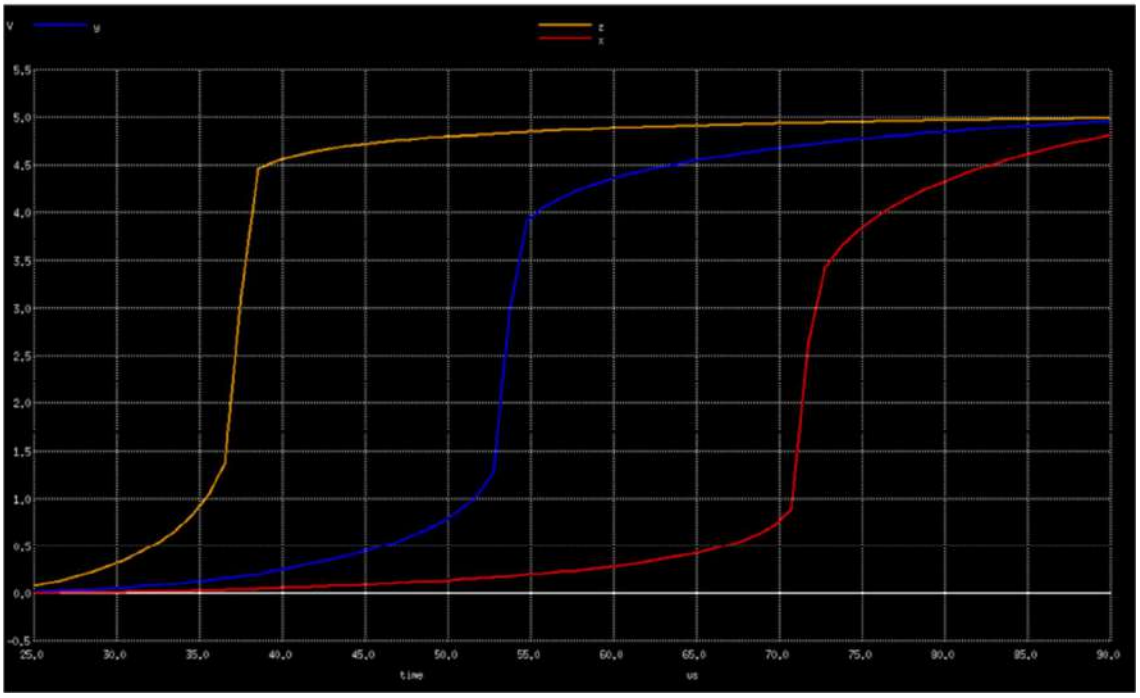
The above code is used to study the characteristics of cmos inverter. .meas command is used to compute risetime, power consumed etc.



Transfer function of the inverter



Transfer function of the inverter with varying width



Effect on traise due to variation of W/L of pmos

Conclusion:

For a given KD, as KL increases

- Trise decreases
- VTC curve shifts to the right.

For a given KL, as KD increases

- Tfall decreases
- VTC curve shifts to the left.

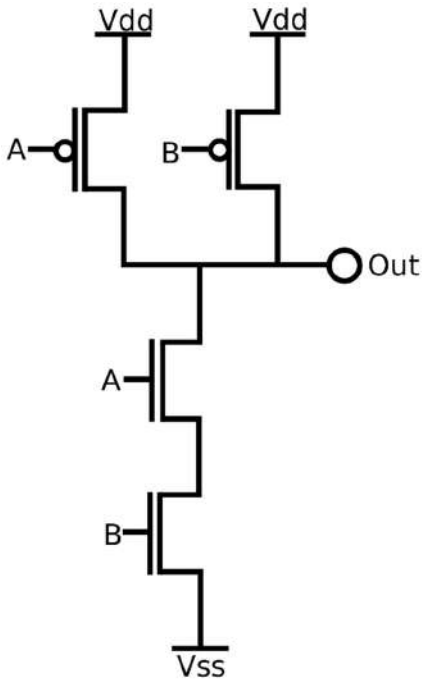
EXPERIMENT-5

STUDY OF CMOS GATES

Objective: Study the behaviour transfer function, noise margin, rise time ,fall time, propagation- delay, power of a CMOS gates like NAND ,NOR functions (2 input AND gate ,2 input OR gate) with variations in L and W of pullup and pulldown transistors.

NAND:

Circuit Diagram:

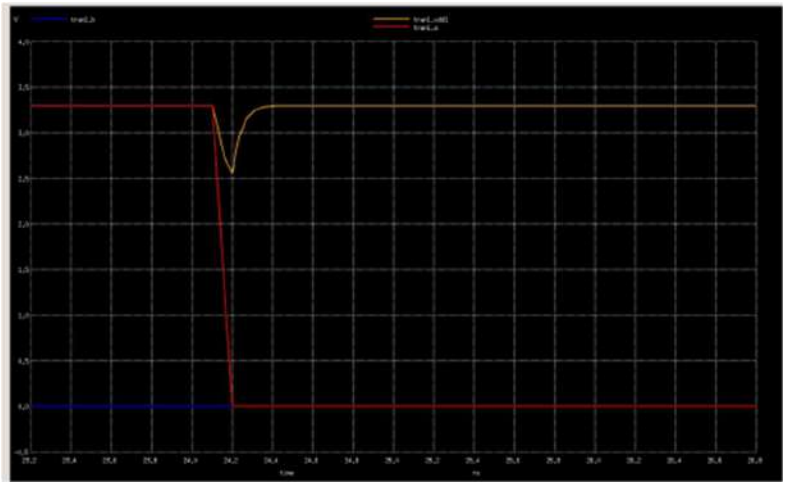


Spice Code Used:

```
*nand gate cmos logic

./include cmos_include.txt


mpa out A VDD VDD cmosp l=1u w=5u
mpb out B VDD VDD cmosp l=1u w=5u
```

```
mna out A midnode 0 cmosn l=1u w=2u
mnb midnode B 0 0 cmosn l=1u w=2u

*sources
V_DD VDD 0 5
V_A A 0 pulse(0 5 0.1n 0.1n 0.1n 2n 4n)
V_B B 0 pulse(5 0 0.1n 0.1n 0.1n 4n 8n)

*analsis to be done
.tran 0.001n 8n

.control
    run
    plot tran1.A tran1.B tran1.out
.endc
.end
```

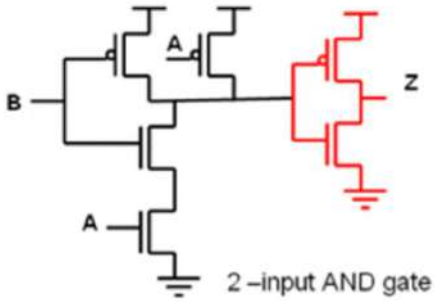
Result Obtained:



The above graph depicts the working of the netlist

AND Gate:

Circuit Diagram:

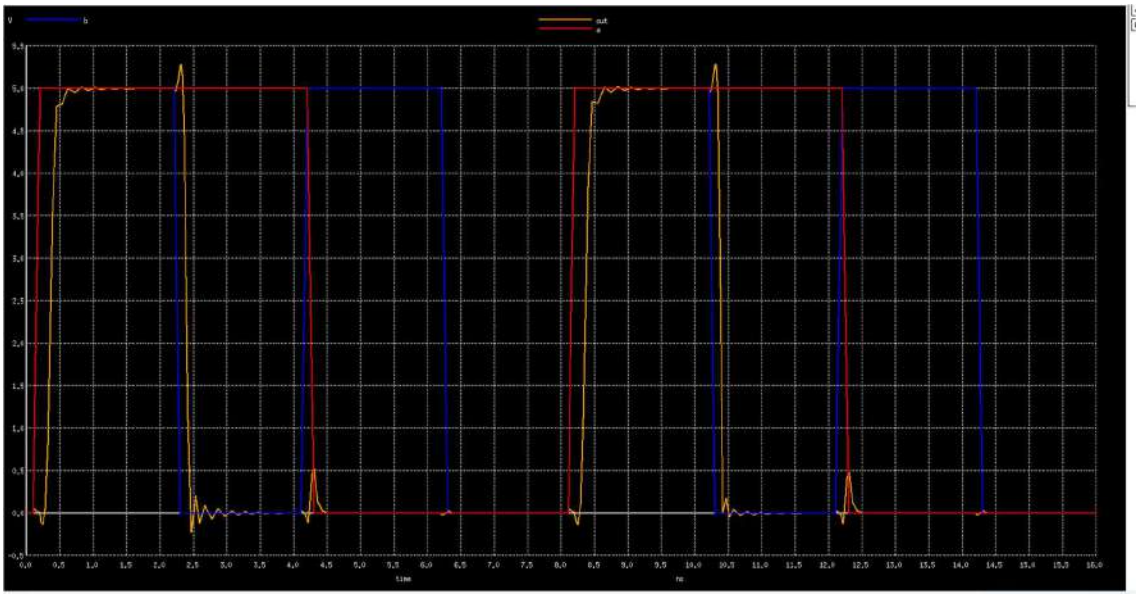


Spice Code Used:

```
* SPICE3 file created from cmos_and_layout.ext - technology: scmos

.model pfet pmos level=3 version=3.3.0
.model nfet nmos level=3 version=3.3.0

.option scale=1u

M1000 nand_mid_1 A gnd Gnd nfet w=5 l=2
+  ad=20 pd=18 as=47 ps=40
M1001 out nandtoinv gnd Gnd nfet w=3 l=2
+  ad=22 pd=20 as=0 ps=0
M1002 out nandtoinv V_DD V_DD pfet w=6 l=2
+  ad=26 pd=22 as=94 ps=70
M1003 nandtoinv A V_DD V_DD pfet w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1004 nandtoinv B nand_mid_1 Gnd nfet w=5 l=2
+  ad=28 pd=22 as=0 ps=0
M1005 V_DD B nandtoinv V_DD pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
C0 V_DD A 2.07fF
C1 gnd Gnd 6.06fF
C2 nandtoinv Gnd 8.41fF
C3 B Gnd 7.42fF
C4 A Gnd 5.26fF

V_A A gnd pulse(0 5 0.1n 0.1n 0.1n 4n 8n)
V_B B gnd pulse(0 5 0.1n 0.1n 0.1n 2n 4n)
v_dd V_DD gnd 5

.control
    tran 0.1n 16n
    setplot tran1
    plot A B out
```

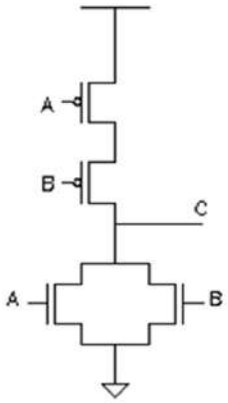
```
.endc

.end
```

Results Obtained:



NOR Gate:

Circuit Diagram:



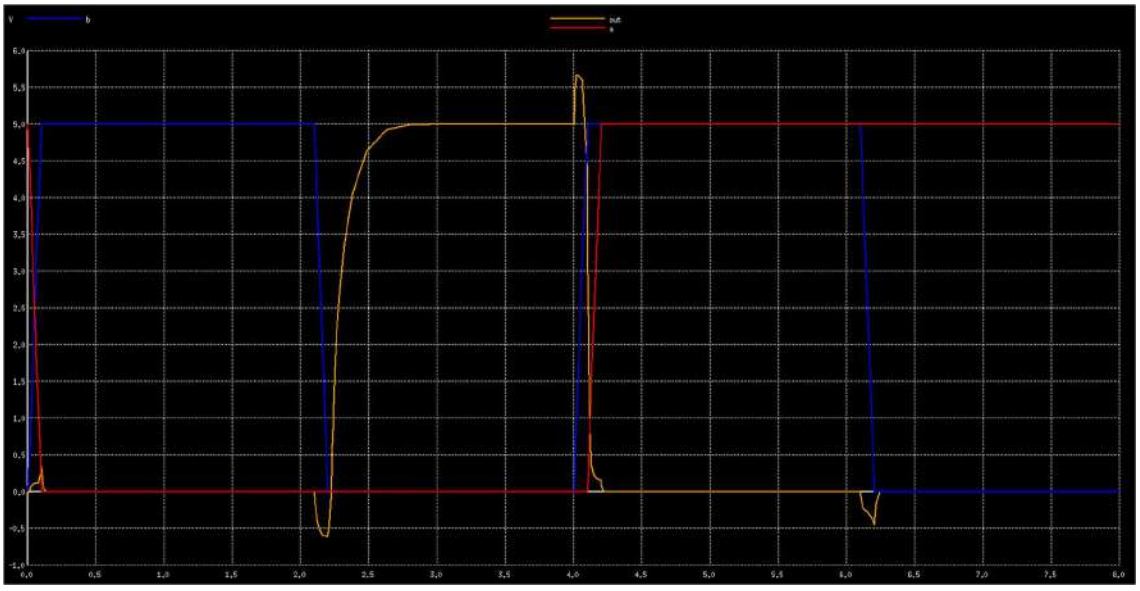
NOR

Spice Code Used:

```
*nor gate using cmos logic
```

```
.include ./cmos_include.txt

mna out a 0 0 cmosn l=1u w=4u
mnb out b 0 0 cmosn l=1u w=4u
mpa midnode a vdd vdd cmosp l=1u w=10u
mpb out b midnode vdd vdd cmosp l=1u w=10u

v_dd vdd 0 5
v_a a 0 pulse(5 0 0 0.1n 0.1n 4n 8n)
v_b b 0 pulse(0 5 0 0.1n 0.1n 2n 4n)

.control
    tran 0.01 8n
    setplot
    plot a b out
.endc

.end
```

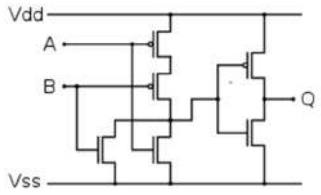
Result:



We can see that out put is 1 only when both inputs are zero.

OR Gate:

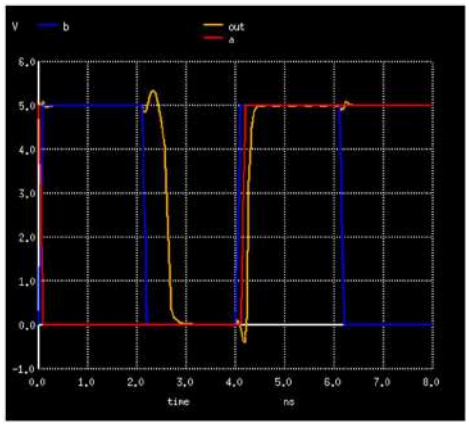
Circuit Diagram:



Spice Code Used:

```
      *nor gate using cmos logic


.include ./cmos_include.txt

mna temp a 0 0 cmosn l=1u w=4u
mnb temp b 0 0 cmosn l=1u w=4u
mpa midnode a vdd vdd cmosp l=1u w=10u
mpb temp b midnode vdd cmosp l=1u w=10u

mn out temp 0 0 cmosn l=1u w=4u
mp out temp vdd vdd cmosp l=1u w=10u
v_dd vdd 0 5
v_a a 0 pulse(5 0 0 0.1n 0.1n 4n 8n)
v_b b 0 pulse(0 5 0 0.1n 0.1n 2n 4n)

.control
    tran 0.01 8n
    setplot
    plot a b out
.endc

.end
```

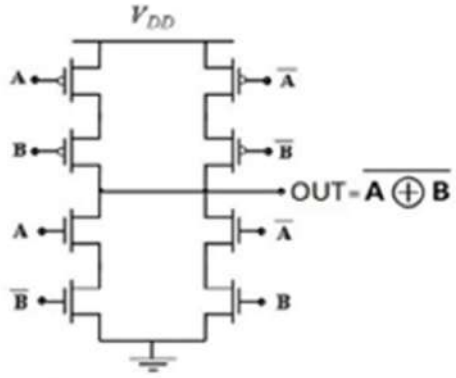
Result:



Output of this graph depicts the characteristics of OR gate.

XNOR Gate:

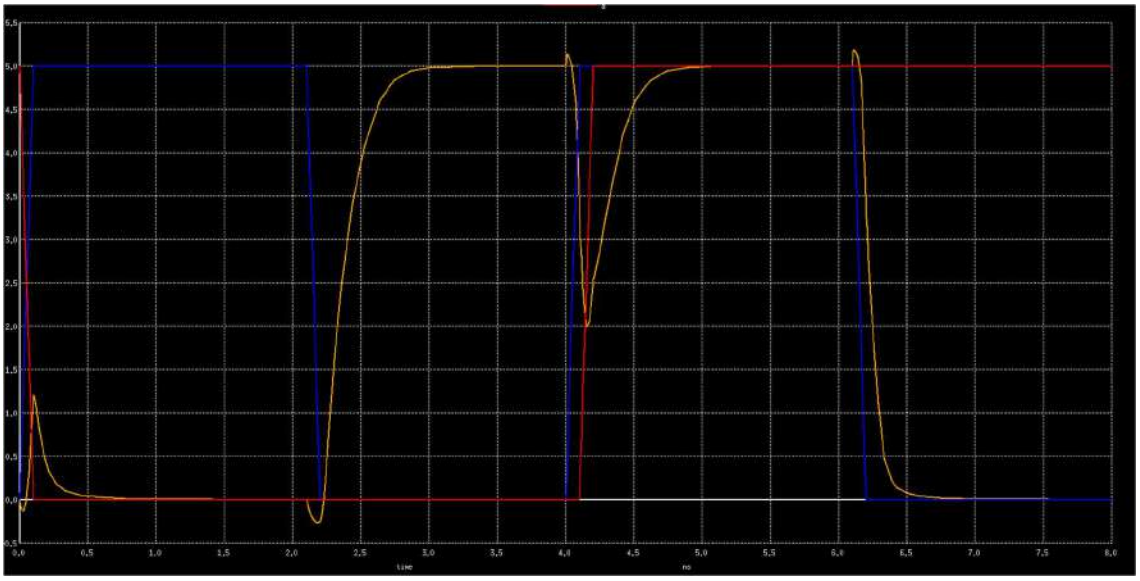
Circuit Diagram:



Spice Code Used:

```
      *xnor gate using cmos logic


.include ./cmos_include.txt

mpa w a vdd vdd cmosp l=1u w=10u
mpb out b w vdd cmosp l=1u w=10u
mpab x nega vdd vdd cmosp l=1u w=10u
mpbb out negb x vdd cmosp l=1u w=10u

mna out a y 0 cmosn l=1u w=4u
mnb z b 0 0 cmosn l=1u w=4u
mnab out nega z 0 cmosn l=1u w=4u
mnbb y negb 0 0 cmosn l=1u w=4u

v_dd vdd 0 5
v_a a 0 pulse(5 0 0 0.1n 0.1n 4n 8n)
v_b b 0 pulse(0 5 0 0.1n 0.1n 2n 4n)
v_nega nega 0 pulse(0 5 0 0.1n 0.1n 4n 8n)
v_negb negb 0 pulse(5 0 0 0.1n 0.1n 2n 4n)

.control
    tran 0.01 8n
    setplot
    plot a b out
.endc

.end
```

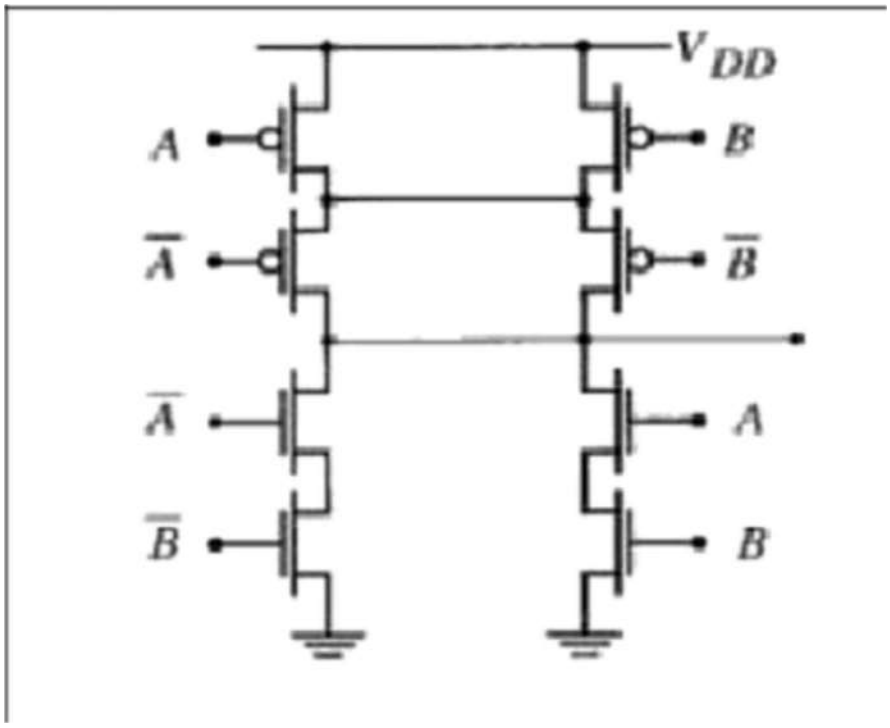
Graph:



We can see that output is 1 only when both A and B are same, this shows that out netlist represent a XNOR gate.

XOR Gate:

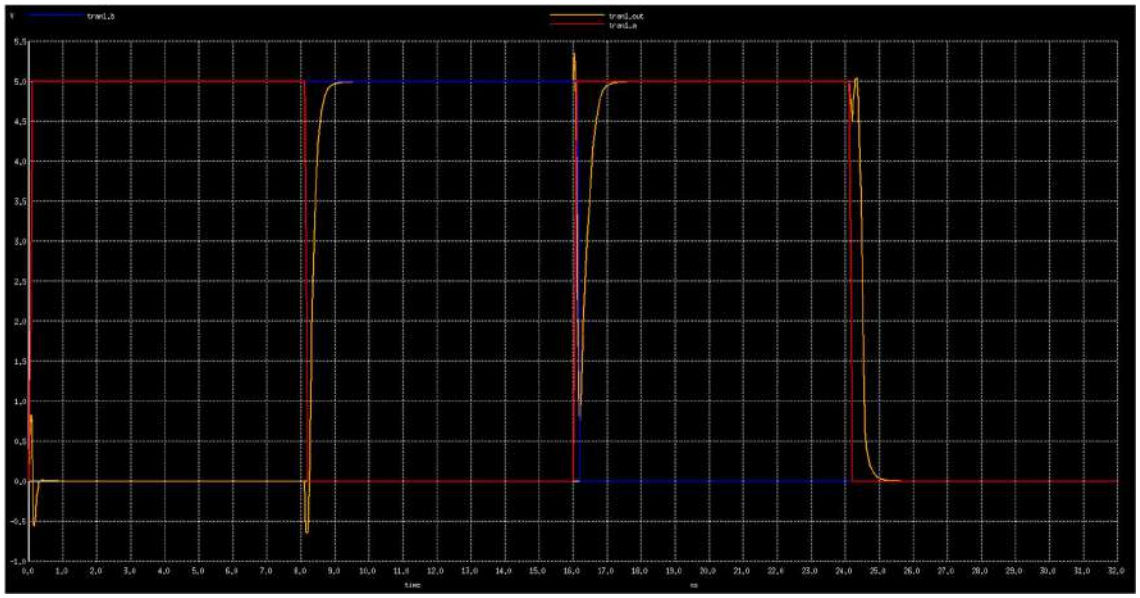
Circuit Diagram:



Spice Code:

```
      .include ./cmos_include.txt


m1 x nega vdd vdd cmosp l=1u w=10u
m2 y A vdd vdd cmosp l=1u w=10u
m3 out B x x cmosp l=1u w=10u
m4 out negb y y cmosp l=1u w=10u

m5 out A temp3 0 cmosn l=1u w=10u
m6 out nega temp4 0 cmosn l=1u w=10u
m7 temp3 B 0 0 cmosn l=1u w=10u
m8 temp4 negb 0 0 cmosn l=1u w=10u
m1_ainv nega A vdd vdd cmosp l=1u w=10u
m2_ainv nega A 0 0 cmosn l=1u w=10u
m1_binv negb B vdd vdd cmosp l=1u w=10u
m2_binv negb B 0 0 cmosn l=1u w=10u v_dd vdd 0 5
v_a A 0 pulse(0 5 0 0 0 8ns 16ns)
v_b B 0 pulse(0 5 0 0 0 16ns 32ns)
.control
    tran 0.1ns 32ns
    setplot
    plot A B out
.endc
.end
```

Result:

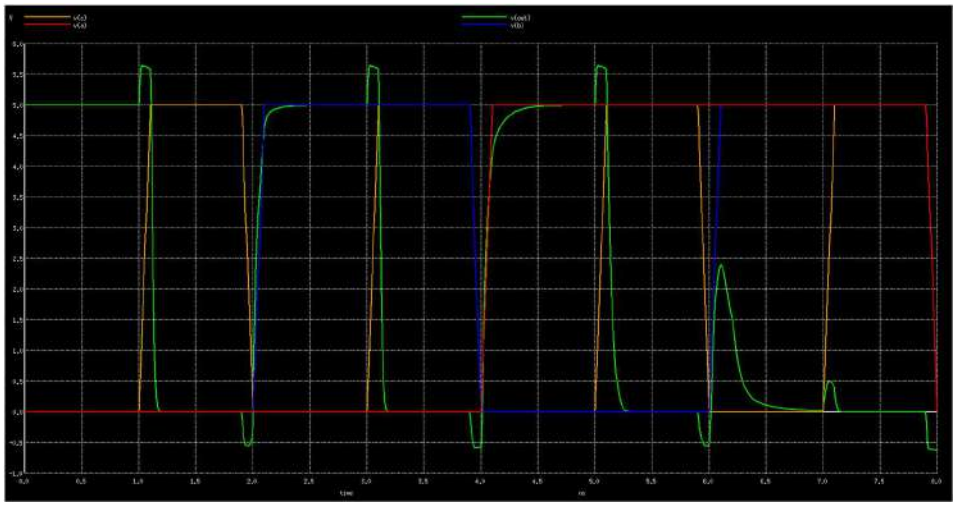


AOI Logic:

Spice Code:

```
      .include ./cmos_include.txt

*3 input AOI GATE

mpa nabc a pos pos cmosp w=4u l=1u
mpb nabc b pos pos cmosp w=4u l=1u
mpc out c nabc pos cmosp w=4u l=1u
mna out a nab 0 cmosn w=1u l=1u
mnb nab b 0 0 cmosn w=1u l=1u
mnc out c 0 0 cmosn w=1u l=1u

*vout1 out out1 0
*vout2 out out2 0
vpos pos 0 5
va a 0 0 pulse(0 5 4n 0.1n 0.1n 3.8n 8n)
vb b 0 0 pulse(0 5 2n 0.1n 0.1n 1.8n 4n)
vc c 0 0 pulse(0 5 1n 0.1n 0.1n 0.8n 2n)
.control
    tran 0.01n 8n
    plot v(a) v(b) v(c) v(out)
    let power = -5*vpos#branch
    meas tran pavg AVG power from=0n to=4n
.endc
.end
```

Result:

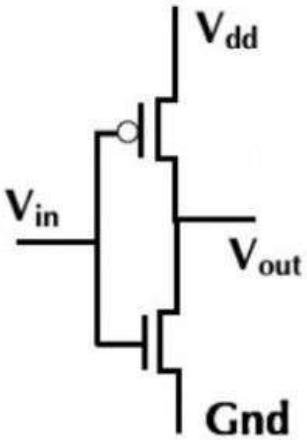


EXPERIMENT-6

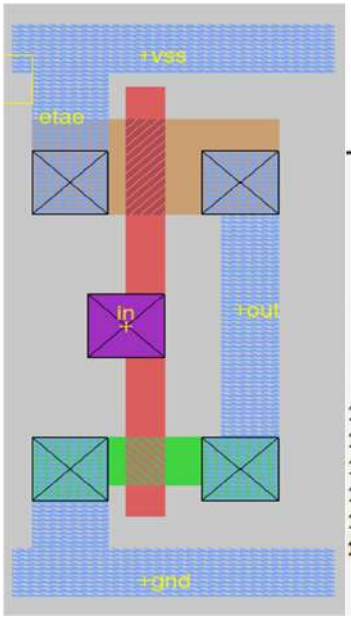
LAYOUT DESIGN OF A CMOS INVERTER

Objective: Learn layout extraction, LVS and characterization process in the design flow with CMOS inverter as an example.

Circuit Diagram:



Layout Drawn:




```
timestamp 1635400088
version 8.2
tech scmos
style lambda=1.0(scna20_orb)
scale 1000 1 100
resistclasses 26670 59550 23860 19690 27260 2000000 49 26 2505830
node "gnd" 45 2961 -5 -18 ndc 19 18 0 0 0 0 0 0 0 0 0 0 79 54 0 0 0 0
node "out" 115 1974 2 -17 ndiff 22 20 36 24 0 0 0 0 0 0 0 0 74 54 0 0 0 0
node "vss" 72 2961 -5 0 pdc 0 0 30 22 0 0 0 0 0 0 0 0 87 58 0 0 0 0
node "in" 320 5876 -2 -9 pc 0 0 0 0 62 62 0 0 0 0 0 0 16 16 0 0 0 0
device mosfet nfet 0 -17 1 -16 2 3 "Gnd!" "in" 4 0 "gnd" 3 0 "out" 3 0
device mosfet pfet 0 0 1 1 2 6 "Vdd!" "in" 4 0 "vss" 6 0 "out" 6 0
subcap "gnd" -1269
subcap "out" -1316
subcap "vss" -1833
```

Spice Code Generated:

```
* SPICE3 file created from cmos_inv_layout.ext - technology: scmos
.model pfet pmos level=3 version=3.3.0
.model nfet nmos level=3 version=3.3.0
.option scale=1u

M1000 out in gnd gnd nfet w=3 l=2
+  ad=22 pd=20 as=19 ps=18
M1001 out in V_DD V_DD pfet w=6 l=2
+  ad=26 pd=22 as=26 ps=22
C0 in gnd 4.00fF

v_dd V_DD gnd 5
v_in in gnd dc 2.5 pulse(5 0 0 0.05n 0.05n 1n 2n)
.control
    tran 0.01n 2n
    meas tran t1 when v(out)=0
    meas tran t2 when v(out)=5
    meas tran power INTEG i(V_DD) from=0 to=1n
    meas tran power1 INTEG i(V_DD) from=1n to=2n
    print (-power+power1)/2
    print t2-t1
    setplot tran1
    plot in out
    plot -V_DD#branch
    dc v_in 0 5 0.1
    setplot dc1
    plot in out
    plot -V_DD#branch
.endc

.end
```

The above code is extracted from the optimized layout of the cmos_inverter using magic.

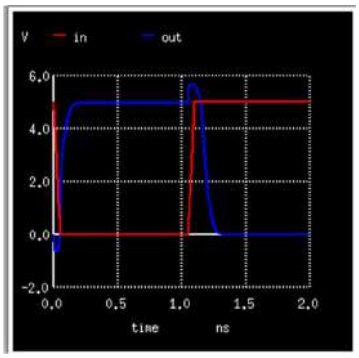
As we can observe there is no output capacitance for the layout, Only input capacitance.

Meas is used to measure the rise time of the netlist. The results of the netlist and the graphs are shown below.

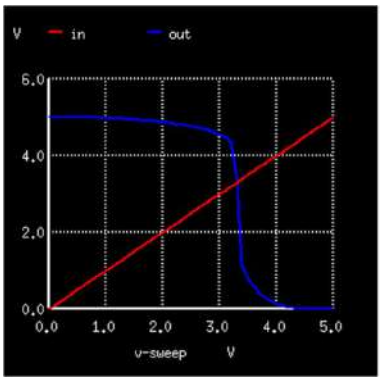
For the above netlist the trise = tfall = 1ns

Power consumed = 1.99 e-14 W

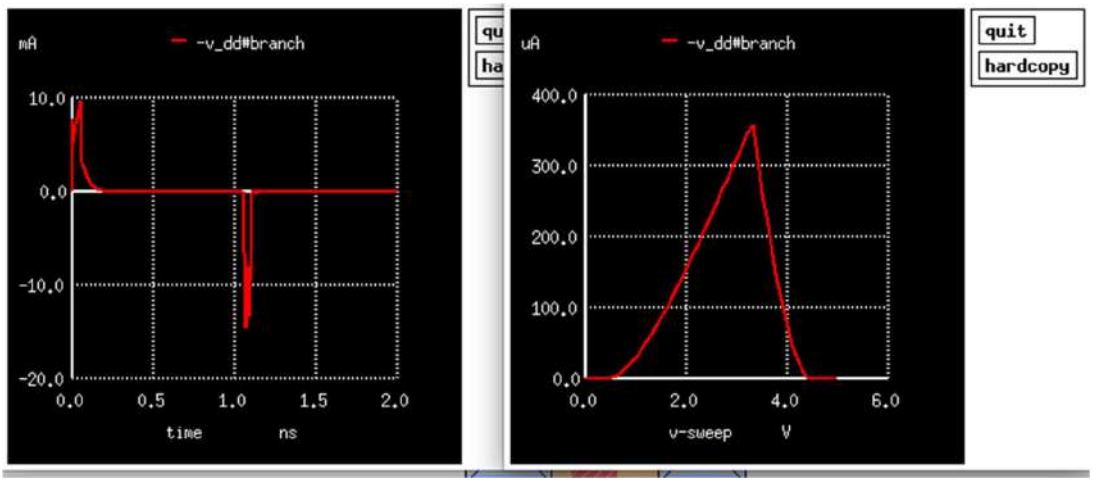
Results:



Transient response of the netlist.



DC Response of the netlist



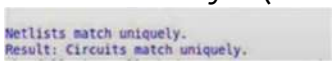
Inference:

- Assuming that mobility of electrons is 2 times more than that of protons and the widths of the transistors are designed in a way that trise = tfall then we can design the gate for a specified trise/tfall using the formula

  $T\_Rise = 2.2RC_{in}$

  $T\_Fall = 2.2RC_{in}$

- Since power rails are needed to run only the inverter I used the minimum width of the metal-1 as mentioned in the design rule (3).
- The spice file from ect2spice is simulated below and we can see that the **graphs on the simulation is similar to graphs in experiment4**
- Netgen helps us to compare two netlists, one is the netlist from exp2spice and other is written by us(used in experiment4)



- Since there is only one transistor in PDN and PUN the transistor are laid in single diffusion and I used the minimum possible width for the transistors so the above netlist produced is the optimal netlist obtained.

Area	Input Cap	Out Cap	Trise/Tfall	PPT
6 + 12	4.00fF	0from layout	0.05ns	1.99 e-14
6 + 24	No change	No change	0.035ns	3.98 e-14
24 + 48	No change	No change	0.030ns	7.7 e-14

PPT = Power Per Transaction.

Area is not equal to the value in table but it is proportional to it.

From the table we can observe that as the area of the diffusion increases the capacitance have a little/no effect but there is change in rise/fall time due to change in resistance of the transistors. Similarly due to decrement of the transistor resistance the power consumed in also increased.

EXPERIMENT-7

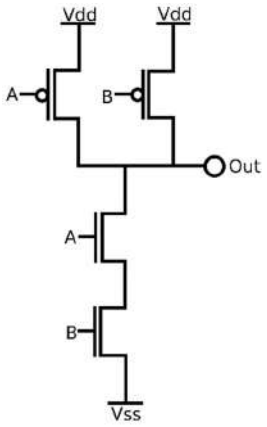
CREATING OUR OWN STANDARD CELL LIBRARY

Objective: To design our own standard cell library of NAND NOR AND OR NOT gates.

- Used SCMOS.tech for all the layout.
- Intra cell connections are done using M1
- Inter cell connections are done using M2
- Rails are of 4width
- Widths are so that worst case trise = worst case tfall
- Height of the each cell is 36

Design of NAND:

Circuit Diagram:



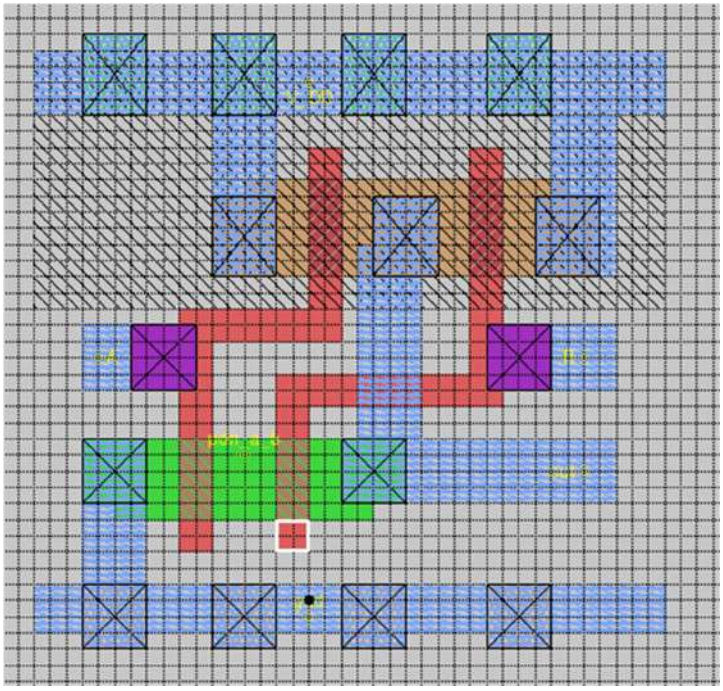
Width Analysis:

Assuming a nmos with width= w offers a resistance of R and pmos with width= 2w offers a resistance R.

In worst case, in PDN two transistors are working, So the resistance offered by each transistor should be R/2 ➔ width = 2W

In worst case, in PUN only 1 pmos is on, So the resistance offered by each transistor should be R➔width = 2W

Layout of Nand:



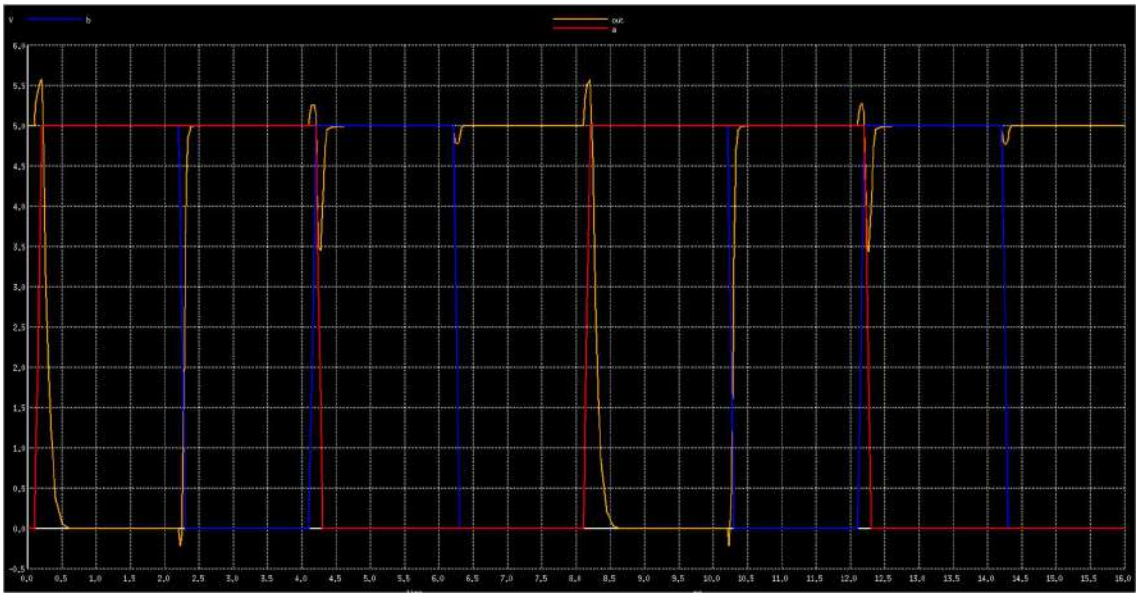
A and B are inputs

Spice Code Generated:

```
* SPICE3 file created from cmos_nand_layout.ext - technology: scmos

.option scale=1u

M1000 pdn_a_b A gnd Gnd nfet w=3 l=2
+  ad=12 pd=14 as=22 ps=20
M1001 out A V_DD V_DD pfet w=6 l=2
+  ad=48 pd=28 as=68 ps=48
M1002 V_DD B out V_DD pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
M1003 out B pdn_a_b Gnd nfet w=3 l=2
+  ad=22 pd=20 as=0 ps=0
C0 A V_DD 2.07fF
C1 gnd Gnd 4.18fF
C2 out Gnd 3.20fF
C3 B Gnd 7.04fF
C4 A Gnd 5.45fF
```

For the above netlist transient analysis is done while changing the inputs and plotting the outputs. The result of the analysis is shown below.

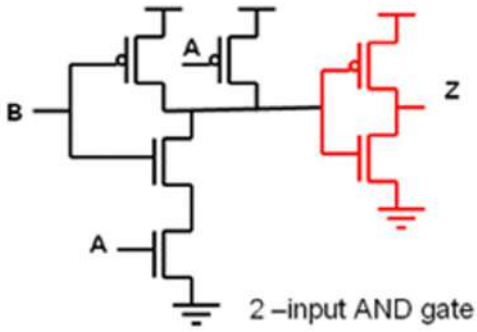
Result:



From the above graph we can see that the output is 0 when both A and B are 1 and 1 else where. Thus our layout works as a NAND gate.

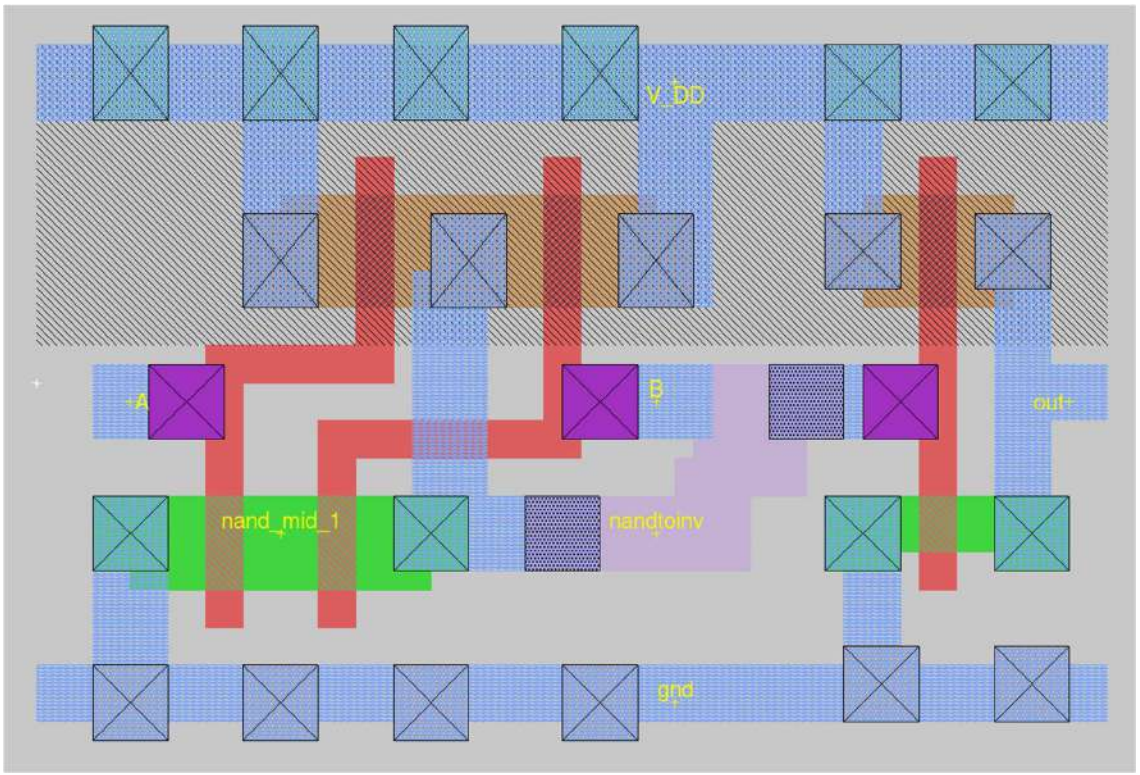
Design of AND Gate:

Circuit Diagram:



Width Analysis: The width analysis of both NAND and AND gates are similar because we just appended a CMOS_INVERTER to the NAND gate. The layout and analysis of the layout is show below.

Layout:



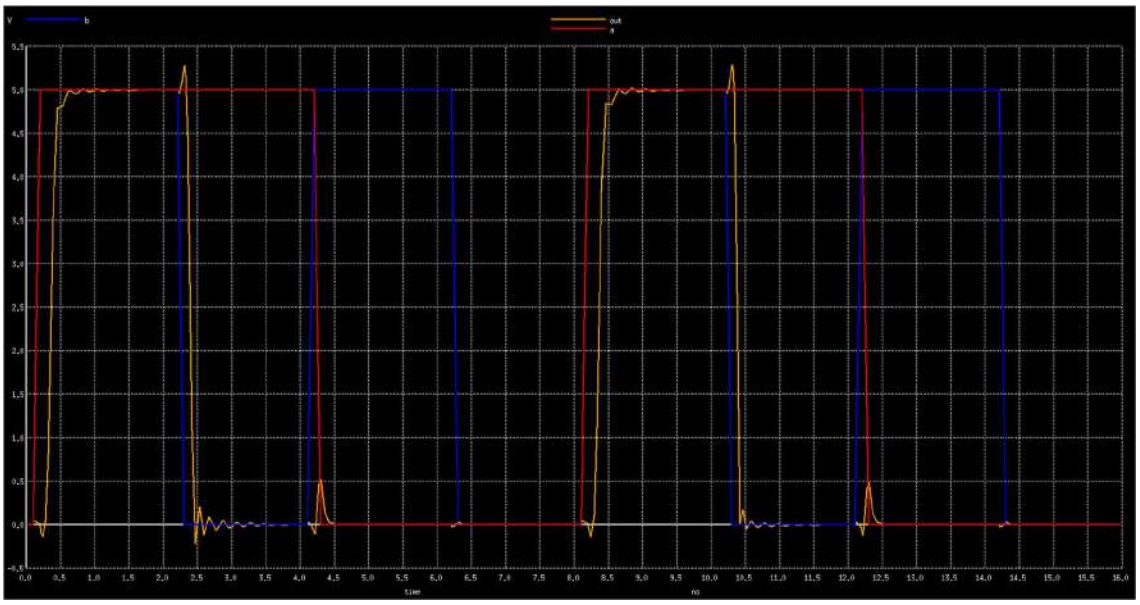
Spice Code Generated:

```
* SPICE3 file created from cmos_and_layout.ext - technology: scmos

.model pfet pmos level=3 version=3.3.0
.model nfet nmos level=3 version=3.3.0

.option scale=1u

M1000 nand_mid_1 A gnd Gnd nfet w=5 l=2
+  ad=20 pd=18 as=47 ps=40
M1001 out nandtoinv gnd Gnd nfet w=3 l=2
+  ad=22 pd=20 as=0 ps=0
M1002 out nandtoinv V_DD V_DD pfet w=6 l=2
+  ad=26 pd=22 as=94 ps=70
M1003 nandtoinv A V_DD V_DD pfet w=6 l=2
+  ad=48 pd=28 as=0 ps=0
M1004 nandtoinv B nand_mid_1 Gnd nfet w=5 l=2
+  ad=28 pd=22 as=0 ps=0
M1005 V_DD B nandtoinv V_DD pfet w=6 l=2
+  ad=0 pd=0 as=0 ps=0
C0 V_DD A 2.07fF
C1 gnd Gnd 6.06fF
C2 nandtoinv Gnd 8.41fF
```

```
C3 B Gnd 7.42fF
C4 A Gnd 5.26fF

V_A A gnd pulse(0 5 0.1n 0.1n 0.1n 4n 8n)
V_B B gnd pulse(0 5 0.1n 0.1n 0.1n 2n 4n)
v_dd V_DD gnd 5

.control
    tran 0.1n 16n
    setplot tran1
    plot A B out
.endc

.end
```

As written in the code we performed the transient analysis and plotted the graph.

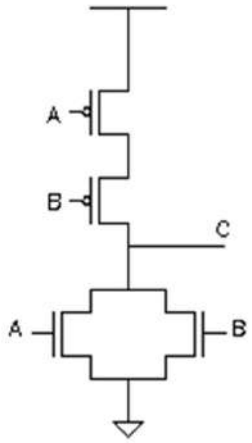
Result:



From the graphs we can observe that the out put is 1 only when both A and B are hight and 0 else where. Thus our layout works as a and gate.

Design of NOR Gate:

Circuit Diagram:

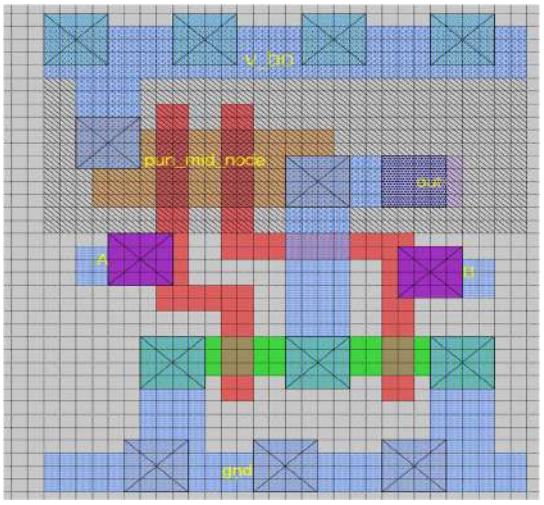


NOR

Width Analysis: In worst case both pmos are on in the PUN, so the resistance offered by each pmos should be R/2 ➔width=4W.

In worst case only 1 cmos is on in PDN, so the resistance offered by each nmos should be R➔width=W.

Layout:



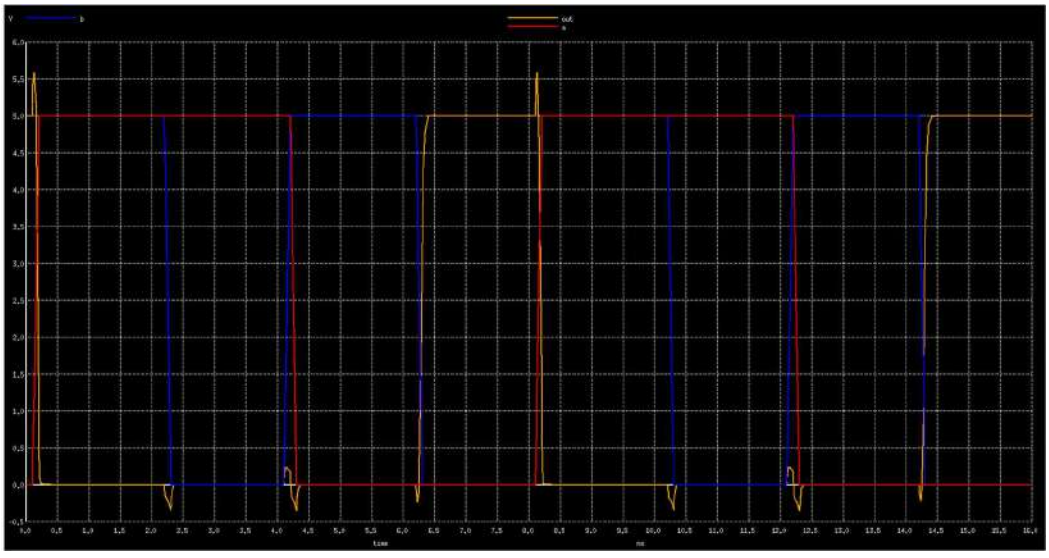
Spice Code Generated:

```
* SPICE3 file created from cmos_nor_layout.ext - technology: scmos


.model pfet pmos level=3 version=3.3.0
.model nfet nmos level=3 version=3.3.0

.option scale=1u
```

```
M1000 pun_mid_node A V_DD V_DD pfet w=6 l=2
+  ad=12 pd=16 as=31 ps=24
M1001 gnd B out Gnd nfet w=3 l=2
+  ad=38 pd=36 as=28 ps=24
M1002 out A gnd Gnd nfet w=3 l=2
+  ad=0 pd=0 as=0 ps=0
M1003 out B pun_mid_node V_DD pfet w=6 l=2
+  ad=34 pd=24 as=0 ps=0
C0 V_DD B 2.23fF
C1 gnd Gnd 4.23fF
C2 B Gnd 5.53fF
C3 A Gnd 4.66fF


V_A A gnd pulse(0 5 0.1n 0.1n 0.1n 4n 8n)
V_B B gnd pulse(0 5 0.1n 0.1n 0.1n 2n 4n)
v_dd V_DD gnd 5

.control
    tran 0.1n 16n
    setplot tran1
    plot A B out
.endc

.end
```

The code above is simulated in ngspice and the results are shown below.

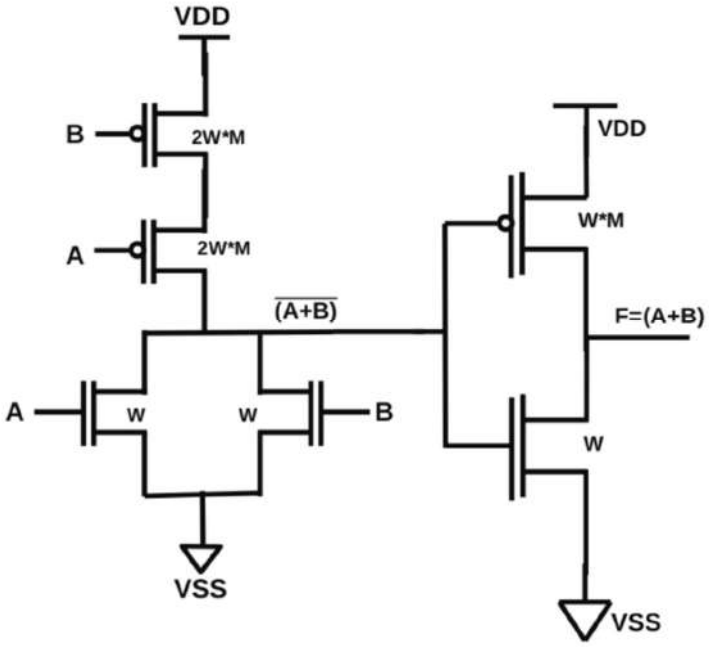
Results:



We can observe that the above graphs is similar to NOR. Thus our layout works.

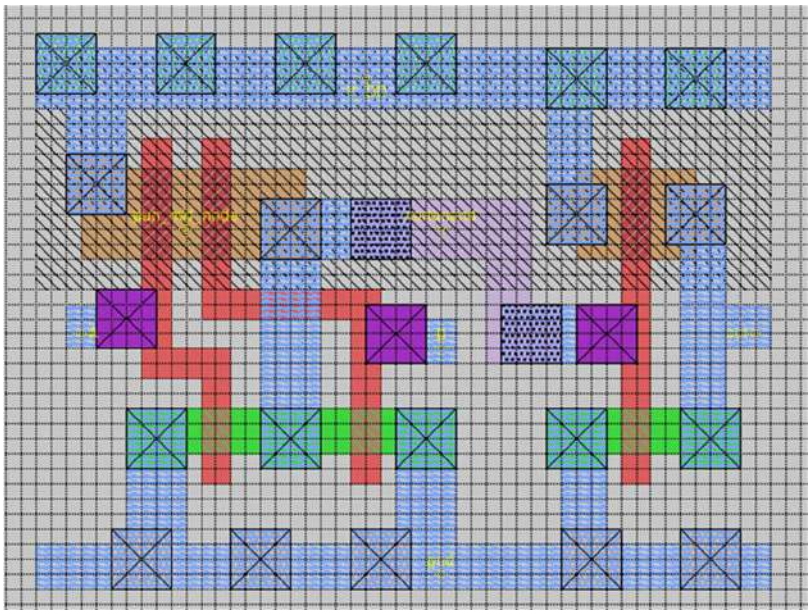
Design of OR Gate:

Circuit Diagram:



Width Analysis: Since we are connecting only inverter to the NOR gate so the worst case rise and fall times will be same if we keep the widths same as in NOR gate.

Layout:

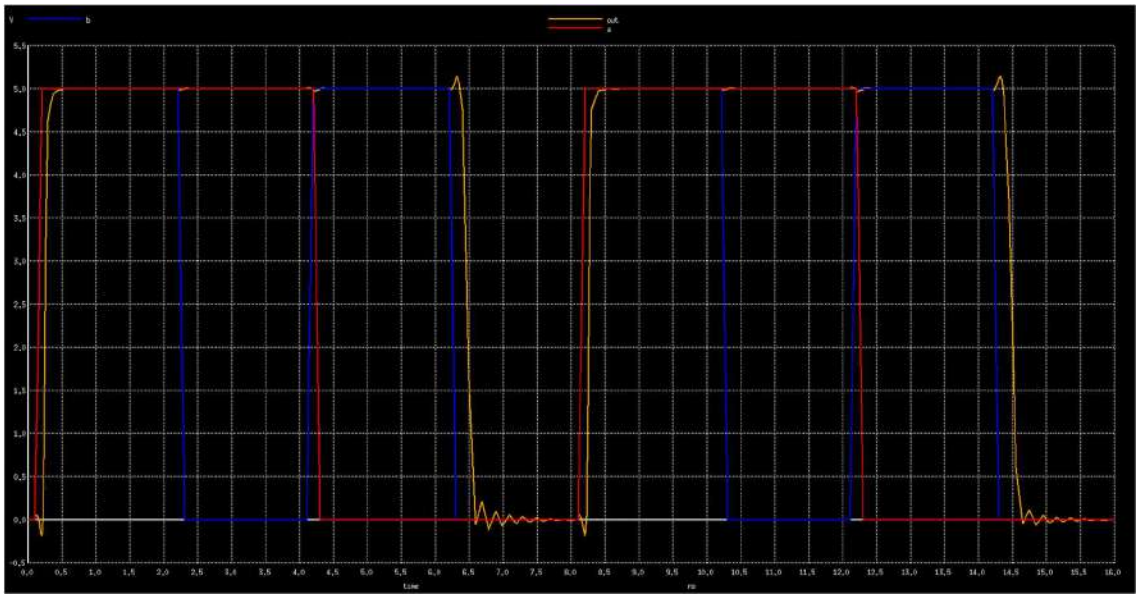


Spice Code Generated:

```
      * SPICE3 file created from cmos_or_layout.ext - technology: scmos


.model pfet pmos level=3 version=3.3.0
.model nfet nmos level=3 version=3.3.0

.option scale=1u

M1000 gnd B nortonand Gnd nfet w=3 l=2
+  ad=57 pd=54 as=28 ps=24
M1001 nortonand B pun_mid_node V_DD pfet w=6 l=2
+  ad=34 pd=24 as=12 ps=16
M1002 out nortonand gnd Gnd nfet w=3 l=2
+  ad=22 pd=20 as=0 ps=0
M1003 pun_mid_node A V_DD V_DD pfet w=6 l=2
+  ad=0 pd=0 as=57 ps=46
M1004 out nortonand V_DD V_DD pfet w=6 l=2
+  ad=26 pd=22 as=0 ps=0
M1005 nortonand A gnd Gnd nfet w=3 l=2
+  ad=0 pd=0 as=0 ps=0
C0 V_DD nortonand 3.66fF
C1 V_DD B 2.23fF
C2 gnd Gnd 6.34fF
C3 nortonand Gnd 6.01fF
C4 B Gnd 5.67fF
C5 A Gnd 4.66fF

V_A A gnd pulse(0 5 0.1n 0.1n 0.1n 4n 8n)
V_B B gnd pulse(0 5 0.1n 0.1n 0.1n 2n 4n)
v_dd V_DD gnd 5

.control
    tran 0.1n 16n
    setplot tran1
    plot A B out
.endc

.end
```

The graph of the above code is given below.

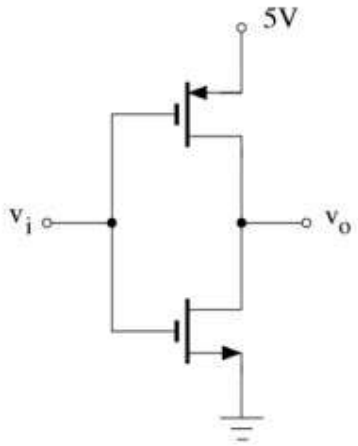
Results:



The above graph is similar to the characteristics of the OR gate so our layout works as a OR gate.

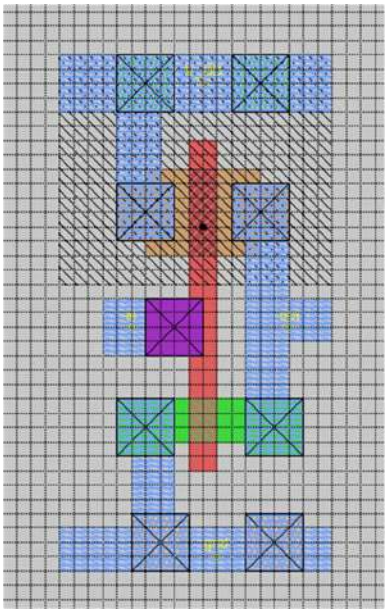
Design of Inverter:

Circuit Diagram:



Width Analysis: Since there is only one transistor in both PUN and PDN there for the width of nmos is W and width of pmos is 2W, since we assumed mobility of electrons is two times that of protons.

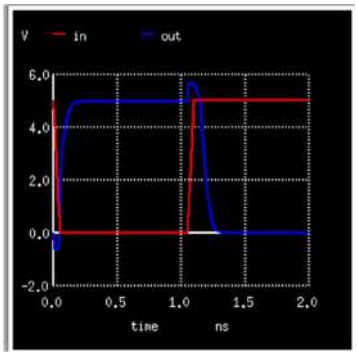
Layout:



Spice Code Generated:

```
      * SPICE3 file created from cmos_inv_layout.ext - technology: scmos


.option scale=1u

M1000 out in gnd Gnd nfet w=3 l=2
+  ad=22 pd=20 as=19 ps=18
M1001 out in V_DD V_DD pfet w=6 l=2
+  ad=26 pd=22 as=26 ps=22
C0 gnd Gnd 2.12fF
C1 in Gnd 4.00fF
```

Results:

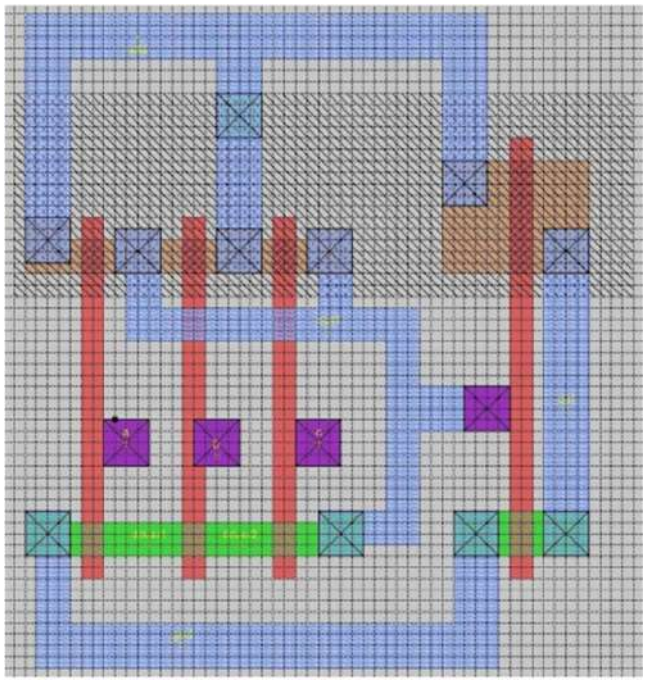


From the graphs we can see that our layout works as a inverter

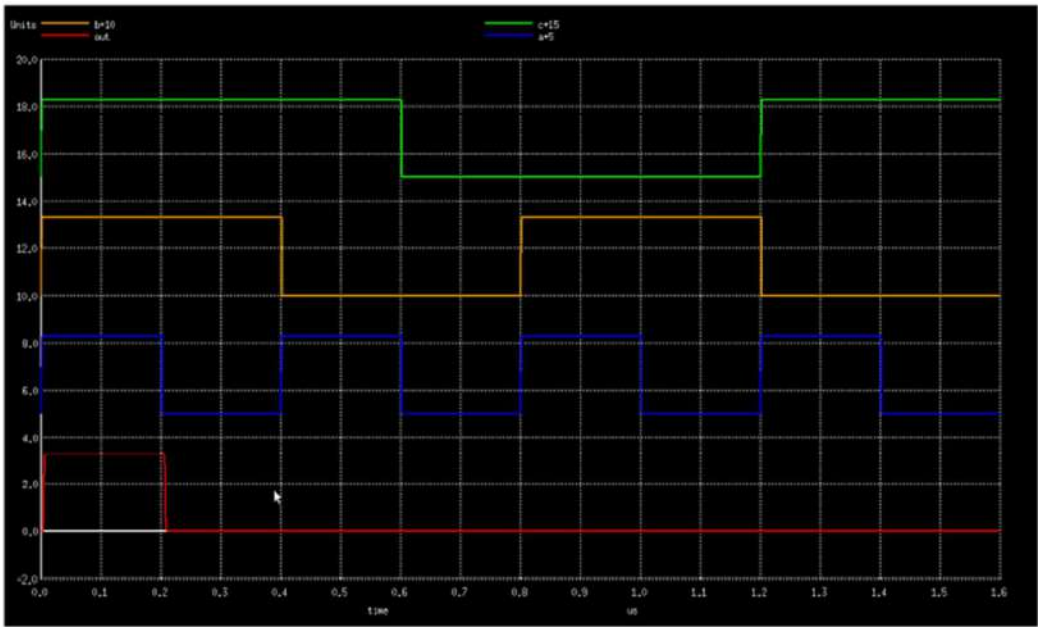
Design of 3input gates:

CMOS 3input NAND Gate:

Layout:

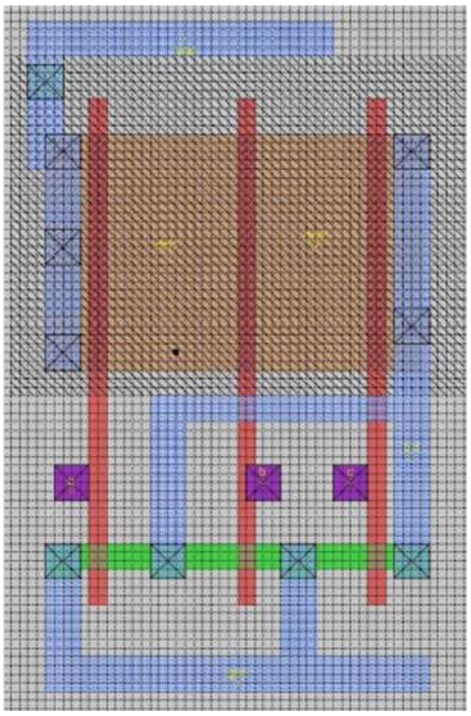


Graph:

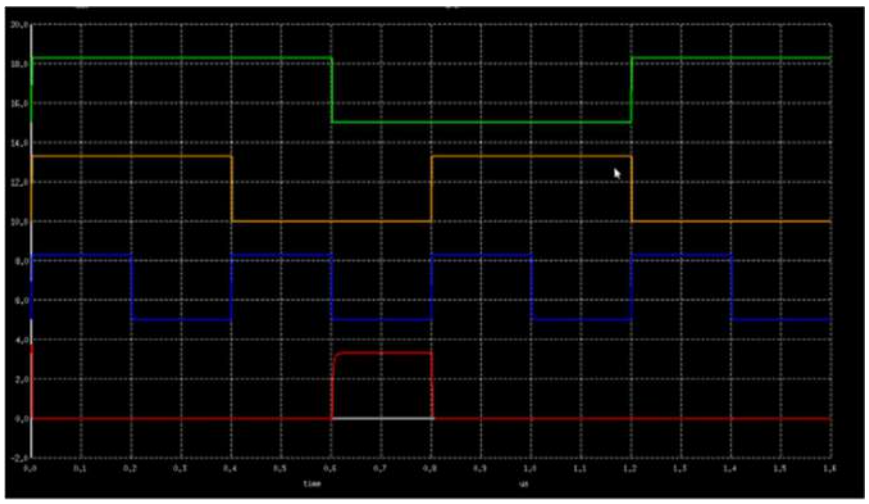


The Values of A, B, C and out added with a constant so that visualization of it is good.

CMOS 3input NOR Layout:

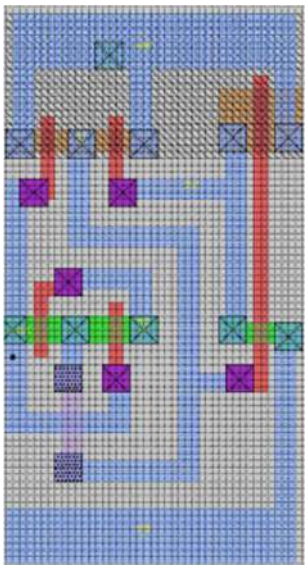


Graph:

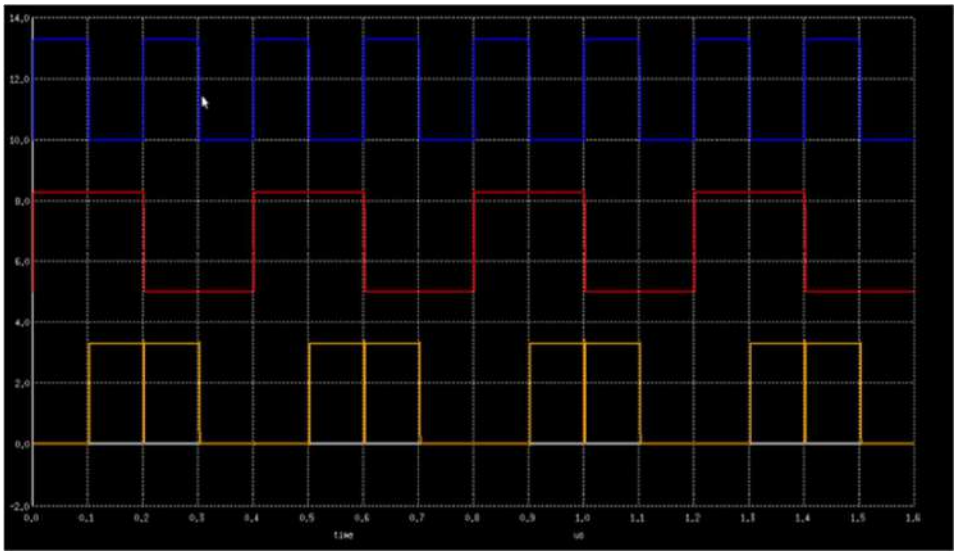


The Values of A, B, C and out added with a constant so that visualization of it is good.

Design of 3 input XOR Gate:



Graph:



The Values of A, B, C and out added with a constant so that visualization of it is good.

Inference of experiment 7:

- In a standard cell library restricted number of metals are used for intra connection, this can be observed from the layout, I used only metal1 and metal2 for intra connections.
- All higher order metals are used for inter-cell connection while making a logic-circuit or an IC

- The height of each cell is fixed in standard cell library.
- Width can be varied in standard cell library.
- Ext2spice can be used for extracting the spice file from the layout.
- Ext2sim can be used for extracting the .sim file and the switch level simulation can be done in the IRSim.
- All the outputs of ngspice, IRsim. Netgen are favourable to us.

********Thank You********