Prof. Cristina Silvano	ACA2022_EXAM_FORM1 Data: 29/06/2022

ACA2022_FORM1_29June2022_SILVANO

ACA Course -- Prof. SILVANO

FORM1 is composed of 15 QUESTIONS to get UP TO 21 POINTS

Duration is 35 minutes!

IMPORTANT: What to do before leaving MS FORM1:

1. **Please click on:** "Inviami una conferma tramite posta elettronica delle risposte" (Send me a confirmation by email of the answers). This is **fundamental** to get an email with subject: **"My responses".** Open the email and click on the link to **VIEW YOUR RESPONSES.**

2. **Please click on SUBMIT** (Click on **INVIA**) and you will get the message: **"Your answer has been sent".** Points will be assigned **manually** to **FORM1**. Therefore, the view of your results is **not** immediate: it will be enabled by prof. Silvano **after** results publication phase.

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Question 1 (format Multiple Choice – Single answer)

Let's consider a directory-based protocol for a distributed shared memory system with 4 Nodes (N0, N1, N2, N3) where we consider the block B1 in the directory of N1:
Directory N1 Block B1 | State: Shared | Sharer Bits: 1001
Which one was the request message sent for the block B1 to become:
Directory N1 Block B1 | State: Modified | Sharer Bits: 1000

(SINGLE ANSWER)
1 point

Answer 1: Write Hit B1 sent from N0 to N1 **(TRUE)**
Answer 2: Write Miss B1 sent from N0 to N1
Answer 3: Read Hit B1 sent from N0 to N1
Answer 4: Read Miss B1 sent from N1 to N0
Answer 5: Write Miss B1 sent from N1 to N0

Question 2 (format Multiple Choice – Single answer)
Let's consider a directory-based protocol for a distributed shared memory system with 4 Nodes (N0, N1, N2, N3) where we consider the block B0 in the directory of N0:
Directory N0 Block B0 | State: Shared | Sharer Bits: 0100 |

During a Read Miss on B0 from N0, please indicate which are the home node, the local node and the remote node(s):

(SINGLE ANSWER)
1 point

Answer 1: N0 home node, N1 local node; N3 remote node.
Answer 2: N0 home node; N0 local node; N1 remote node. **(TRUE)**
Answer 3: N1 home node; N1 local node; N1 remote node.
Answer 4: N1 home node; N0 local node; N1 remote node.

Question 3 (format Multiple Choice – Single answer)

Let's consider the following code sequence executed by the 5 stage MIPS optimized pipeline with all forwarding paths:

```
I1:         LW $s1, 0($r1)
I2:         ADD $s1, $s1, $S1
I3:         ADDI $s2, $s1, C1
I4:         SW $s2, 8($r1)
```

Which one of the following answers is true?
(SINGLE ANSWER)
1 point

Answer 1: No stalls needed because all hazards are solved by forwarding paths.
Answer 2: One stall in ID stage of I2 & MEM/EX forwarding path for RAW $s1. **(TRUE)**
Answer 3: One stall in ID stage of I4 & EX/MEM forwarding path for $s2.

Question 4 (format Multiple Choice – Single answer)

Let's consider a 5-issue processor that can manage up to 5 simultaneous threads.

What are the values of the ideal CPI and the ideal per-thread CPI?

(SINGLE ANSWER)
1 point

Answer 1: Ideal CPI = 5 & Ideal per-thread CPI = 1
Answer 2: Ideal CPI = 1 & Ideal per-thread CPI =0.2
Answer 3: Ideal CPI = 0.20 & Ideal per-thread CPI = 1 **(TRUE)**
Answer 4: Ideal CPI = 0.25 & Ideal per-thread CPI = 5
Answer 5: Ideal CPI = 5 & Ideal per-thread CPI = 0.20

Question 5 (format Single Answers)

In which type of cache coherence protocol we can say that:
In a shared memory multiprocessor, the delay between writing a cache block by one processor and reading the new value by another processor requires less time.

(SINGLE ANSWER)
1 point

Answer 1: Write update protocol **TRUE**
Answer 2: Write invalidate protocol

Question 6 (format Single Answers)

In a shared memory multiprocessor, multiple writes to the same data with no intervening reads require multiple data broadcast in which type of cache coherence protocol?

(SINGLE ANSWER)
1 point

Answer 1: Write update protocol **TRUE**
Answer 2: Write invalidate protocol

Question 7 (format Multiple Choice – Single answer)

Let's consider the following 5 stage MIPS optimized pipeline execution:

```
I1:| IF | ID | EX  | MEM | WB  |
I2:     | IF | ID  | EX  | MEM | WB|   MEM >> MEM forwarding path used
```

Which pair of instructions are executed?

(SINGLE ANSWER)
1 point

Answer 1: `I1: LW $t0, 0($t2): I2: SW $t1, 0 ($t0)`
Answer 2: `I1: LW $t0, 0($t2): I2: SW $t0, 0 ($t2)` **(TRUE)**
Answer 3: `I1: LW $t0, 0($t2): I2: SW $t2, 0 ($t2)`

Question 8 (format true/false)

A (2,2) Correlating Branch Predictor has a double number of prediction bits with respect to a (2,1) Correlating Branch Predictor with the same number of entries in each BHT.

(TRUE/FALSE)
1 point

Answer 1: **T (TRUE)**

Question 9 (format Multiple Choice – Single answer)

Let's consider a (2,1) Correlating Branch Predictor with 4K total entries.

How many Branch History Tables?
How many entries per BHT?
How many bits per entry?

(SINGLE ANSWER)
1 point

Answer 1: 4 BHTs | 1K entries | 1-bit per entry **(TRUE)**
Answer 2: 2 BHTs | 2K entries | 1-bit per entry
Answer 3: 2 BHTs | 2K entries | 2-bit per entry
Answer 4: 1 BHT | 4K entries | 1-bit per entry

Question 10 (format Multiple Choice – Multiple answers)

Which of the following cache improvements are effective in reducing the ***miss penalty?***
(Multiple answers)
2 points

Answer 1: Pseudo-associativity and Way prediction.
Answer 2: Early restart and critical word first. **(TRUE)**
Answer 3: Giving higher priority to read misses over write misses. **(TRUE)**
Answer 4: Introducing a second level cache. **(TRUE)**

Feedback:
Adopting pseudo-associativity and way prediction are optimization techniques to reduce the miss rate. The other two answers instead are reducing the miss penalty by (1) the introduction of early restart and critical word first techniques are used to do not wait for the full block and (2) by giving priority to read misses over writes, they are used to serve the read misses before the write misses. See slides on L11B: Memory_Hierarchy_Advanced Concepts.

Question 11 (format Multiple Answers)

For multithreading processors, which of the following statements are true?

(MULTIPLE ANSWERS)
2 points

Answer 1: Multiple processors communicate through message passing protocols.
Answer 2: Multiple threads can share the functional units of a single processor. **TRUE**
Answer 3: The processor must duplicate the independent state of each thread by a separate copy of the register set. **TRUE**
Answer 4: The processor must keep independent threads by a separate Program Counter for each thread. **TRUE**

Question 12 (format Multiple answers)

In a shared memory multiprocessor, which of the following statements are true?

(Multiple answers)
2 points

Answer 1: Multiple processors communicate through send/receive message passing protocols.

Answer 2: Multiple processors communicate through shared memory variables and data writes generate coherence problems among multiple caches. **TRUE**

Answer 3: Coherent caches provide multiple copies of shared data to reduce both access latency and read contention. **TRUE**

Answer 4: The shared memory can be either centralized on a single node or distributed over the nodes. **TRUE**

Question 13 (format Multiple Choice – Single answer)

Let's consider the following code executed by a Vector Processor with:

- *Vector Register File composed of 8 vectors of 32 elements per 64 bits/element;*
- *Scalar FP Register File composed of 32 registers of 64 bits;*
- *One Load/Store Vector Unit **without operation chaining** and memory bandwidth 64 bits;*
- *One ALU Vector Unit **without operation chaining.***

```
L.V V1, RX              # load vector from memory address RX into V1
ADDVS.D V2, V1, F0      # FP add vector V1 to scalar F0
MULVV.D V3, V1, V2      # FP Multiply vectors V1 and V2
```

How many convoys? How many clock cycles to execute the code?
(SINGLE ANSWER)
2 points

Answer 1: 3 convoys; 96 clock cycles **(TRUE)**
Answer 2: 2 convoys; 64 clock cycles
Answer 3: 8 convoys; 32 clock cycles
Answer 4: 1 convoy; 32 clock cycles

Question 14 (format Multiple Choice – Single answer)

Let us consider to apply a processor optimization resulting ten time faster on computation than the original mode of execution.
What is the fraction of computation needed to achieve an overall speedup of 2?

(SINGLE ANSWER)
2 points

Answer 1: 50%
Answer 2: 55% (TRUE)
Answer 3: 25%
Answer 4: 75%
Answer 5: 20%

Feedback:

1. *To get an overall speedup of 2, we need to apply the Amdahl's law as follows:*
   $1 / [(1-F_V) + (F_V / 10)] = 2 => 10 / (10 – 9 F_V) = 2 => 18 F_V = 10$
   $=> F_V = 10/ 18 = 0.55 =>$ ***$F_V = 55\%$***

Question 15 (format Multiple Choice – Multiple answers)

Let's consider the following loop code executed by a dynamic scheduled processor:

```
S1: LOOP: LD.D $FP1, A($R1)
S2:       LD.D $FP2, B($R1)
S3:       MUL.D $FP1, $FP1, $FP1
S4:       ADD.D $FP2, $FP1, $FP2
S5:       SD.D $FP1, C($R1)
S6:       SD.D $FP2, D($R1)
S7:       ADDI $R1, $R1, 4
S8:       BNE $R1, $R2, LOOP
```

Assuming to consider only the intra-iteration dependencies: Where are the ***OUTPUT DEPENDENCIES*** *that can generate the WAW hazards?*

(MULTIPLE ANSWERS)
2 points

Answer 1: Between S4 and S2 on $FP2; **(TRUE)**
Answer 2: Between S7 and S6 on $R1;
Answer 3: Between S3 and S1 on $FP1; **(TRUE)**
Answer 4: Between S5 and S3 on $FP1;
Answer 5: Between S6 and S4 on $FP2;