

Course on: “Advanced Computer Architectures”

Register Renaming



Prof. Cristina Silvano
Politecnico di Milano
`cristina.silvano@polimi.it`

Loop Unrolling and Register Renaming

Loop Unrolling and Register Renaming

- To avoid **WAR** and **WAW** hazards:
- Tomasulo provides ***Implicit Register Renaming***
 - Register Renaming provided by Reservation Stations
- *Now we introduce:*
 - Compiler transformation called **Loop Unrolling** combined with ***Register Renaming*** *by using more registers specified in the ISA*

Tomasulo Loop Example: Code

```
Loop:    LD      F0    0    R1
         MULTD   F4    F0   F2
         SD      F4    0    R1
         SUBI    R1    R1   #8
         BNEZ    R1    Loop
```

5 instructions per iteration

- Let's consider a simple loop example
- Assume branch predicted as taken
- Are there any dependency?

Tomasulo Loop Example: Code

```
LD      F0      0      R1
MULTD   F4      F0     F2  # RAW F0
SD      F4      0      R1  # RAW F4
SUBI    R1      R1     #8
BNEZ    R1      Loop    # RAW R1; WAR R1
                        Pred. taken
```

Tomasulo Loop Example: Code

Let's consider the first two iterations:

LD	F0	0	R1	
MULTD	F4	F0	F2	# RAW F0
SD	F4	0	R1	# RAW F4
SUBI	R1	R1	#8	
BNEZ	R1	Loop		# RAW R1; WAR F1; Pred. taken
LD	F0	0	R1	# WAW F0
MULTD	F4	F0	F2	# RAW F0 WAW F4
SD	F4	0	R1	# RAW F4
SUBI	R1	R1	#8	
BNEZ	R1	Loop		# RAW R1; WAR R1; Pred. taken

Tomasulo Loop Example: Code

```
Loop:    LD      F0    0    R1
         MULTD   F4    F0   F2
         SD      F4    0    R1
         SUBI    R1    R1   #8
         BNEZ    R1    Loop
```

5 instructions per iteration

- Assume branch predicted as taken
- ***We unroll the loop 4 times by using Register Renaming for F0 and F4 to avoid the WAW hazards among the iterations.***

Unrolled Loop (unrolling factor 4) + Reg. Renaming

1	Loop: LD	F0, 0(R1)	}
2	MULTD	F4, F0, F2	
3	SD	F4, 0(R1)	
4	LD	F6, -8(R1)	}
5	MULTD	F8, F6, F2	
6	SD	F8, -8(R1)	
7	LD	F10, -16(R1)	}
8	MULTD	F12, F10, F2	
9	SD	F12, -16(R1)	
10	LD	F14, -24(R1)	}
11	MULTD	F16, F14, F2	
12	SD	F16, -24(R1)	
13	SUBI	R1, R1, #32	
14	BNEZ	R1, LOOP	

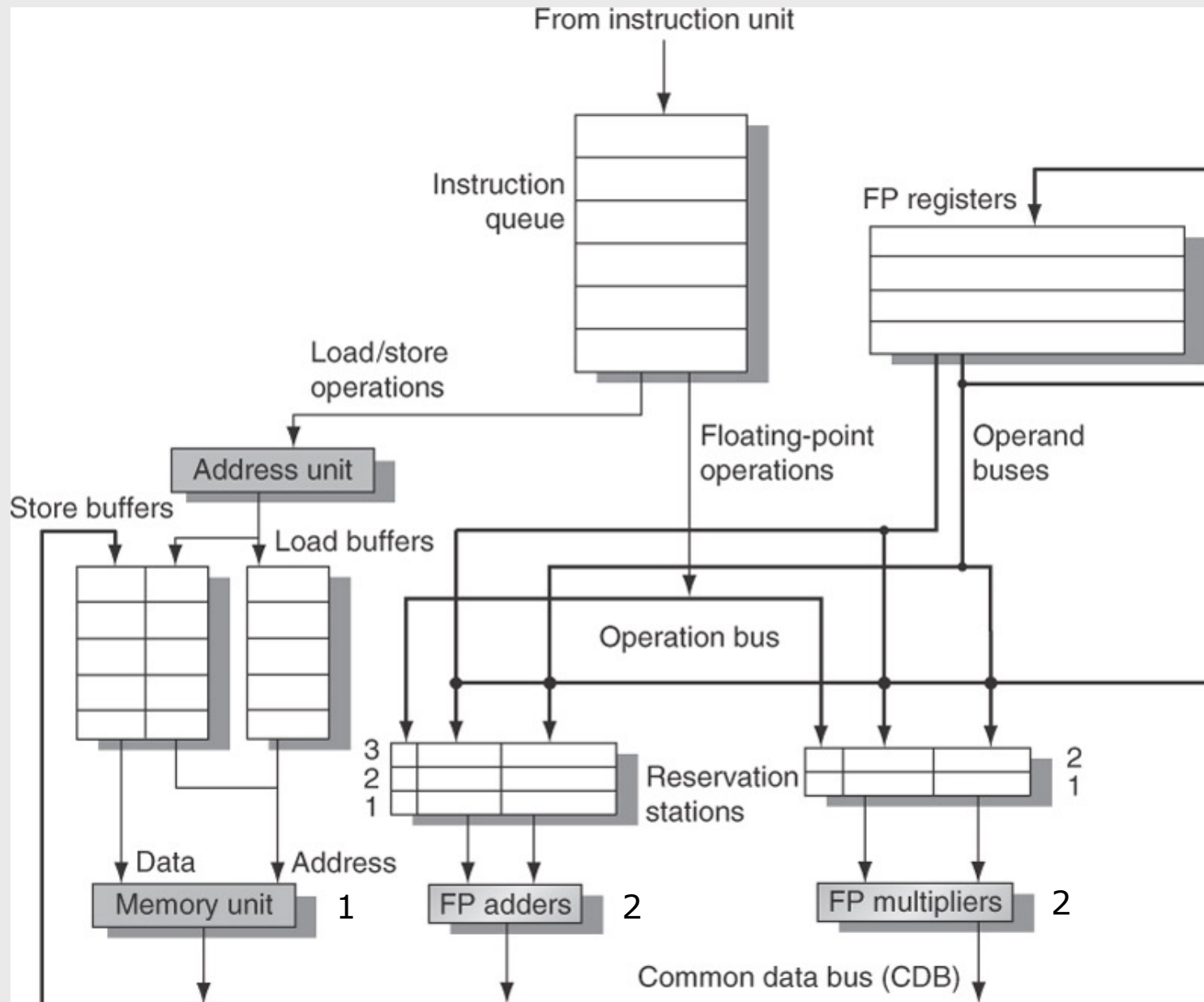
More instructions (14) per 4 iterations => 3.5 instr. per iteration
Used more FP registers in the unrolled loop code!

Unrolled Loop (unrolling factor 4) + Reg. Renaming + Code Rescheduling to minimize RAW stalls

```
1  Loop: LD      F0, 0(R1)
2          LD      F6, -8(R1)
3          LD      F10, -16(R1)
4          LD      F14, -24(R1)
5          MULTD   F4, F0, F2
6          MULTD   F8, F6, F2
7          MULTD   F12, F10, F2
8          MULTD   F16, F14, F2
9          SD      F4, 0(R1)
10         SD      F8, -8(R1)
11         SD      F12, -16(R1)
12         SUBI    R1, R1, #32
13         BNEZ    R1, LOOP
14         SD F16, 8(R1) # branch delay slot (8-32 = -24)
```

Tomasulo and Implicit Register Renaming

Recap on Tomasulo Architecture



How can Tomasulo overlap iterations of loops?

- **Implicit register renaming provided by Reservation Stations** to buffer operands of instructions:
 - Replace register names from original code with *dynamic "pointers" to Reservation Stations*
=> to eliminate WAR and WAW hazards.
- Multiple loop iterations use different Reservation Stations for registers **=> dynamic loop unrolling** without changing the original code.
- Effectively increased the size of Register File by using Reservation Stations.
- **Crucial:** We need multiple FP units to issue multiple iterations **by using branch prediction!**
 - We enable instruction issue to advance past branch control flow operations.

Tomasulo Loop Example: Code

```
Loop:    LD      F0    0    R1
         MULTD   F4    F0   F2
         SD      F4    0    R1
         SUBI    R1    R1   #8
         BNEZ    R1    Loop
```

5 instructions per iteration

- Assume first load takes **8 clocks** (due to a cache miss), second load takes **1 clock** (hit)
- Assume FP multiply takes **4 clocks** latency
- Assume branch predicted as **taken**
- To be clear, we will show only clocks for SUBI, BNEZ

Tomasulo Loop Example: Code

Let's consider the first two iterations:

LD	F0	0	R1	
MULTD	F4	F0	F2	# RAW F0
SD	F4	0	R1	# RAW F4
SUBI	R1	R1	#8	
BNEZ	R1	Loop		# RAW R1; WAR F1; Pred. taken
LD	F0	0	R1	# WAW F0
MULTD	F4	F0	F2	# RAW F0 WAW F4
SD	F4	0	R1	# RAW F4
SUBI	R1	R1	#8	
BNEZ	R1	Loop		# RAW R1; WAR R1; Pred. taken

Loop Example

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue	Comp	Result
1	LD	F0	0	R1			
1	MULTD	F4	F0	F2			
1	SD	F4	0	R1			
2	LD	F0	0	R1			
2	MULTD	F4	F0	F2			
2	SD	F4	0	R1			

Exec Write

Load & Store Buffers:

	Busy	Addr	Fu
Load1	No		
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

Reservation Stations:

Time	Name	Busy	Op	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	Code:
	Add1	No						LD
	Add2	No						MULTD
	Add3	No						SD
	Mult1	No						SUBI
	Mult2	No						BNEZ

Register result status

Clock	R1		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
0	80	<i>Fu</i>									

Rename Table

Loop Example Cycle 1

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	
1	SD	F4	0	R1	
2	LD	F0	0	R1	
2	MULTD	F4	F0	F2	
2	SD	F4	0	R1	

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

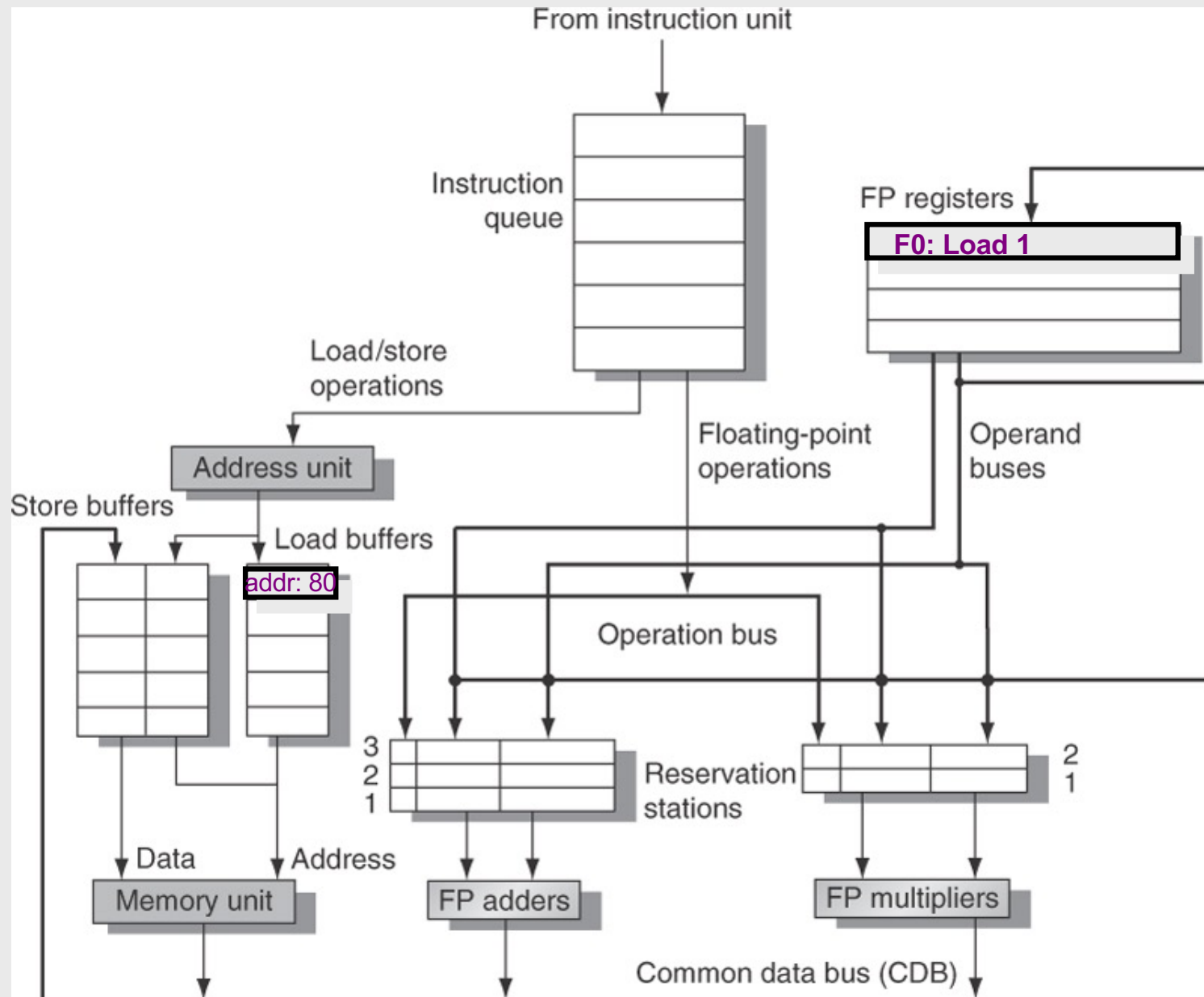
Reservation Stations:

					<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	<i>Code:</i>
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
	Mult1	No						R1
	Mult2	No						F2
								SD
								F4
								0
								R1
								SUBI
								R1
								R1
								#8
								BNEZ
								Loop

Register result status

<i>Clock</i>	<i>R1</i>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
1	80	<i>Fu</i>	Load1								

What does this mean physically?



Loop Example Cycle 2

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	2
1	SD	F4	0	R1	
2	LD	F0	0	R1	
2	MULTD	F4	F0	F2	
2	SD	F4	0	R1	

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
	Add1	No					
	Add2	No					
	Add3	No					
	Mult1	Yes	Multd			R(F2)	Load1
	Mult2	No					

Code:

LD	F0	0	R1
MULTD	F4	F0	F2
SD	F4	0	R1
SUBI	R1	R1	#8
BNEZ	R1	Loop	

Register result status

<i>Clock</i>	<i>R1</i>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
2	80	<i>Fu</i>	Load1		Mult1						

Loop Example Cycle 3

Instruction status:

ITER	Instruction	<i>j</i>	<i>k</i>	Issue	CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	2
1	SD	F4	0	R1	3
2	LD	F0	0	R1	
2	MULTD	F4	F0	F2	
2	SD	F4	0	R1	

Exec Write

Load & Store Buffers:

	Busy	Addr	Fu
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations:

Time	Name	Busy	Op	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	Code:
	Add1	No						LD
	Add2	No						MULTD
	Add3	No						SD
	Mult1	Yes	Multd		R(F2)	Load1		SUBI
	Mult2	No						BNEZ

Register result status

Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30
3	80	Fu	Load1	Mult1						

Implicit renaming sets up "DataFlow" graph

Loop Example Cycle 3

Instruction status:

ITER	Instruction	<i>j</i>	<i>k</i>	Issue	Comp	Result
1	LD	F0	0	R1	1	
1	MULTD	F4	F0	F2	2	
1	SD	F4	0	R1	3	
2	LD	F0	0	R1		
2	MULTD	F4	F0	F2		
2	SD	F4	0	R1		

Exec Write

Load & Store Buffers:

	Busy	Addr	Fu
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations:

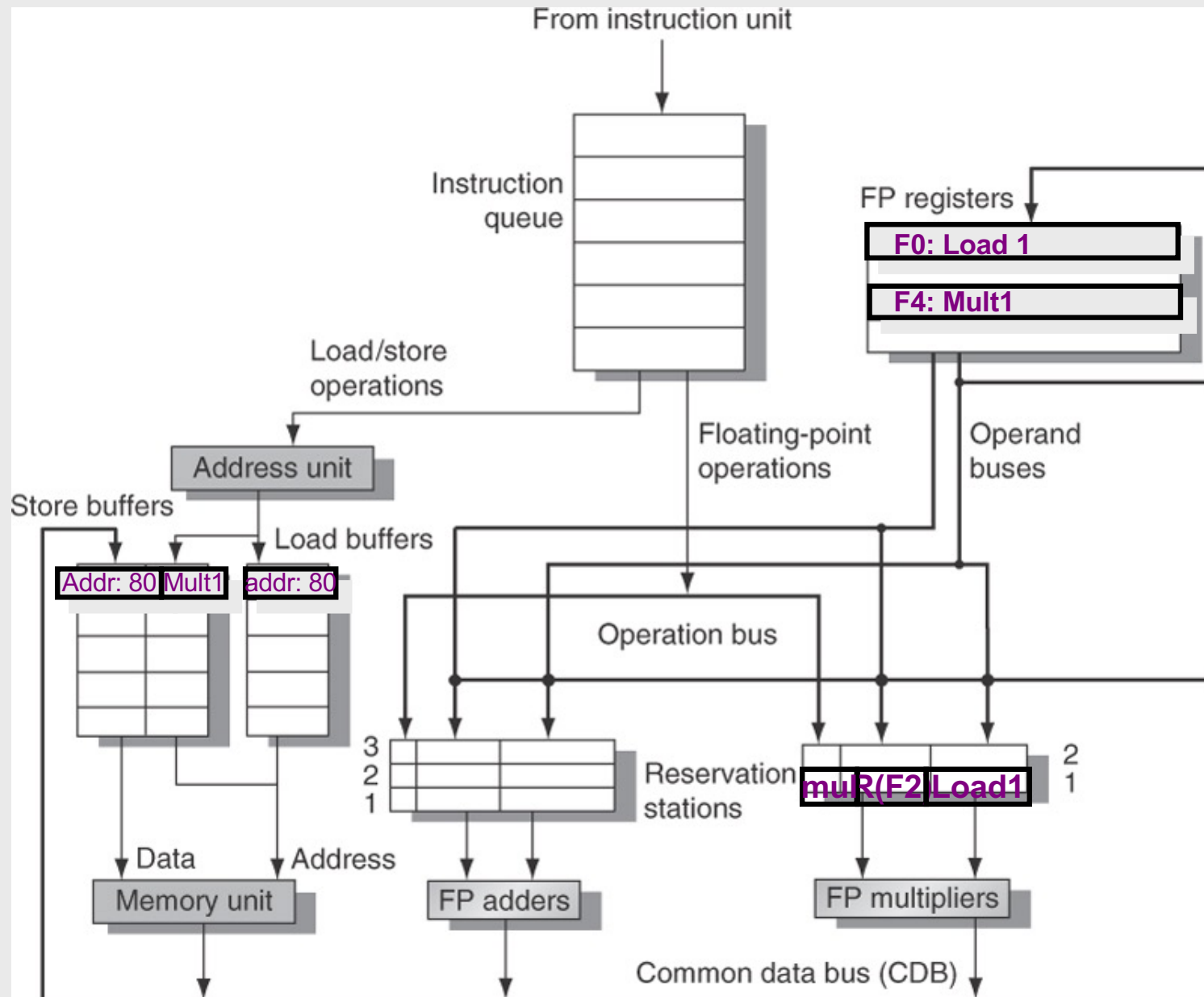
Time	Name	Busy	Op	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	Code:
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
	Mult1	Yes	Multd		R(F2)	Load1		R1
	Mult2	No						F2
								SD
								F4
								0
								R1
								#8
								BNEZ
								R1
								Loop

Register result status

Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30
3	80	Fu	Load1	Mult1						

Implicit renaming sets up "DataFlow" graph

What does this mean physically?



Loop Example Cycle 4

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	2
1	SD	F4	0	R1	3
2	LD	F0	0	R1	
2	MULTD	F4	F0	F2	
2	SD	F4	0	R1	

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
	Add1	No					
	Add2	No					
	Add3	No					
	Mult1	Yes	Multd			R(F2)	Load1
	Mult2	No					

Code:

LD	F0	0	R1
MULTD	F4	F0	F2
SD	F4	0	R1
SUBI	R1	R1	#8
BNEZ	R1	Loop	

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
4	80	<i>Fu</i>	Load1	Mult1						

Dispatching SUBI Instruction

Loop Example Cycle 5

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	2
1	SD	F4	0	R1	3
2	LD	F0	0	R1	
2	MULTD	F4	F0	F2	
2	SD	F4	0	R1	

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	No		
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations:

					<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	<i>Code:</i>
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
	Mult1	Yes	Multd					R1
	Mult2	No						#8
								R(F2) Load1
								SUBI
								R1
								R1
								Loop

Register result status

<i>Clock</i>	<i>R1</i>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
5	72	<i>Fu</i>	Load1		Mult1						

Dispatching BNEZ instruction

Loop Example Cycle 6

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	2
1	SD	F4	0	R1	3
2	LD	F0	0	R1	6
2	MULTD	F4	F0	F2	
2	SD	F4	0	R1	

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	Yes	72	
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
	Add1	No					
	Add2	No					
	Add3	No					
	Mult1	Yes	Multd			R(F2)	Load1
	Mult2	No					

Code:

LD	F0	0	R1
MULTD	F4	F0	F2
SD	F4	0	R1
SUBI	R1	R1	#8
BNEZ	R1	Loop	

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
6	72	<i>Fu</i>	Load2	Mult1						

Notice: F0 does not see Load1 from location 80 (**WAW on F0 solved!**)

Loop Example Cycle 7

Instruction status:

ITER	Instruction	j	k	Issue	Comp	Result
1	LD	F0	0	R1	1	
1	MULTD	F4	F0	F2	2	
1	SD	F4	0	R1	3	
2	LD	F0	0	R1	6	
2	MULTD	F4	F0	F2	7	
2	SD	F4	0	R1		

Exec Write

Load & Store Buffers:

	Busy	Addr	Fu
Load1	Yes	80	
Load2	Yes	72	
Load3	No		
Store1	Yes	80	Mult1
Store2	No		
Store3	No		

Reservation Stations:

Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:
	Add1	No						LD
	Add2	No						MULTD
	Add3	No						SD
	Mult1	Yes	Multd		R(F2)	Load1		SUBI
	Mult2	Yes	Multd		R(F2)	Load2		BNEZ

Register result status

Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30
7	72	Fu	Load2	Mult2						

Register File completely detached from iteration 1
(WAW on F0 and WAW on F4 solved!)

Loop Example Cycle 8

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	Issue CompResult
1	LD	F0	0	R1	1
1	MULTD	F4	F0	F2	2
1	SD	F4	0	R1	3
2	LD	F0	0	R1	6
2	MULTD	F4	F0	F2	7
2	SD	F4	0	R1	8

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	Yes	72	
Load3	No		
Store1	Yes	80	Mult1
Store2	Yes	72	Mult2
Store3	No		

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
	Add1	No					
	Add2	No					
	Add3	No					
	Mult1	Yes	Multd		R(F2)	Load1	
	Mult2	Yes	Multd		R(F2)	Load2	

Code:

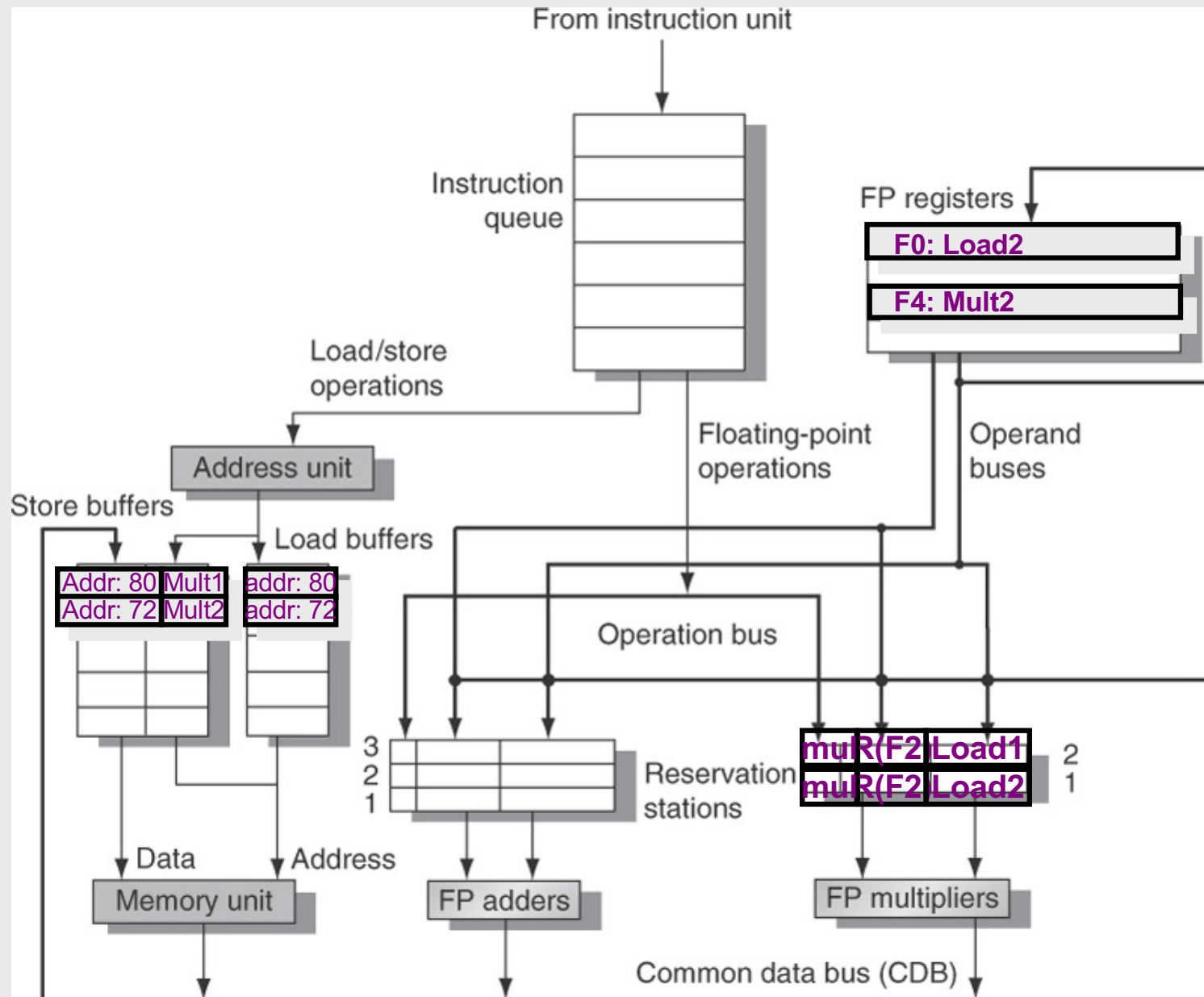
LD	F0	0	R1
MULTD	F4	F0	F2
SD	F4	0	R1
SUBI	R1	R1	#8
BNEZ	R1	Loop	

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
8	72	<i>Fu</i>	Load2	Mult2						

First and second iteration completely overlapped because WAW on F0 and WAW on F4 have been solved!

What does this mean physically?



Loop Example Cycle 9

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	<i>Issue CompResult</i>	
1	LD	F0	0	R1	1	9
1	MULTD	F4	F0	F2	2	
1	SD	F4	0	R1	3	
2	LD	F0	0	R1	6	
2	MULTD	F4	F0	F2	7	
2	SD	F4	0	R1	8	

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	Yes	80	
Load2	Yes	72	
Load3	No		
Store1	Yes	80	Mult1
Store2	Yes	72	Mult2
Store3	No		

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>	
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>
	Add1	No					
	Add2	No					
	Add3	No					
	Mult1	Yes	Multd		R(F2)	Load1	
	Mult2	Yes	Multd		R(F2)	Load2	

Code:

LD	F0	0	R1
MULTD	F4	F0	F2
SD	F4	0	R1
SUBI	R1	R1	#8
BNEZ	R1	Loop	

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
9	72	<i>Fu</i>	Load2	Mult2						

Load1 completing (after 8 cycles due to cache miss): who is waiting?
 Dispatching 2nd SUBI; Load2 started execution in the Memory Unit.

Loop Example Cycle 11

Instruction status:

					<i>Exec Write</i>			<i>Load & Store Buffers:</i>		
<i>ITER</i>	<i>Instruction</i>	<i>j</i>	<i>k</i>		<i>Issue</i>	<i>Comp</i>	<i>Result</i>	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
1	LD	F0	0	R1	1	9	10	Load1	No	
1	MULTD	F4	F0	F2	2			Load2	No	
1	SD	F4	0	R1	3			Load3	Yes	64
2	LD	F0	0	R1	6	10	11	Store1	Yes	80
2	MULTD	F4	F0	F2	7			Store2	Yes	72
2	SD	F4	0	R1	8			Store3	No	

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>				
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	<i>Code:</i>		
	Add1	No						LD	F0	0
	Add2	No						MULTD	F4	F0
	Add3	No						SD	F4	0
3	Mult1	Yes	Multd	M[80]	R(F2)			SUBI	R1	R1
4	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
11	64	<i>Fu</i>	Load3			Mult2				

Load 2 writing result M[72] in CDB for Mult2 to start execution (We assume to have 2 Multiply FP units)

Next load at third iteration is issued at C11 in Load3

Loop Example Cycle 12

Instruction status:

ITER	Instruction		<i>j</i>	<i>k</i>	<i>Issue CompResult</i>		
1	LD	F0	0	R1	1	9	10
1	MULTD	F4	F0	F2	2		
1	SD	F4	0	R1	3		
2	LD	F0	0	R1	6	10	11
2	MULTD	F4	F0	F2	7		
2	SD	F4	0	R1	8		

Exec Write

Load & Store Buffers:

	<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
Load1	No		
Load2	No		
Load3	Yes	64	
Store1	Yes	80	Mult1
Store2	Yes	72	Mult2
Store3	No		

Reservation Stations:

				<i>S1</i>	<i>S2</i>	<i>RS</i>				
<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	<i>Code:</i>		
	Add1	No						LD	F0	0 R1
	Add2	No						MULTD	F4	F0 F2
	Add3	No						SD	F4	0 R1
2	Mult1	Yes	Multd	M[80]	R(F2)			SUBI	R1	R1 #8
3	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ	R1	Loop

Register result status

<i>Clock</i>	<i>R1</i>		<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	...	<i>F30</i>
12	64	<i>Fu</i>	Load3		Mult2						

Why not issue third multiply?

Loop Example Cycle 13

<i>ITER</i>	Instruction			<i>j</i>	<i>k</i>	<i>Issue Comp Result</i>			<i>Busy</i>	<i>Addr</i>	<i>Fu</i>
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2			Load2	No		
1	SD	F4	0	R1	3			Load3	No		
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	Mult1
2	MULTD	F4	F0	F2	7			Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		

Reservation Stations:

<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	<i>Code:</i>
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
1	Mult1	Yes	Multd	M[80]	R(F2)			R1
2	Mult2	Yes	Multd	M[72]	R(F2)			F2
								SD
								F4
								0
								R1
								SUBI
								R1
								R1
								#8
								BNEZ
								R1
								Loop

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	<i>...</i>	<i>F30</i>
13	64	<i>Fu</i>	M[64]	Mult2						

Load 3 completed: Writing the result M[64] in CDB for F0.

Loop Example Cycle 14

<i>ITER</i>	Instruction			<i>j</i>	<i>k</i>	<i>Issue</i>	<i>Comp</i>	<i>Result</i>		<i>Busy</i>	<i>Addr</i>	<i>Fu</i>		
1	LD	F0	0	R1	1	9	10	Load1	No					
1	MULTD	F4	F0	F2				2	14				Load2	No
1	SD	F4	0	R1				3					Load3	No
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	Mult1			
2	MULTD	F4	F0	F2	7			Store2	Yes	72	Mult2			
2	SD	F4	0	R1	8			Store3	No					

Reservation Stations:

<i>Time</i>	<i>Name</i>	<i>Busy</i>	<i>Op</i>	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	<i>Code:</i>
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
0	Mult1	Yes	Multd	M[80]	R(F2)			R1
1	Mult2	Yes	Multd	M[72]	R(F2)			F2
								SD
								F4
								0
								R1
								SUBI
								R1
								R1
								#8
								BNEZ
								Loop

Register result status

<i>Clock</i>	<i>R1</i>	<i>F0</i>	<i>F2</i>	<i>F4</i>	<i>F6</i>	<i>F8</i>	<i>F10</i>	<i>F12</i>	<i>...</i>	<i>F30</i>
14	64	<i>Fu</i>	M[64]	Mult2						

Mult1 completing (started at C10 with latency 4). Who is waiting?

Loop Example Cycle 15

ITER	Instruction		<i>j</i>	<i>k</i>	Issue	Comp	Result		Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3			Load3	No		
2	LD	F0	0	R1	6	10	11	Store1	Yes	80	M[80]*F2
2	MULTD	F4	F0	F2	7	15		Store2	Yes	72	Mult2
2	SD	F4	0	R1	8			Store3	No		

Reservation Stations:

Time	Name	Busy	Op	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	Code:
	Add1	No						LD F0 0 R1
	Add2	No						MULTD F4 F0 F2
	Add3	No						SD F4 0 R1
4	Mult1	Yes	Multd	M[64]	R(F2)			SUBI R1 R1 #8
0	Mult2	Yes	Multd	M[72]	R(F2)			BNEZ R1 Loop

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12	...	F30
15	64	Fu	M[64]		Mult1						

Mult1 writing result (M[80]*F2) in CDB for Store Buffer 1
 Mult2 completing (started at C11 with latency 4). Who is waiting?
 Third Multiply issued in Mult1

Loop Example Cycle 16

Instruction status:

ITER	Instruction	<i>j</i>	<i>k</i>	Exec Write		
				Issue	Comp	Result
1	LD	F0	0	R1	1	9 10
1	MULTD	F4	F0	F2	2	14 15
1	SD	F4	0	R1	3	16
2	LD	F0	0	R1	6	10 11
2	MULTD	F4	F0	F2	7	15 16
2	SD	F4	0	R1	8	

Load & Store Buffers:

	Busy	Addr	Fu
Load1	No		
Load2	No		
Load3	No		
Store1	Yes	80	M[80]*F2
Store2	Yes	72	M[72]*F2
Store3	Yes	64	Mult1

Reservation Stations:

Time	Name	Busy	Op	<i>Vj</i>	<i>Vk</i>	<i>Qj</i>	<i>Qk</i>	Code:
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
3	Mult1	Yes	Multd	M[64]	R(F2)			R1
	Mult2	No						F2
								SD
								F4
								0
								R1
								SUBI
								R1
								R1
								#8
								BNEZ
								Loop

Register result status

Clock	R1		F0	F2	F4	F6	F8	F10	F12	...	F30
16	64	Fu	M[64]		Mult1						

Mult2 writing result (M[72]*F2) in CDB for Store Buffer 2

Loop Example Cycle 17

ITER	Instruction	<i>j</i>	<i>k</i>	Issue	Comp	Result	Load/Store	Busy	Addr	Fu
1	LD	F0	0	R1	1	9	10	Load1	No	
1	MULTD	F4	F0	F2	2	14	15	Load2	No	
1	SD	F4	0	R1	3	16	17	Load3	No	
2	LD	F0	0	R1	6	10	11	Store1	No	
2	MULTD	F4	F0	F2	7	15	16	Store2	Yes	72
2	SD	F4	0	R1	8	17		Store3	Yes	64
										M[72]*F2
										Mult1

Reservation Stations:

Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
2	Mult1	Yes	Multd	M[64]	R(F2)			R1
	Mult2	No						#8
								Loop

Register result status

Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30
17	64	Fu	M[64]	Mult1						

Stored result (M[80]*F2) in M[80] and leave Store1

Loop Example Cycle 18

ITER	Instruction			<i>j</i>	<i>k</i>	Issue Comp Result		Busy	Addr	Fu	
1	LD	F0	0	R1	1	9	10	Load1	No		
1	MULTD	F4	F0	F2	2	14	15	Load2	No		
1	SD	F4	0	R1	3	16	17	Load3	No		
2	LD	F0	0	R1	6	10	11	Store1	No		
2	MULTD	F4	F0	F2	7	15	16	Store2	No		
2	SD	F4	0	R1	8	17	18	Store3	Yes		64

Reservation Stations:

Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code:
	Add1	No						LD
	Add2	No						F0
	Add3	No						0
1	Mult1	Yes	Multd	M[64]	R(F2)			R1
	Mult2	No						F2
								SD
								F4
								0
								R1
								SUBI
								R1
								#8
								BNEZ
								R1
								Loop

Register result status

Clock	R1	F0	F2	F4	F6	F8	F10	F12	...	F30
18	64	Fu	M[64]	Mult1						

Stored result (M[72]*F2) in M[72] and leave Store2
 Third multiply in Multi1 will complete execution at C19 and will write
 result at C20 for Store Buffer 3