NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

ACA2022_FORM2_8Sept2022_SILVANO

ACA Course -- Prof. SILVANO

FORM2 is composed of 5 QUESTIONS to get UP TO 12 POINTS

Duration is 24 minutes!

Question 1 (complete table format)
2 points

Let's consider the following access patterns on a **4-processor** system with a direct-mapped, write-back cache with one cache block per processor and a two-cache block memory.

Assume the **MESI protocol** is used, with **write-back** caches, **write-allocate,** and **write-invalidate** of other caches.

Please COMPLETE the following table:

Cycle	After Operation	P0 cache block state	P1 cache block state	P2 cache block state	P3 cache block state	Memory at bl. 0 up to date?	Memory at bl. 1 up to date?
0	Initial state	Invalid	Invalid	Invalid	Invalid	Yes	Yes
1	P0: Read Bl. 1	Excl (1)	Invalid	Invalid	Invalid	Yes	Yes
2	P1: Read Bl. 0	Excl (1)	Excl (0)	Invalid	Invalid	Yes	Yes
3	P2: Read Bl. 0						
4	P0: Write Bl. 1						
5	P3: Write Bl. 0						
6	P2: Write Bl. 1						
7	P1: Read Bl. 1						
8	P0: Read Bl. 0						

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Feedback

Cycle	After Operation	P0 cache block state	P1 cache block state	P2 cache block state	P3 cache block state	Memory at bl. 0 up to date?	Memory at bl. 1 up to date?
0	Initial state	Invalid	Invalid	Invalid	Invalid	Yes	Yes
1	P0: Read Bl. 1	Excl (1)	Invalid	Invalid	Invalid	Yes	Yes
2	P1: Read Bl. 0	Excl (1)	Excl (0)	Invalid	Invalid	Yes	Yes
3	P2: Read Bl. 0	Excl (1)	Shared (0)	Shared (0)	Invalid	Yes	Yes
4	P0: Write Bl. 1	Mod (1)	Shared (0)	Shared (0)	Invalid	Yes	No
5	P3: Write Bl. 0	Mod (1)	Invalid	Invalid	Mod (0)	No	No
6	P2: Write Bl. 1	Invalid	Invalid	Mod (1)	Mod (0)	No	No
7	P1: Read Bl. 1	Invalid	Shared (1)	Shared (1)	Mod (0)	No	Yes
8	P0: Read Bl. 0	Shared (0)	Shared (1)	Shared (1)	Shared (0)	Yes	Yes

See MESI protocols on the slides on L13: Multiprocessors.

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Question 2 (complete table and open text format)
4 points

Let's consider the following assembly code:

```
FOR1:beq $t6,$t7, END
     lw $t2,VECTA($t6)
     lw $t3,VECTB($t6)
     lw $t4,VECTC($t6)
     addi $t2,$t2,k
     sw $t2,VECTA($t6)
     add $t4,$t3,$t4
     sw $t4,VECTC($t6)
     addi $t6,$t6,4
     j FOR1
```

to be executed on a CPU with dynamic scheduling based on **TOMASULO algorithm** with all cache HITS, a single Common Data Bus and:

- *4 RESERVATION STATIONS **(RS1, RS2, RS3, RS4)** for two LOAD/STORE unit **(LDU1, LDU2)** with latency **6***
- *2 RESERVATION STATION **(RS5, RS6)** for two ALU/BR FUs **(ALU1, ALU2)** with latency **2***
- Static Branch Prediction **BTFNT (BACKWARD TAKEN FORWARD NOT TAKEN)** with Branch Target Buffer

Please complete the following table:

INSTRUCTION	ISSUE	START EXEC	WRITE RESULT	Hazards Type	RSi	UNIT
`FOR1:beq $t6,$t7, END`	**1**	**2**	**4**	None	RS5	ALU1
`lw $t2,VECTA($t6)`	**2**	**3**	**9**	None (Control solved by BP)	RS1	LDU1
`lw $t3,VECTB($t6)`	**3**	**4**	**10**	None	RS2	LDU2
`lw $t4,VECTC($t6)`						
`addi $t2,$t2,k`						
`sw $t2,VECTA($t6)`						
`add $t4,$t3,$t4`						
`sw $t4,VECTC($t6)`						
`addi $t6,$t6,4`						
`j FOR1`						

*Calculate the **CPI** and the **IPC:***

CPI = _____

IPC= _____

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Feedback:

INSTRUCTION	ISSUE	START EXEC	WRITE RESULT	Hazards Type	RSi	UNIT
`FOR1:beq $t6,$t7, END`	**1**	**2**	**4**	None	RS5	ALU1
`lw $t2,VECTA($t6)`	**2**	**3**	**9**	None(Control solved by BP)	RS1	LDU1
`lw $t3,VECTB($t6)`	**3**	**4**	**10**	None	RS2	LDU2
`lw $t4,VECTC($t6)`	4	10	16	**STRUCT LDU1**	RS3	LDU1
`addi $t2,$t2,k`	5	11	13	**RAW $t2 + RF read**	RS5	ALU1
`sw $t2,VECTA($t6)`	6	14	20	**RAW $t2**	RS4	LDU2
`add $t4,$t3,$t4`	7	17	19	**RAW $t4**	RS6	ALU2
`sw $t4,VECTC($t6)`	10	20	26	**STRUCT RS1 + RAW $t4**	RS1	LDU1
`addi $t6,$t6,4`	14	15	17	**STRUCT RS6**	RS5	ALU1
`j FOR1`	18	19	21	**STRUCT RS6**	RS5	ALU2

CPI = # clock cycles / IC = 26 / 10 = 2.6

IPC = 1/CPI = 1/ 2.6 = 0.38

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Question 3 (open text format)
2 points

Let's consider the following *software-pipelined version* of a given loop including start-up and finish-up codes, assuming registers $R1 and $R2 have been initialized to 0 and 40 respectively:

```
START-UP:  LD $F0, 0 ($R1)
           ADDI.D $F0, $F0, 8
           ADD.D $F4, $F0, $F2
           LD $F0, 4 ($R1)

SW-LOOP:   SD $F4, 0 ($R1)
           ADDI.D $F0, $F0, 8
           ADD.D $F4, $F0, $F2
           LD $F0, 8 ($R1)
           ADDI.U $R1, $R1, 4
           BNE $R1, $R2, SW-LOOP

FINISH-UP: SD $F4, 0 ($R1)
           ADDI.D $F0, $F0, 8
           ADD.D $F4, $F0, $F2
           SD $F4, 4 ($R1)
```

1) How many iterations of the SW-LOOP are executed?

_____

2) Write the original de-pipelined version of the loop:

_____

_____

_____

_____

_____

_____

_____

_____

3) How many iterations of the original de-pipelined loop are executed?

_____

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Feedback

*1) **10 iterations** of the SW-LOOP are executed (40/4)*

*2) The original de-pipelined version of the loop is the following where the registers **$R1** and **$R2** have been respectively initialized to **0** and **48:***

```
LOOP: LD $F0, 0 ($R1)
      ADDI.D $F0, $F0, 8
      ADD.D $F4, $F0, $F2
      SD $F4, 0 ($R1)
      ADDI.U $R1, $R1, 4
      BNE $R1, $R2, LOOP
```

*3) **12 iterations** of the original de-pipelined LOOP are executed.*

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Question 4 (open text format)
2 points

Let us consider a 1 GHz processor architecture with 3-level caches and the main memory:

Hit Time $_{L1}$ = 1 ns; Hit Rate $_{L1}$ = 96%
Hit Time $_{L2}$ = 5 ns; Hit Rate $_{L2}$ = 92%
Hit time $_{L3}$ = 10 ns; Hit Rate $_{L3}$ = 90%, Miss Penalty $_{L3}$ = 20 ns.

1. *Write the Global Miss Rate for the last level cache:*

2. *Write the Average Memory Access Time:*

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Feedback

1. *How much is the Global Miss Rate for Last Level Cache?*

Miss Rate $_{L1\ L2\ L3}$ = Miss Rate$_{L1}$ x Miss Rate$_{L2}$ x Miss Rate$_{L3}$ = 0.04 x 0.08 x 0.1 → 0.032%

2. *How much is the AMAT?*

AMAT = Hit Time$_{L1}$ + Miss Rate$_{L1}$ x Miss Penalty$_{L1}$ =

Hit Time$_{L1}$ + Miss Rate$_{L1}$ x (Hit Time$_{L2}$ + Miss Rate$_{L2}$ x (Hit Time$_{L3}$ + Miss Rate$_{L3}$ x Miss Penalty$_{L3}$)) =

Hit Time$_{L1}$ + Miss Rate$_{L1}$ x Hit Time$_{L2}$ + Miss Rate $_{L1\ L2}$ x Hit Time$_{L3}$ + Miss Rate $_{L1\ L2\ L3}$x Miss Penalty$_{L3}$ =

1 ns + 0.04 x 5ns + 0.0032 x 10ns + 0.00032 x 20 ns = 1.2384 ns

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Question 5 (complete table format)
2 points

Let's consider 32-block main memory with a direct-mapped 8-block cache based on a ***write allocate*** with ***write-through*** protocol.

The addresses are expressed as decimal numbers:
Memory Address: $[0, 1, 2, \ldots\ldots\ldots 31]_{10}$
Cache Address: $[0, 1, 2, \ldots 7]_{10}$
and Cache Tags are expressed as binary numbers.

At cold start the cache is empty, then there is the following sequence of memory accesses.

Please complete the following table:

	Type of memory access	Memory Address	HIT/MISS Type	Cache Tag	Cache Address	Write in memory
1	Read	$[16]_{10}$	Cold-start Miss	$[10]_{2}$	$[0]_{10}$	No
2	Write	$[16]_{10}$				
3	Read	$[16]_{10}$				
4	Read	$[10]_{10}$				
5	Write	$[8]_{10}$				
6	Write	$[10]_{10}$				
7	Write	$[16]_{10}$				
8	Read	$[26]_{10}$				
9	Read	$[23]_{10}$				
10	Write	$[24]_{10}$				

NAME SURNAME PERSONAL CODE	ACA2022_EXAM_FORM2 Data: 08/09/2022

Feedback

	Type of memory access	Memory Address	HIT/MISS Type	Cache Tag	Cache Address	Write in memory
1	Read	$[16]_{10}$	Cold-start Miss	$[10]_{2}$	$[0]_{10}$	No
2	Write	$[16]_{10}$	Hit	$[10]_{2}$	$[0]_{10}$	Yes, Wr. in M$[16]_{10}$
3	Read	$[16]_{10}$	Hit	$[10]_{2}$	$[0]_{10}$	No
4	Read	$[10]_{10}$	Cold-start Miss	$[01]_{2}$	$[2]_{10}$	No
5	Write	$[8]_{10}$	Conflict Miss	$[01]_{2}$	$[0]_{10}$	Yes, Wr. in M$[8]_{10}$
6	Write	$[10]_{10}$	Hit	$[01]_{2}$	$[2]_{10}$	Yes, Wr. in M$[10]_{10}$
7	Write	$[16]_{10}$	Conflict Miss	$[10]_{2}$	$[0]_{10}$	Yes, Wr. in M$[16]_{10}$
8	Read	$[26]_{10}$	Conflict Miss	$[11]_{2}$	$[2]_{10}$	No
9	Read	$[23]_{10}$	Cold-start Miss	$[10]_{2}$	$[7]_{10}$	No
10	Write	$[24]_{10}$	Conflict Miss	$[11]_{2}$	$[0]_{10}$	Yes, W in M$[24]_{10}$