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Course on Advanced Computer Architectures

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EX1	**(5 points)**	
EX2	**(5 points)**	
EX3	**(5 points)**	
Q1	**(5 points)**	
Q2	**(5 points)**	
QUIZZES	**(8 points)**	
TOTAL	**(33 points)**	

EXERCISE 1 – DEPENDENCY ANALYSIS + TOMASULO (5 points)

1. *Let's consider the following assembly code containing multiple types of intra-loop dependences. Complete the following table by inserting all types of true-data-dependences, anti-dependences and output dependences for each instruction:*

I#	TYPE OF INSTRUCTION	ANALYSIS OF DEPENDECES: 1. True data dependence with I# for $Fx 2. Anti-dependence with I# for $Fy 3. Output-dependence with I# for $Fz
I0	`FOR:LD $F2, A($R1)`	None
I1	`LD $F4, B($R1)`	None
I2	`LD $F6, C($R1)`	None
I3	`FADD $F4, $F2, $F4`	True data dependence with I0 for $F2 True data dependence with I1 for $F4 Output-dependence with I1 for $F4
I4	`FADD $F6, $F4, $F6`	True data dependence with I3 for $F4 True data dependence with I2 for $F6 Output-dependence with I2 for $F6
I5	`SD $F6, A($R1)`	True data dependence with I4 for $F6
I6	`ADDUI $R1, $R1, 8`	Anti-dependence with I0, I1, I2, I5 for $R1
I7	`BNE $R1, $R2, FOR`	True data dependence with I6 for $R1

Let's consider the previous assembly code to be executed on a CPU with dynamic scheduling based on **TOMASULO algorithm** with all cache HITS, a single Common Data Bus and:

- *2 RESERV. STATIONS **(RS1, RS2)** with 2 LOAD/STORE units **(LDU1, LDU2)** with latency **4***
- *2 RESERVATION STATION **(RS3, RS4)** with 2 FP units **(FPU1, FPU2)** with latency **3***
- *2 RESERVATION STATION **(RS5, RS6)** with 2 INT_ALU/BR units **(ALU1, ALU2)** with latency **2***

Please complete the following table:

INSTRUCTION	ISSUE	START EXEC	WRITE RESULT	Hazards Type	RSi	UNIT
`FOR:LD $F2, A($R1)`	1	2	6	None	RS1	LDU1
`I1: LD $F4, B($R1)`	2	3	7	None	RS2	LDU2
`I2: LD $F6, C($R1)`	7	8	12	Structure RS1	RS1	LDU1
`I3: FADD $F4, $F2, $F4`	8	9	13	Structure CDB	RS3	FPU1
`I4: FADD $F6, $F4, $F6`	9	14	17	RAW $F6, RAW $F4 WAW solved	RS4	FPU2
`I5: SD $F6, A($R1)`	10	18	22	RAW $F6	RS1	LDU1
`I6: ADDUI $R1, $R1, 8`	11	12	14	WAR solved	RS5	ALU1
`I7: BNE $R1, $R2, FOR`	12	15	17	RAW $R1	RS6	ALU2

*Calculate the **CPI** =* **22 / 8 = 2.75**

EXERCISE 2 – VLIW SCHEDULING (5 points)

Given the following software pipelined loop:

```
SP_LOOP: SD F6, 0 (R1)
         SD F8, 0 (R2)
         SD F10, 0 (R3)
         FADD F6, F0, F0
         FADD $F8, F2, F2
         FADD $F10, F4, F4
         LD F0, 16 (R1)
         LD F2, 16 (R2)
         LD F4, 16 (R3)
         ADDUI R1, R1, 8
         ADDUI R2, R2, 8
         ADDUI R3, R3, 8
         BNE R1, R4, SP_LOOP
```

Consider a **4-issue VLIW** machine with **fully pipelined functional units:**

- **2 Memory Units with 3 cycles latency**
- **1 FP ALUs with 3 cycles latency**
- **1 Integer ALU with 1 cycle latency to next Int/FP & 2 cycle latency to next Branch**

The branch is completed with 1 cycle delay slot (branch solved in ID stage). **No branch prediction.** In the Register File, it is possible to read and write at the same address at the same clock cycle.

Considering one iteration of the `SP_LOOP`, *complete the following table by using the* ***list-based scheduling*** (do NOT introduce any loop transformation) on the ***4-issue VLIW*** *machine including the BRANCH DELAY SLOT.* Please do not write in NOPs.

	Memory Unit 1	Memory Unit 2	Floating Point Unit	Integer Unit
C1	`SD F6, 0(R1)`			
C2				
C3				
C4				
C5				
C6				
C7				
C8				
C9				
C10				
C11				
C12				
C13				
C14				
C15				

Answer to the following questions:

How long is the critical path for a single iteration?	
What performance did you achieve in CPI?	
What performance did you achieve in FP ops per cycles?	
How much is the code efficiency?	

EXERCISE 3– PERFORMANCE EVALUATION (5 points)

1. *Given **CPU1** with clock frequency **500 MHz** and **CPU2** with clock frequency **200 MHz,** let's consider the two CPUs execute a kernel of **100** instructions with the following frequencies of occurrence and clock cycles:*

Instruction Type	Instruction Frequency	CPU1 Clock Cycles	CPU2 Clock Cycles
ALU	30%	2	1
LOAD	10%	8	6
STORE	20%	2	3
JUMP	30%	2	2
BRANCH	10%	3	3

	CPU1	CPU2
*How much is the **average CPI** for each CPU?*	**CPI1 =**	**CPI2 =**
*How much is the **CPU time** for each CPU?*	**CPUtime1 =**	**CPUtime2 =**
*How much is CPU1 **faster** than CPU2?*		

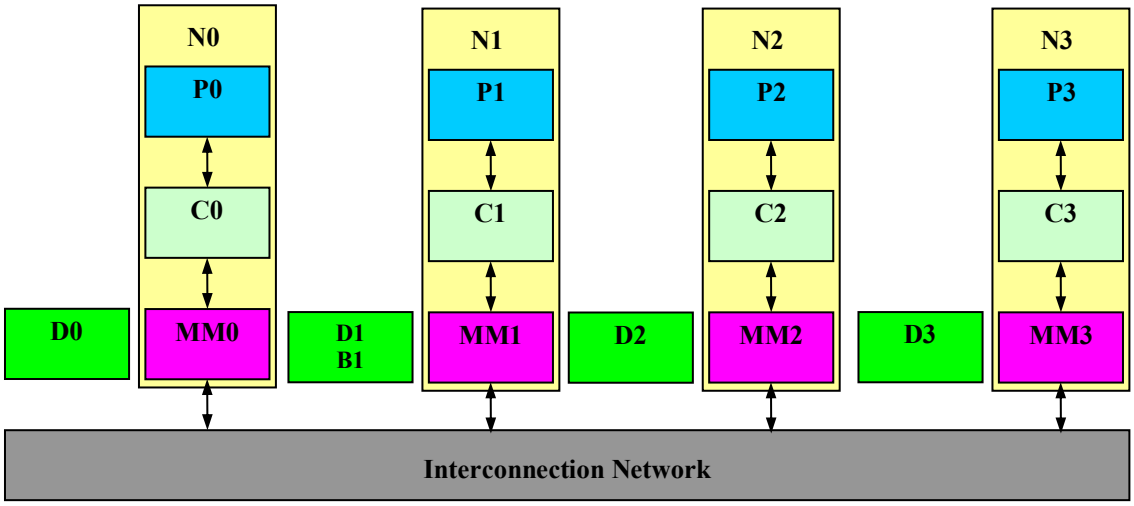
2. *Evaluate the impact of the memory hierarchy on another **CPU3** for which all instructions require **8 clock cycles** in the following cases:*

*How much is the **CPI3** when considering an ideal cache (100% hit)?*	**CPI3_ideal_cache =**
*How much is the **CPI3** when considering a real cache with a miss rate of **50%** and assuming **3** memory accesses on average for each instruction and miss penalty of **3** clock cycles?* *How much is the impact on performance of the real cache with respect to the ideal cache (100% hit)?*	**CPI3_real_cache =**
*How much is the **CPI3** in the case of no cache (100% miss)?* *How much is the impact on performance with respect to the real cache (50% hit)?*	**CPI3_no_cache =**

QUESTION 1: DIRECTORY-BASED PROTOCOL (*5 points)*

Let's consider a directory-based protocol for a distributed shared memory system with 4 Nodes (N0, N1, N2, N3) where we consider the block B1 in the directory of N1:

Directory N1 Block B1 | State: Shared | Sharer Bits: 0 1 0 0 |



*Given the following **sequence of accesses**, please answer to the following questions:*

Read Miss on B1 from node N2				
Home node?	*Local node?*	*Remote node(s)?*	*What is the sequence of messages sent among the nodes?*	*Which are the final coherence state and sharer bits of the block B1 in the home directory?*
N1				**B1:** | State: _____ | | Sharer Bits: _ _ _ _ |
Write Hit on B1 from node N2				
Home node?	*Local node?*	*Remote node(s)?*	*What is the sequence of messages sent among the nodes?*	*Which are the final coherence state and sharer bits of the block B1 in the home directory?*
				B1: | State: _____ | | Sharer Bits: _ _ _ _ |

Write Miss on B1 from node N0				
Home node?	*Local node?*	*Remote node(s)?*	*What is the sequence of messages sent among the nodes?*	*Which are the final coherence state and sharer bits of the block B1 in the home directory?*
				B1: | State: _____ | | Sharer Bits: _ _ _ _ |

QUESTION 2: MULTICORE PROCESSORS (5 points)

High-performance multicore processors today use a combination of several computer architecture techniques. ***Let's consider a single-chip dual-core shared-memory architecture where each core is a dual-issue superscalar processor with multi-threading up to 2 threads per core.***

Explain the preferred technique used to manage the multiple threads for each core.

*Make **an example** of scheduling up to 4 threads per chip where T1 and T2 are executed on Core1 and T3 and T4 on Core2.*

Cycle	Core 1		Core 2	
	Issue 1	Issue 2	Issue 1	Issue 2
C0				
C1				
C2				
C3				
C4				
C5				
C6				
C7				
C8				
C9				

Let's consider our dual-issue SMT processor that can manage up to 4 concurrent threads (2-thread per core)	*How much is the **ideal per core CPI?*** *How much is the **ideal dual-core CPI?*** *How much is the **ideal per-thread CPI?***
Explain the preferred technique used in each superscalar processor to manage the instruction scheduling in each thread.	
Explain the preferred technique used to manage the cache coherency problem in the dual core chip.	

QUIZZES

Question 1

Let's consider the directory-based protocol for multiprocessors.
Which is the message type that can be sent form the remote node to the home node of a block?
(SINGLE ANSWER)
1 point

Answer 1: Data value reply

Answer 2: Data write back

Answer 3: Invalidate

Answer 4: Fetch/Invalidate

Question 2

Let's consider a quad-issue SMT processor that can manage up to 8 simultaneous threads.
What are the values of the ideal CPI and the ideal per-thread CPI?
(SINGLE ANSWER)
1 point

Answer 1: Ideal CPI = 1 & Ideal per-thread CPI = 0.125

Answer 2: Ideal CPI = 0.5 & Ideal per-thread CPI =2

Answer 3: Ideal CPI = 0.25 & Ideal per-thread CPI = 2

Answer 4: Ideal CPI = 0.5 & Ideal per-thread CPI = 4

Answer 5: Ideal CPI = 0.25 & Ideal per-thread CPI = 4

Question 3

In the GP-GPU programming model, the CPU (host) and GPU (device) have separate memory address spaces.
(True/False)
1 point

Answer: True False

Question 4

Let's consider the following code executed by a Vector Processor with:

- *Vector Register File composed of 32 vectors of 8 elements per 64 bits/element;*
- *Scalar FP Register File composed of 32 registers of 64 bits;*
- *One Load/Store Vector Unit with operation chaining and memory bandwidth 64 bits;*
- *One ADD/SUB Vector Unit with operation chaining;*
- *One MUL/DIV Vector Unit with operation chaining.*

```
L.V V1, RA          # Load vector from memory address RA into V1
L.V V2, RB          # Load vector from memory address RA into V1
L.V V3, RC          # Load vector from memory address RB into V3
MULVS.D V1, V1, F1  # FP multiply vector V1 to scalar F1
MULVS.D V2, V2, F2  # FP multiply vector V2 to scalar F2
MULVS.D V3, V3, F3  # FP multiply vector V3 to scalar F3
ADDVV.D V2, V2, V1  # FP add vectors V2 and V1
ADDVV.D V3, V2, V3  # FP add vectors V2 and V3
S.V V3, RD          # Store vector V3 into memory address RD
```

How many convoys? How many clock cycles to execute the code?
(SINGLE ANSWER)
1 point

Answer 1: 2 convoys; 16 clock cycles

Answer 2: 3 convoys; 24 clock cycles

Answer 3: 4 convoys; 32 clock cycles

Answer 4: 5 convoys; 40 clock cycles

Answer 5: 6 convoys; 48 clock cycles

Motivate your answer by completing the following table:
1 point

	Load/Store Vector Unit	**Mul/Div Vector Unit**	**Add/Sub Vector Unit**
1^ convoy	L.V V1, RA		
2^ convoy			
3^ convoy			
4^ convoy			
5^ convoy			
6^ convoy			

Question 5

Let's consider the following LOOP to be executed on a processor with a single-entry 2-bit Branch History Table initialized in the state Strongly Not-Taken:

```
INIT: ADDI.U $R1, $R0, 0
      ADDI.U $R2, $R0, 20
LOOP: LD $F0, 0 ($R1)
      ADDI.D $F2, $F0, $F0
      SD $F2, 0 ($R1)
      ADDI.U $R1, $R1, 4
      BNE $R1, $R2, LOOP
```

After the last iteration, how much is the misprediction rate on the BNE instruction?
(SINGLE ANSWER)
1 point

Answer 1: 60%
Answer 2: 90%
Answer 3: 99 %
Answer 4: 100%
Answer 5: 80 %

After the last iteration, what is the state of the prediction left in the Branch History Table?
(SINGLE ANSWER)
1 point

Answer 1: Strongly Taken
Answer 2: Weakly Taken
Answer 3: Strongly Not Taken
Answer 4: Weakly Not Taken

Motivate your answer by completing the following table:
1 point

Iteration	*1st iteration*	*2^ iteration*	*3^ iteration*	*4^ iteration*	*5^ iteration*
Prediction State	Strongly Not Taken				
Prediction	Not Taken				
Branch Outcome	Taken				