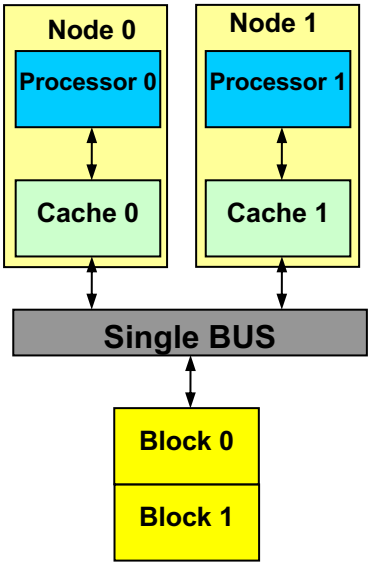
Course on Advanced Computer Architectures
EXERCISES ON MESI PROTOCOL

EXERCISE 3: CACHE COHERENCY (5 points) *EXAM 27/06/2019*

Consider a **dual-processor** shared-memory system with a **direct-mapped, write-back cache** with **one cache-block** per node and a **two cache-blocks in main memory:**



Assume the **MESI protocol** is used, with **write-back** caches, **write-allocate,** and **write-invalidate** of other caches.

Consider the following access pattern and complete the table:

Cycle	After Operation	P0 cache-block state	P1 cache-block state	Memory at block 0 up to date?	Memory at block 1 up to date?
0	P0: read block 1	Exclusive (1)	Invalid	Yes	Yes
1	P1: read block 0				
2	P0: write block 1				
3	P1: read block 0				
4	P0: write block 0				
5	P1: write block 1				
6	P0: write block 0				
7	P0: read block 1				
8	P1: read block 1				
9	P0: write block 1				
10	P1: write block 1				

Solution with some comments:

Cycle	After Operation	P0 cache-block state	P1 cache-block state	Memory at block 0 up to date?	Memory at block 1 up to date?
0	P0: read block 1	Exclusive (1)	Invalid	Yes	Yes
1	P1: read block 0	Exclusive (1)	Exclusive(0)	Yes	Yes
2	P0: write block 1	Modified (1) No INV	Exclusive (0)	Yes	No
3	P1: read block 0	Modified (1)	Exclusive (0)	Yes	No
4	P0: write block 0	Modified (0)	Invalid (WR INV sent)	NO	Yes (W. Back)
5	P1: write block 1	Modified (0)	Modified (1)	No	No
6	P0: write block 0	Modified (0) 2^ write	Modified (1)	No	No
7	P0: read block 1	Shared(1)	Shared(1)	Yes (W.back)	Yes (W.back)
8	P1: read block 1	Shared (1)	Shared (1)	Yes	Yes
9	P0: write block 1	Modified (1)	Invalid WR INV	Yes	NO
10	P1: write block 1	Invalid (WR INV sent)	Modified (1)	Yes	Yes (W.Back) No

EXERCISE 3: CACHE COHERENCY (5 points)

FINAL SOLUTION:

Cycle	After Operation	P0 cache block state	P1 cache block state	Memory at block 0 up to date?	Memory at block 1 up to date?
0	P0: read block 1	Exclusive (1)	Invalid	Yes	Yes
1	P1: read block 0	Exclusive (1)	Exclusive (0)	Yes	Yes
2	P0: write block 1	Modified (1)	Exclusive (0)	Yes	No
3	P1: read block 0	Modified (1)	Exclusive (0)	Yes	No
4	P0: write block 0	Modified (0)	Invalid	No	Yes
5	P1: write block 1	Modified (0)	Modified (1)	No	No
6	P0: write block 0	Modified (0)	Modified (1)	No	No
7	P0: read block 1	Shared (1)	Shared (1)	Yes	Yes
8	P1: read block 1	Shared (1)	Shared (1)	Yes	Yes
9	P0: write block 1	Modified (1)	Invalid	Yes	No
10	P1: write block 1	Invalid	Modified (1)	Yes	No

EXERCISE 3 – MESI PROTOCOL (5 points) – Exam 11 July 2023

Let's consider the following access patterns on a dual processor system with a direct-mapped, write-back cache with one cache block per processor and a 2 cache block memory. Assume the **MESI protocol** is used, with **write-back** caches, **write-allocate,** and **write-invalidate** of other caches.

Please complete the following table:

Cycle	After Operation	P0 cache block state	P1 cache block state	Memory at block 0 up to date?	Memory at block 1 up to date?
1	**P1: read block 0**	Exclusive (1)	Exclusive (0)	Yes	Yes
2		Modified (1)	Exclusive (0)	Yes	No
3		Modified (1)	Exclusive (0)	Yes	No
4		Modified (1)	Exclusive (0)	Yes	No
5		Modified (0)	Invalid	No	Yes
6		Modified (0)	Modified (1)	No	No
7		Shared (0)	Shared (0)	Yes	Yes
8		Exclusive (1)	Exclusive (0)	Yes	Yes

SOLUTION

Cycle	After Operation	P0 cache block state	P1 cache block state	Memory at block 0 up to date?	Memory at block 1 up to date?
1	**P1: read block 0**	Exclusive (1)	Exclusive (0)	Yes	Yes
2	**P0: write block 1**	Modified (1)	Exclusive (0)	Yes	No
3	**P1: read block 0 OR P0 read/write bl.1**	Modified (1)	Exclusive (0)	Yes	No
4	**P1: read block 0 OR P0 read/write bl. 1**	Modified (1)	Exclusive (0)	Yes	No
5	**P0: write block 0**	Modified (0)	Invalid	No	Yes
6	**P1: write block 1**	Modified (0)	Modified (1)	No	No
7	**P1: read block 0**	Shared (0)	Shared (0)	Yes	Yes
8	**P0: read block 1**	Exclusive (1)	Exclusive (0)	Yes	Yes