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Active Voltage Quadrupler Rectifier-Based Ultra-High Boost Ratio Multidirectional Energy Router in 800V DC Microgrids

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ABSTRACT In 800V DC microgrids, an energy router is essential for managing power distribution among the low-voltage photovoltaic (PV) panel, energy storage battery, and high-voltage dc link. Current solutions face challenges in simultaneously achieving high step-up ratios, multidirectional power flow, and maintaining high efficiency across broad input voltage and load ranges. To address these issues, this paper introduces a novel energy router featuring three key innovations. First, it combines an interleaved boost converter with an active voltage quadrupler cell (VQC), reducing voltage stress by 50% compared to conventional designs. Second, it employs an integrated magnetic design that utilizes leakage inductance, reducing magnetic volume by 36%. Third, it uses hybrid modulation, merging pulse-width modulation (PWM) and phase-shift modulation (PSM), to optimize switching and circulating losses while minimizing transformer turns and total power loss. Additionally, this configuration halves the voltage stress experienced by the MOSFETs on the high-voltage side relative to the dc link voltage. A 500W prototype was developed and tested, interfacing with a 15-25 V PV port, 40-50 V battery port, and 800 V dc link. Experimental results demonstrate a peak efficiency of 97.5% with stable operation under 0-100% load transitions. Comprehensive analysis, including dynamic studies (working modes switching, 95% load step changes) confirms the topology's reliability in 800V DC microgrid applications.

INDEX TERMS Energy router, High-voltage bus, multidirectional power flow, voltage multiplier, zero-voltage switching(ZVS).

I. INTRODUCTION

THE global photovoltaic (PV) sector is pivotal to the ongoing energy transition, with installations exceeding 505 GW in 2024 and an anticipated global capacity approaching 10,000 GW by 2030 [1]. This rapid growth highlights the critical role of PV technology in the shift towards more sustainable energy sources. However, the intermittent nature of solar energy presents significant challenges, necessitating the integration of energy storage systems such as batteries to absorb surplus energy and ensure a stable power supply.

Traditionally, the connection between PV panels, energy storage units and loads has been facilitated through multiple discrete converters [2], [3]. While functional, this approach introduces several drawbacks, including reduced efficiency due to multilevel energy transmission, increased system complexity due to individual control of multiple converters, and decreased power density due to the proliferation of components. To mitigate these issues, integrated energy routers have emerged as a promising solution [4]. By consolidating multiple input and output ports into a single converter, the energy router simplified the power flow through fewer transmission stages, enhancing system efficiency. This integration not only improves power density but also simplifies system design and control, reducing costs and increasing reliability [5].

According to the galvanic isolation scheme, energy routers can be classified into non-isolated, fully isolated, and partially isolated types. Non-isolated energy routers are compact and cost-effective but are not suitable for high-voltage (HV) or safety-critical applications due to the absence of galvanic isolation [6], [7]. Fully isolated energy routers, on the other hand, are typically larger and more costly because of the inclusion

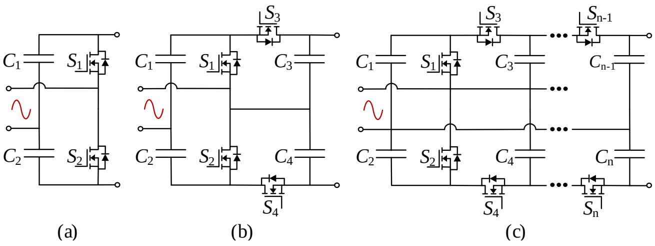

FIGURE 1. Symmetric active voltage multiplier cell in even derivation.(a) Voltage doubler cell. (b) Voltage quadrupler cell; (c) *n*-stage voltage multiplier cell.

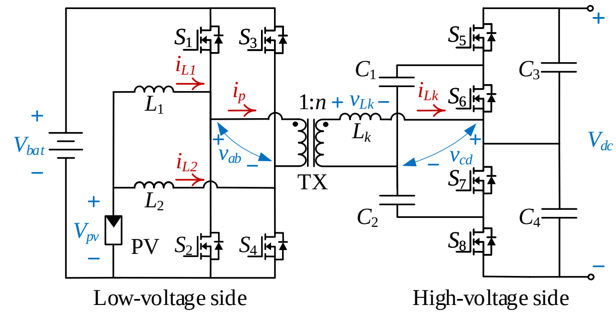

FIGURE 2. Schematic of the proposed energy router.

of bulkier magnetic components and additional switching devices [8]–[10]. In contrast, partially isolated energy routers provide a balanced solution. They offer galvanic isolation between the low-voltage (LV) and HV sides, rather than across all ports. This makes them particularly suitable for renewable energy applications, such as distributed PV systems, where isolation between the PV panel and the battery is not always required [11]–[17].

Typically, the structure of partially isolated energy routers consists of two common-grounded inverters on the LV side, an isolated transformer with a turn ratio of 1:n, and a secondary side rectifier. On the LV side, a boost circuit is added to each input port [11] to achieve high boost ratio. Additionally, [12] integrates a boost circuit with a full-bridge converter to reduce the component count by reusing the bridge arms. A hybrid structure, combining an interleaved boost stage with a full-bridge converter, is introduced in [13], [17], [18]. This configuration minimizes input current ripple, reduces stress on the input components, and efficiently regulates the power exchange between the PV and battery ports.

For the secondary side, an active full-bridge rectifier rather than a classical full-bridge rectifier [19], is used to transfer power with mitigated conduction losses in [20]. In [21], a current-fed full-bridge converter connects the PV and load/grid ports, with diodes replacing the upper bridge arm's active MOSFETs to reduce circulating current and minimize voltage stress on the secondary side.

Voltage multiplier topologies, such as those used in [22]–[24], leverage cascading structures to achieve high voltage levels, reduce output voltage drop and ripple, and extend the voltage step-up range, thereby enhancing their suitability for HV applications [25]. Among these, even-order active voltage multiplier derivations, as illustrated in Fig. 1, are commonly employed in high step-up converters due to their ability to provide symmetrically balanced voltage stress on both capacitors and switches. Fig. 1(a) shows a voltage doubler cell [14]–[16], Fig. 1(b) depicts a voltage quadrupler cell (VQC) [26]–[32], and Fig. 1(c) illustrates the derivation of an n-stage voltage multiplier cell [33], [34]. Among them, the voltage quadrupler cell offers an optimal balance between voltage step-up ratio and component count, making it a preferred solution in HV energy routers. To improve, we propose a novel active voltage quadrupler rectifier based on a partially isolated energy router in [35]. This article is the extension of the conference version. The schematic of the proposed energy router is plotted in Fig. 2. It benefits from the interleaved boost stage's reduced input current ripple and utilizes an active VQC to achieve bidirectional power flow with a high boost ratio. This combination reduces voltage stress on the switching devices, contributing to improved system reliability and efficiency. A pulse-width modulation (PWM) scheme combined with phase-shift modulation (PSM) is introduced to balance the zero voltage switching (ZVS) range and minimize the root mean square (RMS) current across all operating modes, further enhancing efficiency. Additionally, integrating the inductor and transformer into a unified structure reduces the converter's physical size, providing a compact and cost-effective solution. The major extra contributions include:

1) A detailed analysis of circulating current and soft-switching conditions is provided, improving efficiency by suppressing RMS current and operating in the ZVS region.
2) A comprehensive analysis of the operating principles and design guidelines is presented. The compact size is achieved by using the transformer's leakage inductance as the series inductor, significantly reducing the size of magnetic components and the converter, thus enhancing power density. Control strategies are also summarized, and the control block diagram is provided.
3) Extensive experimental results across different modes are presented to validate the proposed concept. The dynamic response, ZVS performance, and efficiency at various input voltages are discussed. A thorough comparison with other partially isolated energy routers and high-boost ratio converters is provided to highlight the advantages of the proposed design.

The manuscript is structured as follows: Section II describes the proposed topology and its operation modes. Section III presents a detailed analysis of six fundamental operation modes, including their operational principles. Section IV analyzes the normalized power and ZVS range. The experimental results validating the theoretical analysis and the performer comparison are reported in Section V. Finally, Section VI concludes this work.

II. OPERATION PRINCIPLES

A. TOPOLOGY DERIVATION

Fig. 2 illustrates the schematic of the proposed energy router. The battery and dc bus both supply and absorb power, while the PV source only provides power.

On the LV side, a hybrid stage is employed, combining a full-bridge converter and an interleaved boost stage. LV side is equipped with two inductors (L_1 and L_2) and four power MOSFETs (S_1 to S_4). The gate signals for S_1 and S_2 (S_3 and S_4) are complementary, with dead times introduced to ensure proper switching. The two parallel phase legs are driven with a 180° phase shift to achieve interleaving. The duty cycle of the gate signal for S_1 is denoted as D, and it regulates the boost ratio between the PV panel and the battery.

The transformer turns ratio is defined as $1{:}n$. L_k is the series inductance which is implemented by the transformer leakage inductance.

On the HV side, an active quadrupler cell is employed, derived from passive voltage multipliers. The rectifier is responsible for power conversion in the forward direction, from the input to the dc bus, while the inverter manages the reverse path. The active voltage multiplier cell enables phase-shifting control and bidirectional power flow between the LV and HV sides. The gate signals for MOSFETs S_5 and S_6 (S_7 and S_8) are complementary, with appropriate dead times. The duty cycle for S_5 and S_7 is fixed at 0.5. Moreover, a phase shift of φ is applied between the switching patterns of S_4 and S_5 to regulate the power delivered to the dc bus.

B. OPERATION MODES

For a energy router-based grid-tied PV-battery system, six main operation modes (see Fig. 3) are necessary for a typical day, all of which can be achieved by the proposed energy router. These modes are designed to optimize power management between the PV panel, the battery, and the dc grid, ensuring that the system operates efficiently under varying conditions [4]. Defining the output power of PV panels, release or absorb the power of batteries, and dc bus demand power as P_{pv}, P_{bat} and P_{dc} respectively. The basic power balance of an energy router architecture can be expressed as follows

$$P_{dc} = P_{pv} + P_{bat}. \tag{1}$$

The operation modes can be classified into two categories based on the number of active ports. In Modes I-III, the converter functions as a two-port converter, while in Modes IV-VI, it operates as a multidirectional energy router.

Mode I: dc bus is offline, and the PV panel generates power that is delivered unidirectionally to the battery.

Mode II: Battery is inactive, and the PV panel generates power that is delivered through the transformer to the dc bus.

Mode III: PV panel is idle during the night and the power flows bidirectionally between the battery and the dc bus, which is defined as forward and backward mode. This enables the battery to provide power to the dc grid to compensate for peak demand, while excess energy from the dc grid can be stored in the battery.

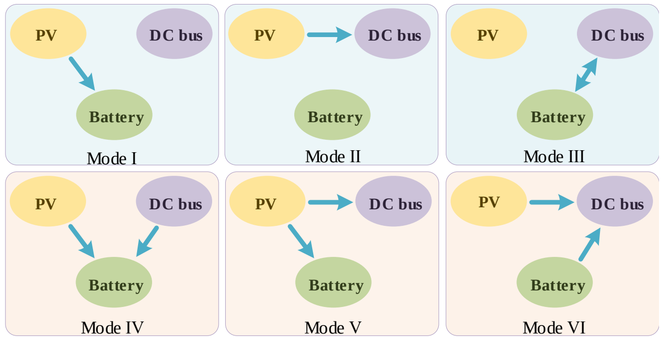

FIGURE 3. Main operating modes.

Modes IV–VI: All three ports are active. The PV panel generates power, which can be delivered unidirectionally to either the battery or the dc bus. Power flow between the two sides of the transformer is bidirectional, regulated by the load demand of the dc grid and the state of charge of the battery. Thus, the system operates in six distinct modes based on the power relationships among the three ports. It is important to note that even in two-port mode, where there is no net power flow from the battery port or PV port, it remains operational and affects the converter's behavior.

III. MODE ANALYSIS

A. MODE I

In Mode I, the energy router operates on the LV side with the dc bus inactive, directing all power from the photovoltaic source to charge the battery. In this mode, the HV side MOSFETs remain off, and the converter behaves like an interleaved boost converter. The driving signals for S_1 and S_2 (S_3 and S_4) are complementary, with a dead time (t_d) introduced, and are driven in an interleaved manner with regulated duty cycles and a 180° phase shift. The duty cycle of the higher side MOSFETs (S_1, S_3) is denoted as D. On the LV side, a three-level voltage v_{ab} with duty cycle D is generated due to PWM control. The duty cycle D is adjusted to perform Maximum Power Point Tracking (MPPT) based on the battery voltage and PV operating conditions.

The interleaved boost converter establishes a direct relationship between the PV source voltage (V_{pv}) and the battery voltage (V_{bat})

$$V_{bat} = \frac{V_{pv}}{D}. \tag{2}$$

The minimum valley values of the inductor currents, i_{L_1} and i_{L_2}, are given by

$$i_{L_1.\text{min}} = i_{L_2.\text{min}} = \frac{1}{2}\left(\frac{P_{pv}}{V_{pv}} - \frac{V_{pv}(1-D)}{L_1 f_s}\right) \tag{3}$$

where f_s is the switching frequency.

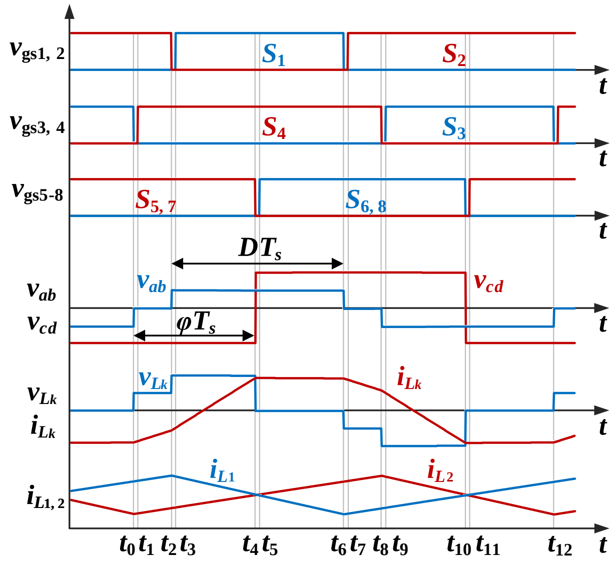

FIGURE 4. Critical steady-state waveforms.

B. MODES II AND III

These two modes are analyzed together as their power flow occurs between the LV side and the HV side. The voltage at the LV side, either from the PV or the battery, through the full-bridge or interleaved boost stage, is represented by v_{ab}.

In Mode II, the battery is offline, and the PV panel generates power to the dc bus via the interleaved boost stage (using PWM) and an active VQC.

In Mode III, during nighttime operation when the PV source is inactive, power flows bidirectionally between the battery and the dc bus to manage the battery state of charge and provide grid power. This mode combines a full bridge and an active VQC.

Power flow in both modes is mainly controlled by phase-shift modulation, with the converter operating in either forward or backward mode. Furthermore, the primary and secondary sides of the converter are connected through a transformer with a turns ratio of 1:n. Notably, even when the PV port is inactive in Mode III, the interleaved boost still operates with interleaved currents, although the current bias is zero. Following the principles governing the HV side MOSFETs, the relationship between the amplitude of V_{cd} and V_{dc} is given by

$$V_{cd} = \frac{V_{dc}}{4}. \tag{4}$$

The relationship between the amplitude of V_{pv} and V_{dc} is expressed as

$$V_{dc} = \frac{4nV_{pv}}{D}. \tag{5}$$

C. MODES IV-VI

Steady-state operation of the proposed converter combines LV side PWM with HV side phase-shift modulation, which depends on the values of $D < 0.5$ and φ. Based on the range of D and φ, the system exhibits 8 distinct steady-state operations. This analysis focuses on the operational state characterized by $D < 0.5$ and $0.5 - D \leq \varphi < 0.5$. Within this state, the system operates in 12 distinct states over one switching period. Key waveforms are shown in Fig. 4, and the corresponding equivalent circuits are provided in Fig. 5. Inductors L_1 and L_2 are designed with equal values to support continuous inductor currents.

Combining equations (2) and (4), the voltage conversion ratio M is defined as

$$M = \frac{V_{dc}}{4nV_{bat}}. \tag{6}$$

The conversion ratio M adapts to variations in V_{pv} through different D values, ensuring voltage matching, with the conversion ratio equal to 1.

State I $[t_0, t_1)$: Before t_0, $S_{2,3}$ on the LV side and $S_{5,7}$ on the HV side are ON, and L_1 and L_2 are energized by the PV panel. i_{L_k} is negative and decreases. At t_0, S_3 is turned OFF, and v_{cd} is clamped at $V_{dc}/4$. In this state, i_{L_k} is given by

$$i_{L_k} = \frac{V_{dc}/4}{L_k}(t - t_0) + i_{L_k}(t_0). \tag{7}$$

State II $[t_1, t_2)$: At t_1, S_4 is turned ON. C_2 and C_3 are charged, while C_1 is discharged. i_{L_k} continues to decrease at the same rate as in state I.

State III $[t_2, t_3)$: At t_2, S_2 is turned OFF, and v_{ab} is clamped at V_{pv}/D. At t_3, i_{L_k} is expressed as

$$i_{L_k} = \frac{nV_{bat} + V_{dc}/4}{L_k}(t - t_2) + i_{L_k}(t_2). \tag{8}$$

State IV $[t_3, t_4)$: At t_3, S_1 is turned ON, and i_{L_k} continues to increase at the same rate as in state III.

State V $[t_4, t_5)$: At t_4, S_5 and S_7 are turned OFF. i_{L_k} flows from the source to the drain of S_6 and S_8. In this state, i_{L_k} increases linearly as

$$i_{L_k} = \frac{nV_{bat} - V_{dc}/4}{L_k}(t - t_4) + i_{L_k}(t_4). \tag{9}$$

State VI $[t_5, t_6)$: The positive current of i_{L_k} contributes to the ZVS turn-on of S_6 and S_8. C_1 and C_4 are charged, while C_2 is discharged. i_{L_k} continues to decrease at the same rate as in state V.

Since states VII to XII are symmetric to states I to VI, we obtain the following relationship

$$i_{L_k}(t_0) = -i_{L_k}(t_6). \tag{10}$$

Combining equations (7)-(9), the inductor current expressions at different instants are derived as

$$\begin{aligned} i_{L_k}(t_0) &= -i_{L_k}(t_6) = I_N(M - 2D - 4M\varphi) \\ i_{L_k}(t_2) &= -i_{L_k}(t_8) = I_N(3M - 2D - 4M\varphi - 4DM) \\ i_{L_k}(t_4) &= -i_{L_k}(t_{10}) = I_N(M + 2D + 4\varphi - 2) \end{aligned} \tag{11}$$

where I_N is the normalized current, defined as

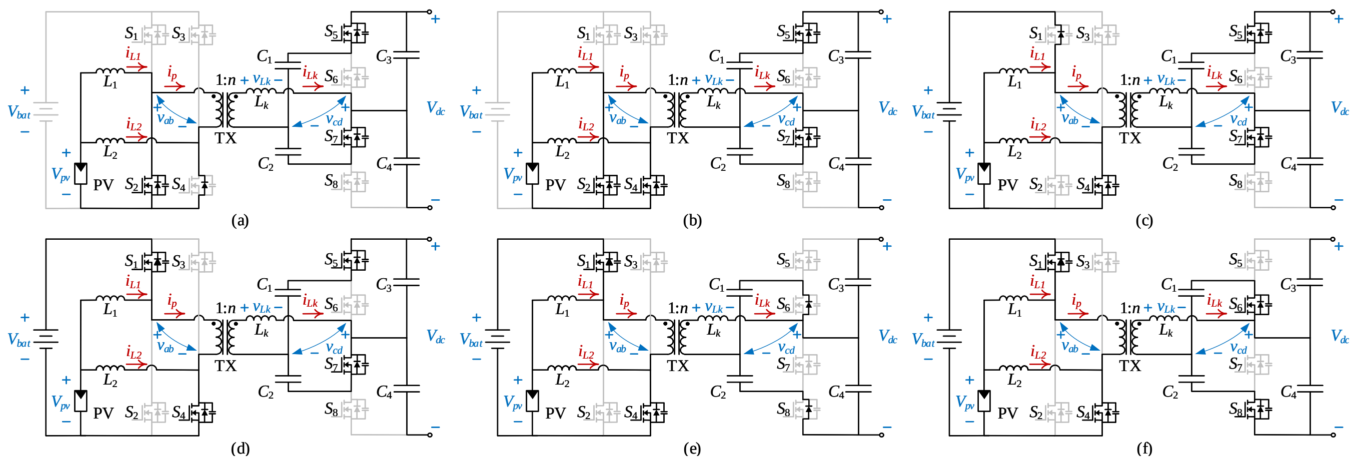

FIGURE 5. Equivalent circuits: (a) State I, $t_0 \le t < t_1$. (b) State II, $t_1 \le t < t_2$. (c) State III, $t_2 \le t < t_3$. (d) State IV, $t_3 \le t < t_4$. (e) State V, $t_4 \le t < t_5$. (f) State VI, $t_5 \le t < t_6$.

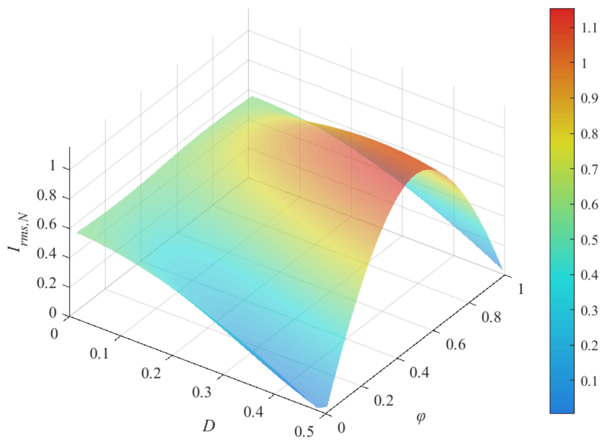

FIGURE 6. $I_{rms,N}$ varies from D and φ.

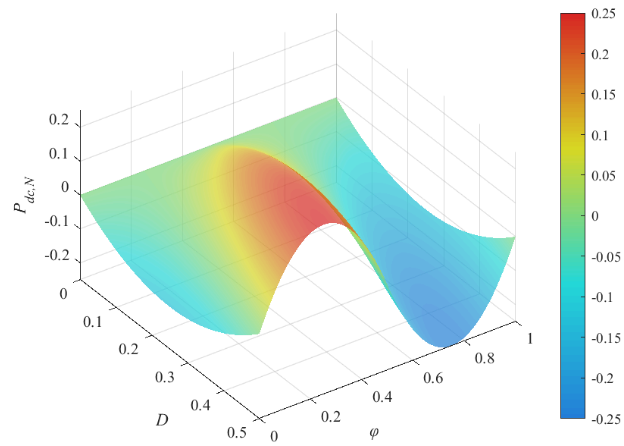

FIGURE 7. $P_{dc,N}$ versus D and φ.

$$I_N = \frac{nV_{bat}}{4f_s L_k}. \tag{12}$$

Due to the symmetry of D with respect to 0.5 and φ with respect to 0, situations with different values of $0.5 < D < 1$ and $\varphi < 0$ can also be analyzed using the same method. These solutions serve as valuable tools for the power flow analysis and ZVS condition in Section IV.

The inductor current changes linearly within each steady-state period, and the current $i_{L_k}(t)$ can be derived accordingly. The normalized RMS current, $I_{rms,N}$, can be calculated by

$$I_{rms,N} = \frac{1}{I_N}\sqrt{f_s \int_{t_0}^{t_{12}} i_{L_k}^2(t)} \tag{13}$$

and is plotted in Fig. 6.

As φ increases, $I_{rms,N}$ initially increases, then decreases, and gradually transitions into a sinusoidal function. The variation of $I_{rms,N}$ with D exhibits three distinct trends when φ is between 0 and 0.5: first trend: $I_{rms,N}$ decreases and then increases as D increases; second, $I_{rms,N}$ continuously increases with D; and third, $I_{rms,N}$ continuously decreases with D. Specifically, when $D = 0.5$, $I_{rms,N}$ corresponds to the classic value of $I_{rms,N}$ for single-phase shift modulation. In the design process, conduction losses must be considered, so the values of D and φ should be chosen within the region where $I_{rms,N}$ remains relatively small to optimize efficiency.

IV. POWER FLOW AND ZVS ANALYSIS

A. OUTPUT POWER

In the analysis within the range $D < 0.5$ and $0.5 - D \le \varphi < 0.5$, the dc bus power P_{dc} is calculated as

$$\begin{aligned} P_{dc} &= \frac{1}{T_s}\int_0^{T_s} v_{cd}(t)\cdot i_{L_k}(t)\,dt \\ &= P(D,\varphi) \\ &= P_N P_{dc,N}(0.5-D\le\varphi<0.5) \\ &= P_N\left(2D^2+4D\varphi-3D+4\varphi^2-4\varphi+1\right) \end{aligned} \tag{14}$$

where P_N is the normalized power, defined as

$$P_N = \frac{nV_{bat}V_{dc}}{8f_sL_k}. \tag{15}$$

Based on the values of D and φ, the normalized output power $P_{dc,N}$ is derived as

$$P_{dc,N}(D,\varphi) = \begin{cases} \sigma, & 0\le\varphi<0.5-D \\ -\sigma+2D-(2\varphi-1)^2, & 0.5-D\le\varphi<0.5 \\ -\sigma+2D, & 0.5\le\varphi<1-D \\ \sigma-4D+4(\varphi-1)^2, & 1-D\le\varphi<1 \end{cases} \tag{16}$$

where

$$\sigma = 2D^2+4D\varphi-D. \tag{17}$$

The output power function $P_{dc,N}$, based on the variation of D and φ, is plotted in Fig. 7. It is important to note that P_{dc} represents the dc bus demand power. Both P_{dc} and $P_{dc,N}$ share the same signs. When $P_{dc,N}$ is positive, the energy router operates in forward mode, and when $P_{dc,N}$ is negative, it operates in backward mode. The backward mode occurs in Modes III and IV.

By examining the relationship among $P_{dc,N}$, D, and φ, it can be observed that $P_{dc,N}$ first increases, then decreases, and increases again as φ increases. The maximum value of $P_{dc,N}$ gradually shifts from $\varphi=0.5$ to $\varphi=0.25$. The variation of $P_{dc,N}$ with D exhibits two distinct parabolic curves. From the formula of $P_{dc,N}$, it is evident that near the center, the curve is convex, while near the edges, it is concave. When $\varphi=0$ or 1, $P_{dc,N}$ follows a parabolic shape concerning D and less than 0, indicating power transmission still occurs but in backward mode.

This formula can be used to adjust parameters for controlling both the magnitude and direction of power. The control strategy for the digital control block diagram in three-port modes is shown in Fig. 8.

B. CONTROL STRATEGIES

The control diagram, shown in Fig. 8, generates PWM control signals for all MOSFETs based on the input voltage V_{pv} and current I_{pv}. The MPPT algorithm is first applied to determine the optimal power point. The duty cycle D for the LV side MOSFETs is calculated using equation (2), while the power values P_{pv} and P_{bat} are determined. The duty cycle D, along with the calculated dc power P_{dc} (derived from V_{dc} and I_{dc}), is substituted into equation (14) to compute φ. Finally, the PWM signals for both high- and LV sides are generated by comparing the values of φ and D, with the HV MOSFETs maintaining a fixed duty cycle of 0.5. The operation mode and modulation strategy are then determined by the operation mode unit.

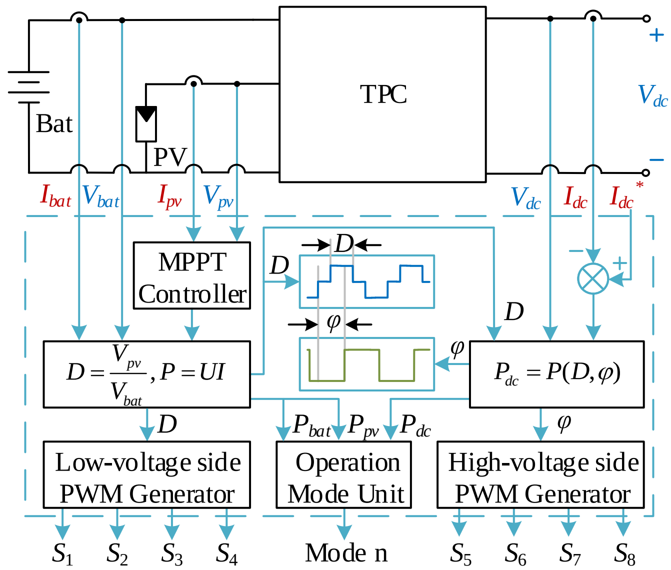

FIGURE 8. Block diagram of the digital controller.

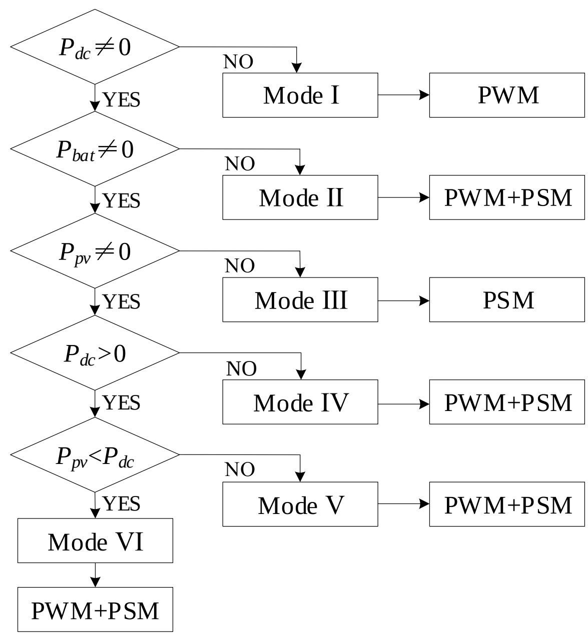

FIGURE 9. Operating mode flow chart.

The control diagram for different operating modes is shown in Fig. 9. The control process begins by evaluating the three power values: P_{pv}, P_{bat}, and P_{dc}. The energy router operates in at least two-port mode, meaning that at least two ports must have non-zero power values. The first step is to check whether P_{dc} is zero. If $P_{dc}=0$, the system operates in Mode I, with power flow only between the LV ports, corresponding to interleaved parallel boost PWM modulation. If $P_{dc}\neq0$, the next step is to check P_{bat}. If $P_{bat}=0$, the system enters Mode

II, requiring both PWM and PSM modulation. If $P_{bat} \neq 0$, the next check is P_{pv}. If $P_{pv} = 0$, Mode III is activated, where PWM is omitted, and only PSM modulation is used due to the unrestricted duty cycle D when $V_{pv} = 0$. If $P_{pv} \neq 0$, the direction of power flow is determined by the sign of P_{dc}: if $P_{dc} < 0$, Mode IV is activated; if $P_{dc} > 0$, the system enters either Mode V ($P_{pv} > P_{dc}$) or Mode VI ($P_{pv} < P_{dc}$). Modes IV–VI involve simultaneous operation of all three ports, requiring both PWM and PSM modulation.

C. ZVS CONDITION

1) HV Side MOSFETs

To ensure ZVS, C_{oss} of MOSFET should be fully discharged before the channel conducts. From an energy storage perspective, the minimum current required to charge and discharge the C_{oss} of two complementary MOSFETs in VQC is defined as

$$I_{ZVS1} = \sqrt{\frac{C_{oss(S_5-S_8)}V_{cd}^2}{2L_k}}. \tag{18}$$

To achieve ZVS, assuming I_{ZVS1} remains constant during the dead time, the following condition should be satisfied

$$I_{ZVS1} = V_{cd}C_{oss(S_5-S_8)}/t_d. \tag{19}$$

The current values of MOSFETs at the switching time derived in (11) should be larger than I_{ZVS}. Because of duty cycle of HV side MOSFETs equals to 0.5 and symmetry properties, the ZVS condition of HV side MOSFETs can be calculated

$$i_{L_k}(t_4) = -i_{L_k}(t_{10}) > I_{ZVS1}. \tag{20}$$

Based on the range of D and φ, the ZVS boundary can be derived as

$$\begin{cases} I_N(M-2D) > I_{ZVS1}, & 0 \leq \varphi < 0.5-D \\ I_N(M+2D+4\varphi-2) > I_{ZVS1}, & 0.5-D \leq \varphi < 0.5 \\ I_N(-M-2D) > I_{ZVS1}, & 0.5 \leq \varphi < 1-D \\ I_N(-M+2D+4\varphi-4) > I_{ZVS1}, & 1-D \leq \varphi < 1. \end{cases} \tag{21}$$

The ZVS boundary of HV side MOSFETs is plotted in Fig. 10, and the curved surface depends on three parameters D, φ and M. Below the surface is non-ZVS region, and the above region is ZVS range. When M is less than 1, there is a non-ZVS region when φ is close to 0/1 and D is close to 0.5. It can be seen that ZVS is achieved over the entire range of the HV side MOSFETs when the conversion ratio M is greater than or equal to 1.

2) LV side MOSFETs

According to the perspective of energy storage, the minimum current required to charge and discharge the C_{oss} of two complementary MOSFETs is defined as

$$I_{ZVS2} = \sqrt{2C_{oss}V_{bat}^2/L_k}. \tag{22}$$

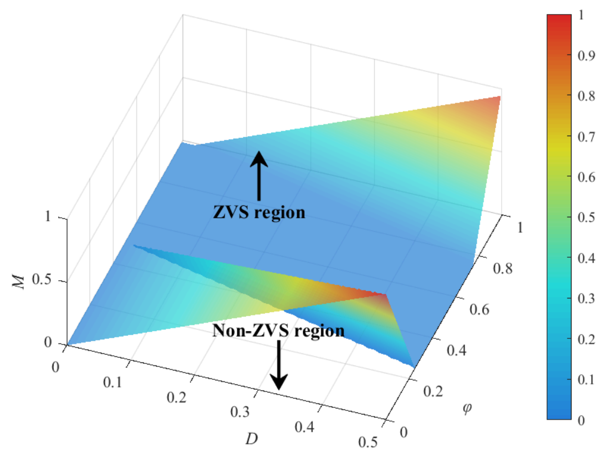

FIGURE 10. ZVS boundary of HV side MOSFETs S_5-S_8.

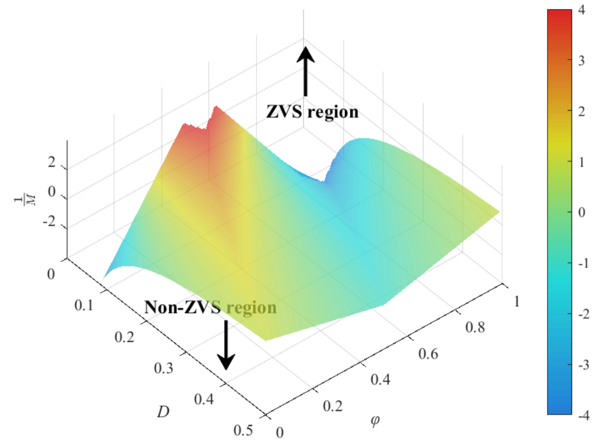

FIGURE 11. ZVS boundary of LV side MOSFETs S_1 and S_3.

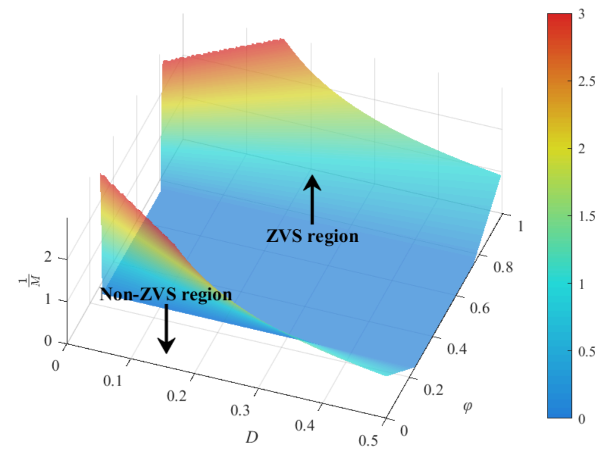

FIGURE 12. ZVS boundary of LV side MOSFETs S_2 and S_4.

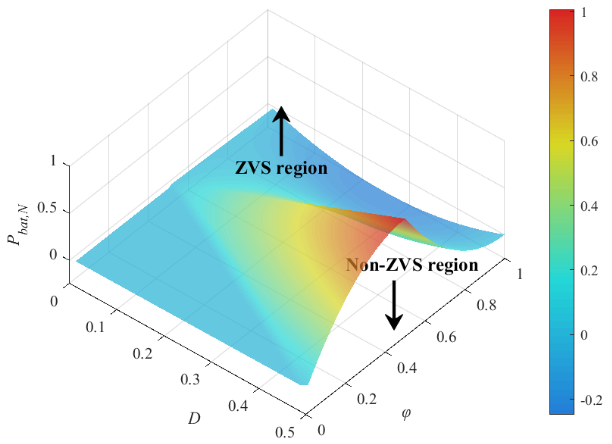

FIGURE 13. ZVS boundary of LV side MOSFETs vary with input power.

To achieve ZVS, assuming I_{ZVS2} remains constant during the dead time, the following condition should be satisfied

$$I_{ZVS2} = 2V_{bat}C_{oss(S_1-S_4)}/t_d. \tag{23}$$

The ZVS of LV side MOSFETs can be contributed by the interleaved boost units. As demonstrated in Fig. 5, the ZVS condition of the LV side MOSFETs can be expressed as

$$\begin{cases} S_1 : i_{L_1}(t_{S_1}) - ni_{L_k}(t_{S_1}) > I_{ZVS2} \\ S_2 : i_{L_1}(t_{S_2}) - ni_{L_k}(t_{S_2}) < -I_{ZVS2} \\ S_3 : i_{L_2}(t_{S_3}) + ni_{L_k}(t_{S_3}) > I_{ZVS2} \\ S_4 : i_{L_2}(t_{S_4}) + ni_{L_k}(t_{S_4}) < -I_{ZVS2} \end{cases} \tag{24}$$

where $t_{S_1}-t_{S_4}$ correspond to the turn-ON instants of S_1-S_4, respectively. According to the basic principles of the boost converter, i_{L_1} and i_{L_2} are derived as

$$\begin{cases} i_{L_1}(t_{S_1}) = i_{L_2}(t_{S_3}) = \dfrac{P_{pv}}{2V_{pv}} + \dfrac{V_{pv}(1-D)}{2f_sL} \\ i_{L_1}(t_{S_2}) = i_{L_2}(t_{S_4}) = \dfrac{P_{pv}}{2V_{pv}} - \dfrac{V_{pv}(1-D)}{2f_sL}. \end{cases} \tag{25}$$

Based on basic interleaved boost converter principles and steady-state analysis of the LV side circuit, the ZVS range can be derived as

$$\begin{cases} S_1 : P_{dc} + \gamma - 2(ni_{L_k}(t_2) + I_{ZVS2})DV_{bat} > P_{bat} \\ S_2 : P_{dc} - \gamma + 2(ni_{L_k}(t_0) + I_{ZVS2})DV_{bat} < P_{bat} \\ S_3 : P_{dc} + \gamma - 2(ni_{L_k}(t_2) + I_{ZVS2})DV_{bat} > P_{bat} \\ S_4 : P_{dc} - \gamma + 2(ni_{L_k}(t_0) + I_{ZVS2})DV_{bat} < P_{bat} \end{cases} \tag{26}$$

where γ defined as

$$\gamma = \frac{{V_{bat}}^2D^2(1-D)}{Lf_s}. \tag{27}$$

Combine (11), (14) and (26) the ZVS condition of low voltage side MOSFETs can be derived as equation (28) ,an the parameters are D, φ , M and input power.

Therefore, the ZVS region varies with D, φ, M, and input power can be plotted in Fig. 11-13. The region above the surface represents the ZVS range, while the region below corresponds to the non-ZVS area. It is worth noting that the ZVS conditions for S_1 and S_3 are identical, as are those for S_2 and S_4. Fig. 13 shows the ZVS boundary of the LV side MOSFETs as a function of input power, based on Equation 28. The trend indicates that the normalized battery power $P_{bat,N}$ increase with φ from 0 to 0.5, and decrease with φ from 0.5 to 1.

V. PARAMETER DESIGN METHODOLOGY

The proposed hybrid modulation scheme requires co-optimization of duty cycle D and phase shift φ to achieve three critical objectives:

1) Maintain zero-voltage switching (ZVS) across all active switches
2) Minimize circulating current (Fig. 6)
3) Ensure stable operation under 20% input voltage deviation

A. LEAKAGE INDUCTANCE OPTIMIZATION

Base the equations (12), (15), (18) and (20) ,the leakage inductance L_k directly governs three key performance metrics:

$$\begin{cases} I_{\text{rms}} \propto \frac{1}{L_k} & \text{(Conduction loss)} \\ P_{\max} \propto \frac{1}{L_k} & \text{(Power transfer capability)} \\ ZVS_{\text{range}} \propto \sqrt{L_k} & \text{(Soft-switching boundary)} \end{cases} \tag{29}$$

L_k=35 μH was selected to ensure the widest ZVS range and minimal circulating current. Specifically, it achieves less than 5% current ripple at full load, and 12.5 W total losses at rated power, compared to 18.4 W with L_k=80 μH.

B. TRANSFORMER DESIGN

The integrated magnetic structure, which combines leakage inductance with the main transformer, results in a 36% reduction in volume compared to conventional designs, decreasing from 213.1 cm^3 [35] to 136.1 cm^3 as shown in Fig. 14. Their magnetic component volume are summarized and compared with the conventional structures in Table 1. The key design parameters are as follows:

The turns ratio is determined by the equation:

$$n = \frac{4V_{pv,\min}}{DV_{dc}} = \frac{4\times 15}{D\times 800} = \left(\frac{0.3}{D}\right) : 4$$

For practical implementation, the turns ratio is adjusted to 1:4. The transformer uses a PC40 core and incorporates the following optimizations:

Leakage inductance is controlled by adjusting the airgap between 0.5-1.2mm, achieving a target L_k of 35μH. Additionally, the transformer employs an interleaved winding structure, which reduces AC resistance compared to conventional sandwich winding, thereby balancing the losses.

$$\begin{cases} P_N\sigma - \gamma + 2(nI_N(M-2D-4M\varphi) + I_{ZVS2})DV_{bat} < P_{bat}, & 0 \le \varphi < 0.5-D \\ P_N(-\sigma+2D-(2\varphi-1)^2) - \gamma + 2(nI_N(M-2D-4M\varphi) + I_{ZVS2})DV_{bat} < P_{bat}, & 0.5-D \le \varphi < 0.5 \\ P_N(-\sigma+2D) - \gamma + 2(nI_N(-3M-2D+4M\varphi) + I_{ZVS2})DV_{bat} < P_{bat}, & 0.5 \le \varphi < 1-D \\ P_N(\sigma-4D+4(\varphi-1)^2) - \gamma + 2(nI_N(-3M-2D+4M\varphi) + I_{ZVS2})DV_{bat} < P_{bat}, & 1-D \le \varphi < 1. \end{cases} \tag{28}$$

TABLE 1. Magnetic Component Volume Comparison

Component	Conventional	Proposed
Transformer	136.1 cm^3	136.1 cm^3
Inductor	77 cm^3	Integrated
Total	213.1 cm^3	136.1 cm^3

C. COMPONENT STRESS ANALYSIS

Table 2 compares voltage stresses across different rectifier topologies. The proposed VQC structure achieves a 50% reduction in MOSFET voltage stress (400 V vs. 800 V conventional). The improvement significantly enhances the reliability and efficiency of the system.

For practical implementation, 650 V/60 mΩ SiC MOSFETs (GC3M0060065K) were selected. Capacitor derating was applied with a high voltage rating (630 V caps for 420 V actual stress), ensuring long-term reliability and performance. These design choices strike a balance between component stress and system efficiency, making the proposed design suitable for high-performance applications.

TABLE 2. Comparison of Component Voltage Stress

Secondary-side Rectifier	MOSFETs & Diodes	Capacitors
Half-wave rectifier	$2V_{dc}$	V_{dc}
Full-wave rectifier	$2V_{dc}$	V_{dc}
Full-bridge rectifier	V_{dc}	V_{dc}
This work	$V_{dc}/2$	$V_{dc}/2, V_{dc}/4$

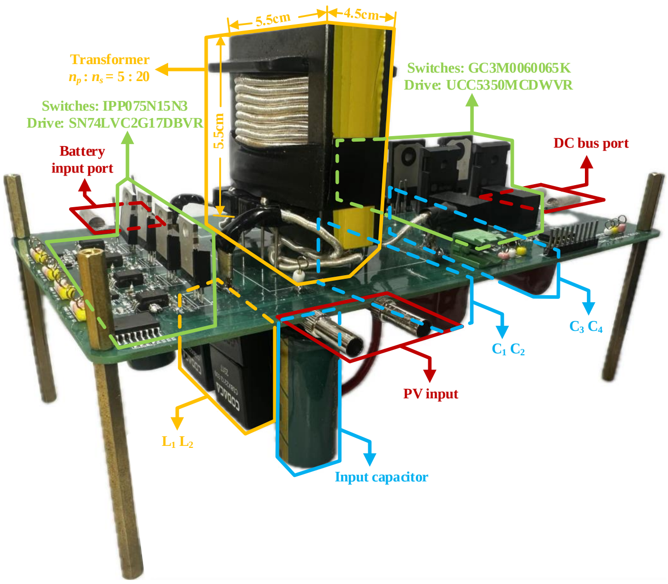

FIGURE 14. Photo of the designed prototype

TABLE 3. Design Parameters

Symbol	Description	Parameters
V_{pv}	PV voltage	15-40 V
V_{bat}	Battery voltage	40-50 V
V_{dc}	dc bus voltage	800 V
f_s	switching frequency	100 kHz
$L_{1,2}$	Buck/Boost inductor	80 μH
T	Transformer core	PC40
L_k	Leakage inductance of TX	35 μH
$n_p : n_s$	Winding ratio of TX	5:20
$C_1 - C_4$	HV side capacitor	3.3 μF
$S_1 - S_4$	LV side MOSFETs	IPP075N15N3
$S_5 - S_8$	HV side MOSFETs	GC3M0060065K

VI. EXPERIMENTAL RESULTS AND COMPARISON

To validate the effectiveness of the proposed converter, a 500 W prototype is designed, with key design parameters listed in Table 3. The prototype is presented in Fig. 14. The PV source is emulated by a programmable dc power supply. The battery and dc bus are emulated by a programmable dc power source in parallel with an electric load. The digital control algorithm is implemented in TMS28379 microcontroller from Texas Instruments.

A. EXPERIMENTAL RESULTS

In Mode I, Fig. 15 shows the steady-state inductor current waveforms, highlighting a significant reduction in current ripple at the PV source due to the interleaved structure. PWM control is employed in this mode, enabling MPPT of the PV source. Fig. 15(a) presents the waveforms with V_{pv} = 15 V, V_{bat} = 50 V, and P_{pv} = 120 W, resulting in a duty cycle D of 30%. In Fig. 15(b), with V_{pv} = 25 V, V_{bat} = 50 V, and P_{pv} = 200 W, the duty cycle of the LV side MOSFETs is 50%.

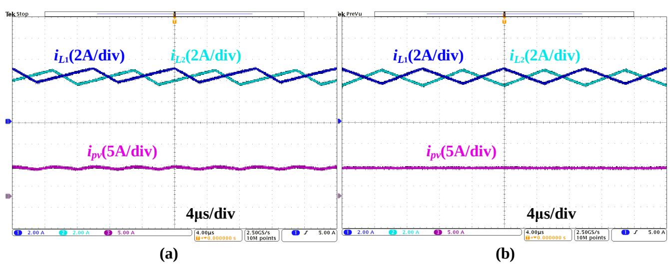

FIGURE 15. Mode I interleaved current waveforms (a) V_{pv} = 15 V, V_{bat} = 50 V, P_{pv} = 150 W. (b) V_{pv} = 25 V, V_{bat} = 50 V, P_{pv} = 250 W.

Under these conditions, the current ripple from the PV source is effectively canceled.

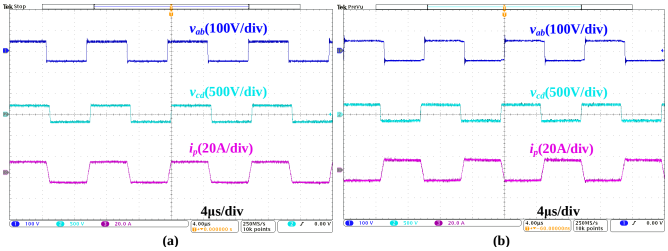

FIGURE 16. **Steady-state waveforms in Mode III forward and backward power flow waveforms:(a) forward V_{bat} = 50 V, V_{dc} = 800 V, P_{dc} = 500 W; (b) backward V_{bat} = 50 V, V_{dc} = 800 V, P_{dc} = -500 W.**

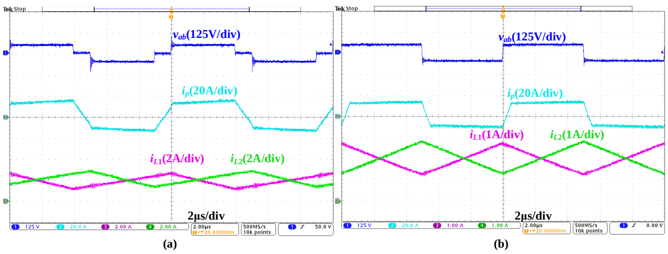

FIGURE 17. **Steady-state waveforms in Mode VI when (a) V_{pv} = 20V, V_{bat} = 50V, V_{dc} = 800V, P_{pv} = 160W, P_{dc} = 500W. (b)V_{pv} = 25V, V_{bat} = 50V, V_{dc} = 800V, P_{pv} = 200W, P_{dc} = 500W.**

The steady-state experimental waveforms for Mode III are shown in Fig. 16. The operating principles of Modes II-VI which using PWM plus PSM control are similar, with differences only in the power distribution among the three ports. Therefore, only the waveforms for Mode III and Mode VI are presented. In Mode III, the PV source is idle, and the average currents of i_{L_1} and i_{L_2} are zero. The power flow is controlled by the phase shift angle between the LV and HV sides. The side with the leading phase acts as the source, while the lagging side functions as the load. Fig. 16(a) presents the steady-state waveforms for forward power flow at 500 W. In contrast, Fig. 16(b) shows the steady-state waveforms for backward power flow at 500 W. The phase shift angles are determined using the equation 14, and the system operates within the ZVS region, as confirmed by the analysis results from equations (21) and (28).

Experimental waveforms of v_{ab}, i_p, i_{L_1}, and i_{L_2} for different PV voltages in three-port modes are shown in Fig. 17. Fig. 17(a) shows the experimental results in Mode VI, where the PV source provides 20 V and 160 W, while the dc bus absorbs 500 W. The excess power is supplied by the battery. The current ripple at the PV terminal is reduced due to the interleaved structure. Although ZVS is lost at this operating point, the RMS current remains relatively small, which results from a trade-off between switching losses and conduction losses. In Fig. 17(b), the PV source operates at 25 V and provides 200 W, with the battery supplying the remaining power. The waveforms illustrate that the sum of the currents through L_k, L_1, and L_2 contributes to achieving ZVS for the primary side MOSFETs. Additionally, the current through the series inductor aids in achieving ZVS for the active MOSFETs on the HV side.

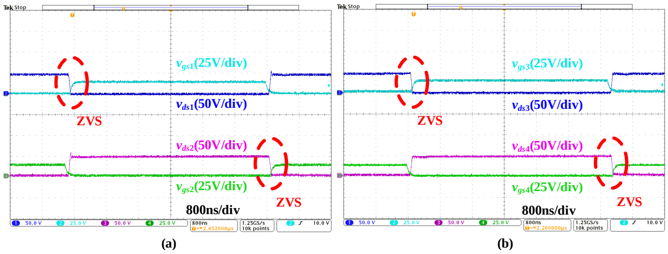

FIGURE 18. **Soft-switching waveforms of the LV side MOSFETs of (a) $S_{1,2}$. (b) $S_{3,4}$.**

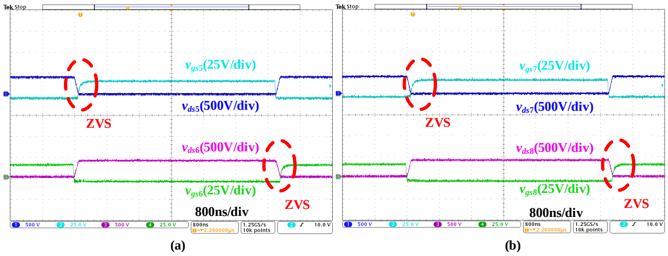

FIGURE 19. **Soft-switching waveforms of the HV side MOSFETs of (a) $S_{5,6}$. (b) $S_{7,8}$.**

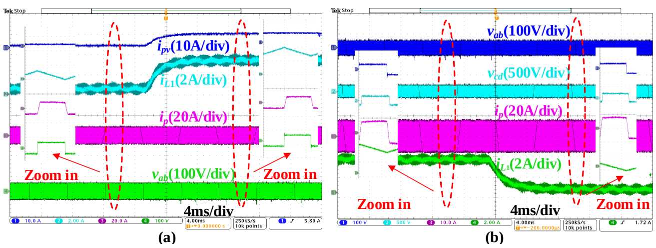

FIGURE 20. **Dynamics when (a) PV power steps from 10 to 200 W in Mode VI. (b) mode transition Mode VI to III.**

Critical soft-switching waveforms for Modes IV–VI are shown in Figs. 18 and 19. As illustrated in Fig. 18, there is no overlap between the rising edge of v_{gs} and the falling edge of v_{ds}, confirming ZVS for the LV side MOSFETs (S_{1-4}). In Fig. 19, ZVS for the HV side MOSFETs (S_{5-8}) is also demonstrated. In this case, the v_{gs} of HV side MOSFETs experience a negative voltage during turn-off, and ZVS is still achieved as the devices turn on when the voltage across v_{ds} is zero. Those soft-switching conditions ensure efficient operation by reducing switching losses.

Fig. 20 illustrates the dynamic waveforms during power and operation mode transitions. Fig. 20(a) shows the power transition resulting from a step change in the PV source. In this case, the converter operates in Mode VI, where both the PV source and the battery provide power to the dc bus. As seen in this figure, the power from the PV source jumps from 10 W to 200 W instantaneously, while the dc bus power remains constant at 500 W. Consequently, the currents i_{L_1}, i_{L_2}, and i_{pv} experience a sudden increase. To maintain the dc bus power, the battery side power is reduced, and the total power flow through the energy router remains constant during the transition. As observed, there is minimal effect on i_p and

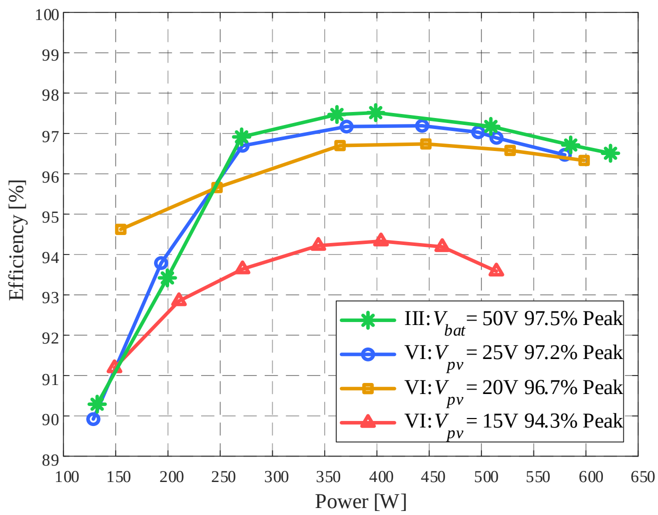

FIGURE 21. Measured efficiency versus output power with different PV voltages.

i_{L_k} during this process. Fig. 20(b) demonstrates the dynamic waveforms during the operation mode transition from Mode VI to Mode III, emulating the transition from daytime to nighttime operation. During this transition, the battery compensates for the decrease in PV power to maintain the dc bus power, P_{dc}, which is set to 400 W in this experiment. The transition occurs smoothly without any noticeable transients, which confirms the excellent dynamic performance of the proposed converter.

Conversion efficiency at different modes and input voltages is recorded and plotted in Fig. 21. The efficiency data is calibrated using a high-precision power analyzer (LMG641 from ZIMMER Ltd). In Mode III, the efficiency is measured under the conditions $V_{bat} = 50$ V and $V_{dc} = 800$ V, with a peak efficiency of 97.5%. In Modes IV-VI, the efficiency is measured for $V_{pv} = 15$ V, 25 V, and 25 V, respectively. Only the efficiency data for Mode VI, where all ports are actively involved in power flow, is presented. The peak efficiency for the different input voltages of V_{pv}= 25 V, 20 V, and 15 V are 97.2%, 96.7%, and 94.3%, respectively. The overall efficiency remains above 90% across the entire power range in all operation modes. Compared to the efficiency at heavy load, the light-load efficiency decreases when the power is below 200 W due to the loss of ZVS in light-load conditions. Additionally, the efficiency curve for $V_{pv} = 25$ V drops faster than those for V_{pv} = 15 V and 20 V. This is because the duty cycle for $V_{pv} = 25$ V is 50%, resulting in a two-level voltage (v_{ab}) on the LV side, whereas the other two cases exhibit a three-level voltage on the LV side.

B. PERFORMANCE COMPARISON

A qualitative comparison between the proposed converter and several recently reported partially isolated energy routers and high boost ratio converters is summarized in Table **??**. As shown, the proposed solution offers flexible power flow control through a combination of PWM and PSM, while maintaining a simplified structure without the need for additional components. Notably, unlike conventional control methods that require complex modulations or inner phase shifts on both sides, the proposed topology only requires phase-shift modulation between the LV and HV sides, without the need for internal phase shifts or PFM modulation. Additionally, the proposed converter is characterized by a medium ZVS range, multidirectional power flow, MPPT capability, and high efficiency. In addition, compared to high boost ratio converters, the proposed converter achieves a higher boost ratio and offers the advantage of bidirectional power flow.

VII. CONCLUSION

This manuscript presents a novel energy router topology to achieve high step-up ratio, multidirectional power flow, and efficiency across a wide input voltage range simultaneously in 800V dc microgrid applications. By incorporating a VQC with an interleaved boost stage and a full-bridge stage, the converter achieves high boost ratio, reduced component count, and balanced voltage stress on both capacitors and MOSFETs. A hybrid modulation scheme combining PWM and PSM is introduced. The hybrid modulation scheme ensures ZVS and minimizes circulating current, optimizing efficiency and enhancing system reliability. Experimental results demonstrate efficient operation with input voltages ranging from 15 V to 25 V at the PV port, delivering a high output voltage of 800 V and a rated power of 500 W. The peak efficiency reaches 97.5%, with the overall efficiency exceeding 90% in various operating modes and power levels, demonstrating excellent dynamic response and minimal voltage stress. Comparative analysis also highlights the superior performance of the proposed converter in modulation simplicity, efficiency, and operational flexibility.

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TABLE 4. Comparison with Existing Reported Partially Isolated Energy Routers and High Boost Ratio Converters

Converters	Ref.	Modulation	Low-voltage side		V_{dc} [V]	ZVS*	Bi-dir§	$\eta(\%)^\dagger$	Voltage gain
			V_{pv}[V]	V_{bat}[V]					
Energy routers	[13]	PWM+PFM+PSM	200	60-110	64.5	W	No	92	0.32
	[15]	PWM+PSM	70-100	42	300	W	No	97.6	7.1
	[16]	PWM	45	90	380	W	No	95.6	8.4
	[20]	PWM+PFM+PSM	70-100	180-210	400	W	Yes	98	5.7
	[33]	PWM+PSM	20-40	60	760	W	No	98.2	38
This work	-	PWM+PSM	15-40	40-50	800	M	Yes	97.5	53
High boost ratio converters	[14]	PWM	35-45		380	M	Yes	97.3	11
	[23]	PWM+PSM	20		400	N	No	96	20
	[27]	PWM	38-48		380	W	No	96.4	10
	[28]	PWM	30-60		600	N	No	94	20
	[29]	PWM	42		326-400	M	No	97.1	10
	[31]	PWM+PSM	20-28		380	W	No	96.3	19
	[32]	PWM	26		380	M	Yes	95.8	15

* ZVS range: W = Wide, M = Medium, N = Narrow.
§ 'Yes' indicates bidirectional power flow, while 'No' denotes unidirectional power flow.
† $\eta(\%)$ shows the peak efficiency within all the working modes.

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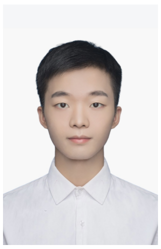

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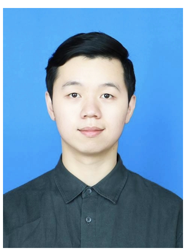

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