## Название документа

Спецификация на A7105, 2.4ГГц FSK/GFSK Приемопередатчик со скоростью передачи данных 2 Кбит/с ~ 500 Кбит/с

## История изменений

| Изм. No. | История | Дата выпуска | Замечание |
|---|---|---|---|
| 0.0 | Первоначальный выпуск. | Дек 27, 2007 | Предварительный |
| 0.1 | Изменена спецификация и добавлен раздел для настройки мощности TX | Фев 20, 2008 | Предварительный |
| 0.2 | Добавлена информацию о маркировке, профиль оплавления, размеры ленты и катушки для транспортировки | Окт. 9 , 2008 | Предварительный |
| 0.3 | Изменено описание состояния и режима FIFO<br>Переименовано IRQS1/IRQS2 в GIO1S/GIO2S<br>Переименовано GPIO1/GPIO2 в GIO1/GIO2<br>Добавлены Легкий режим FIFO, Сегментный режим FIFO<br>Удалена функция термодатчика / измерение внешнего напряжения<br>Удалена функция TWWS<br>Добавлена диаграмма состояния быстрого/нормального/энергосберегающего режима FIFO<br>Добавлена диаграмма состояния прямого режима<br>Переименовать MAster Clock $F_{CSCK}$ в $F_{MCLK}$<br>Измените поддержку скорости передачи данных с 1K~500K на 2K ~ 500K | Янв. 7, 2009 | Предварительный |
| 1.0 | Пересмотрено описание статуса и режима FIFO<br>Удалены ненужные компоненты схемы в приложении<br>Добавлена кривая RSSI<br>Добавлено руководство по макету | Август, 2009 | Полный Производство |
| 1.1 | Пересмотрено мин. рабочее напряжение от 1.9V до 2.0V и типичный ток TX (0dBm) с 19мА до 20мА | Фев., 2010 | Полный Производство |
| 1.2 | Добавлено примечание 9 в главу 8, спецификация.<br>Исправлена опечатка на страницах (51, 52, 57, 62, 66, 78, 79). | Ноя., 2010 | Полный Производство |
| 1.3 | Изменено Английское Название Компании | Ноя. 30, 2010 | Полный Производство |
| 1.4 | Пересмотрено описание контактов VDA1, VDA2, VDA3 в Ch5. и изменена информация о катушке ленты и добавлен адрес офиса Shenzhen. | Янв., 2011 | Полный Производство |

## Содержание

## 1. Общее описание

A7105 - это высокопроизводительный и недорогой беспроводной приемопередатчик диапазона ISM 2,4 ГГц. Это устройство объединяет в себе как высокочувствительный приемник (-95дБм при 500 Кбит/с), так и высокоэффективный усилитель мощности (до 1 дБм). При низкой скорости передачи данных A7105 обладает особой устойчивостью на дальнем расстоянии прямой видимости из-за своей сверхвысокой чувствительности (-107дБм при 2 Кбит/с, -104дБм при 25 Кбит/с) без необходимости внешней LNA или PA. Регистр скорости передачи данных (0x0E) позволяет пользователю настроить скорость передачи данных от 2 Кбит/с до 500 Кбит/с.

A7105 имеет быстрое время настройки (130 мкс) для систем скачкообразной перестройки частоты. Для обработки пакетов A7105 имеет встроенный разделенный 64-байтовый TX/RX FIFO (может быть расширен до 256 байт) для буферизации данных и пакетной передачи, CRC для обнаружения ошибок, FEC для 1-битной коррекции данных на кодовое слово, RSSI для оценки качества канала, отсеивание данных для шифрования / дешифрования данных. Эти функции очень просты в использовании при разработке беспроводной системы. Все функции интегрированы в небольшой чип QFN 4X4 20 контактов.

К управляющим регистрам A7105 можно легко получить доступ через 3-проводную или 4-проводную шину SPI. Для экономии энергии A7105 поддерживает спящий режим, режим ожидания. Для удобства использования A7105 имеет уникальный набор команд SPI под названием Strobe commAnd, которые используются для управления. Основываясь на стробоскопических командах через шину SPI, MCU может управлять всем: от энергосбережения, отправки TX, приема RX, мониторинга каналов, скачкообразной перестройки частоты до автоматической калибровки. Кроме того, A7105 поддерживает две линии ввода-вывода общего назначения, GIO1 и GIO2, чтобы сообщить MCU его статус, чтобы MCU мог использовать либо опрос, либо схему прерывания для выполнения радиоуправления. Следовательно, очень легко контролировать радиопередачу между MCU и A7105 из-за его цифрового интерфейса.

## 2. Типичные области применения

- Беспроводные клавиатуры и мыши
- Дистанционное управление
- Радиоуправление вертолетом и самолетом
- 2400 ~ 2483.5 МГц ISM система
- Беспроводное измерение и автоматизация зданий
- Беспроводные игрушки и игровые контроллеры

## 3. Характеристики

- Малый размер (QFN4 X4, 20 контактов).
- Частотный диапазон: 2400 ~ 2483.5МГц.
- FSK или GFSK модуляция
- Низкое потребление тока: RX 16мА, TX 20мА (при выходной мощности 0 дБм).
- Низкий ток сна (1.5 мкА).
- Имеет регулятор напряжения, поддерживаемое напряжение 2.0 ~ 3.6 В.
- Программируемая скорость передачи данных от 2 Кбит/с до 500 Кбит/с.
- Программируемый уровень мощности TX – от 20 дБм до 1 дБм.
- Сверхвысокая чувствительность:
  - -95дБм при скорости передачи данных 500Кбит/с.
  - -97дБм при скорости передачи данных 250Кбит/с
  - -104дБм при скорости передачи данных 25Кбит/с
  - -107дБм при скорости передачи данных 2Кбит/с
- Быстрое время настройки (130 us) для системы скачкообразной перестройки частоты.
- Встроенный детектор батареи.
- Поддержка недорогого генератора (6 / 8 /12 / 16 / 20 / 24МГц).
- Поддержка совместного использования генератора, (1 / 2 / 4 / 8МГц) с MCU.
- Поддержка частотной компенсации.
- Простота использования.
  - Поддержка 3-проводного или 4-проводного SPI.
  - Уникальная стробоскопическая команда через SPI.
  - Настройка ОДНОГО регистра для новой частоты канала.
  - 8-битный цифровой RSSI для четкой индикации канала.
  - Режим быстрого обмена при переключении ролей TRX.
  - Автоматическое измерение RSSI.
  - Автоматическая калибровка.
  - Автоматическая функция IF.
  - Автоматическая проверка CRC.
  - Авто FEC (7, 4) код Хэмминга (1 бит коррекции ошибок/кодовое слово).

- Отсеивание данных для шифрования и дешифрования.
- Разделенные 64 байта RX и TX FIFO.
- Простое расширение FIFO / Segment FIFO / FIFO (до 256 байт).
- Поддержка прямого режима тактового выхода на MCU.
- Поддержка режима FIF с сигналом синхронизации кадров с MCU.

## 4. Конфигурация контактов

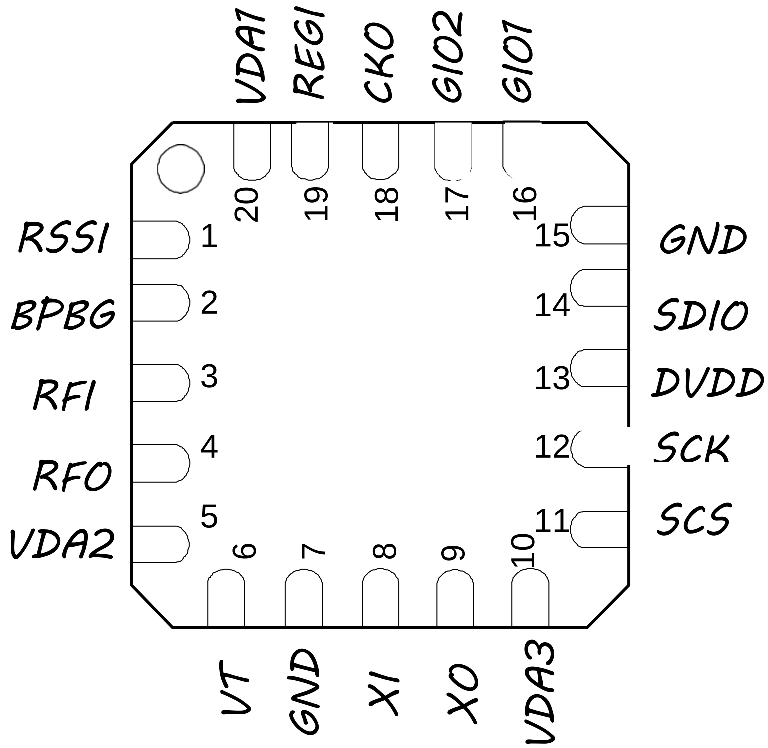



Рис 4-1. A7105 QFN 4x4 Вид сверху

## 5. Описание контактов (I: ввод; O: вывод, I/O: ввод и вывод)

| Контакт No. | Обозначение | I/O | Описание функции |
|---|---|---|---|
| 1 | RSSI | O | Подключен к байпасному конденсатору для считывания RSSI. |
| 2 | BPBG | O | Соединен с байпасным конденсатором для внутренней точки смещения регулятора |
| 3 | RFI | I | Вход усилителя с низким уровнем шума. |
| 4 | RFO | O | Выход усилителя мощности. (питается от VDA1) |
| 5 | VDA2 | I/O | Источник напряжения TRX **(от внутреннего аналогового регулятора IC)**, подключенный к байпасному конденсатору. |
| 6 | VT | I | Вход управления частотой VCO |
| 7 | GND | G | Земля |
| 8 | XI | I | Входной узел кварцевого генератора |
| 9 | XO | O | Выходной узел кварцевого генератора |
| 10 | VDA3 | I | Источник напряжения **(от VDA1, конт. 20)** для PLL |
| 11 | SCS | I | 3-проводный SPI выбор чипа. |
| 12 | SCK | I | 3-проводный SPI тактирование. |
| 13 | DVDD | I | Источник напряжения TRX (от внутреннего цифрового регулятора IC), подключенный к байпасному конденсатору. |
| 14 | SDIO | I/O | 3-проводный SPI для чтения/записи данных SPI. |
| 15 | GND | G | Земля |
| 16 | GIO1 | I/O | Многофункциональный GIO 1 / 4-проводной вывод данных SPI. |
| 17 | GIO2 | I/O | Многофункциональный GIO 2 / 4-проводной вывод данных SPI. |
| 18 | CKO | O | Многофункциональный тактовый выход. |
| 19 | REGI | I | Вход внутреннего регулятора **(Внешний Вход Питания)** |
| 20 | VDA1 | I/O | Выход внутреннего аналогового регулятора для питания **RFO (конт. 4) и VDA3 (конт. 10).** |
| | **Задняя пластина** | G | Земля.<br>Задняя пластина должна быть хорошо припаяна к земле; в противном случае это повлияет на радиочастотные характеристики. |

## 6. Блок-схема чипа

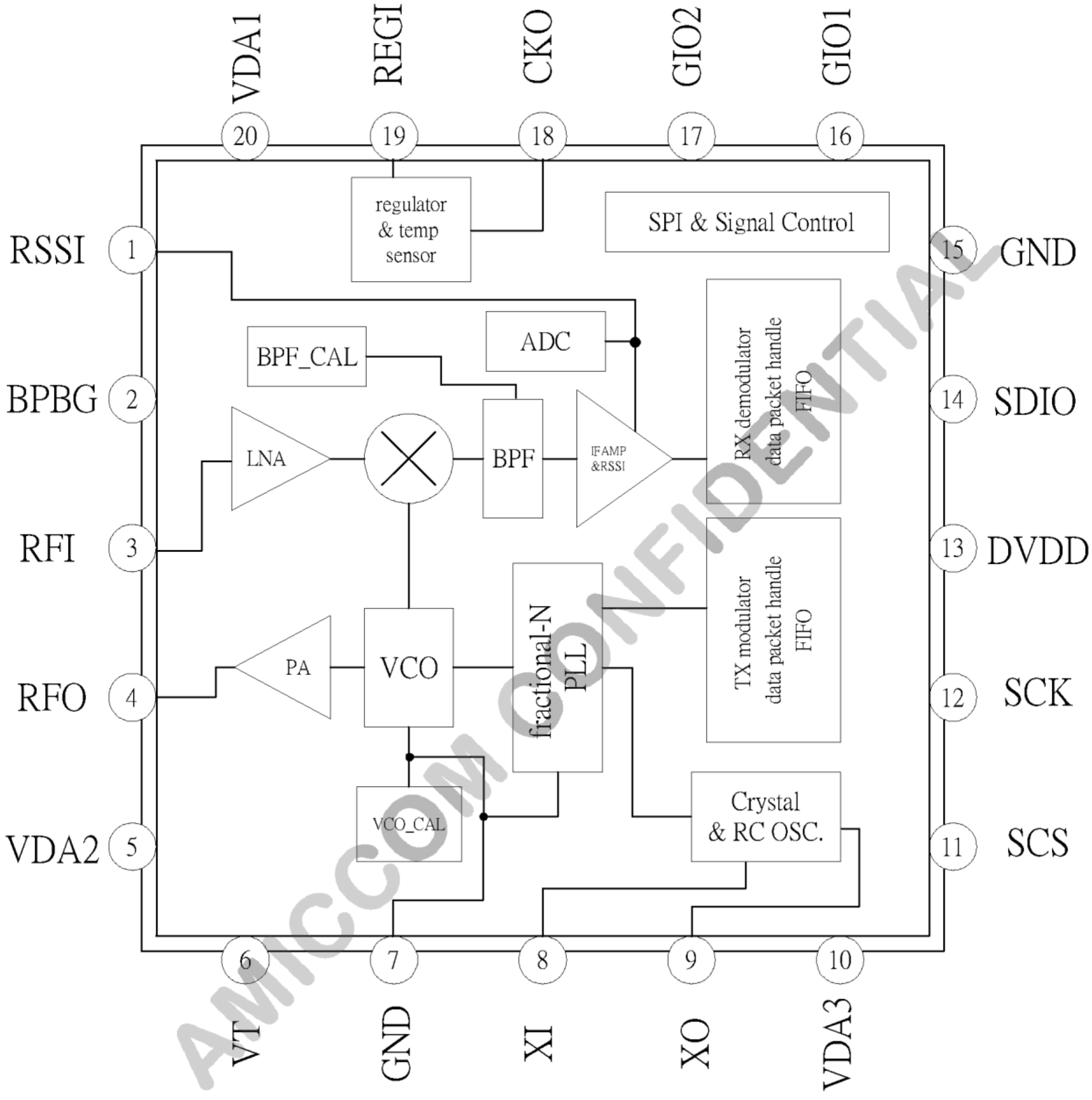



Рис 6-1. A7105 Блок-схема

## 7. Абсолютный максимум номинальных параметров

| Параметр | Относительно | Номинальное значение | Единица измерения |
|---|---|---|---|
| Питающее напряжение (VDD) | GND | -0.3 ~ 3.6 | В |
| Цифровые IO выводы | GND | -0.3 ~ VDD+0.3 | В |
| Напряжение на аналоговых выводах | GND | -0.3 ~ 2.1 | В |
| Входной RF уровень | | 5 | дБм |
| Температура хранения | | -55 ~ 125 | °C |
| ESD | HBM | ± 2K | В |
| | MM | ± 100 | В |

*Напряжения, превышающие значения, указанные в разделе “ Абсолютный максимум номинальных параметров”, могут привести к необратимому повреждению устройства. Это только номинальные напряжения; функциональная работа устройства при этих или любых других условиях, превышающих указанные в эксплуатационных разделах настоящей спецификации, не подразумевается. Воздействие абсолютных максимальных номинальных условий в течение длительного периода времени может повлиять на надежность устройства.

* Устройство чувствительно к ESD. Используйте соответствующие меры предосторожности при ESD. HBM (Режим человеческого тела) тестируется по методу MIL-STD-883FMethod 3015.7. MM (Машинный режим) тестируется по методуJEDEC EIA/JESD22-A115-A.
* Прибор имеет уровень чувствительности к влаге III (MSL 3).

## 8. Электрические характеристики

(Ta=25℃, VDD=3.0В, скорость передачи данных = 500Кбит/с, IF пропускная способность = 500кГц, $F_{XTAL}$ =16МГц, с матчевой сетью и фильтром нижних частот, регулятор в чипе = 2.1В, если не указано иное.)

| Параметр | Описание | Мин. | Типичное | Макс. | Единица измерения |
|---|---|---|---|---|---|
| **Общие** | | | | | |
| Рабочая температура | | -40 | | 85 | °C |
| Напряжение питания (VDD) | с внутренним регулятором | 2.0 | | 3.6 | В |
| Потребляемый ток | Спящий режим (RC OSC off) | | 1.5*1 | | мкА |
| | Холостой ход (Regulator on) | | 0.3*1 | | мА |
| | Режим ожидания (XOSC on,clock generator on) | | 1.9 | | мА |
| | PLL mode | | 9 | | мА |
| | RX Mode | | 16 | | мА |
| | TX Mode (@0дБм output) | | 20 | | мА |
| | TX Mode (@-3дБм output) | | 16 | | мА |
| | TX Mode (@-6дБм output) | | 14.5 | | мА |
| | TX Mode (@-11дБм output) | | 13.9 | | мА |
| | TX Mode (@-20дБм output) | | 12.5 | | мА |
| **PLL блок** | | | | | |
| Время запуска *2 | | | 0.6 | | мс |
| Частота | | 6, 8, 12, **16**, 20, 24 | | | МГц |
| Допуск | без FW FC | ±1<br>0 | | | ppm |
| | с FW FC | ±2<br>0 | | | ppm |
| ESR | | | | 80 | Ом |
| VCO Рабочая частота | | 2400 | | 2483.5 | МГц |
| PLL фазовый шум | Смещение 10k<br>Смещение 100K<br>Смещение 1M | | 80<br>85<br>90 | | дБн |
| PLL время успокоения *3 | @Loop BW = 500КГц | | 70 | | мкс |
| **Передатчик** | | | | | |
| Диапазон выходной мощности | | -20 | 0 | | дБм |
| Внеполосное паразитное излучение *4 | 30МГц~1ГГц | | | -36 | дБм |
| | 1ГГц~12.75ГГц | | | -30 | дБм |
| | 1.8ГГц~ 1.9ГГц | | | -47 | дБм |
| | 5.15ГГц~ 5.3ГГц | | | -47 | дБм |
| Отклонение частоты *5 | Data rate > 50КБит/с | | 186K | | Гц |
| | Date rate <=50КБит/с | | 124K | | Гц |
| Скорость передачи данных | | 2K | | 500K | Бит/с |
| Время готовности TX *6 (PLL к WPLL + WPLL к TX) | @Loop BW = 500 КГц, LO fixed | | 10+60 | | мкс |
| | @Loop BW = 500 КГц, Hopping | | 70+60 | | мкс |
| **Приемник** | | | | | |
| Чувствительность приемника @ BER = 0.1% | Data rate 500K ($F_{IF}$ = 500КГц) | | -95 | | дБм |
| | Data rate 250K ($F_{IF}$ = 500КГц) | | -97 | | дБм |

| | | | | | |
|---|---|---|---|---|---|
| | Data rate 25K ($F_{IF}$ = 500КГц) | | -104 | | дБм |
| | Data rate 2K ($F_{IF}$ = 500КГц) | | -107 | | дБм |
| IF полоса пропускания частоты | | | 250/500 | | КГц |
| IF центральная частота | | | 250/500 | | КГц |
| Вмешательство *7 | Co-Channel ($C/I_0$) | | 11 | | дБ |
| | ±1МГц Adjacent Channel | | - 20 | | дБ |
| | ±2МГц Adjacent Channel | | - 30 | | дБ |
| | > ±5МГц Adjacent Channel | | - 40 | | дБ |
| | IмAge ($C/I_{IM}$) | | - 12 | | дБ |
| Максимальная рабочая входная мощность | @RF input (BER=0.1%) | | | 0 | дБм |
| Паразитная эмиссия *4 | 30МГц~1ГГц | | | -57 | дБм |
| | 1ГГц~12.75ГГц | | | -47 | |
| RSSI Диапазон | @RF input | -105 | | -50 | дБм |
| Время готовности RX *8 (PLL к WPLL + WPLL к RX) | LO fixed: Data rate < = 125 КБит/с | | 10+40 | | мкс |
| | LO fixed: Data rate = 250 КБит/с | | 10+100 | | мкс |
| | LO fixed: Data rate = 500 КБит/с | | 10+60 | | мкс |
| | Hopping: Data rate < = 125 КБит/с | | 70+40 | | мкс |
| | Hopping: Data rate = 250 КБит/с | | 70+100 | | мкс |
| | Hopping: Data rate = 500 КБит/с | | 70+60 | | мкс |
| RX Паразитная эмиссия | свыше 1ГГц | | | -47 | дБм |
| **Регулятор** | | | | | |
| Время установления регулятора | Вывод 2 соединить с 1.5 нФ | | 500*9 | | мкс |
| Опорное напряжение | | | 1.23 | | В |
| Выходное напряжение регулятора | | 1.8 | 2.1 | 2.3 | В |
| Линейное регулирование | Ток нагрузки 30мА | 35 | 40 | | дБн |
| **Характеристики уровней цифрового ввода-вывода** | | | | | |
| Высокий Входное напряжение ($V_{IH}$) | | 0.8*VDD | | VDD | В |
| Низкий Входное напряжение ($V_{IL}$) | | 0 | | 0.2*VDD | В |
| Высокий Выходное напряжение ($V_{OH}$) | @$I_{OH}$= -0.5мА | VDD-0.4 | | VDD | В |
| Низкий Выходное напряжение ($V_{OL}$) | @$I_{OL}$= 0.5мА | 0 | | 0.4 | В |

Примечание 1: Когда цифровые контакты ввода-вывода сконфигурированы на ввод, эти контакты НЕ должны быть плавающими, а должны подтягиваться либо питанию, либо к земле (SCS должен подтягиваться только к питанию); в противном случае будет индуцирован ток утечки.
Примечание 2: Обратитесь к Регистру задержки II (17h), чтобы настроить задержку успокоения.
Примечание 3: Обратитесь к Регистру задержки I (17h) для настройки PDL (PLL settling delay).
Примечание 4: С внешним радиочастотным фильтром, который обеспечивает минимальное затухание 17 дБ в диапазоне: 30МГц~2ГГц и 3ГГц~12,75ГГц.
Примечание 5: Обратитесь к регистру TX II (15h) для настройки FD [4:0].
Примечание 6: Для настройки задержки PDL и TDL обратитесь к Регистру задержки I (17h).
Примечание 7: Уровень мощности искомого сигнала устанавливается на уровне чувствительности +3 дБ. Данные модуляции для искомого сигнала и интерферометра PN9 и PN15 соответственно. Расстояние между каналами составляет 500 кГц.
Примечание 8: Для 250К/500КБит/с установите DCM[1:0]= [10b] по ID, (29h). Для <= 125Кбит/с установите DCM[1:0]= [01b] по преамбуле (29h).
Примечание 9: При VDD < 2,1В и температуре < -30°C время установления регулятора составит до 20мс.

## 9. Управляющие регистры

A7105 содержит 51 x 8-бит управляющий регистр. MCU может получить доступ к этим управляющим регистрам через 3-проводный (SCS, SCK, SDIO) или 4-проводный (SCS, SCK, SDIO, GIO1/GIO2) SPI-интерфейс (поддержка макс. скорость передачи данных SPI до 10 Мбит/с). Пользователь может обратиться к главе 10 для получения подробной информации о временных задержках SPI. A7105 управляется просто регистрами и выводит свое состояние на микроконтроллер выводами GIO1 и GIO2.

### 9.1 Таблица управляющих регистров

| Адрес / Имя | R/W | Бит 7 | Бит 6 | Бит 5 | Бит 4 | Бит 3 | Бит 2 | Бит 1 | Бит 0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h Mode | W | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN |
| | R | -- | FECF | CRCF | CER | XER | PLLER | TRSR | TRER |
| 01h Mode control | W | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| | R | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| 02h Calc | R/W | -- | -- | -- | -- | -- | VCC | VBC | FBC |
| 03h FIFO I | W | FEP7 | FEP6 | FEP5 | FEP4 | FEP3 | FEP2 | FEP1 | FEP0 |
| 04h FIFO II | W | FPM1 | FPM0 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| 05h FIFO Data | R/W | FIFO7 | FIFO6 | FIFO5 | FIFO4 | FIFO3 | FIFO2 | FIFO1 | FIFO0 |
| 06h ID Data | R/W | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 07h RC OSC I | W | WWS_SL7 | WWS_SL6 | WWS_SL5 | WWS_SL4 | WWS_SL3 | WWS_SL2 | WWS_SL1 | WWS_SL0 |
| | R | -- | -- | RCOC5 | RCOC4 | RCOC3 | RCOC2 | RCOC1 | RCOC0 |
| 08h RC OSC II | W | WWS_SL9 | WWS_SL8 | WWS_AC5 | WWS_AC4 | WWS_AC3 | WWS_AC2 | WWS_AC1 | WWS_AC0 |
| 09h RC OSC III | W | BBCKS1 | BBCKS0 | -- | -- | -- | RCOSC_E | TSEL | TWWS_E |
| 0Ah CKO Pin | W | ECKOE | CKOS3 | CKOS2 | CKOS1 | CKOS0 | CKOI | CKOE | SCKI |
| 0Bh GPIO1 Pin I | W | -- | -- | GIO1S3 | GIO1S2 | GIO1S1 | GIO1S0 | GIO1I | GIO1OE |
| 0Ch GPIO2 Pin II | W | -- | -- | GIO2S3 | GIO2S2 | GIO2S1 | GIO2S0 | GIO2I | GIO2OE |
| 0Dh Clock | R/W | GRC3 | GRC2 | GRC1 | GRC0 | CSC1 | CSC0 | CGS | XS |
| 0Eh Data rate | R/W | SDR7 | SDR6 | SDR5 | SDR4 | SDR3 | SDR2 | SDR1 | SDR0 |
| 0Fh PLL I | R/W | CHN7 | CHN6 | CHN5 | CHN4 | CHN3 | CHN2 | CHN1 | CHN0 |
| 10h PLL II | R/W | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | IP8 |
| 11h PLL III | R/W | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| 12h PLL IV | W | FP15 | FP14 | FP13 | FP12 | FP11 | FP10 | FP9 | FP8 |
| | R | -- | AC14 | AC13 | AC12 | AC11 | AC10 | AC9 | AC8 |
| 13h PLL V | W | FP7 | FP6 | FP5 | FP4 | FP3 | FP2 | FP1 | FP0 |
| | R | AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |
| 14h TX I | W | TXSM1 | TXSM0 | TXDI | TME | FS | FDP2 | FDP1 | FDP0 |
| 15h TX II | W | -- | PDV1 | PDV0 | FD4 | FD3 | FD2 | FD1 | FD0 |
| 16h Delay I | W | DPR2 | DPR1 | DPR0 | TDL1 | TDL0 | PDL2 | PDL1 | PDL0 |
| 17h Delay II | W | WSEL2 | WSEL1 | WSEL0 | AGC_D1 | AGC_D0 | RS_DLY2 | RS_DLY1 | RS_DLY0 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 18h RX | W | -- | RXSM1 | RXSM0 | FC | RXDI | DMG | BWS | ULS |
| 19h RX Gain I | R/W | MVGS | -- | IGC | MGC1 | MGC0 | LGC2 | LGC1 | LGC0 |
| 1Ah RX Gain II | W | RH7 | RH6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 |
| 1Bh RX Gain III | W | RL7 | RL6 | RL5 | RL4 | RL3 | RL2 | RL1 | RL0 |
| 1Ch RX Gain IV | W | ENGC | -- | -- | -- | MHC | LHC1 | LHC0 | VGCE |
| 1Dh RSSI Threshold | W | RTH7 | RTH6 | RTH5 | RTH4 | RTH3 | RTH2 | RTH1 | RTH0 |
| | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| 1Eh ADC | W | RSM1 | RSM0 | ERSS | FSARS | -- | XADS | RSS | CDM |
| 1Fh Code I | W | -- | MCS | WHTS | FECS | CRCS | IDL | PML1 | PML0 |
| 20h Code II | W | -- | DCL2 | DCL1 | DCL0 | ETH1 | ETH0 | PMD1 | PMD0 |
| 21h Code III | W | -- | WS6 | WS5 | WS4 | WS3 | WS2 | WS1 | WS0 |
| 22h IF Calibration I | W | -- | -- | -- | MFBS | MFB3 | MFB2 | MFB1 | MFB0 |
| | R | -- | -- | -- | FBCF | FB3 | FB2 | FB1 | FB0 |
| 23h IF Calibration II | R | -- | -- | -- | FCD4 | FCD3 | FCD2 | FCD1 | FCD0 |
| 24h VCO current Calibration | W | -- | -- | VCCS | MVCS | VCOC3 | VCOC2 | VCOC1 | VCOC0 |
| | R | -- | -- | -- | FVCC | VCB3 | VCB2 | VCB1 | VCB0 |
| 25h VCO Single band Calibration I | W | -- | -- | -- | -- | MVBS | MVB2 | MVB1 | MVB0 |
| | R | -- | -- | DVT1 | DVT0 | VBCF | VB2 | VB1 | VB0 |
| 26h VCO Single band Calibration II | W | -- | -- | VTH2 | VTH1 | VTH0 | VTL2 | VTL1 | VTL0 |
| 27h Battery detect | W | RGS | RGV1 | RGV0 | -- | BVT2 | BVT1 | BVT0 | BDS |
| | R | RGS | RGV1 | RGV0 | BDF | BVT2 | BVT1 | BVT0 | BDS |
| 28h TX test | W | -- | -- | TXCS | PAC1 | PAC0 | TBG2 | TBG1 | TBG0 |
| 29h Rx DEM test I | W | DMT | DCM1 | DCM0 | MLP1 | MLP0 | SLF2 | SLF1 | SLF0 |
| 2Ah Rx DEM test II | W | DCV7 | DCV6 | DCV5 | DCV4 | DCV3 | DCV2 | DCV1 | DCV0 |
| 2Bh CPC | W | -- | -- | -- | -- | -- | -- | CPC1 | CPC0 |
| 2Ch Crystal test | W | -- | -- | -- | -- | DBD | XCC | XCP1 | XCP0 |
| 2Dh PLL test | W | -- | PMPE | PRRC1 | PRRC0 | PRIC1 | PRIC0 | SDPW | NSDO |
| 2Eh VCO test I | W | -- | -- | -- | TLB | TLB | RLB | RLB | VCBS |
| 2Fh VCO test II | W | -- | -- | -- | -- | RFT3 | RFT2 | RFT1 | RFT0 |
| 30h IFAT | W | IGFI2 | IGFI1 | IGFI0 | IGFQ2 | IGFQ1 | IGFQ0 | IFBC | LIMC |
| 31h RScale | R/W | RSC7 | RSC6 | RSC5 | RSC4 | RSC3 | RSC2 | RSC1 | RSC0 |
| 32h Filter test | W | FT7 | FT6 | FT5 | FT4 | FT3 | FT2 | FT1 | FT0 |

Обозначение: -- = зарезервировано

## 9.2 Описание управляющих регистров

### 9.2.1 Регистр Mode (Адрес: 00h)

| Имя | R/W | Бит 7 | Бит 6 | Бит 5 | Бит 4 | Бит 3 | Бит 2 | Бит 1 | Бит 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode | R | -- | FECF | CRCF | CER | XER | PLLER | TRSR | TRER |
| | W | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN |
| Сброс | | -- | -- | -- | -- | -- | -- | -- | -- |

**RESETN: Запись в этот регистр 0x00 приведет к выдаче команды сброса, после регистр автоматически очистится**

**FECF: FEC флаг.**
**[0]:** FEC пройдено. **[1]:** FEC ошибка. (FECF доступен только для чтения, обновляется при приеме каждого пакета.)

**CRCF: CRC флаг.**
**[0]:** CRC пройдено. **[1]:** CRC ошибка. (CRCF доступен только для чтения, обновляется при приеме каждого пакета.)

**CER: Статус включения радиочастотного(RF) чипа.**
**[0]:** RF чип выключен. **[1]:** RF чип включен.

**XER: Статус включения внутреннего кварцевого генератора.**
**[0]:** Кварцевого генератора выключен. **[1]:** Кварцевого генератора включен.

**PLLE: Статус включения PLL.**
**[0]:** PLL выключено. **[1]:** PLL включено.

**TRER: Состояние включения TRX.**
**[0]:** TRX выключено. **[1]:** TRX включено.

**TRSR: Регистр состояния TRX.**
**[0]:** Прием(RX). **[1]:** Передача(TX).
Пригодный, если TRER=1 (TRX включено).

### 9.2.2 Регистр Mode Control (Адрес: 01h)

| Имя | R/W | Бит 7 | Бит 6 | Бит 5 | Бит 4 | Бит 3 | Бит 2 | Бит 1 | Бит 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control I | R | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| | W | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| Сброс | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DDPC: В прямом режиме, если DDPC=1, MCU отправляет/получает необработанные данные пакета через SDIO контакт вместо GIO1 или GIO2 пинов.**

[0]: **Выключено.** [1]: **Включено.**

**ARSSI: Автоматическое измерение RSSI при входе в режим RX.**
**[0]:** Выключено. **[1]:** Включено.

**AIF (Авто смещение IF): LO частота RF будет автоматически смещаться на одну IF частоту при входе в режим RX.**
**[0]:** Выключено. **[1]:** Включено.

**CD / DFCD: DFCD (Фильтр данных по CD): Полученный пакет будет отфильтрован, если CD неактивен.**
**[0]:** Выключено. **[1]:** Включено.

**CD (Только для чтения): Сигнал детектора несущей.**
**[0]:** Входная мощность ниже порога. **[1]:** Входная мощность выше порога.

**WWSE: Зарезервировано для внутренних нужд. Должно быть установлено значение [0].**

**FMT: Зарезервировано для внутренних нужд. Должно быть установлено значение [0].**

**FMS: Выбор режима Direct/FIFO.**
**[0]:** Direct режим. **[1]:** FIFO режим.

**ADCM: ADC measurement enable (Auto clear when done).**
**[0]:** Disable measurement or measurement finished. **[1]:** Enable measurement.

| ADCM | A7105 @ Standby mode | A7105 @ RX mode |
|---|---|---|
| [0] | Disable ADC | Disable ADC |
| [1] | No function | Measure RSSI, carrier detect |

Refer to chapter 17 for details.

### 9.2.3 Calibration Control Register (Address: 02h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control II | R/W | -- | -- | -- | -- | -- | VCC | VBC | FBC |
| Reset | | -- | -- | -- | -- | -- | 0 | 0 | 0 |

**VCC: VCO Current calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.

**VBC: VCO Bank calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.

**FBC: IF Filter Bank calibration enable (Auto clear when done).**
**[0]:** Disable. **[1]:** Enable.

### 9.2.4 FIFO Register I (Address: 03h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| FIFO I | W | FEP7 | FEP6 | FEP5 | FEP4 | FEP3 | FEP2 | FEP1 | FEP0 |
| Reset | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

**FEP [7:0]: FIFO End Pointer for TX FIFO and Rx FIFO.**
Refer to chapter 16 for details.

### 9.2.5 FIFO Register II (Address: 04h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| FIFO II | W | FPM1 | FPM0 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**FPM [1:0]: FIFO Pointer MArgin**

**PSA [5:0]: Used for Segment FIFO.**
Refer to chapter 16 for details.

### 9.2.6 FIFO DATA Register (Address: 05h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| FIFO DATA | R/W | FIFO7 | FIFO6 | FIFO5 | FIFO4 | FIFO3 | FIFO2 | FIFO1 | FIFO0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**FIFO [7:0]: FIFO data. TX FIFO (Write only) and RX FIFO (Read only).**
TX FIFO and RX FIFO share the same address (05h).
Refer to chapter 16 for details.

### 9.2.7 Регистр ID DATA (Address: 06h)

| Имя | R/W | Бит 7 | Бит 6 | Бит 5 | Бит 4 | Бит 3 | Бит 2 | Бит 1 | Бит 0 |
|---|---|---|---|---|---|---|---|---|---|
| ID DATA | R/W | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| Сброс | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ID [7:0]: Идентификатор.**
При обращении к этому регистру идентификационные данные вводятся или выводятся последовательно (байт идентификатора 0,1, 2 и 3). Рекомендуется установить 0 байт идентификатора равный 5xh или Axh. Подробности см. в разделе 10.6.

### 9.2.8 RC OSC Register I (Address: 07h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC I | R | | | RCOC5 | RCOC4 | RCOC3 | RCOC2 | RCOC1 | RCOC0 |
| | W | WWS_SL7 | WWS_SL6 | WWS_SL5 | WWS_SL4 | WWS_SL3 | WWS_SL2 | WWS_SL1 | WWS_SL0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**RCOC [5:0]: Reserved for internal usage only.**

### 9.2.9 RC OSC Register II (Address: 08h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC II | W | WWS_SL9 | WWS_SL8 | WWS_AC5 | WWS_AC4 | WWS_AC3 | WWS_AC2 | WWS_AC1 | WWS_AC0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**WWS_AC [5:0]: Reserved for internal usage only.**

**WWS_SL [9:0]: Reserved for internal usage only.**

### 9.2.10 RC OSC Register III (Address: 09h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RC OSC III | W | BBCKS1 | BBCKS0 | -- | -- | -- | RCOSC_E | TSEL | TWWS_E |
| Reset | | 0 | 0 | -- | -- | -- | 1 | 0 | 1 |

**BBCKS [1:0]: Clock select for internal digital block Recommend BBCKS = [00]**
**[00]:** $F_{SYCK}$ / 8. **[01]:** $F_{SYCK}$ / 16. **[10]:** $F_{SYCK}$ / 32. **[11]:** $F_{SYCK}$ / 64.

**RCOSC_E: RC-oscillator enable. Reserved for internal usage only.**
**[0]:** Disable. **[1]:** Enable.

**TSEL: Timer select for TWWS function. Reserved for internal usage only.**
**[0]:** Use WWS_AC. **[1]:** Use WWS_SL.

**TWWS_E: Enable TWWS function. Reserved for internal usage only.**
**[0]:** Disable. **[1]:** Enable.

### 9.2.11 CKO Pin Control Register (Address: 0Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| CKO Pin Control | W | ECKOE | CKOS3 | CKOS2 | CKOS1 | CKOS0 | CKOI | CKOE | SCKI |
| Reset | | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

**ECKOE: External Clock Output Enable for CKOS [3:0]= [0100] ~ [0111].**
**[0]:** Disable. **[1]:** Enable.

**CKOS [3:0]: CKO pin output select.**
**[0000]:** DCK (TX data clock) in TX mode, RCK (RX recovery clock) in RX mode.
**[0001]:** DCK (TX data clock) in TX mode, RCK (RX recovery clock) in RX mode.
**[0010]:** FPF (FIFO pointer flag).
**[0011]:** EOP, EOVBC, EOFBC, EOADC, EOVCC, OKADC (Internal usage only).
**[0100]:** External clock output= $F_{SYCK}$.
**[0101]:** External clock output / 2= $F_{SYCK}$ / 2.
**[0110]:** External clock output / 4= $F_{SYCK}$ / 4.
**[0111]:** External clock output / 8= $F_{SYCK}$ / 8.
**[1xxx]:** Reserved.

**CKOI: CKO pin output signal invert.**
**[0]:** Non-inverted output. **[1]:** Inverted output.

**CKOE: CKO pin Output Enable.**
**[0]:** High Z. **[1]:** Enable.

**SCKI: SPI clock input invert.**
**[0]:** Non-inverted input. **[1]:** Inverted input.

### 9.2.12 GIO1 Pin Control Register I (Address: 0Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| GIO1 Pin Control I | W | -- | -- | GIO1S3 | GIO1S2 | GIO1S1 | GIO1S0 | GIO1I | GIO1OE |
| Reset | | -- | -- | 0 | 0 | 0 | 0 | 0 | 1 |

**GIO1S [3:0]: GIO1 pin function select.**

| GIO1S [3:0] | TX state | RX state |
|---|---|---|
| [0000] | WTR (Wait until TX or RX finished) | |
| [0001] | EOAC (end of access code) | FSYNC (frame sync) |
| [0010] | TMEO (TX modulation enable) | CD (carrier detect) |
| [0011] | Preamble Detect Output (PMDO) | |
| [0100] | (Reserved.) | |
| [0101] | In phase demodulator input (DMII) | |
| [0110] | SDO ( 4 wires SPI data out) | |
| [0111] | TRXD In/Out (Direct mode) | |
| [1000] | RXD (Direct mode) | |
| [1001] | TXD (Direct mode) | |
| [1010] | In phase demodulator external input (EXDI0) | |
| [1011] | External FSYNC input in RX direct mode | |
| [11xx] | (Inhibited.) | |

**GIO1I: GIO1 pin output signal invert.**
**[0]:** Non-inverted output. **[1]:** Inverted output.

**GIO1OE: GIO1pin output enable.**
**[0]:** High Z. **[1]:** Enable.

### 9.2.13 GIO2 Pin Control Register II (Address: 0Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| GIO2 Pin Control II | W | -- | -- | GIO2S3 | GIO2S2 | GIO2S1 | GIO2S0 | GIO2I | GIO2OE |
| Reset | | -- | -- | 0 | 1 | 0 | 0 | 0 | 1 |

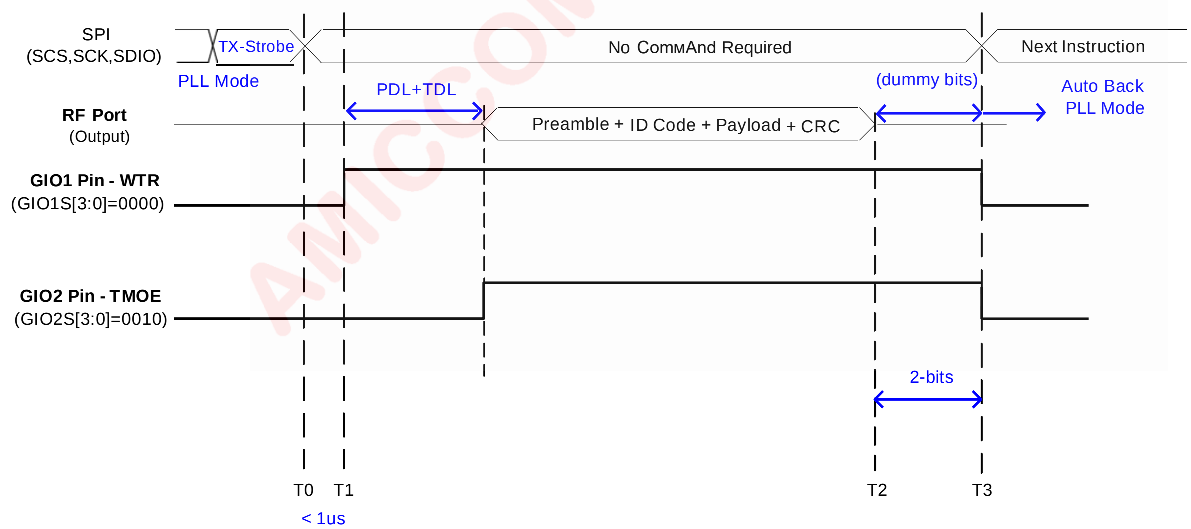
**GIO2S [3:0]: GIO2 pin function select.**

| GIO2S | TX state | RX state |
|---|---|---|
| [0000] | WTR (Wait until TX or RX finished) | |
| [0001] | EOAC (end of access code) | FSYNC (frame sync) |
| [0010] | TMEO (TX modulation enable) | CD (carrier detect) |
| [0011] | Preamble Detect Output (PMDO) | |
| [0100] | (Reserved.) | |
| [0101] | Quadrature phase demodulator input (DMIQ) | |
| [0110] | SDO (4 wires SPI data out) | |
| [0111] | TRXD In/Out (Direct mode) | |
| [1000] | RXD (Direct mode) | |
| [1001] | TXD (Direct mode) | |
| [1010] | Quadrature phase demodulator external input (EXDI1) | |
| [1011] | External FSYNC input in RX direct mode | |
| [11xx] | (Inhibited.) | |

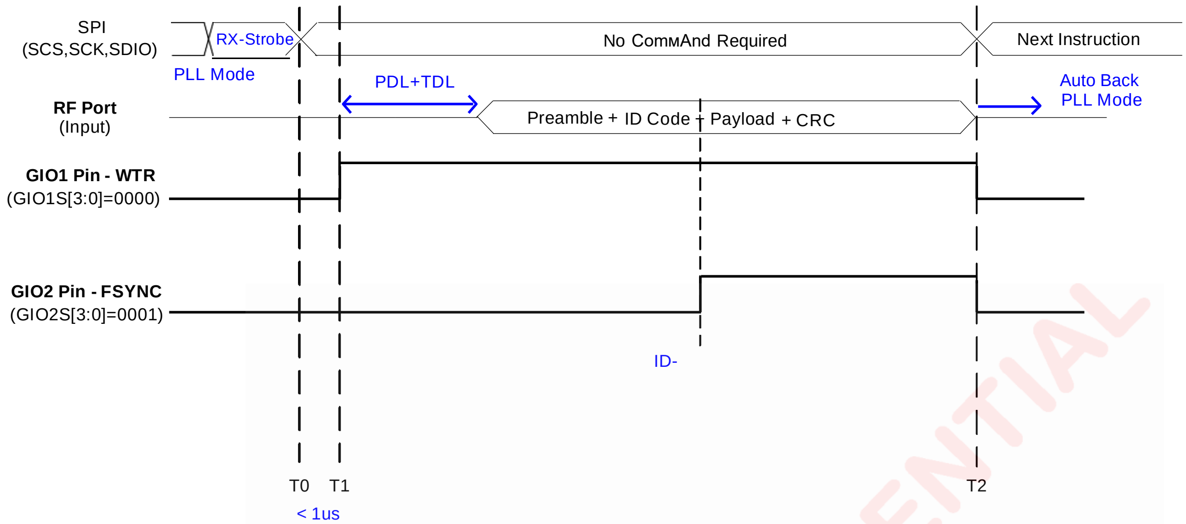
**GIO2I: GIO2 pin output signal invert.**
**[0]:** Non-inverted output. **[1]:** Inverted output.

**GIO2OE: GIO2 pin Output Enable.**
**[0]:** High Z. **[1]:** Enable.

**In TX mode**



**In RX mode**




### 9.2.14 Clock Register (Address: 0Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Clock | R/W | GRC3 | GRC2 | GRC1 | GRC0 | CSC1 | CSC0 | CGS | XS |
| Reset | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

**Refer to chapter 14 for details.**

**CGS: Clock generator enable. Recommend CGS = [0]**
**[0]:** Disable. **[1]:** Enable.

| CGS = 0 (recommend) | CGS = 1 |
|---|---|
| Disable internal 32МГцPLL clock | $F_{MCLK}$ = 32 MHz |

**XS: Crystal oscillator select. Recommend XS = [1]**
**[0]:** External clock. **[1]:** Crystal.

**GRC [3:0]: Clock generation reference counter.**

| GRC[3:0] | Note |
|---|---|
| **Don't care** | **Recommend when CGS = 0** |
| $F_{XTAL}$ x (DBL+1) / (GRC+1) = 2M | When CGS = 1 |

**CSC [1:0]: system clock $F_{SYCK}$ divider select.**

| CSC [1:0] | System Clock $F_{SYCK}$ | Note |
|---|---|---|
| 00 | $F_{MCLK}$ | $F_{SYCK}$ is used to determine 1. Data rate (0Eh) 2. ADC clock (1Eh) 3. Internal digital clock (09h) 4. CKO pin (0Ah) |
| 01 (Recommend) | $F_{MCLK}$ / 2 | |
| 10 | $F_{MCLK}$ / 2 | |
| 11 | $F_{MCLK}$ / 4 | |

### 9.2.15 Data Rate Register (Address: 0Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Data Rate | R/W | SDR7 | SDR6 | SDR5 | SDR4 | SDR3 | SDR2 | SDR1 | SDR0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SDR [7:0]: Data rate division selection.**
Data rate = **$F_{SYCK}$** / 32 / (SDR [7:0]+1). Refer to chapter 13 for details.

### 9.2.16 PLL Register I (Address: 0Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL I | R/W | CHN7 | CHN6 | CHN5 | CHN4 | CHN3 | CHN2 | CHN1 | CHN0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**CHN [7:0]: LO channel number select.**
Refer to chapter 14 for details.

### 9.2.17 PLL Register II (Address: 10h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL II | R | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | IP8 |
| | W | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | BIP8 |
| Reset | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

**DBL: Crystal frequency doubler selection. Recommend DBL = [1]**
**[0]:** Disable. $F_{XREF} = F_{XTAL}$. **[1]:** Enable. $F_{XREF} = 2 * F_{XTAL}$.

**RRC [1:0]: RF PLL reference counter setting.**

**CHR [3:0]: PLL channel step setting.**

Refer to chapter 14 for details.

### 9.2.18 PLL Register III (Address: 11h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL III | R | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| | W | BIP7 | BIP6 | BIP5 | BIP4 | BIP3 | BIP2 | BIP1 | BIP0 |
| Reset | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

**BIP [8:0]: LO base frequency integer part setting. Recommend BIP[8:0] = [0x04B]**
BIP [8:0] are from address (0Fh) and (10h),

**IP [8:0]: LO frequency integer part value.**
IP [8:0] are from address (0Fh) and (10h),

Refer to chapter 14 for details.

### 9.2.19 PLL Register IV (Address: 12h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL IV | R | --/FP15 | AC14/FP14 | AC13/FP13 | AC12/FP12 | AC11/ FP11 | AC10/FP10 | AC9/FP9 | AC8/FP8 |
| | W | BFP15 | BFP14 | BFP13 | BFP12 | BFP11 | BFP10 | BFP9 | BFP8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 9.2.20 PLL Register V (Address: 13h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL V | R | AC7/FP7 | AC6/FP6 | AC5/FP5 | AC4/FP4 | AC3/FP3 | AC2/FP2 | AC1/FP1 | AC0/FP0 |
| | W | BFP7 | BFP6 | BFP5 | BFP4 | BFP3 | BFP2 | BFP1 | BFP0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**BFP [15:0]: LO base frequency fractional part setting. Recommend BFP[15:0] = [0x0002]**
BFP [15:0] are from address (11h) and (12h),

**AC [14:0] (Read): Auto Frequency compensation value (if FC (18h) =1).**

**FP [15:0] (Read): LO frequency fractional part setting.**

Refer to chapter 14 for details.

### 9.2.21 TX Register I (Address: 14h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TX I | W | TXSM1 | TXSM0 | TXDI | TME | FS | FDP2 | FDP1 | FDP0 |
| Reset | | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

**TXSM [1:0]: Moving average for non-filter select. Recommend TXSM = [00]**
**[00]:** not average. **[01]:** 2 bit average. **[10]:** 4 bit average. **[11]:** 8 bit average

**TXDI: TX data invert. Recommend TXDI = [0].**
**[0]:** Non-invert. **[1]:** Invert.

**TME: TX modulation enable.**
**[0]:** Disable. **[1]:** Enable.

**FS: Filter select. Recommend FS = [0]**
Gaussian filter (BT=0.7).
**[0]:** disable. **[1]:** enable.

**FDP [2:0]: Frequency deviation power setting. Refer to control register (15h). Recommend FDP = [110].**

### 9.2.22 TX Register II (Address: 15h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TX II | W | -- | PDV1 | PDV0 | FD4 | FD3 | FD2 | FD1 | FD0 |
| Reset | | -- | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

**PDV [1:0]: Reserved for internal usage only. Shall be set to [01].**
**FD [4:0]: Frequency deviation setting.**
$F_{DEV} = F_{PFD} \times 127 \times (FD\,[4:0] + 1) \times 2^{(FDP\,[2:0])} / 2^{24}$.
Where $F_{PFD} = F_{XTAL} * (DBL+1) / (RRC\,[1:0]+1)$, PLL comparison frequency.

| Data Rate (КБит/с) | $F_{PFD}$ | FDP [2:0] | PDV [1:0] | FD[4:0] | Fdev (КГц) |
|---|---|---|---|---|---|
| <= 50КБит/с | 12MHz | 110b | 01b | 10110b (0x16) | 122 |
| | 16MHz | | | 01111b (0x0F) | 124 |
| | 24MHz | | | 01010b (0x0A) | 127 |
| | 32MHz | | | 00111b (0x07) | 124 |
| **Data Rate (КБит/с)** | **$F_{PFD}$** | **FDP [2:0]** | **PDV [1:0]** | **FD[4:0]** | **Fdev (КГц)** |
| > 50КБит/с | 16MHz | 110b | 01b | 10111b (0x17) | 186 |
| | 24MHz | | | 01111b (0x0F) | |
| | 32MHz | | | 01011b (0x0B) | |

### 9.2.23 Delay Register I (Address: 16h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Delay | W | DPR2 | DPR1 | DPR0 | TDL1 | TDL0 | PDL2 | PDL1 | PDL0 |
| Reset | | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

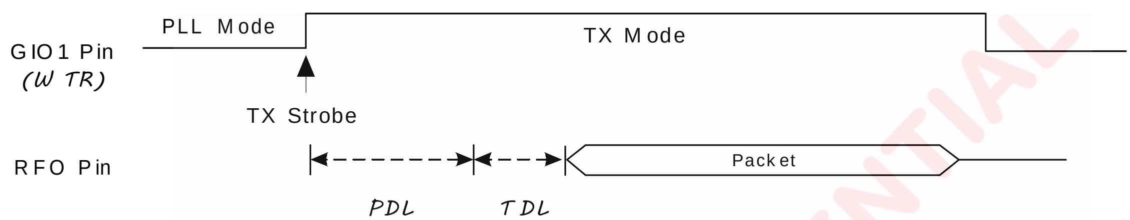
**DPR [2:0]: Delay scale. Recommend DPR = [000].**

**TDL [1:0]: Delay for TX settling from WPLL to TX.**
Delay= 20 * (TDL [1:0]+1)*(DPR [2:0]+1) us.

| DPR [2:0] | TDL [1:0] | WPLL to TX | Note |
|---|---|---|---|
| 000 | 00 | 20 us | |
| 000 | 01 | 40 us | |
| 000 | 10 | 60 us | **Recommend** |
| 000 | 11 | 80 us | |

**PDL [2:0]: Delay for TX settling from PLL to WPLL.**
Delay= 10+20 * (PDL [2:0]+1)*(DPR [2:0]+1) us.

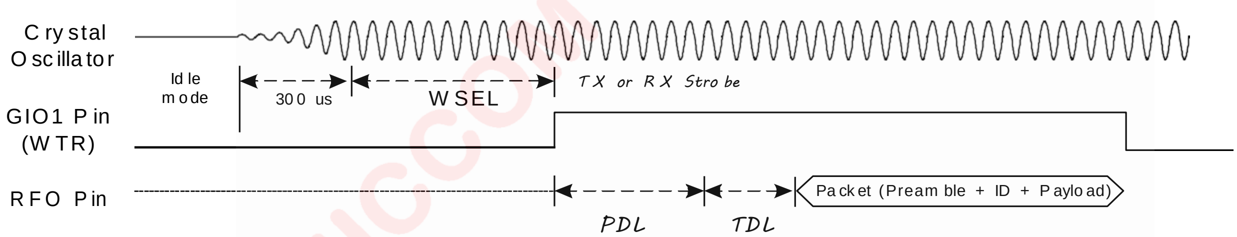
| DPR [2:0] | PDL [2:0] | PLL to WPLL (LO freq. fixed) | PLL to WPLL (LO freq changed) | Note |
|---|---|---|---|---|
| 000 | 001 | 10 us | 50 us | |
| 000 | 010 | 10 us | 70 us | **Recommend** |
| 000 | 011 | 10 us | 90 us | |
| 000 | 100 | 10 us | 110 us | |




### 9.2.24 Delay Register II (Address: 17h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Delay | W | WSEL2 | WSEL1 | WSEL0 | AGC_D1 | AGC_D0 | RS_DLY2 | RS_DLY1 | RS_DLY0 |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

**WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [010].**
**[000]:** 200us. **[001]:** 400us. **[010]:** 600us. **[011]:** 800us.
**[100]:** 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.




**AGC_D [1:0]: AGC delay settling Recommend AGC_D[1:0] = [00].**
**[00]:** 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

**RS_DLY [2:0]: RSSI measurement delay (10us ~ 80us)· Recommend RS_DLY = [000].[000]:** 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us.
**[100]:** 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

### 9.2.25 RX Register (Address: 18h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX | W | -- | RXSM1 | RXSM0 | FC | RXDI | DMG | BWS | ULS |
| Reset | | -- | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**RXSM0: Reserved for internal usage only. Shall be set to [1].**

**RXSM1: Reserved for internal usage only. Shall be set to [1].**

**FC: Frequency compensation select.**

**[0]:** Disalbe . **[1]:** Enable.
Refer to section 14.4 for details.

**RXDI: RX data output invert. Recommend RXDI = [0].**
**[0]:** Non-inverted output. **[1]:** Inverted output.

**DMG: Reserved for internal usage only. Shall be set to [0].**

**BWS: BPF bandwidth select. Recommend BWS = [1].**
**[0]:** 250КГц. **[1]:** 500КГц.

| Data Rate (КБит/с) | BWS | Note |
|---|---|---|
| 2~ 500 | 1 | $F_{IF}$= 500КГц |

**ULS: RX Up/Low side band select.**
**[0]:** Up side band, **[1]:** Low side band.
Refer to section 14.2 for details.

### 9.2.26 RX Gain Register I (Address: 19h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain I | R/W | MVGS | -- | IGC | MGC1 | MGC0 | LGC2 | LGC1 | LGC0 |
| Reset | | 0 | -- | 1 | 0 | 0 | 0 | 0 | 0 |

**MVGS: MAnual VGA calibrate. Recommend MVGS = [1].[0]:** Auto. **[1]:** MAnual

**IGC: Reserved for internal usage only. Shall be set to [0].**

**MGS [1:0]: Mixer gain. Recommend MGS = [00].**
**[00]:** 24dB. **[01]:** 18dB. **[10]:** 12dB. **[11]:** 6dB.

**LGS [2:0]: LNA gain. Recommend LGS = [000].**
**[000]:** 24dB. **[001]:** 18dB. **[010]:** 12dB. **[011]:** 6dB. **[1XX]:** 0dB.

### 9.2.27 RX Gain Register II (Address: 1Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain II | R/W | RH7 | RH6 | RH5 | RH4 | RH3 | RH2 | RH1 | RH0 |
| Reset | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**RH [7:0]: Reserved for internal usage only.**

### 9.2.28 RX Gain Register III (Address: 1Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain III | W | RL7 | RL6 | RL5 | RL4 | RL3 | RL2 | RL1 | RL0 |
| Reset | | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

**RL [7:0]: Reserved for internal usage only.**

### 9.2.29 RX Gain Register IV (Address: 1Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX Gain III | W | ENGC | | | | MHC | LHC1 | LHC0 | VGCE |
| Reset | | 1 | | | | 1 | 1 | 1 | 0 |

**ENGC: Reserved for internal usage only. Shall be set to [0]**

**MHC: Reserved for internal usage only. Shall be set to [1].**

**LHC: Reserved for internal usage only. Shall be set to [01].**

**VGCE: Reserved for internal usage only. Shall be set to [0]**

### 9.2.30 RSSI Threshold Register (Address: 1Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RSSI Threshold | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| | W | RTH7 | RTH6 | RTH5 | RTH4 | RTH3 | RTH2 | RTH1 | RTH0 |
| Reset | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**RTH [7:0]: Carrier detect threshold.**
Refer to Chapter 17 for details.

**ADC [7:0]: ADC output value for RSSI measurement.**
ADC input voltage= 1.2 * ADC [7:0] / 256 V.
Refer to chapter 17 for details.

### 9.2.31 ADC Control Register (Address: 1Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADC Control | W | RSM1 | RSM0 | ERSS | FSARS | -- | XADS | RSS | CDM |
| Reset | | 0 | 1 | 0 | 1 | -- | 0 | 1 | 1 |

**RSM [1:0]: RSSI мArgin = RTH – RTL. Recommend RSM = [11].**
**[00]:** 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.
Refer to Chapter 17 for details.

**ERSS: End for RSSI measurement**
**[0] :** RSSI measurement continues until leave off RX mode.
**[1] :** RSSI measurement will end when carrier detected and ID code word received.

**FSARS: ADC clock select. Recommend FSARS = [0].**
**[0]:** 4MHz. **[1]:** 8MHz.

**XADS: ADC input signal select.**
**[0]:** Convert RSS signal. **[1]:** Reserved for internal usage.

**RSS: RSSI measurement select.**
**[0]:** Reserved for internal usage. **[1]:** RSSI or carrier-detect measurement.

**CDM: RSSI measurement mode.**
**[0]:** Single mode. **[1]:** Continuous mode.

### 9.2.32 Code Register I (Address: 1Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code I | W | -- | MCS | WHTS | FECS | CRCS | IDL | PML1 | PML0 |
| Reset | | -- | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**WHTS: Data whitening (Data Encryption) select.**
**[0]:** Disable. **[1]:** Enable.

**FECS: FEC select.**
**[0]:** Disable. **[1]:** Enable.

**CRCS: CRC select.**
**[0]:** Disable. **[1]:** Enable.

**IDL: ID code length select. Recommend IDL= [1].**
**[0]:** 2 bytes. **[1]:** 4 bytes.

**PML [1:0]: Preamble length select. Recommend PML= [11].**
**[00]:** 1 byte. **[01]:** 2 bytes. **[10]:** 3 bytes. **[11]:** 4 bytes.
Refer to chapter 16 for details.

### 9.2.33 Code Register II (Address: 20h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code II | W | -- | DCL2 | DCL1 | DCL0 | ETH1 | ETH0 | PMD1 | PMD0 |
| Reset | | -- | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

**DCL [2:0]: Demodulator DC estiмAtion average mode. Recommend DCL[2:0] = [001]**

**ETH [1:0]: ID code error tolerance. Recommend ETH = [01].**
**[00]:** 0 bit, **[01]:** 1 bit. **[10]:** 2 bits. **[11]:** 3 bits.

**PMD [1:0]: Preamble pattern detection length.**
**[00]:** 0bit. **[01]:** 4bits. **[10]:** 8bits. **[11]:** 16bits.

| Data Rate (КБит/с) | PMD[1:0] | Note |
|---|---|---|
| 2 ~ 125 | 11 | Also refer to addr. 29h |
| 250 / 500 | 10 | |

Refer to chapter 16 for details.

### 9.2.34 Code Register III (Address: 21h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code III | W | -- | WS6 | WS5 | WS4 | WS3 | WS2 | WS1 | WS0 |
| Reset | | -- | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

**WS [6:0]: Data Whitening seed setting (data encryption key).**
Refer to chapter 16 for details.

### 9.2.35 IF Calibration Register I (Address: 22h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| IF Calibration I | R | | | | FBCF | FB3 | FB2 | FB1 | FB0 |
| | W | -- | -- | -- | MFBS | MFB3 | MFB2 | MFB1 | MFB0 |
| Reset | | -- | -- | -- | 0 | 0 | 1 | 1 | 0 |

**MFBS: IF filter calibration value select. Recommend MFBS = [0].**
**[0]:** Auto calibration value. **[1]:** MAnual calibration value.

**MFB [3:0]: IF filter мAnual calibration value.**

**FBCF: IF filter auto calibration flag.**
**[0]:** Pass. **[1]:** Fail.

**FB [3:0]: IF filter calibration value.**
MFBS= 0: Auto calibration value (AFB),
MFBS= 1: MAnual calibration value (MFB).

Refer to chapter 15 for details.

### 9.2.36 IF Calibration Register II (Address: 23h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| IF Calibration II | R | -- | -- | | FCD4 | FCD3 | FCD2 | FCD1 | FCD0 |
| Reset | | -- | -- | -- | -- | -- | -- | -- | -- |

**FCD [4:0]: IF filter calibration deviation from goal (Read only).**

### 9.2.37 VCO current Calibration Register (Address: 24h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO current Calibration | R | | | | FVCC | VCB3 | VCB2 | VCB1 | VCB0 |
| | W | -- | -- | VCCS | MVCS | VCOC3 | VCOC2 | VCOC1 | VCOC0 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Reset | | -- | -- | 0 | 0 | 1 | 0 | 0 | 0 |

**VCCS: Reserved for internal usage only. Shall be set [0].**

**MVCS: VCO current calibration value select. Recommend MVCS = [1].**
**[0]:** Auto calibration value. **[1]:** MAnual calibration value.

**VCOC [3:0]: VCO current мAnual calibration value. Recommend VCOC = [011].**

**FVCC: VCO current auto calibration flag.**
**[0]:** Pass. **[1]:** Fail.

**VCB [3:0]: VCO current calibration value.**
MVCS= 0: Auto calibration value (VCB).
MVCS= 1: MAnual calibration value (VCOC).

Refer to chapter 15 for details.

### 9.2.38 VCO Single band Calibration Register I (Address: 25h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO Single band Calibration I | R | -- | -- | DVT1 | DVT0 | VBCF | VB2 | VB1 | VB0 |
| | W | -- | -- | -- | -- | MVBS | MVB2 | MVB1 | MVB0 |
| Reset | | -- | -- | -- | -- | 0 | 1 | 0 | 0 |
| Reset | | -- | -- | -- | -- | 0 | 1 | 0 | 0 |

**MVBS: VCO bank calibration value select. Recommend MVBS = [0].**
**[0]:** Auto calibration value. **[1]:** MAnual calibration value.

**MVB [2:0]: VCO band мAnual calibration value.**
**DVT [1:0]: digital VCO tuning voltage output.**
**[00]:** VT<VTL<VTH. **[01]:** VTL<VT<VTH. **[10]:** No used. **[11]:** VTL<VTH<VT.

**VBCF: VCO band auto calibration flag.**
**[0]:** Pass. **[1]:** Fail.

**VB [2:0]: VCO bank calibration value.**
MVBS= 0: Auto calibration value (AVB).
MVBS= 1: MAnual calibration value (MVB).

Refer to chapter 15 for details.

### 9.2.39 VCO Single band Calibration Register II (Address: 26h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO Single band Calibration II | W | -- | -- | VTH2 | VTH1 | VTH0 | VTL2 | VTL1 | VTL0 |
| Reset | | -- | -- | 1 | 1 | 1 | 0 | 1 | 1 |

**VTH [2:0]: VCO tuning voltage upper threshold level setting. Recommend VTH = [111].**
**[000]:** VDD_A – 0.6V. **[001]:** VDD_A – 0.7V. **[010]:** VDD_A – 0.8V. **[011]:** VDD_A – 0.9V
**[100]:** VDD_A – 1.0V. **[101]:** VDD_A – 1.1V. **[110]:** VDD_A – 1.2V. **[111]:** VDD_A – 1.3V

VDD_A is on chip analog regulator output voltage

**VTL [2:0]: VCO tuning voltage lower threshold level setting. Recommend VTL = [011].**
**[000]:** 0.1V. **[001]:** 0.2V. **[010]:** 0.3V. **[011]:** 0.4V.
**[100]:** 0.5V. **[101]:** 0.6V. **[110]:** 0.7V. **[111]:** 0.8V

### 9.2.40 Battery detect Register (Address: 27h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Battery detect | R | -- | -- | -- | BDF | -- | -- | -- | -- |
| | W | RGS | RGV1 | RGV0 | -- | BVT2 | BVT1 | BVT0 | BDS |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Reset | | 0 | 0 | 0 | -- | 0 | 1 | 1 | 0 |

**RGS: VDD_D voltage setting in Sleep mode.**
**[0]:** 3/5 * REGI. **[1]:** 3/4 * REGI.

**RGV [1:0]: VDD_D and VDD_A voltage setting in non-Sleep mode. Recommend RGV = [00].**
**[00]:** 2.1V. **[01]:** 2.0V. **[10]:** 1.9V. **[11]:** 1.8V.

**BVT [2:0]: Battery voltage detect threshold.**
**[000]:** 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.
**[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

**BDS: Battery detect select.**
**[0]:** Disable. **[1]:** Enable. It will be clear after battery detection done.

**BDF: Battery detection flag.**
**[0]:** Battery voltage less than threshold. **[1]:** Battery voltage greater than threshold.

Refer to chapter 18 for details.

### 9.2.41 TX test Register (Address: 28h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| TX test | W | -- | -- | TXCS | PAC1 | PAC0 | TBG2 | TBG1 | TBG0 |
| Reset | | -- | -- | 0 | 1 | 0 | 1 | 1 | 1 |

**TXCS: TX Current Setting. [0]**

**PAC [1:0]: PA Current Setting. [10]**

**TBG [2:0]: TX Buffer Setting. [111]**

| Typical Output Power (dBm) | Recommend setting | | | Typical TX current (мA) |
|---|---|---|---|---|
| | TXCS | TBG | PAC | |
| 1 | 0 | 7 | 3 | 21 |
| 0 | 0 | 7 | 1 | 19 |
| -10 | 0 | 3 | 1 | 14 |
| -20 | 0 | 1 | 0 | 13 |

Refer to chapter 19 and A7105 App. Note for more settings.

### 9.2.42 Rx DEM test Register I (Address: 29h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Rx DEM test I | W | DMT | DCM1 | DCM0 | MLP1 | MLP0 | SLF2 | SLF1 | SLF0 |
| Reset | | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**DMT: Reserved for internal usage only. Shall be set to [0].**

**DCM [1:0]: Demodulator DC estiмAtion mode.**
**[00] :** Fix mode (For testing only). DC level is set by DCV [7:0].
**[01] : Preamble hold mode. DC level is preamble average value.**
**[10] : Average and hold mode. DC level is the average value hold about 8 bit data rate later if preamble is detected.**
**[11]:** Payload average mode (For internal usage). DC level is payload data average.

| DCM [1:0] | Data Rate (КБит/с) | DCL[2:0] (20h) | Note |
|---|---|---|---|
| 01 | 2 ~ 125 | 001 | By Preamble |
| 10 | 250 / 500 | 001 | By ID |

**MLP [1:0]: Reserved for internal usage only. Shall be set to [00].**

**SLF [2:0]: Reserved for internal usage only. Shall be set to [111].**

### 9.2.43 Rx DEM test Register II (Address: 2Ah)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Rx DEM test II | W | DCV7 | DCV6 | DCV5 | DCV4 | DCV3 | DCV2 | DCV1 | DCV0 |
| Reset | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].**

### 9.2.44 Charge Pump Current Register (Address: 2Bh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Charge Pump Current | W | -- | -- | -- | -- | -- | -- | CPC1 | CPC0 |
| Reset | | -- | -- | -- | -- | -- | -- | 0 | 1 |

**CPC [1:0]: Charge pump current setting. Recommend CPC = [11].**
**[00]:** 0.5мА. **[01]:** 1.0мА. **[10]:** 1.5мА. **[11]:** 2.0мА

### 9.2.45 Crystal test Register (Address: 2Ch)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Crystal test | W | -- | -- | -- | -- | DBD | XCC | XCP1 | XCP0 |
| Reset | | -- | -- | -- | -- | 0 | 1 | 0 | 1 |

**DBD: Reserved for internal usage only. Shall be set to [0].**

**XCC: Reserved for internal usage only. Shall be set to [0].**

**XCP [1:0]: Reserved for internal usage only. Shall be set to [01].**

### 9.2.46 PLL test Register (Address: 2Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL test | W | -- | PMPE | PRRC1 | PRRC0 | PRIC1 | PRIC0 | SDPW | NSDO |
| Reset | | -- | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

**PMPE: Reserved for internal usage only. Shall be set to [1].**

**PRRC [1:0]: Reserved for internal usage only. Shall be set to [00].**

**PRIC [1:0]: Reserved for internal usage only. Shall be set to [01].**

**SDPW: Reserved for internal usage only. Shall be set to [0].**

**NSDO: Reserved for internal usage only. Shall be set to [1].**

### 9.2.47 VCO test Register I (Address: 2Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO test I | W | -- | -- | -- | TLB1 | TLB0 | RLB1 | RLB0 | VCBS |
| Reset | | -- | -- | -- | 1 | 1 | 0 | 1 | 0 |

**TLB [1:0]: Reserved for internal usage only. Shall be set to [11].**

**RLB [1:0]: Reserved for internal usage only. Shall be set to [00].**

**VCBS: Reserved for internal usage only. Shall be set to [0].**

### 9.2.48 VCO test Register II (Address: 2Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO test II | W | -- | -- | -- | -- | RFT3 | RFT2 | RFT1 | RFT0 |
| Reset | | -- | -- | -- | -- | 0 | 0 | 0 | 0 |

**RFT [3:0]: RF analog pin configuration for testing. Recommend RFT= [0000].**

### 9.2.49 IFAT Register (Address: 30h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO test II | W | IGFI2 | IGFI1 | IGFI0 | IGFQ2 | IGFQ1 | IGFQ0 | IFBC | LIMC |
| Reset | | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

**IGFI [2:0]: Reserved for internal usage only. Shall be set to [000].**

**IGFQ [2:0]: Reserved for internal usage only. Shall be set to [000].**

**IFBC: Reserved for internal usage only. Shall be set to [0].**

**LIMC: Reserved for internal usage only. Shall be set to [1].**

### 9.2.50 RScale Register (Address: 31h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Rscale | W | RSC7 | RSC6 | RSC5 | RSC4 | RSC3 | RSC2 | RSC1 | RSC0 |
| Reset | | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

**RSC [7:0]: Reserved for internal usage only. Shall be set to = [0x0F].**

### 9.2.51 Filter test Register (Address: 32h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Filter test | W | FT7 | FT6 | FT5 | FT4 | FT3 | FT2 | FT1 | FT0 |
| Reset | | | | | | | | | |

**FT [7:0]: Reserved for internal usage only. Shall be set to = [0x00].**

## 10. SPI

A7105 only supports one SPI interface with мAximum data rate up to 10Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A7105. Via SPI interface, user can access **control registers** and issue **Strobe commAnd**. Figure 10.1 gives an overview of SPI access мAnners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1/GIO2) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 (or GIO2) pin is data output. In such case, GIO1S (0bh) or GIO2S (0ch) should be set to [0110].

For SPI write operation, SDIO pin is latched into A7105 at the rising edge of SCK. For SPI read operation, if input address is latched by A7105, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A7105's internal state мAchine, it is very easy to send Strobe commAnd via SPI interface. The Strobe commAnd is a unique commAnd set with total 8 commAnds. See section 10.3, 10.4 and 10.5 for details.

| | SPI chip select | Data In | Data Out |
|---|---|---|---|
| **3-Wire SPI** | SCS pin = 0 | SDIO pin | SDIO pin |
| **4-Wire SPI** | SCS pin = 0 | SDIO pin | GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110) |


Figure 10.1 SPI Access MAnners

## 10.1 SPI ForмAt

The first bit (A7) is critical to indicate A7105 the following instruction is “Strobe commAnd” or “control register”. See Table 10.1 for SPI forмAt. Based on Table 10.1, To access control registers, just set A7=0, then A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 (3-wire SPI) and Figure 10.3 (4-wire SPI) for details.

| Address Byte (8 bits) | | | | | | | | Data Byte (8 bits) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMD | R/W | Address | | | | | | Data | | | | | | | |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Table 10.1 SPI ForмAt

**Address byte:**

**Bit 7: CommAnd bit**
[0] : Control registers.
[1] : Strobe commAnd.

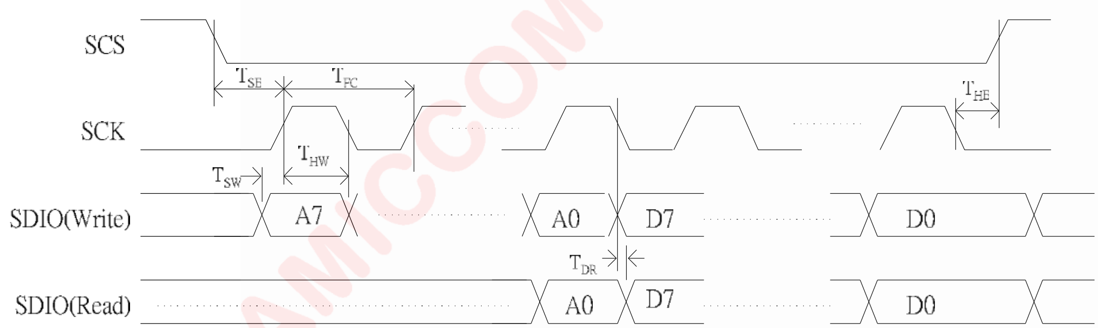
**Bit 6: R/W bit**
[0]: Write data to control register.
[1]: Read data from control register.

**Bit [5:0]: Address of control register**

**Data Byte:**
**Bit [7:0]:** SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

## 10.2 SPI Timing Characteristic

No мAtter 3-wire or 4-wire SPI interface is configured, the мAximum SPI data rate is 10 Mbps. To active SPI interface, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for SPI timing characteristic.




| Parameter | Description | Min. | MAx. | Unit |
|---|---|---|---|---|
| $F_C$ | FIFO clock frequency. | | 10 | MHz |
| $T_{SE}$ | Enable setup time. | 50 | | ns |
| $T_{HE}$ | Enable hold time. | 50 | | ns |
| $T_{SW}$ | TX Data setup time. | 50 | | ns |
| $T_{HW}$ | TX Data hold time. | 50 | | ns |
| $T_{DR}$ | RX Data delay time. | 0 | 50 | ns |

Table 10.2 SPI Timing Characteristic

## 10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI interface read / write timing are described.

### 10.3.1 Timing Chart of 3-wire SPI

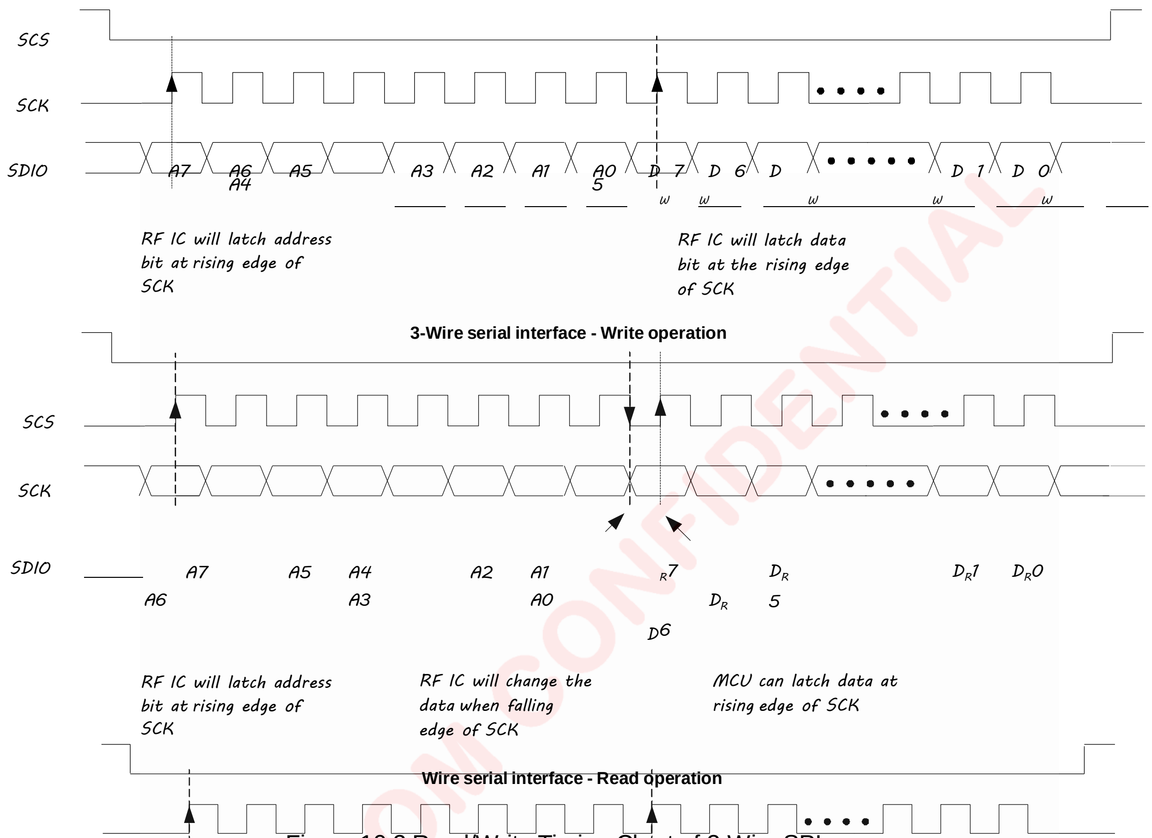
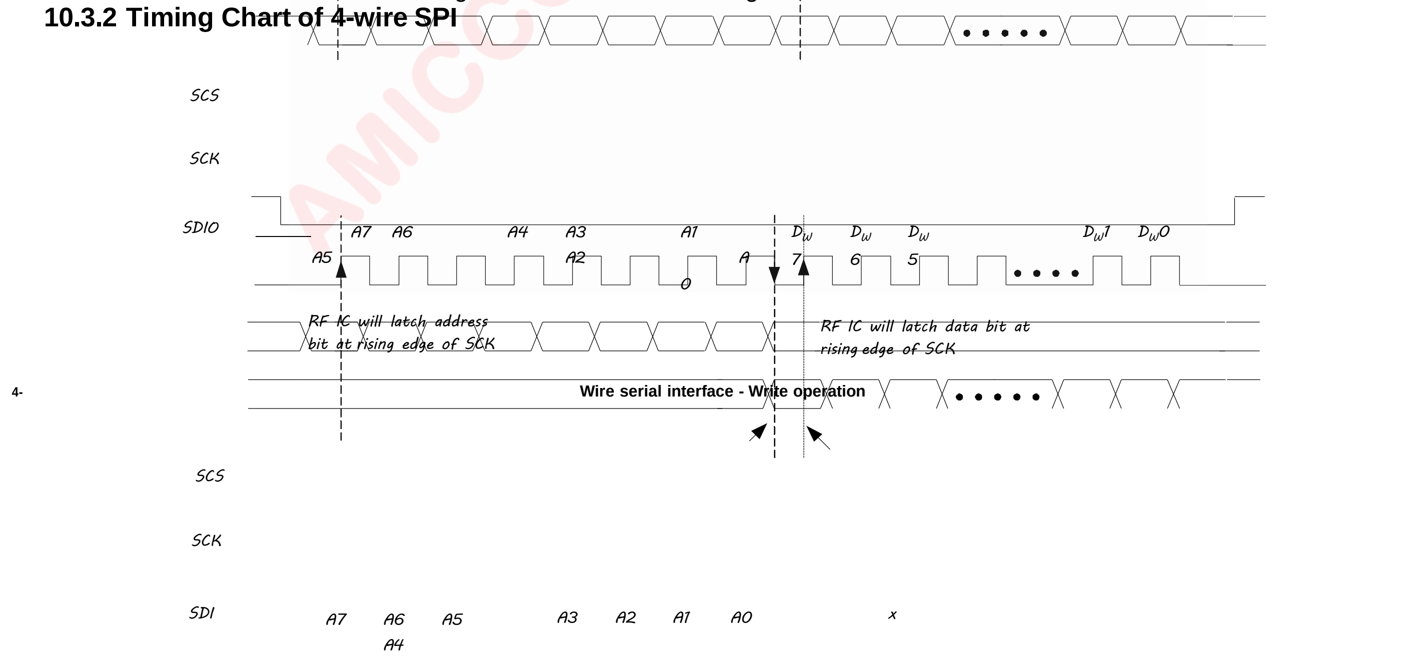



Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

### 10.3.2 Timing Chart of 4-wire SPI



x 7 DR6 DR5 DR2 DR DR1 DR0

RF IC will latch address bit at rising edge of SCK

RF IC will change the data when falling edge of SCK

MCU can latch data at the rising edge of SCK

**4-Wire serial interface - Read operation**

Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

## 10.4 Strobe CommAnds

A7105 supports 8 Strobe commAnds to control internal state mAchine for chip's operations. Table 10.3 is the summAry of Strobe commAnds.

Be notice, Strobe commAnd could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe commAnd is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remAining low for asserting next commAnds.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | **Description** |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 0 | 0 | 0 | x | X | x | x | Sleep mode |
| 1 | 0 | 0 | 1 | x | X | x | x | Idle mode |
| 1 | 0 | 1 | 0 | x | X | x | x | Standby mode |
| 1 | 0 | 1 | 1 | x | X | x | x | PLL mode |
| 1 | 1 | 0 | 0 | x | X | x | x | RX mode |
| 1 | 1 | 0 | 1 | x | X | x | x | TX mode |
| 1 | 1 | 1 | 0 | x | X | x | x | FIFO write pointer reset |
| 1 | 1 | 1 | 1 | x | X | x | x | FIFO read pointer reset |

Table 10.3 Strobe CommAnds by SPI interface

### 10.4.1 Strobe CommAnd - Sleep Mode

Refer to Table 10.3 user can issue 4 bits (1000) Strobe commAnd directly to set A7105 into Sleep mode. Below are the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | **Description** |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 0 | 0 | 0 | x | X | x | x | Sleep mode |

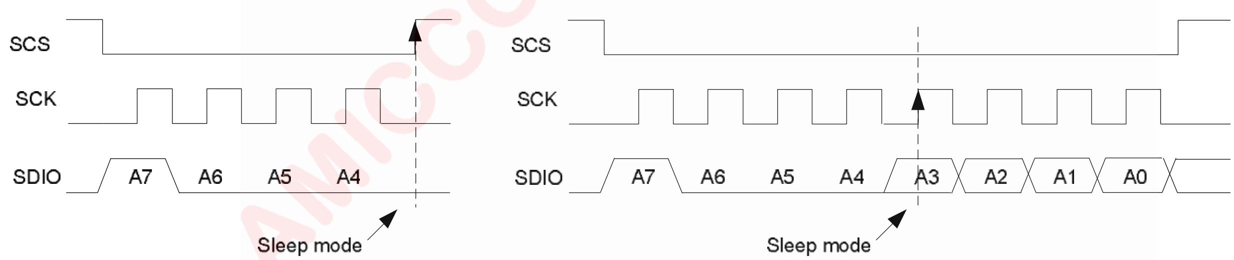



Figure 10.4 Sleep mode CommAnd Timing Chart

### 10.4.2 Strobe CommAnd - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe commAnd directly to set A7105 into Idle mode. Below is the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | **Description** |
|---|---|

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | x | X | x | x | Idle mode |

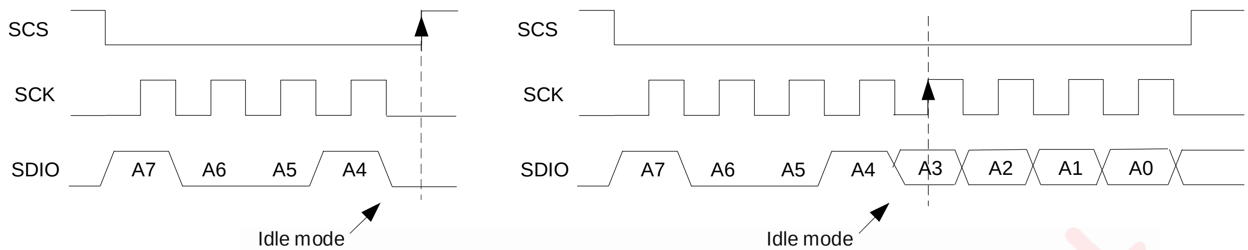



Figure 10.5 Idle mode CommAnd Timing Chart

### 10.4.3 Strobe CommAnd - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe commAnd directly to set A7105 into Standby mode. Below is the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 0 | 1 | 0 | x | X | x | x | Standby mode |

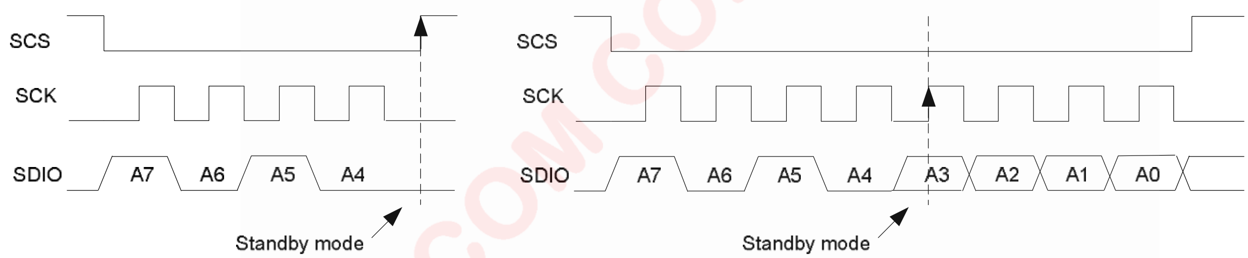



Figure 10.6 Standby mode CommAnd Timing Chart

### 10.4.4 Strobe CommAnd - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe commAnd directly to set A7105 into PLL mode. Below are the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 0 | 1 | 1 | x | X | x | x | PLL mode |

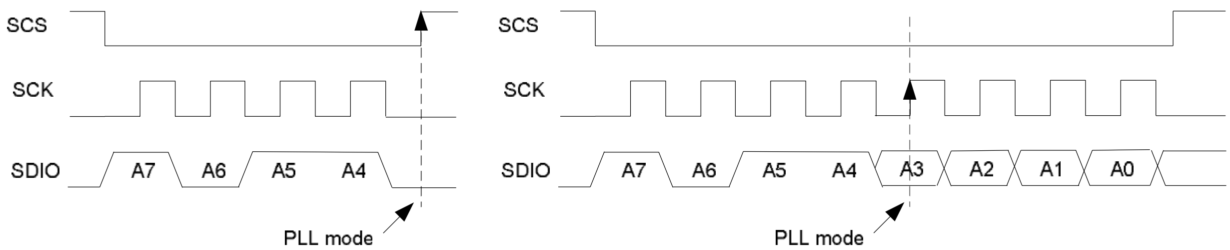



Figure 10.7 PLL mode CommAnd Timing Chart

### 10.4.5 Strobe CommAnd - RX Mode

Refer to Table 10.3, user can issue 4 bits (1100) Strobe commAnd directly to set A7105 into RX mode. Below are the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 1 | 0 | 0 | x | X | x | x | RX mode |

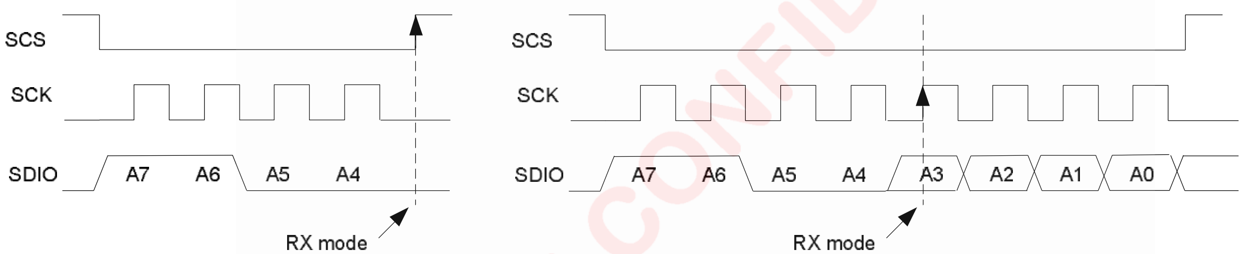



Figure 10.8 RX mode CommAnd Timing Chart

### 10.4.6 Strobe CommAnd - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe commAnd directly to set A7105 into TX mode. Below are the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 1 | 0 | 1 | x | x | x | x | TX mode |

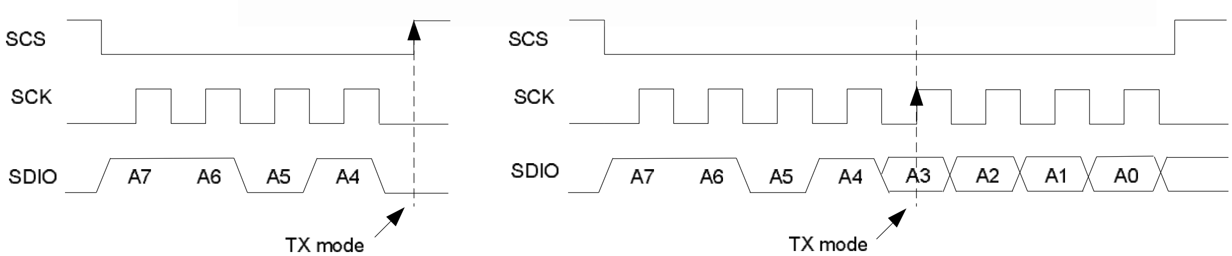



Figure 10.9 TX mode CommAnd Timing Chart

### 10.4.7 Strobe CommAnd – FIFO Write Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1110) Strobe commAnd directly to reset A7105 FIFO write pointer. Below is the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 1 | 1 | 0 | x | x | x | x | FIFO write pointer reset |

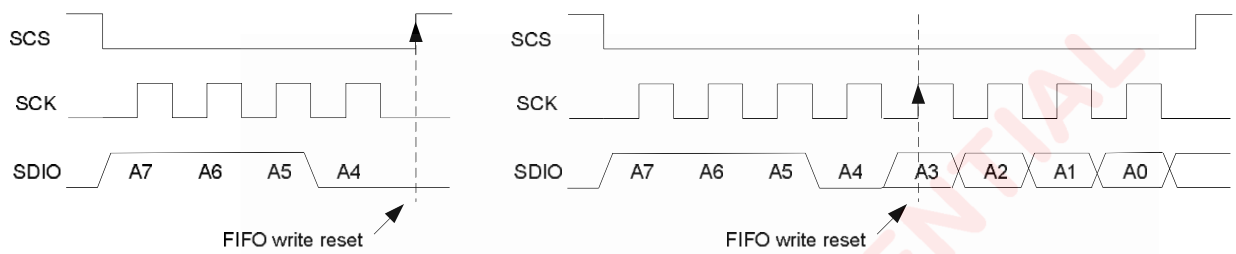



Figure 10.10 FIFO write pointer reset CommAnd Timing Chart

### 10.4.8 Strobe CommAnd – FIFO Read Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1111) Strobe commAnd directly to reset A7105 FIFO read pointer. Below are the Strobe commAnd table and timing chart.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 1 | 1 | 1 | x | x | x | x | FIFO read pointer reset |

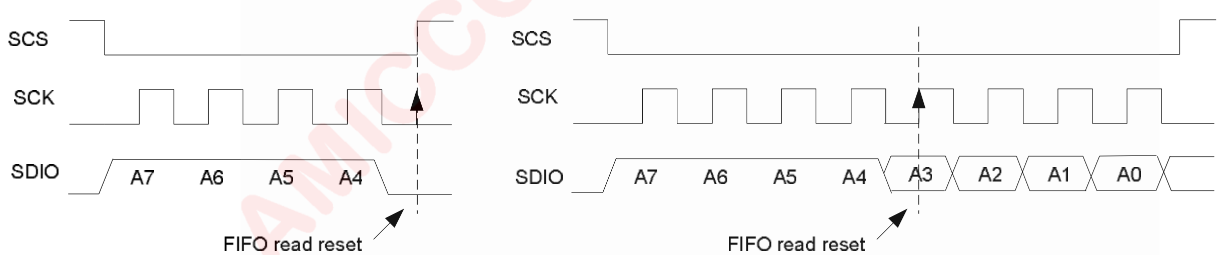



Figure 10.11 FIFO read pointer reset CommAnd Timing Chart

## 10.5 Reset CommAnd

In addition to power on reset (POR), MCU could issue software reset to A7105 by setting Mode Register (00h) through SPI interface as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A7105 is informed to generate internal signal “RESETN” to initial itself. After reset commAnd, A7105 is in standby mode and calibration procedure shall be issued again.

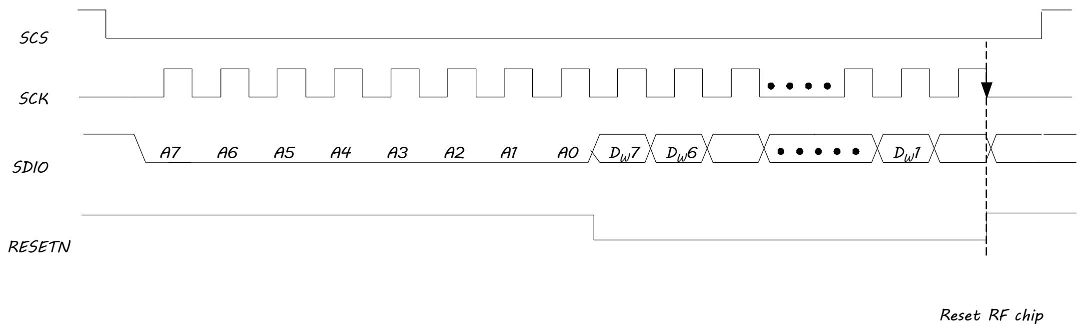



Figure 10.12 Reset CommAnd Timing Chart

## 10.6 Команды доступа к ID

A7105 имеет встроенный 32-битный идентификационный регистр для индивидуального идентификатора. Доступ к нему осуществляется через интерфейс SPI. Длину идентификатора рекомендуется оставлять 32 бита, установив IDL (регистр 1Fh). Пользователь может переключить вывод SCS на высокий, чтобы завершить команду доступа к ID, когда данные ID полностью переданы.

На рис.10.13 и 10.14 представлены временные диаграммы обращения к 32-битному ID через 3-проводный SPI.

### 10.6.1 Команда записи ID

Пользователь может подробно ознакомиться с временной диаграммой записи SPI на рис.10.2. Ниже приведена процедура выполнения команды записи ID.

Шаг 1: Передайте A7~A0 = 00000110 (A6=0 для записи, A5~A0 = 000110 регистр ID DATA, 06h).
Шаг 2: Через вывод SDIO передайте 32-битный идентификатор в A7105 в последовательности байтов данных 0 **(рекомендуется 5xh или Axh)**, 1, 2 и 3.
Шаг 3: Переключите вывод SCS на высокий уровень, когда шаг 2 будет завершен.



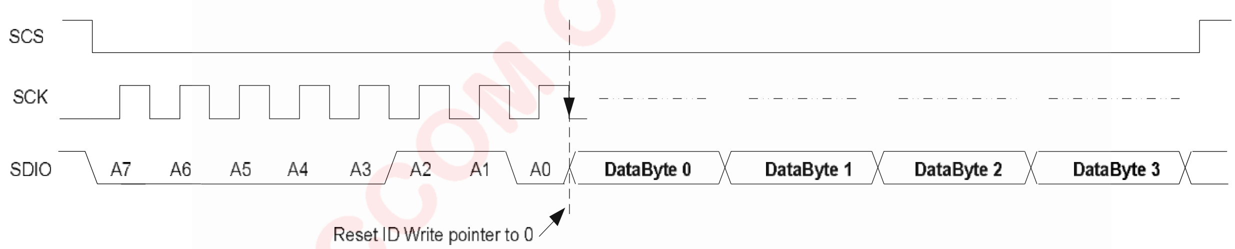



Рис.10.13 Временная диаграмма команды записи идентификатора

### 10.6.2 Команда чтения ID

Пользователь может подробно ознакомиться с временной диаграммой записи SPI на рис.10.2. Ниже приведена процедура выполнения команды чтения ID.

Шаг 1: Передайте A7~A0 = 01000110 (A6=1 для чтения, A5~A0 = 000110 регистр ID DATA, 06h).
Шаг 2: Вывод SDIO выводит 32-битный идентификатор в последовательности байтов данных 0, 1, 2 и 3.
Шаг 3: Переключите вывод SCS на высокий уровень, когда шаг 2 будет завершен.

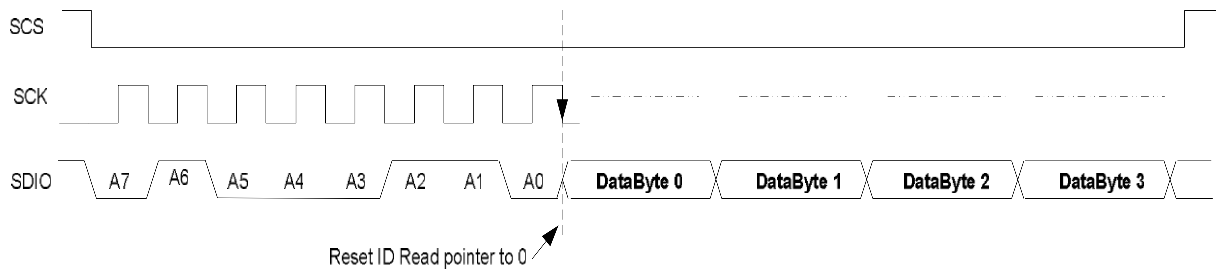



Рис.10.14 Временная диаграмма команды чтения идентификатора

## 10.7 FIFO Accessing CommAnd

To use A7105's FIFO mode, enable FMS (01h) =1 via SPI interface. Before TX delivery, just write wanted data into TX FIFO (05h) then issue TX Strobe commAnd. Similarly, user can read RX FIFO (05h) once payload data is received.

MCU can use polling or interrupt scheme to do FIFO accessing. FIFO status can output to GIO1 (or GIO2) pin by setting GIO1S (0Bh) or GIO2S (0Ch).

Figure 10.15 and 10.16 are timing charts of FIFO accessing via 3-wire SPI.

### 10.7.1 TX FIFO Write CommAnd

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of TX FIFO write commAnd.

Step1: Deliver A7~A0 = 00000101 (A6=0 for write control register and issue FIFO A [5:0] = 05h).
Step2: By SDIO pin, deliver (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n**.**
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send Strobe commAnd of TX mode (Figure 10.9) to do TX delivery.

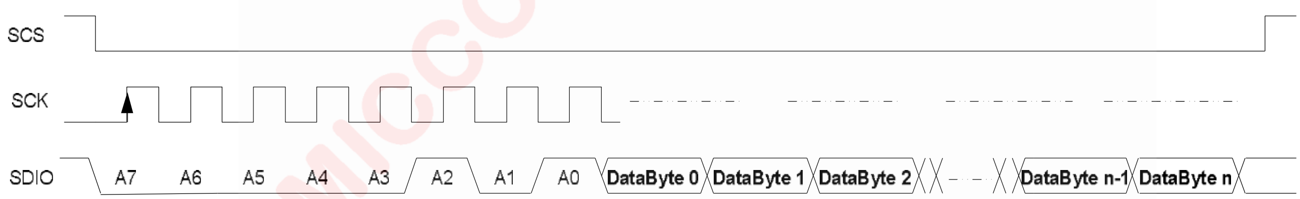



Figure 10.15 TX FIFO Write CommAnd Timing Chart

### 10.7.2 Rx FIFO Read CommAnd

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of RX FIFO read commAnd.

Step1: Deliver A7~A0 = 01000101 (A6=1 for read control register and issue FIFO at address 05h).
Step2: SDIO pin outputs RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when RX FIFO is read completely.

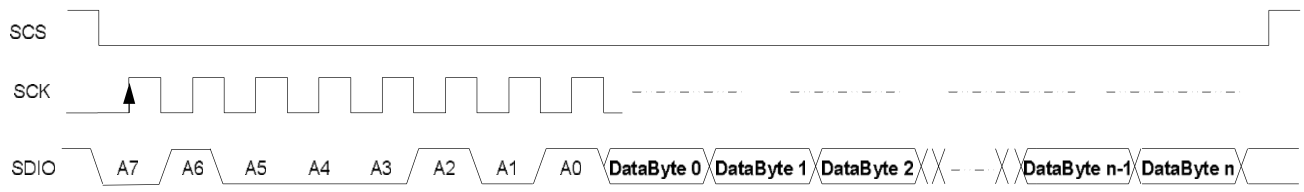



Figure 10.16 RX FIFO Read CommAnd Timing Chart

# 11. State мAchine

In chapter 9 and chapter 10, user can not only learn A7105's control registers but also know how to issue Strobe commAnd. From section 10.2 ~ 10.6, it is clear to know configurations of 3-wire SPI and 4-wire SPI, Strobe commAnd, software reset, and how to access ID Registers as well as TX/RX FIFO.

Section 11.1 introduces 7 states of built-in state мAchine. Combined with Strobe commAnd and accessing control registers, section 11.2, 11.3 and 11.4 demonstrate 3 state diagrams to explain how transitions of A7105's operation.

From accessing data point of view, if FMS=1 (01h), FIFO mode is enabled, otherwise, A7105 is in direct mode. If FMS=1 and FIFO Read/Write in Standby mode, we call it NorмAl FIFO mode. Otherwise, If FMS=1 and FIFO Read/Write in PLL mode, we called it Quick FIFO mode due to the time reduction of PLL settling. If FMS=1 and FIFO Read/Write in IDLE mode, we called it Power Saving FIFO mode due to the reduction of average current.

| | SPI chip select | Data In | Data Out | Operation Mode | Clock Recovery for Direct Mode |
|---|---|---|---|---|---|
| **3-Wire SPI** | SCS pin = 0 | SDIO pin | SDIO pin | FIFO (FMS=1)<br>Direct (FMS=0) | CKO pin<br>(CKOS = 0001) |
| **4-Wire SPI** | SCS pin = 0 | SDIO pin | GIO1 (GIO1S=0110) /<br>GIO2 (GIO2S=0110) | FIFO (FMS=1)<br>Direct (FMS=0) | CKO pin<br>(CKOS = 0001) |

(1) NorмAl FIFO Mode (FMS=1 and FIFO R/W @ Standby mode)
(2) Quick FIFO Mode (FMS=1 and FIFO R/W @ PLL mode)
(3) Power Saving FIFO Mode (FMS=1 and FIFO R/W @ IDLE mode)
(4) Quick Direct Mode (FMS=0 and FIFO ignored, write packet @ TX mode, read packet @ RX mode)

## 11.1 Key states

A7105 supports 7 key operation states. Those are,
(1) Standby mode
(2) Sleep mode
(3) Idle mode
(4) PLL mode
(5) TX mode
(6) RX mode
(7) CAL mode

After power on reset or software reset, A7105 is in standby mode. User has to do calibration process because all control registers are in initial values. The calibration process is very easy, user only needs to issue Strobe commAnds and enable calibration registers. Then, check the calibration flag because it is done autoмAtic by internal state мAchine. Refer to 11.2, 11.3, 11.4 and chapter 15 for details. After calibration, A7105 is ready to do TX and RX operation.

### 11.1.1 Standby mode

If Standby Strobe commAnd is issued, A7105 enters standby mode autoмAtically. Internal power мAnagement is listed below. Be notice, A7105 is in standby mode once power on reset or software reset occurs.

| Standby mode | | | | | | Strobe CommAnd |
|---|---|---|---|---|---|---|
| On Chip Regulator | Crystal Oscillator | VCO | PLL | RX Circuitry | TX Circuitry | |
| ON | ON | OFF | OFF | OFF | OFF | 1010xxxxb<br>See Figure 10.6 |

### 11.1.2 Sleep mode

If Sleep Strobe commмAnd is issued, A7105 enters sleep mode autoмAtically. In sleep mode, A7105 still can accept MCU's commмAnds via SPI interface. But, NOT support to Read/Write FIFO. Internal power мAnagement is listed below.

| Sleep mode | | | | | | Strobe CommмAnd |
|---|---|---|---|---|---|---|
| On Chip Regulator | Crystal Oscillator | VCO | PLL | RX Circuitry | TX Circuitry | |
| OFF | OFF | OFF | OFF | OFF | OFF | 1000xxxxb<br>See Figure 10.4 |

### 11.1.3 Idle mode

If Idle Strobe commмAnd is issued, A7105 enters idle mode autoмAtically. In idle mode, A7105 can accept MCU's commмAnds via SPI interface as well as supporting Read/Write FIFO. Internal power мAnagement is listed below.

| Idle mode | | | | | | Strobe CommмAnd |
|---|---|---|---|---|---|---|
| On Chip Regulator | Crystal Oscillator | VCO | PLL | RX Circuitry | TX Circuitry | |
| ON | OFF | OFF | OFF | OFF | OFF | 1001xxxxb<br>See Figure 10.5 |

### 11.1.4 PLL mode

If PLL Strobe commмAnd is issued, A7105 enters PLL mode autoмAtically. In PLL mode, internal PLL and VCO are both turned on to generate LO (local oscillator) frequency before TX and RX operation. Internal power мAnagement is listed below. According to PLL Register I, II, III, IV and V, PLL circuitry is easy to be controlled by user's definition.

| PLL mode | | | | | | Strobe CommмAnd |
|---|---|---|---|---|---|---|
| On Chip Regulator | Crystal Oscillator | VCO | PLL | RX Circuitry | TX Circuitry | |
| ON | ON | ON | ON | OFF | OFF | 1011xxxxb<br>See Figure 10.7 |

### 11.1.5 TX mode

If TX Strobe commмAnd is issued, A7105 enters TX mode autoмAtically for data delivery. Internal power мAnagement is listed below.

(1) In FIFO mode, once TX data packet (Preamble + ID + Payload) is delivered, A7105 supports auto-back function to previous state for next delivered packet.

(2) In Direct mode, once TX data packet is delivered, A7105 stays in TX mode. User has to issue Strobe commмAnd to back to previous state.

| TX mode | | | | | | Strobe CommмAnd |
|---|---|---|---|---|---|---|
| On Chip Regulator | Crystal Oscillator | VCO | PLL | RX Circuitry | TX Circuitry | |
| ON | ON | ON | ON | OFF | ON | (1101xxxx)b<br>See Figure 10.9 |

### 11.1.6 RX mode

If RX Strobe commмAnd is issued, A7105 enters RX mode autoмAtically for data receiving. Internal power мAnagement is listed below.

(1) In FIFO mode, once RX data packet (Preamble + ID + Payload) is received completely, A7105 supports auto-back function to previous state for next receiving packet.

(2) In Direct mode, once RX data packet is received, A7105 stays in RX mode. User has to issue Strobe commAnd to back to previous state.

| RX mode | | | | | | Strobe CommAnd |
|---|---|---|---|---|---|---|
| On Chip Regulator | Crystal Oscillator | VCO | PLL | RX Circuitry | TX Circuitry | |
| ON | ON | ON | ON | ON | OFF | (1101xxxx)b<br>See Figure 10.9 |

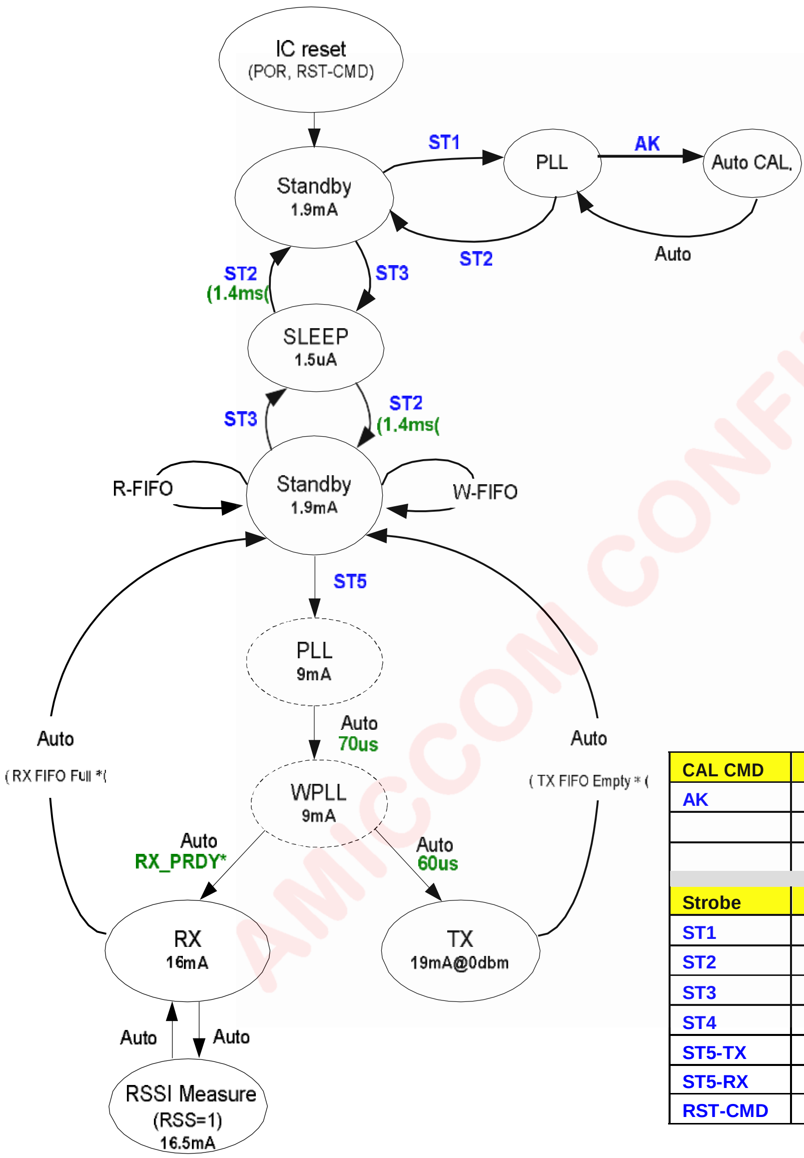
### 11.1.7 CAL mode

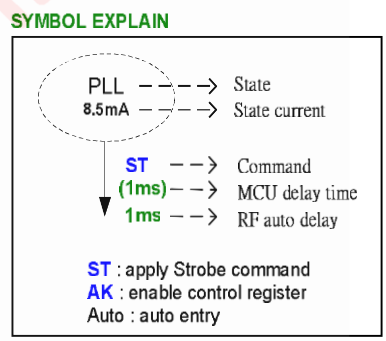
Calibration process shall be done after power on reset or software reset. Calibration items include VCO and IF Filter. It is easy to implement calibration process by Strobe commAnd and enable CALC (02h) control register. See chapter 15 for details.

Be notice, VCO Calibration is only executable in PLL mode. However, IF Filter Calibration can be executed in Standby or PLL mode.

## 11.2 NorмAl FIFO Mode

This mode is suitable for requirement of general purpose applications. After calibration flow, user can issue Strobe commAnd to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet transmission, only one Strobe commAnd is needed. Once transmission is done, A7105 is auto back to standby mode. If all packets are finished and deeper power saving is necessary, user can issue Strobe commAnd to ask A7105 staying in sleep mode. Figure 11.1 is the state diagram of NorмAl FIFO mode.




| CAL CMD | CMD Value | Calibration | Section |
|---|---|---|---|
| AK | CALC.0=1, | IF Filter | 15.2 |
| | CALC.1=1, | VCO Band | 15.3 |
| | CALC.2=1, | VCO Current | 15.4 |

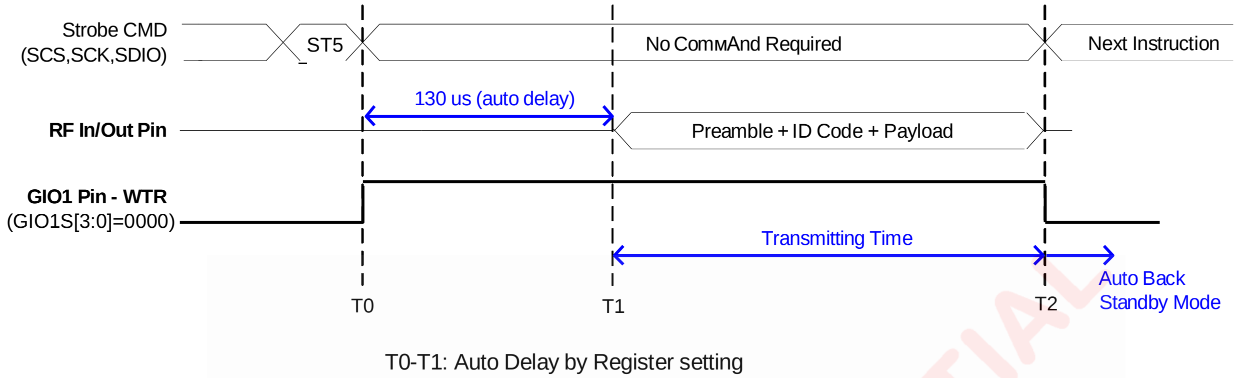
| Strobe | CMD Value | Note | Section |
|---|---|---|---|
| ST1 | 1011b | Enter to PLL | 10.4.4 |
| ST2 | 1010b | Enter to Standby | 10.4.3 |
| ST3 | 1000b | Enter to SLEEP | 10.4.1 |
| ST4 | 1001b | Enter to IDLE | 10.4.2 |
| ST5-TX | 1101b | Enter to TX | 10.4.6 |
| ST5-RX | 1100b | Enter to RX | 10.4.5 |
| RST-CMD | 00000000b | Software Reset | 10.5 |



- Refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.
- See Table 11.3 (next page) for RX-PRDY.

Figure 11.1 State diagram of NorмAl FIFO Mode

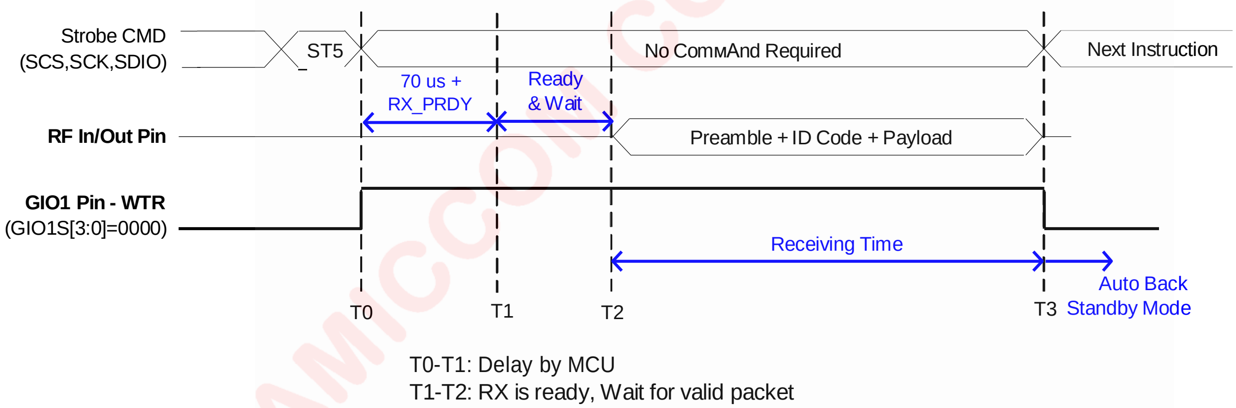
From Figure 11.1, when ST5 commAnd is issued for TX operation, see Figure 11.2 for detailed timing. A7105 status can be represented to GIO1 or GIO2 pin to MCU for timing control.




| LO Freq. | Standby to WPLL | WPLL to TX | TX Ready Time |
|---|---|---|---|
| Changed | 70 us | 60 us | 130 us |
| No Changed | 70 us | 60 us | 130 us |

Figure 11.2 Transmitting Timing Chart of NormAl FIFO Mode

From Figure 11.1, when ST5 commAnd is issued for RX operation, see Figure 11.3 for detailed timing. A7105 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



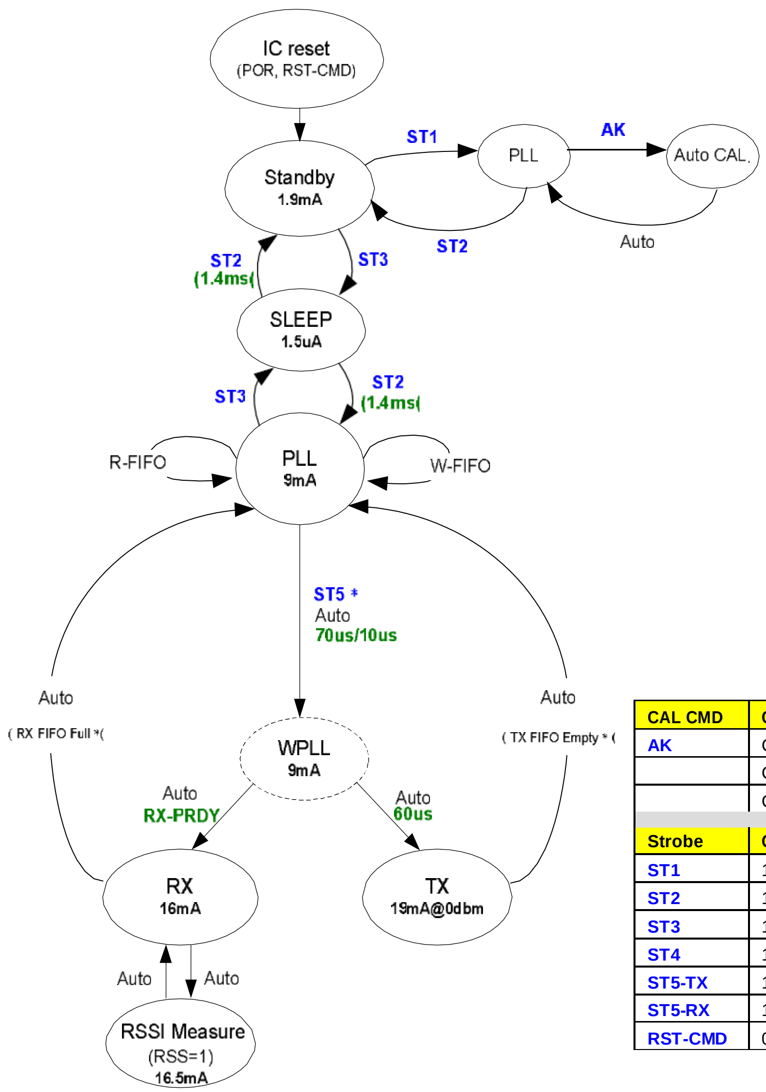

| LO Freq. | Date Rate (bps) | DCM[1:0] (29h) | Standby to WPLL | WPLL to RX (RX-PRDY) | RX Ready Time (Delay by MCU) |
|---|---|---|---|---|---|
| Changed / Fixed | <=125K | By preamble (01b) | 70 us | 40 us | 110 us |
| Changed /Fixed | 250K | By ID (10b) | 70 us | 100 us | 170 us |
| Changed / Fixed | 500K | By ID (10b) | 70 us | 60 us | 130 us |

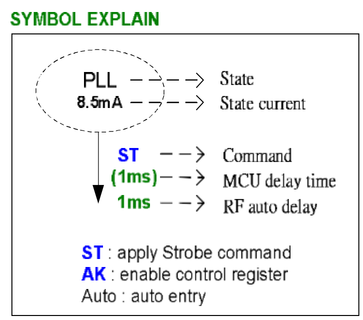
Figure 11.3 Receiving Timing Chart of NormAl FIFO Mode

### 11.3 Quick FIFO Mode

This mode is suitable for requirement of fast transceiving. After calibration flow, user can issue Strobe commAnd to enter PLL mode where write TX FIFO or read RX FIFO. From PLL mode to packet data transceiving, only one Strobe commAnd is needed. Once transceiving is finished, A7105 is auto back to PLL mode.

When packets are finished and deeper power saving is necessary, user can issue Strobe commAnd to ask A7105 staying in sleep mode. Figure 11.4 is the state diagram of Quick FIFO mode.



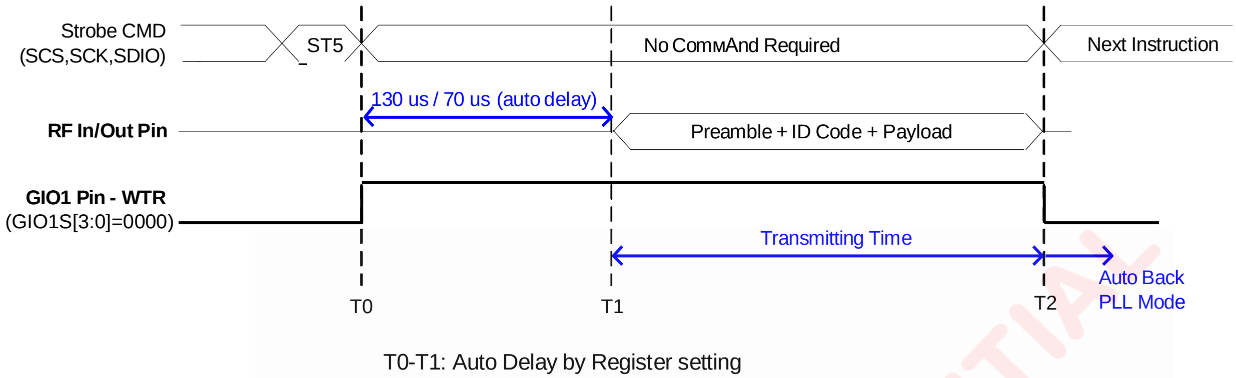




| CAL CMD | CMD Value | Calibration | Section |
|---|---|---|---|
| AK | CALC.0=1, | IF Filter | 15.2 |
| | CALC.1=1, | VCO Band | 15.3 |
| | CALC.2=1, | VCO Current | 15.4 |
| **Strobe** | **CMD Value** | **Note** | **Section** |
| ST1 | 1011b | Enter to PLL | 10.4.4 |
| ST2 | 1010b | Enter to Standby | 10.4.3 |
| ST3 | 1000b | Enter to SLEEP | 10.4.1 |
| ST4 | 1001b | Enter to IDLE | 10.4.2 |
| ST5-TX | 1101b | Enter to TX | 10.4.6 |
| ST5-RX | 1100b | Enter to RX | 10.4.5 |
| RST-CMD | 00000000b | Software Reset | 10.5 |

- Refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.
- See Table 11.6 (next page) for RX-PRDY.
- From PLL to WPLL, it is either 70 us (LO frequency changed) or 10 us (LO frequency NOT changed)

Figure 11.4 State diagram of Quick FIFO Mode

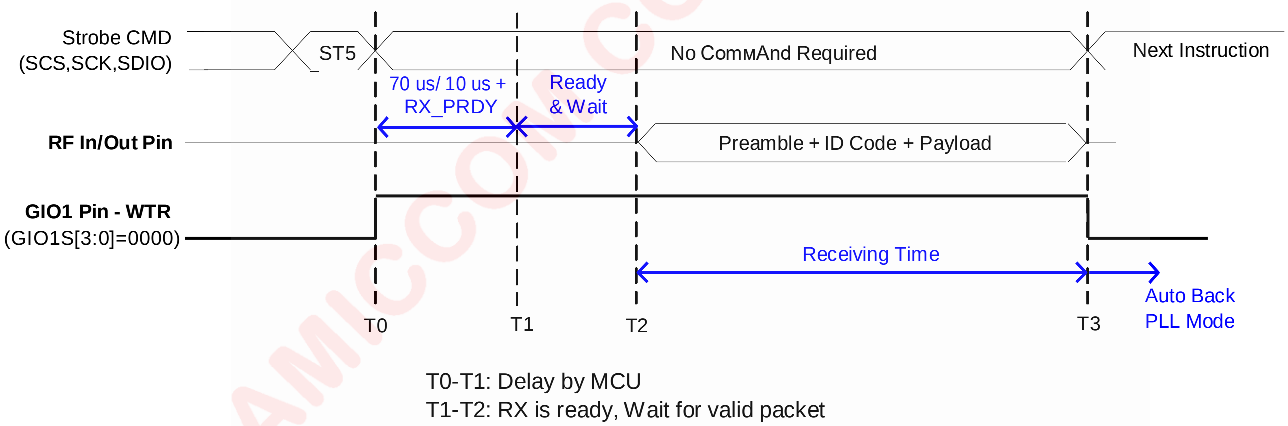
From Figure 11.4, when ST5 commAnd is issued for TX operation, see Figure 11.5 for detailed timing. A7105 status can be represented to GIO1 or GIO2 pin to MCU for timing control.




| LO Freq. | PLL to WPLL | WPLL to TX | TX Ready Time |
|---|---|---|---|
| Changed | 70 us | 60 us | 130 us |
| No Changed | 10 us | 60 us | 70 us |

Figure 11.5 Transmitting Timing Chart of Quick FIFO Mode

From Figure 11.4, when ST5 commAnd is issued for RX operation, see Figure 11.6 for detailed timing. A7105 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



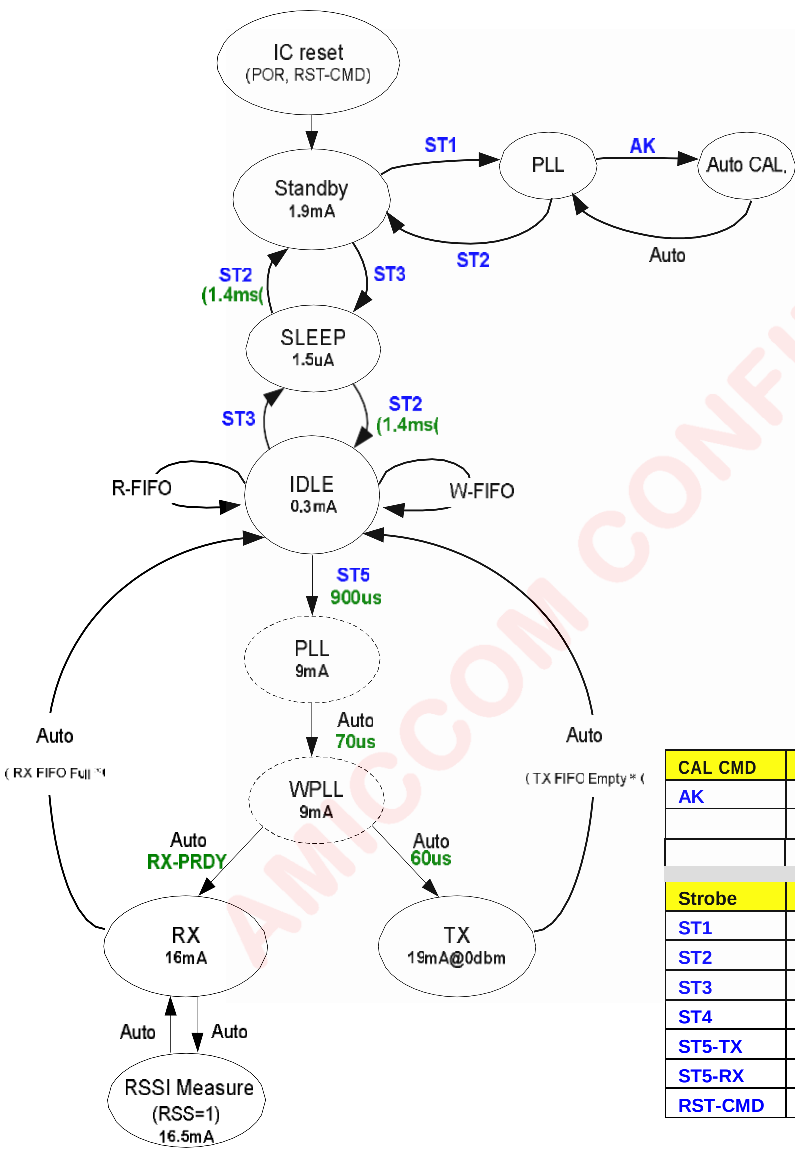

| LO Freq. | Date Rate (bps) | DCM[1:0] (29h) | PLL to WPLL | WPLL to RX (RX-PRDY) | RX Ready Time (Delay by MCU) |
|---|---|---|---|---|---|
| Changed | <=125K | By preamble (01b) | 70 us | 40 us | 110 us |
| Changed | 250K | By ID (10b) | 70 us | 100 us | 170 us |
| Changed | 500K | By ID (10b) | 70 us | 60 us | 130 us |
| Fixed | <=125K | By preamble (01b) | 10 us | 40 us | 50 us |
| Fixed | 250K | By ID (10b) | 10 us | 100 us | 110 us |
| Fixed | 500K | By ID (10b) | 10 us | 60 us | 70 us |

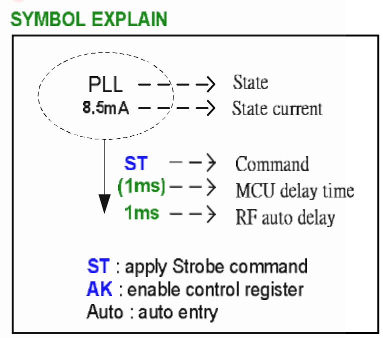
Figure 11.6 Receiving Timing Chart of Quick FIFO Mode

## 11.4 Power Saving FIFO Mode

This mode is suitable for requirement of low power consumption. After calibration flow, user can issue Strobe commAnd to enter idle mode where write TX FIFO or read RX FIFO. From idle mode to packet data transceiving, only one Strobe commAnd is needed. Once transmission is done, A7105 is auto back to idle mode.

When packets are finished and deeper power saving is necessary, user can issue Strobe commAnd to ask A7105 staying in sleep mode. Figure 11.7 is the state diagram of Power Saving FIFO mode.



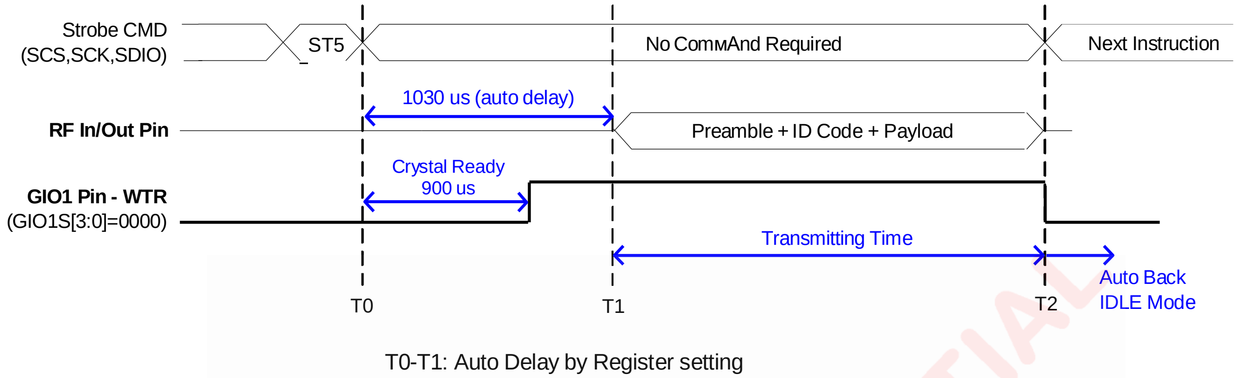




| CAL CMD | CMD Value | Calibration | Section |
|---|---|---|---|
| AK | CALC.0=1, | IF Filter | 15.2 |
| | CALC.1=1, | VCO Band | 15.3 |
| | CALC.2=1, | VCO Current | 15.4 |
| **Strobe** | **CMD Value** | **Note** | **Section** |
| ST1 | 1011b | Enter to PLL | 10.4.4 |
| ST2 | 1010b | Enter to Standby | 10.4.3 |
| ST3 | 1000b | Enter to SLEEP | 10.4.1 |
| ST4 | 1001b | Enter to IDLE | 10.4.2 |
| ST5-TX | 1101b | Enter to TX | 10.4.6 |
| ST5-RX | 1100b | Enter to RX | 10.4.5 |
| RST-CMD | 00000000b | Software Reset | 10.5 |

- Refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.
- See Table 11.9 (next page) for RX-PRDY..

Figure 11.7 State diagram of Power Saving FIFO Mode

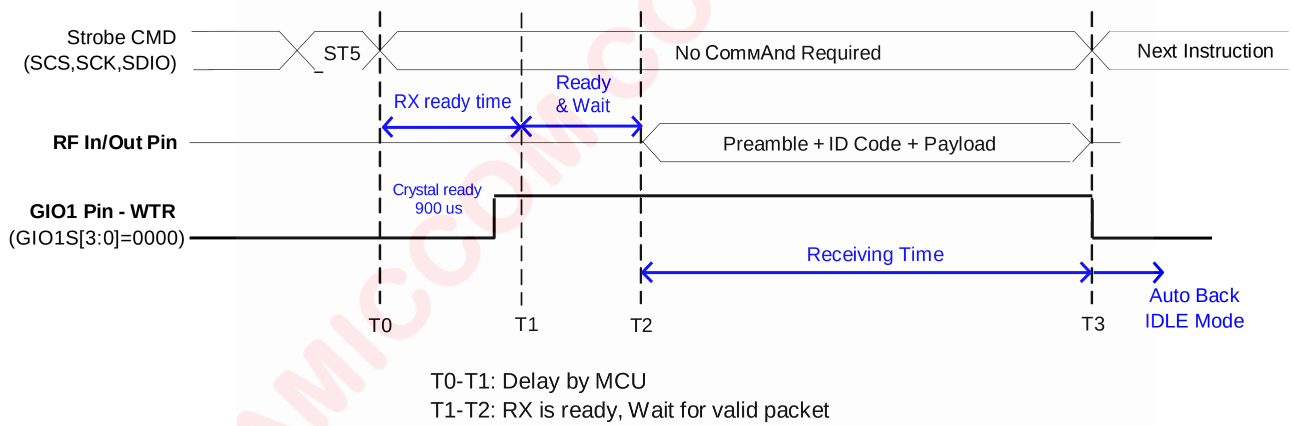
From Figure 11.7, when ST5 commAnd is issued for TX operation, see Figure 11.8 for detailed timing. A7105 status can be represented to GIO1 or GIO2 pin to MCU for timing control.




| LO Freq. | IDLE to WPLL | WPLL to TX | TX Ready Time |
|---|---|---|---|
| Changed | 970 us | 60 us | 1030 us |
| No Changed | 970 us | 60 us | 1030 us |

Figure 11.8 Transmitting Timing Chart of Power Saving FIFO Mode

From Figure 11.7, when ST5 commAnd is issued for RX operation, see Figure 11.9 for detailed timing. A7105 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



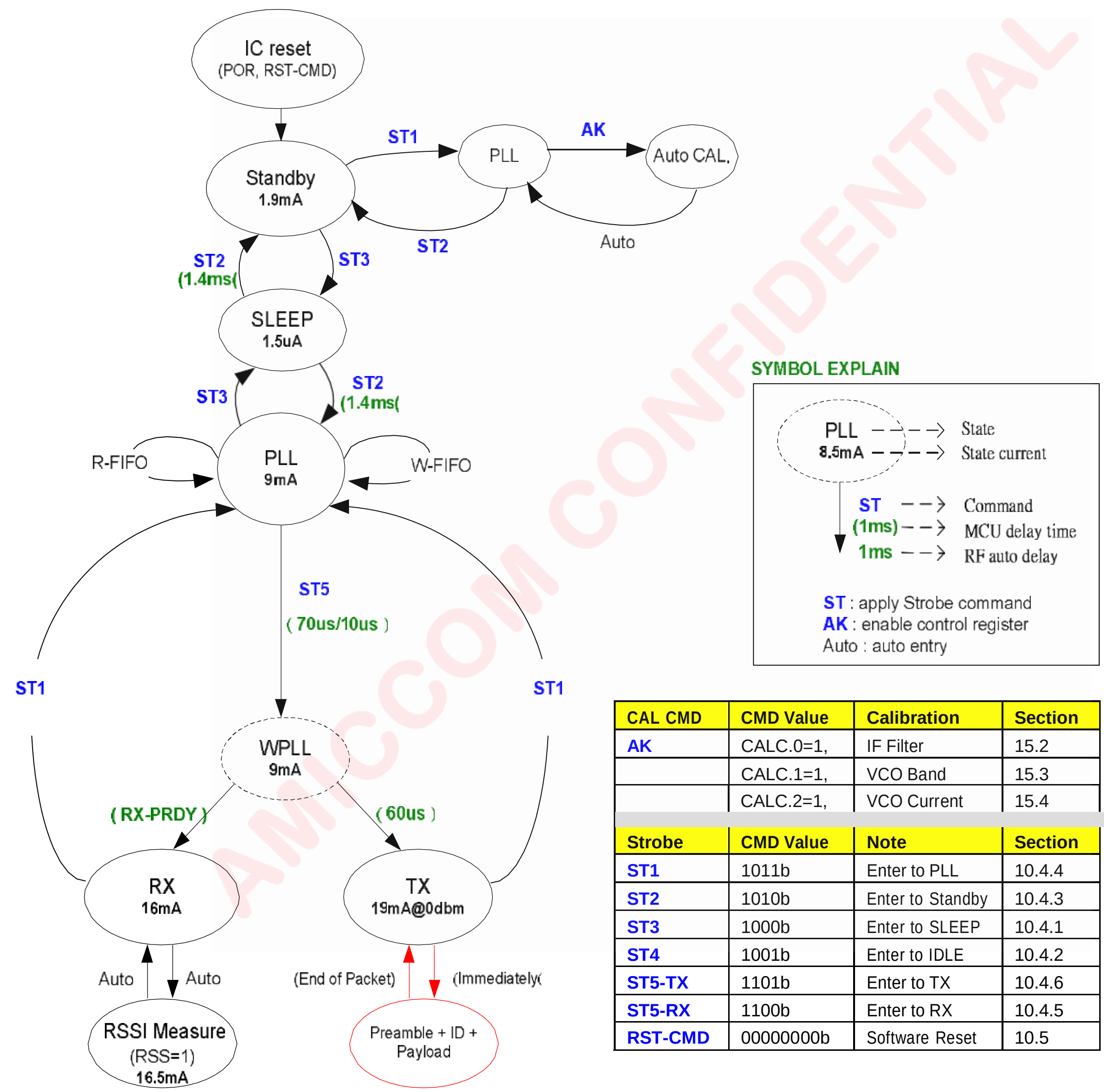

| LO Freq. | Date Rate (bps) | DCM[1:0] (29h) | IDLE to WPLL | WPLL to RX (RX-PRDY) | RX Ready Time (Delay by MCU) |
|---|---|---|---|---|---|
| Changed / Fixed | <=125K | By preamble (01b) | 970 us | 40 us | 1010 us |
| Changed / Fixed | 250K | By ID (10b) | 970 us | 100 us | 1080 us |
| Changed / Fixed | 500K | By ID (10b) | 970 us | 60 us | 1030 us |

Figure 11.9 Receiving Timing Chart of Power Saving FIFO Mode

## 11.5 Quick Direct Mode

This mode is suitable for fast transceiving. After calibration flow, for every state transition, user has to issue Strobe commAnd to A7105.This mode is also suitable for the requirement of versatile packet formAt. Noted that user needs to take care the transition time by MCU's timer.

When packets are finished and deeper power saving is necessary, user can issue Strobe commAnd to ask A7105 staying in idle mode (or sleep mode). Figure 11.3 is the state diagram of Quick Direct mode.






| CAL CMD | CMD Value | Calibration | Section |
|---|---|---|---|
| AK | CALC.0=1, | IF Filter | 15.2 |
| | CALC.1=1, | VCO Band | 15.3 |
| | CALC.2=1, | VCO Current | 15.4 |
| **Strobe** | **CMD Value** | **Note** | **Section** |
| ST1 | 1011b | Enter to PLL | 10.4.4 |
| ST2 | 1010b | Enter to Standby | 10.4.3 |
| ST3 | 1000b | Enter to SLEEP | 10.4.1 |
| ST4 | 1001b | Enter to IDLE | 10.4.2 |
| ST5-TX | 1101b | Enter to TX | 10.4.6 |
| ST5-RX | 1100b | Enter to RX | 10.4.5 |
| RST-CMD | 00000000b | Software Reset | 10.5 |

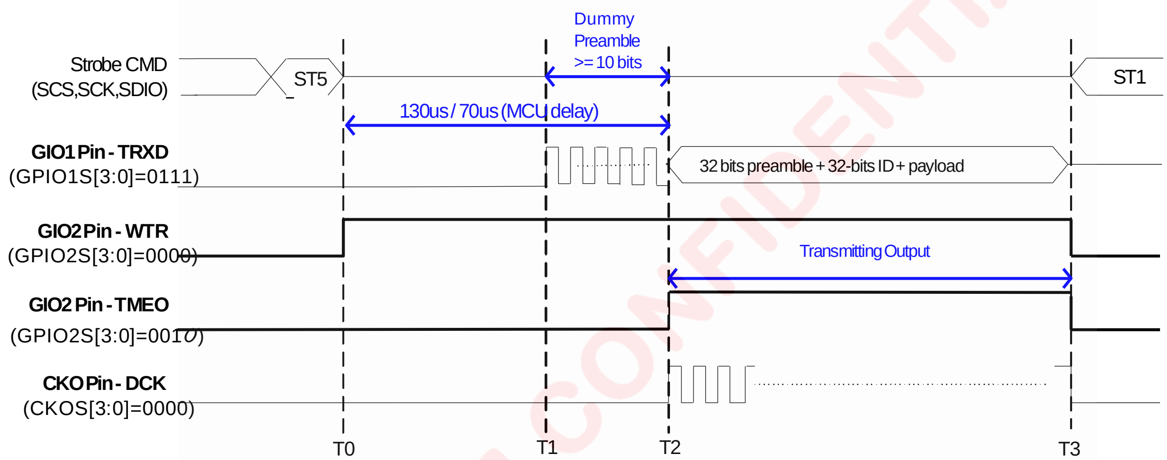
- See Table 11.12 (next page) for RX-PRDY..
- From PLL to WPLL, it is either 70 us (LO frequency changed) or 10 us (LO frequency NOT changed)

Figure 11.10 State diagram of Quick Direct Mode

From Figure 11.10, After A7105 enters TX mode, MCU should immediately deliver preamble. Therefore, user can send dummy preamble since WTR goes high or plus a delay loop to мAke sure dummy preamble is 10 bits at least before DCK is active. See below figure for detail timing.

| A7105 Data Rate | Dummy Preamble | Packet | | | Note |
|---|---|---|---|---|---|
| | | Preamble | ID (06h) | MAx Payload | |
| **2K~500КБит/с** | **≧ 10 bits** | 32 bits | 32 bits | 512 bytes | Total Preamble = **42 bits** |

Table 11.2 FormAt of dummy preamble and packet.



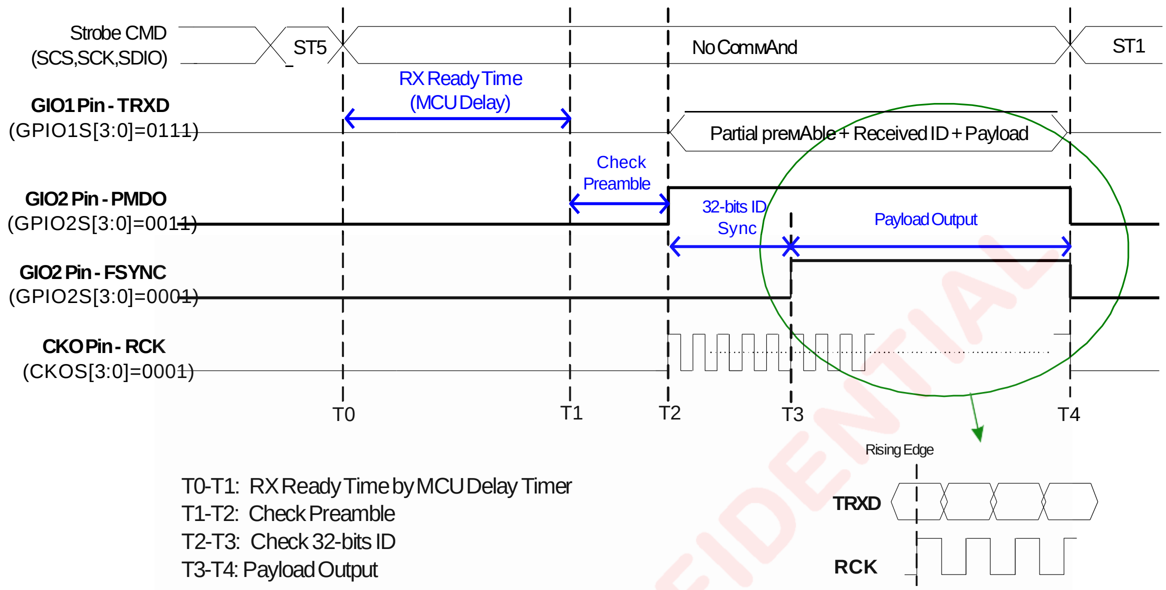

T0-T1: MCU delay loop
T1-T2: Dummy Preamble.
T2: TMEO (TX Modulation Enable) is auto triggered
T2-T3: Transmitting Time

| LO Freq. | PLL to WPLL | WPLL to TX | TX Ready Time |
|---|---|---|---|
| Changed | 70 us | 60 us | 130 us |
| No Changed | 10 us | 60 us | 70 us |

Figure 11.11 Transmitting Timing Chart of Quick Direct Mode



From Figure 11.10, in RX mode, A7105 will check received ID compared to ID register (06h). If ID is мAtched, FSYNC will be output. MCU can decode received ID and payload from GIO1 pin (TRXD) via rising edge of RCK (recovery clock). Then, GIO2 pin can be used to inform MCU reference timing by PMDO (Preamble Detect Output) or FSYNC (Frame Sync).




| LO Freq. | Date Rate (bps) | DCM[1:0] (29h) | PLL to WPLL | WPLL to RX (RX-PRDY) | RX Ready Time (Delay by MCU) |
|---|---|---|---|---|---|
| Changed | <=125K | By preamble (01b) | 70 us | 40 us | 110 us |
| Changed | 250K | By ID (10b) | 70 us | 100 us | 170 us |
| Changed | 500K | By ID (10b) | 70 us | 60 us | 130 us |
| No Changed | <=125K | By preamble (01b) | 10 us | 40 us | 50 us |
| No Changed | 250K | By ID (10b) | 10 us | 100 us | 110 us |
| No Changed | 500K | By ID (10b) | 10 us | 60 us | 70 us |

Figure 11.12 Receiving Timing Chart of Quick Direct Mode

# 12 Crystal Oscillator

A7105 needs external crystal or external clock that is either 6 or 8/12/16/20/24 МГцto generate internal wanted clock. Be noted if external clock is equal or lower than 8MHz, A7105 only supports data rate up to 250K.

**Relative Control Register**

Clock Register (Address: 0Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Clock | R/W | GRC3 | GRC2 | GRC1 | GRC0 | CSC1 | CSC0 | CGS | XS |
| Reset | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

## 12.1 Use External Crystal

Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance are used to adjust different crystal loading. A7105 supports crystal accuracy within ±20 ppm under firmware frequency compensation. Be noted that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

| A7105 | Crystal Accuracy | Crystal ESR |
|---|---|---|
| Firmware FC = On | ±20 ppm | ≦ 80 ohm |
| Firmware FC = Off | ±10 ppm | ≦ 80 ohm |

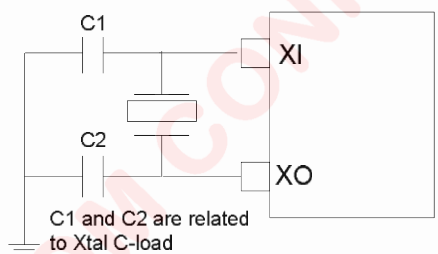



Fig12.1 Crystal oscillator circuit, refer to A7105 App. Note for C1 and C2.

## 12.2 Use external clock

A7105 has built-in AC couple capacitor to support external clock input. Figure 12.2 shows how to connect. In such case, XI pin is left opened. XS shall be low (0Dh) for selecting external clock. The frequency accuracy of external clock shall be controlled within ± 20 ppm, and the amplitude of external clock shall be within 1.2 ~ 1.8 V peak-to-peak.

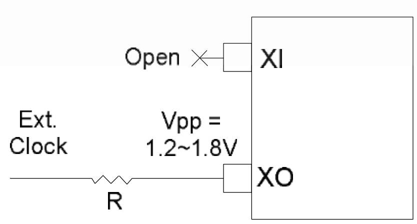



Fig12.2 External clock source. R is used to tune Vpp = 1.2~1.8V

## 13. System Clock

A7105 supports different crystal frequency by programмAble “Clock Register” (0Dh). Based on this, three important internal clocks $F_{CGR}$ , $F_{DR}$ and $F_{SYCK}$ are generated.

(1) $F_{XTAL}$: Crystal frequency.
(2) $F_{XREF}$: Crystal Ref. Clock = $F_{XTAL}$ * (DBL+1).
(3) $F_{CGR}$: Clock Generation Reference = 2МГц= $F_{XREF}$ / (GRC+1), where $F_{CGR}$ is used to generate 32M PLL.
(4) $F_{MCLK}$: MAster Clock is either $F_{XREF}$: or 32M PLL, where $F_{MCLK}$ is used to generate $F_{SYCK}$.
(5) $F_{SYCK}$: System Clock = 16MHz=$F_{MCLK}$ / CSC= 32 * $F_{IF}$, where $F_{IF}$ is recommended to set 500КГц.
(6) $F_{DR}$: Data Rate Clock = $F_{IF}$ / (SDR+1).
(7) $F_{FPD}$: VCO Compared Clock = = $F_{XREF}$ / (RRC+1).

### Relative Control Register

Clock Register (Address: 0Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Clock | R/W | GRC3 | GRC2 | GRC1 | GRC0 | CSC1 | CSC0 | CGS | XS |
| Reset | | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

Data Rate Register (Address: 0Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Data Rate | R/W | SDR7 | SDR6 | SDR5 | SDR4 | SDR3 | SDR2 | SDR1 | SDR0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PLL Register II (Address: 10h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL II | W | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | BIP8 |
| | R | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | IP8 |
| Reset | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

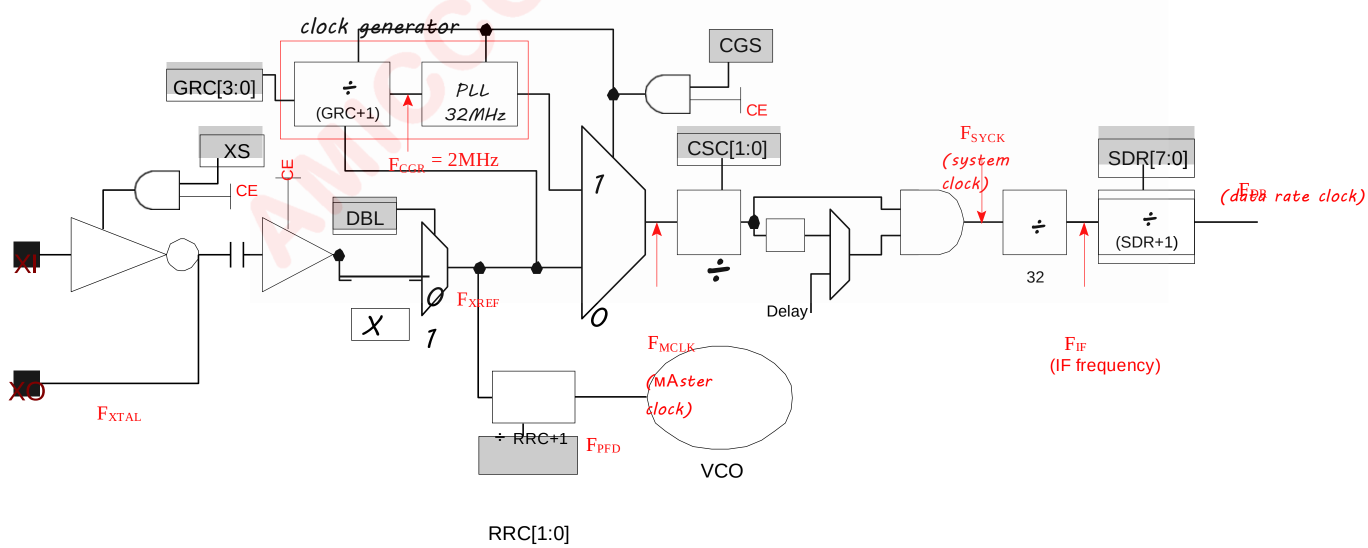



Fig13.1 System clock block diagram

As show in Fig 13.1, $F_{MCLK}$, the мAster clock either come from $F_{XREF}$ (CGS = 0) or PLL 32МГц(CGS = 1). The relation between $F_{SYCK}$ (the system clock) and $F_{MCLK}$ (мAster clock) show in table 13.1

| $F_{SYCK}$ (MAster Clock) | | |
|---|---|---|
| | CGS = 0 | CGS = 1 |
| DBL=0 | $F_{XTAL}$ | 32 MHz |
| DBL=1 | **2 * $F_{XTAL}$ (Recommend)** | 32 MHz |

| CSC [1:0] | $F_{SYCK}$ (system clock) | Note |
|---|---|---|
| 00 | $F_{MCLK}$ | $F_{SYCK}$ is used to determine<br>1. Data rate clock (0Eh)<br>2. ADC clock (1Eh)<br>3. Internal digital clock (09h)<br>4. CKO pin (0Ah) |
| 01 | $F_{MCLK}$ /2 | |
| 10 | $F_{MCLK}$ /2 | |
| 11 | $F_{MCLK}$ /4 | |

Table 13.1 System clock and мAster clock

## 13.1 Bypass clock generation

If crystal frequency is multiplier of 8MHz, the clock generator block can be turned off by setting CGS = 0.The relation between $F_{XTAL}$ (crystal frequency) and data rate show below:

**$F_{XREF}$ = $F_{XTAL}$ * (DBL+1)**
**$F_{PFD}$ = $F_{XREF}$ / (RRC [1:0]+1)**
**$F_{DR}$ = $F_{XREF}$ / (CSC [1:0]+1) / 32 / (SDR+1)**

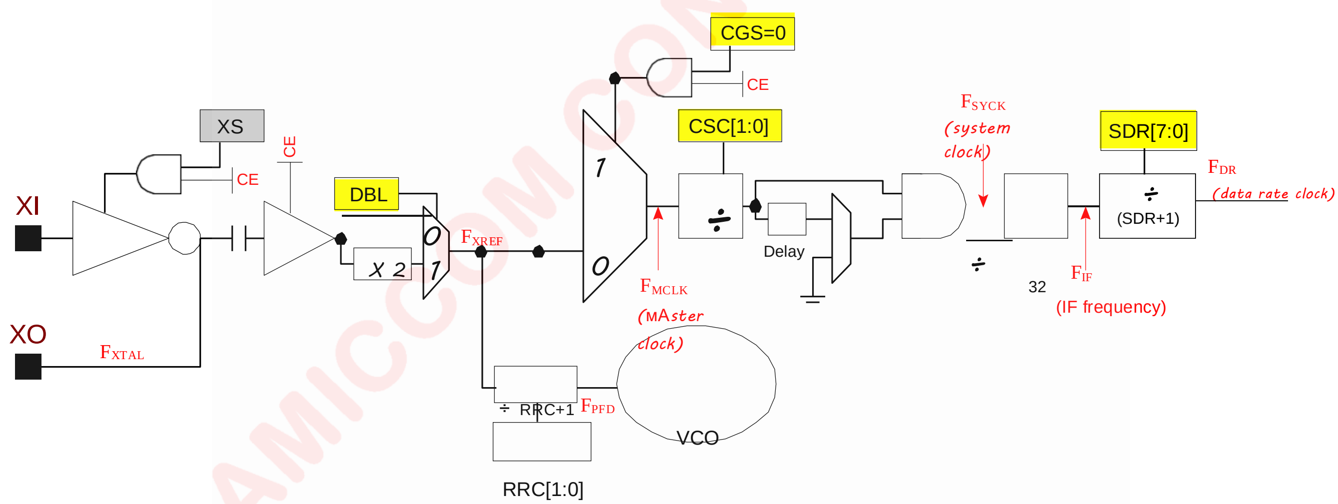



Fig13.2 By pass clock generator to get system clock



For various data rate application, list some examples below.
For more data rate options, please contact AMICCOM FAE team.

**Data rate 500КБит/с**

| Crystal source | CGS (0Dh) | DBL (10h) | CSC[1:0] (0Dh) | GRC [3:0] (0Dh) | $F_{IF}$ (КГц) | BWS (18h) | RRC [1:0] (10h) | $F_{PFD}$ (MHz) | CHR [3:0] (10h) | $F_{CHSP}$ (MHz) | SDR [7:0] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 16MHz | 0 | 1 | 01 | Don't care | 500 | 1 | 00 | 32 | 1111 | 0.5 | 0x00 |

**Data rate = 250K / 125K / 100K / 50K / 25K / 10K / 2КБит/с**

| Crystal source | CGS (0Dh) | DBL (10h) | CSC[1:0] (0Dh) | GRC [3:0] (0Dh) | $F_{IF}$ (КГц) | BWS (18h) | RRC [1:0] (10h) | $F_{PFD}$ (MHz) | CHR [3:0] (10h) | $F_{CHSP}$ (MHz) | SDR [7:0] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8MHz | 0 | 1 | 01 | Don't care | 500 | 1 | 00 | 16 | 0111 | 0.5 | See next table |
| 16MHz | | | | | | | | 32 | 1111 | | |

**SDR Table**

| | 250КБит/с | 125КБит/с | 100КБит/с | 50КБит/с | 25КБит/с | 10КБит/с | 2КБит/с |
|---|---|---|---|---|---|---|---|
| **SDR [7:0]** | 0x01 | 0x03 | 0x04 | 0x09 | 0x13 | 0x31 | 0xF9 |

## 13.2 Enable clock generation

If crystal frequency is the multiplier of 2МГцand larger than 6MHz, set CGS = 1 to enable **$F_{SYCK}$**= 32МГц(internal 32МГцPLL). The comparison frequency of clock generator $F_{CGR}$ shall be 2МГцby setting GRC[3:0] to meets the below equations.

**$F_{CRG}$ = $F_{XTAL}$ * (1+DBL) / (GRC+1) = 2MHz.**
**$F_{DR}$ = $F_{SYCK}$ / 32 / (SDR+1).**

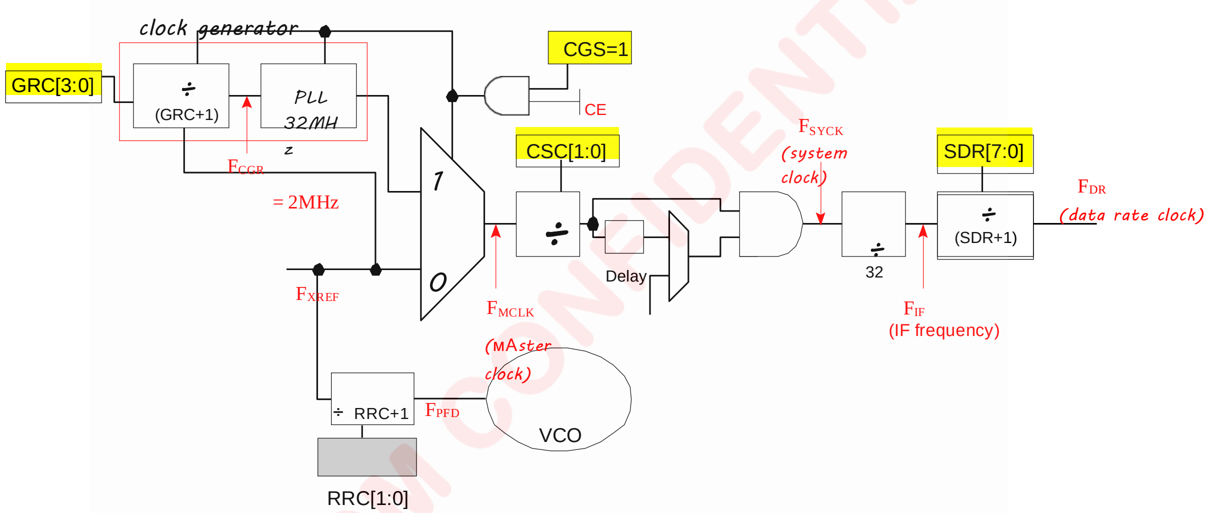



Fig13.3 Enable clock generator to get system clock



For various data rate application, list some examples below. For more data rate options, please contact AMICCOM FAE team.

**Data rate 500КБит/с**

| Crystal source | CGS (0Dh) | DBL (10h) | CSC[1:0] (0Dh) | GRC [3:0] (0Dh) | $F_{IF}$ (КГц) | BWS (18h) | RRC [1:0] (10h) | $F_{PFD}$ (MHz) | CHR [3:0] (10h) | $F_{CHSP}$ (MHz) | SDR [7:0] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 12MHz | 1 | 1 | 01 | 1011 | 500 | 1 | 00 | 24 | 1011 | 0.5 | 0x00 |
| 16MHz | | 1 | | 1111 | | | | 32 | 1111 | | |
| 24MHz | | 0 | | 1011 | | | | 24 | 1011 | | |

**Data rate = 250K / 125K / 100K / 50K / 25K / 10K / 2КБит/с**

| Crystal source | CGS (0Dh) | DBL (10h) | CSC[1:0] (0Dh) | GRC [3:0] (0Dh) | $F_{IF}$ (КГц) | BWS (18h) | RRC [1:0] (10h) | $F_{PFD}$ (MHz) | CHR [3:0] (10h) | $F_{CHSP}$ (MHz) | SDR [7:0] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 6MHz | 1 | 1 | 01 | 0101 | 500 | 1 | 00 | 12 | 0101 | 0.5 | See next table |
| 8MHz | | 1 | | 0111 | | | | 16 | 0111 | | |
| 12MHz | | 1 | | 1011 | | | | 24 | 1011 | | |
| 16MHz | | 1 | | 1111 | | | | 32 | 1111 | | |
| 24MHz | | 0 | | 1011 | | | | 24 | 1011 | | |

**SDR Table**

| | 250КБит/с | 125КБит/с | 100КБит/с | 50КБит/с | 25КБит/с | 10КБит/с | 2КБит/с |
|---|---|---|---|---|---|---|---|
| SDR [7:0] | 0x01 | 0x03 | 0x04 | 0x09 | 0x13 | 0x31 | 0xF9 |

## 14. Transceiver LO Frequency

A7105 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO (Local Oscillator) frequency for two ways radio transmission.

To target full range of 2.4ГГц ISM band (2400 МГцto 2483.5 MHz), A7105 applies offset concept by LO frequency $\mathbf{F_{LO} = F_{LO\_BASE} + F_{OFFSET}}$. Therefore, this device is easy to implement frequency hopping and multi-channels by just **ONE** register setting, **PLL Register I (CHN [7:0], 0Eh).**

Below is the LO frequency block diagram.

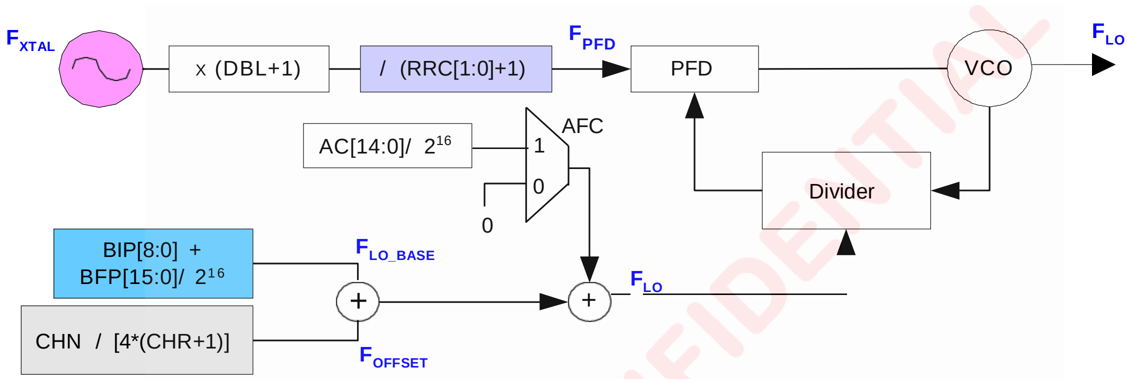



Fig14.1 Frequency synthesizer block diagram



**Relative Control Register**

PLL Register I (Address: 0Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL I | R/W | CHN7 | CHN6 | CHN5 | CHN4 | CHN3 | CHN2 | CHN1 | CHN0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PLL Register II (Address: 10h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL II | W | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | BIP8 |
| | R | DBL | RRC1 | RRC0 | CHR3 | CHR2 | CHR1 | CHR0 | IP8 |
| Reset | | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

PLL Register III (Address: 11h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL III | W | BIP7 | BIP6 | BIP5 | BIP4 | BIP3 | BIP2 | BIP1 | BIP0 |
| | R | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| Reset | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

PLL Register IV (Address: 12h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| PLL IV | W | BFP15 | BFP14 | BFP13 | BFP12 | BFP11 | BFP10 | BFP9 | BFP8 |
| | R | --/FP15 | AC14/FP14 | AC13/FP13 | AC12/P12 | AC11/ FP11 | AC10/FP10 | AC9/FP9 | AC8/FP8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PLL Register V (Address: 13h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| PLL V | W | BFP7 | BFP6 | BFP5 | BFP4 | BFP3 | BFP2 | BFP1 | BFP0 |
| | R | AC7/FP7 | AC6/FP6 | AC5/FP5 | AC4/FP4 | AC3/FP3 | AC2/FP2 | AC1/FP1 | AC0/FP0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

RX Register (Address: 18h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RX | W | -- | RXSM1 | RXSM0 | FC | RXDI | DMG | BWS | ULS |
| Reset | | -- | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

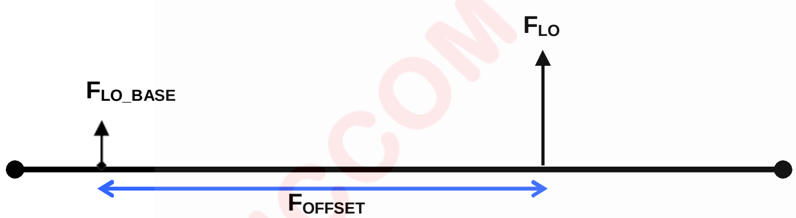
Mode Control Register (Address: 01h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control I | W | R | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS |
| | R | W | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 14.1 LO Frequency Setting

From Figure 14.1, $F_{LO}$ is not only for TX radio frequency but also to be RX LO frequency. To set up $F_{LO,}$ it is easy to implement by below 4 steps.

1. Set the base frequency ($F_{LO\_BASE}$) by PLL Register II, III, IV and V (10h, 11h, 12h and 13h).
   **Recommend to set $F_{LO\_BASE}$ ~ 2400.001MHz.**
2. Set the channel step ($F_{CHSP}$) by PLL Register II (10h).
   **$F_{CHSP} = F_{XTAL}$ * (DBL+1) / 4 / (CHR+1), Recommend $F_{CHSP}$ = 500 КГц.**
3. Set CHN [7:0] to get offset frequency by PLL Register I (0Fh).
   **$F_{OFFSET}$ = CHN [7:0] x $F_{CHSP}$**
4. LO frequency is equal to base frequency plus offset frequency.
   **$F_{LO} = F_{LO\_BASE} + F_{OFFSET}$**




**$F_{LO\_BASE}$**

$$F_{LO\_BASE} = F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) = (DBL+1) \cdot \frac{F_{XTAL}}{RRC[1:0]+1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

Base on the above formula, for example, if $F_{XTAL}$ = 16 МГцand set channel step $F_{CHSP}$ = 500 КГц, to get **$F_{LO\_BASE}$ and $F_{LO}$**, see Table 14.1, 14.2, and Figure 14.2 for details.

| STEP | ITEMS | VALUE | NOTE |
|---|---|---|---|
| 1 | $F_{XTAL}$ | 16 MHz | Crystal Frequency |
| 2 | DBL | 1 | Enable double function |
| 3 | RRC | 0 | If so, $F_{PFD}$= 32MHz |
| 4 | BIP | 0x4B | To get $F_{LO\_BASE}$ =2400 MHz |
| 5 | BFP | 0x0002 | To get $F_{LO\_BASE}$ ~ 2400.001 MHz |
| 6 | **$F_{LO\_BASE}$** | **~2400.001 MHz** | LO Base frequency |

Table 14.1 How to set $F_{LO\_BASE}$

How to set $F_{TXRF} = F_{LO} = F_{LO\_BASE} + F_{OFFSET}$ ~ 2405.001 MHz

| STEP | ITEMS | VALUE | NOTE |
|---|---|---|---|
| 1 | $F_{LO\_BASE}$ | ~2400.001 MHz | After set up BIP and BFP |
| 2 | CHR | 0x0F | To get $F_{CHSP}$= 500 КГц |
| 3 | $F_{CHSP}$ | 500 КГц | Channel step = 500КГц |
| 4 | CHN | 0x0A | Set channel number = 10 |
| 5 | $F_{OFFSET}$ | 5 MHz | $F_{OFFSET}$= 500 КГц * (CHN) = 5MHz |
| 6 | $F_{LO}$ | ~2405.001 MHz | Get $F_{LO}$= $F_{LO\_BASE}$ + $F_{OFFSET}$ |
| 7 | **$F_{TXRF}$** | **~2405.001 MHz** | $F_{TXRF} = F_{LO}$ |

Table 14.2 How to set $F_{TXRF}$

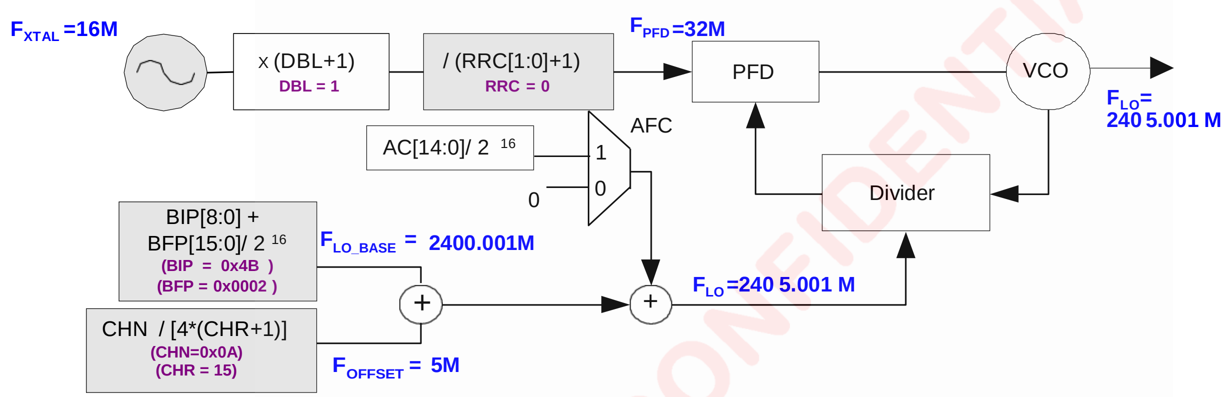



Figure 14.2 Block Diagram of set up $F_{LO}$ ~ 2405.001 MHz



For different crystal frequency, 24МГц/ 16МГц/ 12 МГц/ 8МГц/ 6MHz, below are calculation details for $F_{FPD}$ and $F_{CHSP}$

$$F_{PFD} = \frac{(DBL+1)\cdot f_{XTAL}}{RRC[1:0]+1}$$

| $F_{XTAL}$ (MHz) | DBL | RRC | $F_{PFD}$ (MHz) | Note |
|---|---|---|---|---|
| 24 | 0 | 0 | 24 | |
| 16 | 1 | 0 | 32 | (reference design) |
| 12 | 1 | 0 | 24 | |
| 8 | 1 | 0 | 16 | |
| 6 | 1 | 0 | 12 | |

$$F_{CHSP} = \frac{F_{PFD}}{4\cdot(CHR[3:0]+1)}$$

| $F_{XTAL}$ (MHz) | $F_{PFD}$ (MHz) | CHR [3:0] | $F_{CHSP}$ (КГц) | CHN [7:0] | $F_{OFFSET}$ (MHz) | $F_{LO}$ (MHz) |
|---|---|---|---|---|---|---|
| 24 | 24 | 1011 | 500 | 0x00 ~ 0xA8 | 0 ~ 84 | 2400 ~ 2484 |
| 16 | 32 | 1111 | 500 | 0x00 ~ 0xA8 | 0 ~ 84 | 2400 ~ 2484 |
| 12 | 24 | 1011 | 500 | 0x00 ~ 0xA8 | 0 ~ 84 | 2400 ~ 2484 |
| 8 | 16 | 0111 | 500 | 0x00 ~ 0xA8 | 0 ~ 84 | 2400 ~ 2484 |
| 6 | 12 | 0101 | 500 | 0x00 ~ 0xA8 | 0 ~ 84 | 2400 ~ 2484 |

## 14.2 IF Side Band Select

In two ways radio, both мAster and slave have two roles, TX and RX. In general, slave usually has to reply an ACK-packet or status update. In such case, A7105 offers two methods to set up $\mathbf{F_{LO}}$ while TRX exchanging.

(1) Auto IF exchange
(2) Fast exchange

**Relative Control Register**

Mode Control Register (Address: 01h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| | W | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RX Register (Address: 18h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | -- | RXSM1 | RXSM0 | FC | RXDI | DMG | BWS | ULS |
| Reset | | -- | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

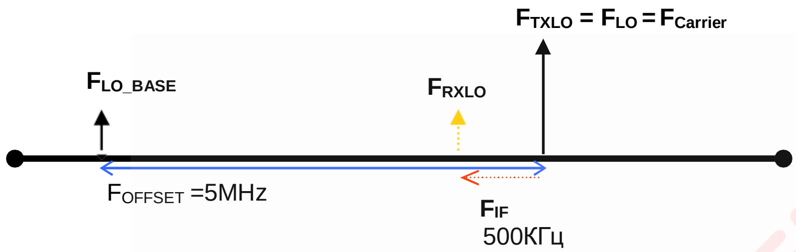
| Register Setting | AIF Function | $F_{RXLO}$ Formula |
|---|---|---|
| ULS=0 | Disable (AIF=0) | $F_{RXLO} = F_{LO}$ |
| ULS=1 | | $F_{RXLO} = F_{LO}$ |
| ULS=0 | Enable (AIF=1) | $F_{RXLO} = F_{LO}$ − 500КГц |
| ULS=1 | | $F_{RXLO} = F_{LO}$ + 500Kz |

Table 14.3 $F_{RXLO}$ Formula

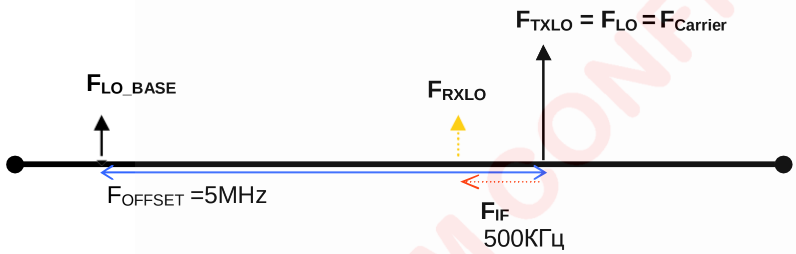
### 14.2.1 Auto IF Exchange

A7105 supports Auto IF offset function (AIF, 01h). If AIF is enabled, only one on-air occupied frequency (Fcarrier). In this case, user has no need to change $F_{RXLO}$ while TRX exchanging because $F_{RXLO}$ is auto shifted $F_{IF}$. See below Figures and Table 14.4 for details.

**<MAster>**
AIF=1 and ULS=0, $F_{RXLO}$ is auto shifted lower than $F_{TXLO}$ for 500КГц ($F_{IF}$).




**<Slave>**
AIF=1 and ULS=0, $F_{RXLO}$ is auto shifted lower than $F_{TXLO}$ for 500КГц ($F_{IF}$).



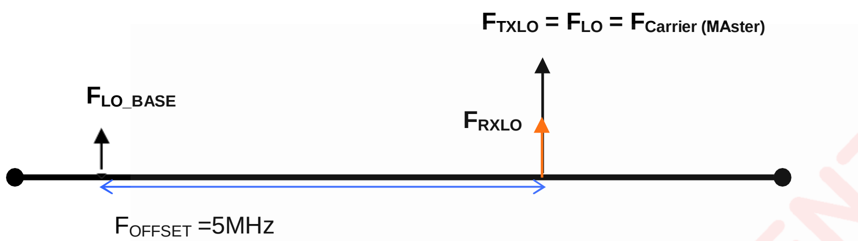

| Item | Role | AIF | ULS | CHN[7:0] | $F_{CHSP}$ (КГц) | $F_{TXLO}$ (КГц) | $F_{RXLO}$ (MHz) | NOTE |
|---|---|---|---|---|---|---|---|---|
| **MAster** | TX | 1 | 0 | **10** | 500 | 2405.001 | - | |
| | RX | 1 | 0 | **10** | 500 | - | 2404.501 | Up side band $F_{RXLO}$ is auto shifted |
| **Slave** | TX | 1 | 0 | **10** | 500 | 2405.001 | - | |
| | RX | 1 | 0 | **10** | 500 | - | 2404.501 | Up side band $F_{RXLO}$ is auto shifted |

Table 14.4 AIF function while TRX exchanging

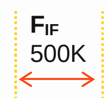
### 14.2.2 Fast Exchange

To reduce PLL settling time, user can disable AIF function. If AIF is disabled, two On-air frequency (**F**$_{\mathbf{Carrier\ (MAster)}}$, **F**$_{\mathbf{Carrier\ (slave)}}$) are occupied. In this case, user has to control ULS =0 (MAster side) and ULS = 1 (Slave side) for fast exchange in two-way radio. See below Figures and Table 14.5 for details.

**<MAster>**
**AIF=0 and ULS=0, MAster is set Up side band.**




**<Slave>**
**AIF=0 and ULS=1, Slave is set Low side band.**





| Item | Role | AIF | ULS | CHN[7:0] | $F_{CHSP}$ (КГц) | $F_{TXLO}$ (КГц) | $F_{RXLO}$ (MHz) | NOTE |
|---|---|---|---|---|---|---|---|---|
| **MAster** | TX | 0 | **0** | **10** | 500 | 2405.001 | - | |
| | RX | 0 | **0** | **10** | 500 | - | 2405.001 | Up side band |
| **Slave** | TX | 0 | **1** | **14** | 500 | 2405.501 | - | |
| | RX | 0 | **1** | **14** | 500 | - | 2405.501 | Low side band |

Table 14.5 Fast exchange function while TRX exchanging

## 14.3 Frequency Compensation

Frequency Compensation function (FC) supports low accuracy crystal (±20 ppm) without sensitivity degradation. The FC concept is to fine tune RX LO frequency (**$F_{RXLO}$**). MCU can read AC[14:0], (12h) and (13h), to executes frequency drift calculation and update new setting to PLL IV (12h) and PLL V (13h) to adjust the best RX LO frequency (**$F_{RXLO}$**).

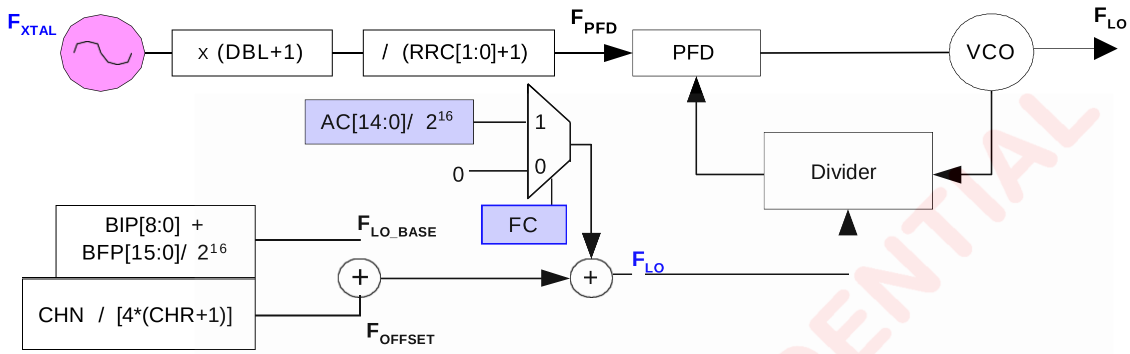



Figure 14.3 Block Diagram of enabling FC function

**Relative Control Register**

RX Register (Address: 18h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | -- | RXSM1 | RXSM0 | FC | RXDI | DMG | RAW | ULS |
| Reset | | -- | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

PLL Register IV (Address: 12h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | --/FP15 | AC14/FP14 | AC13/FP13 | AC12/P12 | AC11/ FP11 | AC10/FP10 | AC9/FP9 | AC8/FP8 |
| | W | BFP15 | BFP14 | BFP13 | BFP12 | BFP11 | BFP10 | BFP9 | BFP8 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PLL Register V (Address: 13h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R | AC7/FP7 | AC6/FP6 | AC5/FP5 | AC4/FP4 | AC3/FP3 | AC2/FP2 | AC1/FP1 | AC0/FP0 |
| | W | BFP7 | BFP6 | BFP5 | BFP4 | BFP3 | BFP2 | BFP1 | BFP0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

For Frequency Compensation procedure, please refer to AMICCOM's reference code and contact AMICCOM FAE team for details.

# 15. Calibration

A7105 needs calibration process after power on reset or software reset by 3 calibration items, they are, VCO Current, VCO Bank, and IF Filter Bank.

1. VCO Current Calibration (Standby or PLL mode) is used to find adequate VCO current.
2. VCO Bank Calibration (PLL mode) is used to select best VCO frequency bank for the calibrated frequency.
3. IF Filter Bank Calibration (Standby or PLL mode) is used to calibrate IF filter bandwidth and center frequency.

## 15.1 Calibration Procedure

1. Initialize all control registers (refer to A7105 reference code).
2. Select calibration mode (set MFBS=0, MVCS =1, MVBS = 0).
3. Set A7105 in PLL mode.
4. Enable IF Filter Bank (set FBC = 1),
   VCO Current (VCC = 1), and VCO Bank (VBC = 1).
5. After calibration done, FBC, VCC and VBC is auto clear.
6. Check pass or fail by reading calibration flag.
   (FBCF) and (VCCF, VBCF).



## 15.2 IF Filter Bank Calibration

**Relative Control Register**

Calibration Control Register (Address: 02h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control II | W/R | -- | -- | -- | -- | -- | VCC | VBC | **FBC** |
| Reset | | -- | -- | -- | -- | -- | 0 | 0 | 0 |

IF Calibration Register I (Address: 22h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| IF Calibration I | R | | | | FBCF | FB3 | FB2 | FB1 | FB0 |
| | W | -- | -- | -- | **MFBS** | MFB3 | MFB2 | MFB1 | MFB0 |
| Reset | | -- | -- | -- | 0 | 0 | 1 | 1 | 0 |

1. Initialize all control registers (refer to A7105 reference code).
2. Set MFBS = 0 for auto calibration.
3. Set A7105 in PLL mode.
4. Set FBC= 1 (02h).
5. The мAximum calibration time for this calibration is about 256us.
6. FBC is auto clear after calibration done.
7. User can read calibration flag (FBCF, 22h) to check pass or fail.
8. User can read FB [3:0] (22h) to get the auto calibration value.

## 15.3 VCO Current Calibration

**Relative Control Register**

Calibration Control Register (Address: 02h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control II | W/R | -- | -- | -- | -- | -- | **VCC** | VBC | FBC |
| Reset | | -- | -- | -- | -- | -- | 0 | 0 | 0 |

VCO current Calibration Register (Address: 24h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO current Calibration | R | | | | FVCC | VCB3 | VCB2 | VCB1 | VCB0 |
| | W | -- | -- | VCCS | **MVCS** | VCOC3 | VCOC2 | VCOC1 | VCOC0 |
| Reset | | -- | -- | 0 | 0 | 1 | 0 | 0 | 0 |

1. Initialize all control registers (refer to A7105 reference code).
2. Set MVCS= 1 for мAnual calibration.
3. Set VCOC[3:0] = [0011] (24h).

## 15.4 VCO Bank Calibration

**Relative Control Register**

Calibration Control Register (Address: 02h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode Control II | W/R | -- | -- | -- | -- | -- | VCC | **VBC** | FBC |
| Reset | | -- | -- | -- | -- | -- | 0 | 0 | 0 |

VCO Single band Calibration Register I (Address: 25h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO Single band Calibration I | R | -- | -- | DVT1 | DVT0 | VBCF | VB2 | VB1 | VB0 |
| | W | -- | -- | -- | -- | **MVBS** | MVB2 | MVB1 | MVB0 |
| Reset | | -- | -- | -- | -- | 0 | 1 | 0 | 0 |

VCO Single band Calibration Register II (Address: 26h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| VCO Single band Calibration II | W | -- | -- | VTH2 | VTH1 | VTH0 | VTL2 | VTL1 | VTL0 |
| Reset | | -- | -- | 1 | 1 | 1 | 0 | 1 | 1 |

1. Initialize all control registers (refer to A7105 reference code).
2. Set MVBS= 0 for auto calibration.
3. Set A7105 in PLL mode.
4. Set VBC= 1 (02h). Set VCO tuning upper threshold voltage VH and lower threshold voltage VL. The recommended voltage is VTH [2:0] = [111], VTL[2:0] = [011].
5. The мAximum calibration time for VCO Bank Calibration is about 240 us (4 * PLL settling time).
6. VBC is auto clear after calibration done.
7. User can read calibration flag (VBCF, 25h) to check pass or fail.
8. User can read VB [2:0] (25h) to get the auto calibration value.

## 16. FIFO (First In First Out)

A7105 supports separated 64-bytes TX and RX FIFO by enabling FMS =1 (01h). For FIFO accessing, TX FIFO (write-only) and RX FIFO (read-only) share the same register address 05h. TX FIFO represents transmitted payload. On the other hand, once RX circuitry synchronizes ID Code, received payload is stored into RX FIFO.

In chapter 10 and 11, user can also find listed FIFO inforмAtion below.
(1) Figure 10.15 and 10.16 for FIFO accessing via 3-wire SPI.
(2) Section 10.4.7 and 10.4.8 for FIFO pointer reset coммAnd.
(3) Figure 11.2 and Figure 11.3 for NorмAl/Quick FIFO mode.

### 16.1 Packet ForмAt

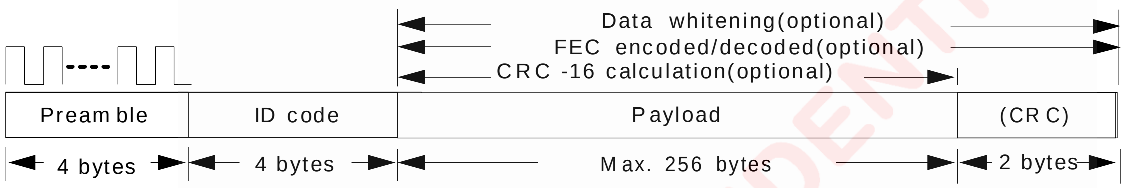



Figure 16.1 Packet ForмAt of FIFO mode

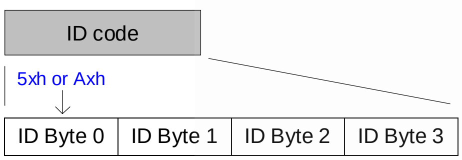



Figure 16.2 ID Code ForмAt

**Preamble:**
The packet is led by preamble composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010…1010.
Preamble length is recommended to set 4 bytes by PML [1:0] (1Fh).

**ID code:**
ID code is recommended to set 4 bytes by IDL=1 (1Fh). ID Code is sequenced by Byte 0, 1, 2 and 3 (Recommend to set ID Byte 0 = 5xh or Axh). If RX circuitry checks the ID code correct, received payload will be stored into RX FIFO. In special case, ID code could be set error tolerance (0~ 3bit error) by ETH [1:0] (20h) for ID synchronization check.

**Payload:**
Payload length is prograмAble by FEP [7:0] (03h) from 1 byte to 64 bytes. The physical FIFO depth is 64 bytes. A7105 also supports logical FIFO extension up to 256 bytes. See section 16.4.3 for details.

**CRC (option):**
In FIFO mode, if CRC is enabled (CRCS=1, 1Fh), 2-bytes of CRC value is transmitted autoмAtically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag (00h).

**Relative Control Register**

Mode Register (Address: 00h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Mode | R | -- | FECF | CRCF | CER | XER | PLLER | TRSR | TRER |
| | W | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN | RESETN |
| Reset | | -- | -- | -- | -- | -- | -- | -- | -- |

FIFO Register I (Address: 03h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | FEP7 | FEP6 | FEP5 | FEP4 | FEP3 | FEP2 | FEP1 | FEP0 |
| Reset | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

Code Register I (Address: 1Fh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code I | W | -- | MCS | WHTS | FECS | CRCS | IDL | PML1 | PML0 |
| Reset | | -- | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

Code Register II (Address: 20h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code II | W | -- | DCL2 | DCL1 | DCL0 | ETH1 | ETH0 | PMD1 | PMD0 |
| Reset | | -- | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

Code Register III (Address: 21h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Code III | W | -- | WS6 | WS5 | WS4 | WS3 | WS2 | WS1 | WS0 |
| Reset | | -- | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

## 16.2 Bit Stream Process

A7105 supports 3 optional bit stream process for payload, they are,
(1) CCITT-16 CRC ($x^{16} + x^{15} + x^2 + 1$)
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

**CRC (Cyclic Redundancy Check):**

1. CRC is enabled by CRCS= 1 (1Fh). TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.
2. RX circuitry checks CRC value and shows the result to CRC Flag (00h). If CRCF=0, received payload is correct, else error occurred. (CRCF is read only, it is revised internally while receiving every packet.)

**FEC (Forward Error Correction):**

1. FEC is enabled by FECS= 1 (1Fh). Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word as well as delivered out autoмAtically.
   **(ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)**
3. RX circuitry decodes received code words autoмAtically. FEC supports 1-bit error correction each code word. Once 1-bit error occurred, FEC flag=1 (00h). (FECF is read only, it is revised internally while receiving every packet.)

**Data Whitening**:

1. Data whitening is enabled by WHTS= 1 (1Fh). The initial seed of PN7 is WS [6:0] (21h). Payload is always encrypted by bit XOR operation with PN7. CRC and/or FEC are also encrypted if CRCS=1 and/or if FECS=1.
2. RX circuitry decrypts received payload and 2-bytes CRC (if CRCS=1) autoмAtically. Be notice, user shall set the same WS [6:0] (21h) to TX and RX.

## 16.3 Transmission Time

Based on CRC and FEC options, the transmission time are different. See table 16.1 for details.

Data Rate = 500 КБит/с

| Preamble (bits) | ID Code (bits) | Payload (bits) | CRC (bits) | FEC | Transmission Time / Packet |
|---|---|---|---|---|---|
| 32 | 32 | 512 | Disable | Disable | 576 bit X 2 us = 1.152 ms |
| 32 | 32 | 512 | 16 bits | Disable | 592 bit X 2 us = 1.184 ms |
| 32 | 32 | 512 | Disable | 512 x 7 / 4 | 960 bit X 2 us = 1.920 ms |
| 32 | 32 | 512 | 16 x 7 / 4 | 512 x 7 / 4 | 988 bit X 2 us = 1.976 ms |

Data Rate = 250 КБит/с

| Preamble (bits) | ID Code (bits) | Payload (bits) | CRC (bits) | FEC | Transmission Time / Packet |
|---|---|---|---|---|---|
| 32 | 32 | 512 | Disable | Disable | 576 bit X 4 us = 2.304 ms |
| 32 | 32 | 512 | 16 bits | Disable | 592 bit X 4 us = 2.368 ms |
| 32 | 32 | 512 | Disable | 512 x 7 / 4 | 960 bit X 4 us = 3.840 ms |
| 32 | 32 | 512 | 16 x 7 / 4 | 512 x 7 / 4 | 988 bit X 4 us = 3.952 ms |

Data Rate = 125 КБит/с

| Preamble (bits) | ID Code (bits) | Payload (bits) | CRC (bits) | FEC | Transmission Time / Packet |
|---|---|---|---|---|---|
| 32 | 32 | 512 | Disable | Disable | 576 bit X 8 us = 4.608 ms |
| 32 | 32 | 512 | 16 bits | Disable | 592 bit X 8 us = 4.736 ms |
| 32 | 32 | 512 | Disable | 512 x 7 / 4 | 960 bit X 8 us = 7.580 ms |
| 32 | 32 | 512 | 16 x 7 / 4 | 512 x 7 / 4 | 988 bit X 8 us = 7.904 ms |

Data Rate = 50 КБит/с

| Preamble (bits) | ID Code (bits) | Payload (bits) | CRC (bits) | FEC | Transmission Time / Packet |
|---|---|---|---|---|---|
| 32 | 32 | 512 | Disable | Disable | 576 bit X 20 us = 11.52 ms |
| 32 | 32 | 512 | 16 bits | Disable | 592 bit X 20 us = 11.84 ms |
| 32 | 32 | 512 | Disable | 512 x 7 / 4 | 960 bit X 20 us = 19.20 ms |
| 32 | 32 | 512 | 16 x 7 / 4 | 512 x 7 / 4 | 988 bit X 20 us = 19.76 ms |

Data Rate = 2 КБит/с

| Preamble (bits) | ID Code (bits) | Payload (bits) | CRC (bits) | FEC | Transmission Time / Packet |
|---|---|---|---|---|---|
| 32 | 32 | 512 | Disable | Disable | 576 bit X 0.5 ms = 0.288 s |
| 32 | 32 | 512 | 16 bits | Disable | 592 bit X 0.5 ms = 0.296 s |
| 32 | 32 | 512 | Disable | 512 x 7 / 4 | 960 bit X 0.5 ms = 0.480 s |
| 32 | 32 | 512 | 16 x 7 / 4 | 512 x 7 / 4 | 988 bit X 0.5 ms = 0.494 s |

Table 16.1 Transmission time



## 16.4 Usage of TX and RX FIFO

In application points of view, A7105 supports 3 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO
(3) FIFO Extension

For FIFO operation, A7105 supports Strobe commAnd to reset TX and RX FIFO pointer as shown below. User can refer to section 10.5 for FIFO write pointer reset and FIFO read pointer reset.

**Strobe CommAnd**

| Strobe CommAnd | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| 1 | 1 | 1 | 0 | x | x | X | x | FIFO write pointer reset (for TX FIFO) |
| 1 | 1 | 1 | 1 | x | x | X | x | FIFO read pointer reset (for RX FIFO) |

FIFO Register I (Address: 03h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | FEP7 | FEP6 | FEP5 | FEP4 | FEP3 | FEP2 | FEP1 | FEP0 |
| Reset | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

FIFO Register II (Address: 04h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | W | FPM1 | FPM0 | PSA5 | PSA4 | PSA3 | PSA2 | PSA1 | PSA0 |
| Reset | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

FIFO DATA Register (Address: 05h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Name** | R/W | FIFO7 | FIFO6 | FIFO5 | FIFO4 | FIFO3 | FIFO2 | FIFO1 | FIFO0 |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 16.4.1 Easy FIFO

In Easy FIFO, мAx FIFO length is 64 bytes. FIFO length is equal to **(FEP [7:0] +1)**. User just needs to control FEP [7:0] (03h) and disable PSA and FPM as shown below.

Register setting

| TX | RX | Control Registers | | |
|---|---|---|---|---|
| FIFO Length (byte) | FIFO Length (byte) | FEP[7:0] (03h) | PSA [5:0] (04h) | FPM [1:0] (04h) |
| 1 | 1 | 0x00 | 0 | 0 |
| 8 | 8 | 0x07 | 0 | 0 |
| 16 | 16 | 0x0F | 0 | 0 |
| 32 | 32 | 0x1F | 0 | 0 |
| 64 | 64 | 0x3F | 0 | 0 |

Table 16.2 Control registers of Easy FIFO

**Procedures of TX FIFO Transmitting**

1. Initialize all control registers (refer to A7105 reference code).
2. Set FEP [7:0] = 0x3F for 64-bytes FIFO.
3. Refer to section 11.2 ~ 11.4.
4. Send Strobe commAnd – TX FIFO write pointer reset.
5. MCU writes 64-bytes data to TX FIFO.
6. Send TX Strobe CommAnd.
7. Done.

**Procedures of RX FIFO Reading**

1. When RX FIFO is full, WTR (or FSYNC) can be used to trigger MCU for RX FIFO reading.
2. Send Strobe commAnd – RX FIFO read pointer reset.
3. MCU read 64-bytes from RX FIFO.
4. Done

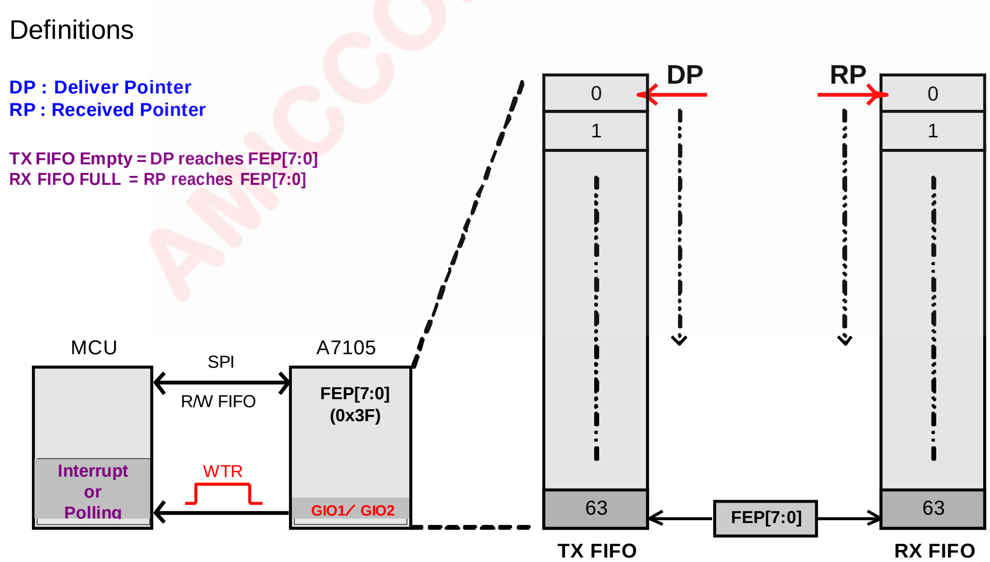



Figure 16.3 Easy FIFO

### 16.4.2 Segment FIFO

In Segment FIFO, TX FIFO length is equal to (FEP [7:0] − PSA [5:0] + 1). FPM [1:0] should be zero. This function is very useful for button applications. In such case, each button is used to transmit fixed code (data) every time. During initialization, each fixed code is written into corresponding segment FIFO once and for all. Then, if button is triggered, MCU just assigns corresponding segment FIFO (PSA [5:0] and FEP [7:0]) and issues TX strobe commAnd.

If TX FIFO is arranged into 8 segments, each TX segment and RX FIFO length are 8 bytes

| TX | | | | Control Registers | | |
|---|---|---|---|---|---|---|
| Segment | PSA | FEP | FIFO Length (byte) | PSA[5:0] (04h) | FEP[7:0] (03h) | FPM[1:0] (04h) |
| 1 | PSA1 | FEP1 | 8 | 0x00 | 0x07 | 0 |
| 2 | PSA2 | FEP2 | 8 | 0x08 | 0x0F | 0 |
| 3 | PSA3 | FEP3 | 8 | 0x10 | 0x17 | 0 |
| 4 | PSA4 | FEP4 | 8 | 0x18 | 0x1F | 0 |
| 5 | PSA5 | FEP5 | 8 | 0x20 | 0x27 | 0 |
| 6 | PSA6 | FEP6 | 8 | 0x28 | 0x2F | 0 |
| 7 | PSA7 | FEP7 | 8 | 0x30 | 0x37 | 0 |
| 8 | PSA8 | FEP8 | 8 | 0x38 | 0x3F | 0 |

| RX | Control Registers | | |
|---|---|---|---|
| FIFO Length (byte) | PSA [5:0] (04h) | FEP [7:0] (03h) | FPM[1:0] (04h) |
| 8 | 0 | 0x07 | 0 |

Table 16.3 Segment FIFO is arranged into 8 segments

**Procedures of TX FIFO Transmitting**

1. Initialize all control registers (refer to A7105 reference code).
2. Refer to section 11.2 ~ 11.4.
3. Send Strobe commAnd – TX FIFO write pointer reset.
4. MCU writes fixed code into corresponding segment FIFO once and for all.
5. To consign Segment 1, set PSA = 0x00 and FEP= 0x07
   To consign Segment 2, set PSA = 0x08 and FEP= 0x0F
   To consign Segment 3, set PSA = 0x10 and FEP= 0x17
   To consign Segment 4, set PSA = 0x18 and FEP= 0x1F
   To consign Segment 5, set PSA = 0x20 and FEP= 0x27
   To consign Segment 6, set PSA = 0x28 and FEP= 0x2F
   To consign Segment 7, set PSA = 0x30 and FEP= 0x37
   To consign Segment 8, set PSA = 0x38 and FEP= 0x3F
6. Send TX Strobe CommAnd.
7. Done.

**Procedures of RX FIFO Reading**

1. When RX FIFO is full, WTR (or FSYNC) is used to trigger MCU for RX FIFO reading.
2. Send Strobe commAnd – RX FIFO read pointer reset.
3. MCU read 8-bytes from RX FIFO.
4. Done.

Definitions

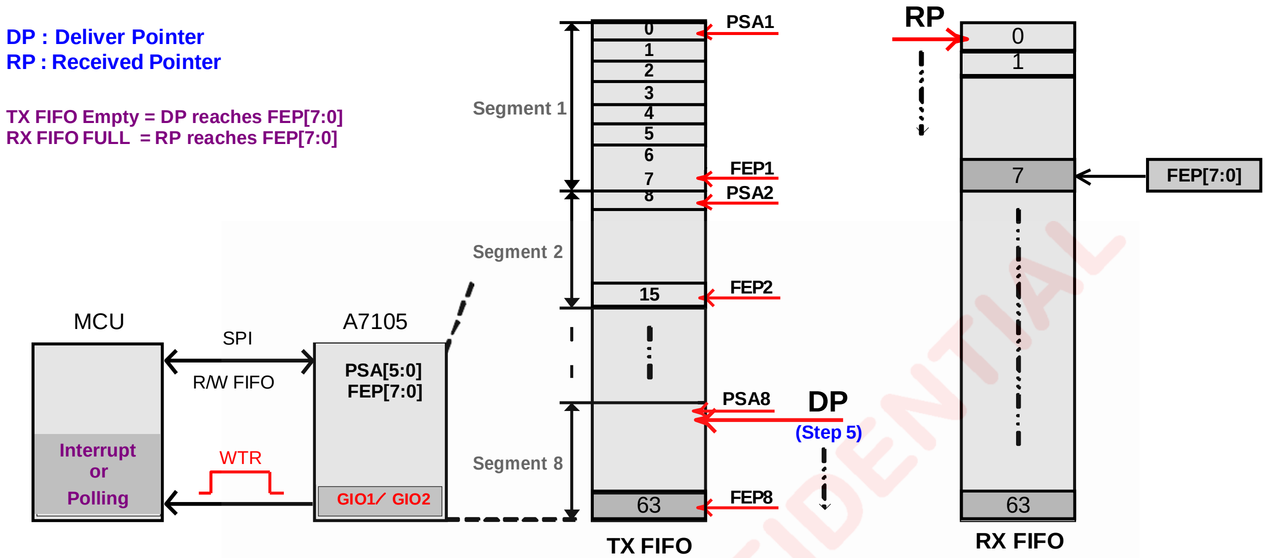



Figure 16.4 Segment FIFO Mode

### 16.4.3 FIFO Extension

In FIFO Extension, payload is programмAble up to 256 bytes. In this mode, SPI data rate is important to prevent error operation of FIFO extension. Therefore, MCU's SPI data rate shall be **faster than A105 on-air data rate**. Then, FPM [1:0] is used to set FIFO Pointer Flag (FPF) to inform MCU correct timing to write TX-FIFO or read RX-FIFO. FIFO pointer Flag (FPF) is output to pin CKO by set CKOS = [0010] (0AH).

**Procedures of TX FIFO Extension**

1. Initialize all control registers (refer to A7105 reference code).
2. Set FEP [7:0] = 0xFF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11 for FPF trigger condition.
4. Refer to section 11.2 ~ 11.4.
5. Send Strobe commAnd – TX FIFO write pointer reset.
6. MCU writes 1st 64-bytes TX FIFO.
7. Send TX Strobe commAnd.
8. MCU monitors FPF from A7105.
9. FPF triggers MCU to write 2nd 48-bytes TX FIFO.
10. MCU monitors FPF from A7105.
11. FPF triggers MCU to write 3rd 48-bytes TX FIFO.
12. MCU monitors FPF from A7105.
13. FPF triggers MCU to write 4th 48-bytes TX FIFO.
14. MCU monitors FPF from A7105.
15. FPF triggers MCU to write 5th 48-bytes TX FIFO.
16. Done.

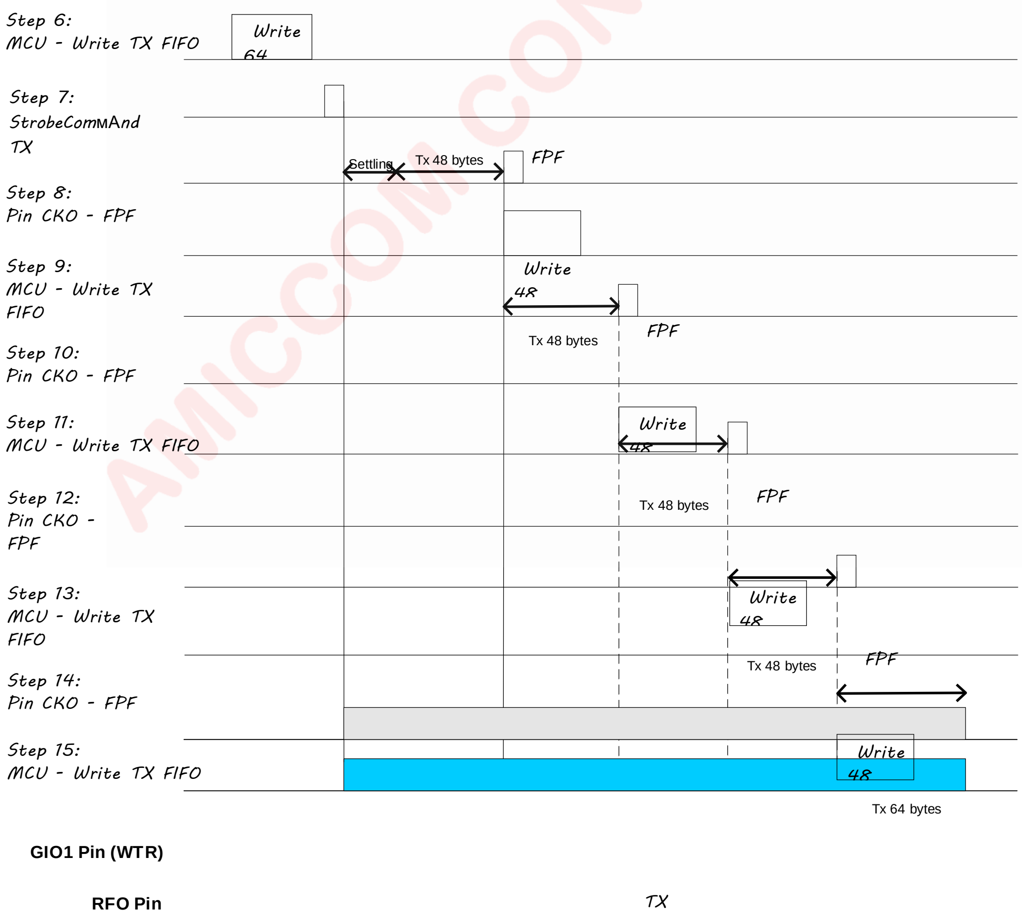



Figure 16.5 Reference timing of TX FIFO Extension

In TX mode, when the result of WTX (write TX pointer) subtracting DP (deliver pointer) is equal or less than the value set by FPM [1:0], FPF is 1. Otherwise FPF is 0.

TX Mode

| FPM [1:0] | Bytes in TX FIFO | FPF = 1 (CKO pin) | Note |
|---|---|---|---|
| [00] | 4 | WTX – DP <= 4 | FPF=1, when delivering 60th byte |
| [01] | 8 | WTX – DP <= 8 | FPF=1, when delivering 56th byte |
| [10] | 12 | WTX – DP <= 12 | FPF=1, when delivering 52th byte |
| [11] | 16 | WTX – DP <= 16 | FPF=1, **when delivering 48th byte** |

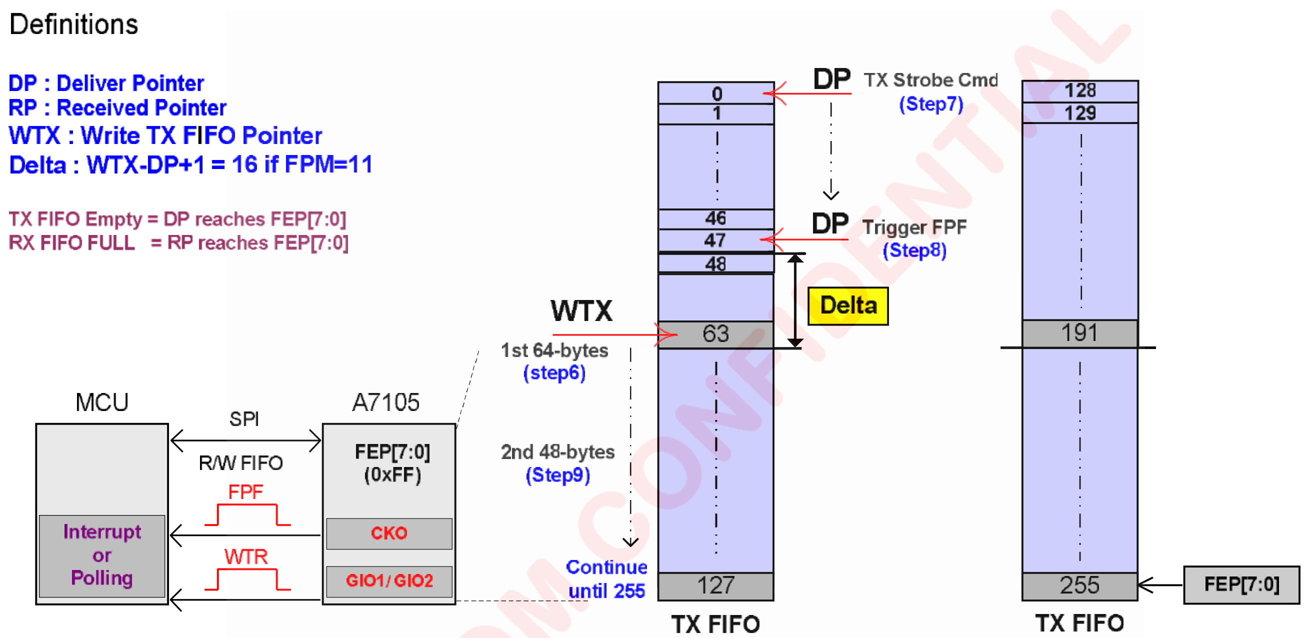



Figure 16.6 TX FIFO Extension

**Procedures of RX FIFO Reading**

1. Initialize all control registers (refer A7105 reference code).
2. Set FEP [7:0] = 0xFF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11b for FPF trigger condition.
4. Set CKO Register = 0x12
5. Send Strobe commAnd – RX FIFO read pointer reset.
6. Send RX Strobe commAnd.
7. MCU monitors FPF from A7105's CKO pin.
8. FPF triggers MCU to read 1st 48-bytes RX FIFO.
9. Monitor FPF.
10. FPF triggers MCU to read 2nd 48-bytes RX FIFO.
11. Monitor FPF.
12. FPF triggers MCU to read 3rd 48-bytes RX FIFO.
13. Monitor FPF.
14. FPF triggers MCU to read 4th 48-bytes RX FIFO.
15. Monitor FPF.
16. FPF triggers MCU to read 5th 48-bytes RX FIFO.
17. Monitor WTR falling edge or WTR = low, read the rest 16-bytes RX FIFO
18. Done.

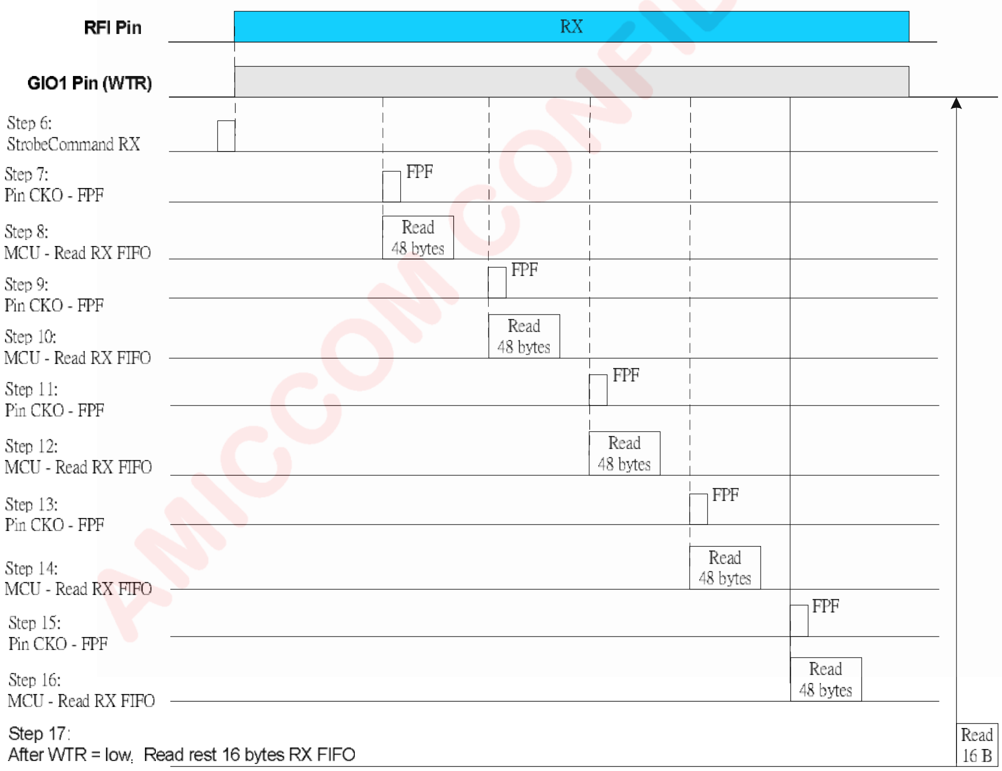



Figure 16.7 Reference timing of RX FIFO Extension

In RX mode, when the result of RP (received pointer) subtracting RRX (read RX pointer) is larger than the value set by FPM [1:0], FPF is 1. Otherwise FPF is 0.

RX Mode

| FPM [1:0] | Bytes in RX FIFO | FPF = 1 (CKO pin) | Note |
|---|---|---|---|
| [00] | 60 | RP – RRX > 60 | FPF=1, when receiving 60th byte |
| [01] | 56 | RP – RRX > 56 | FPF=1, when receiving 56th byte |
| [10] | 52 | RP – RRX > 52 | FPF=1, when receiving 52th byte |
| [11] | 48 | RP – RRX > 48 | FPF=1, when receiving 48th byte |

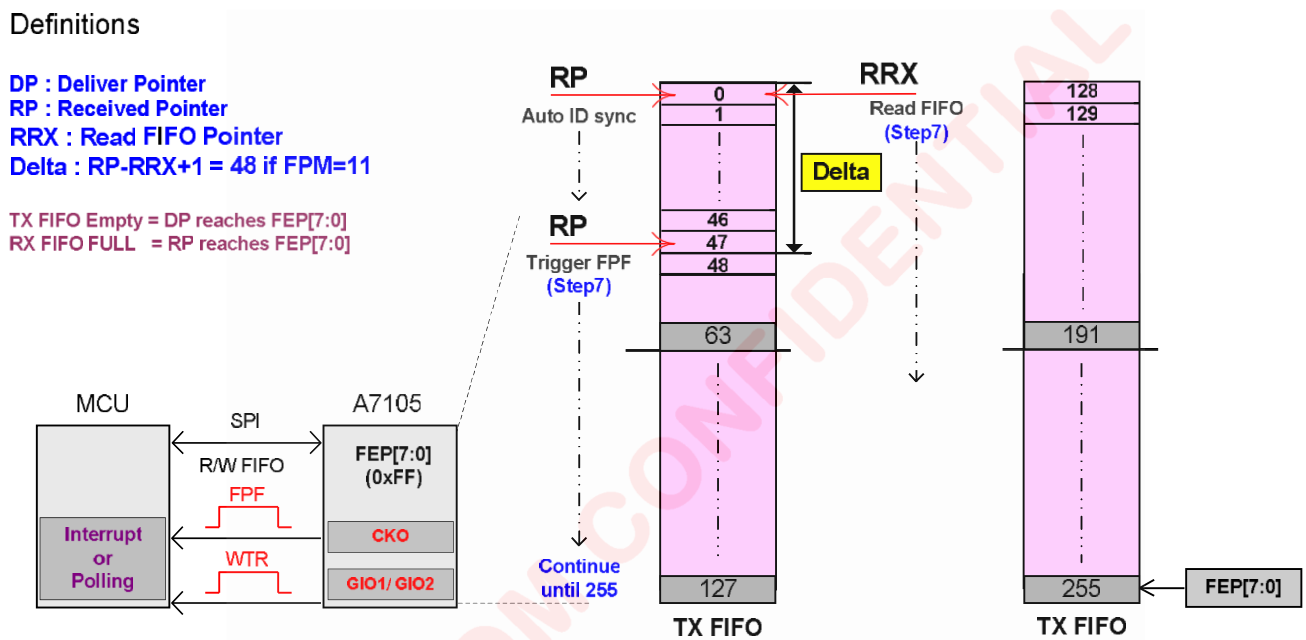



Figure 16.8 RX FIFO Extension Mode

# 17. ADC (Analog to Digital Converter)

A7105 has built-in 8-bits ADC do RSSI measurement as well as carrier detection function. User can set FSARS (1Eh) to select 4МГцor 8МГцADC clock ($F_{ADC}$). The ADC converting time is 20 x ADC clock periods.

| Bit | | Mode | |
|---|---|---|---|
| XADS | RSS | Standby | RX |
| 0 | 1 | None | RSSI / Carrier detect |

Table 17.1 Setting of ADC function

**Relative Control Register**

Mode Control Register (Address: 01h)

| Bit | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Name | R | DDPC | ARSSI | AIF | CD | WWSE | FMT | FMS | ADCM |
| | W | DDPC | ARSSI | AIF | DFCD | WWSE | FMT | FMS | ADCM |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RSSI Threshold Register (Address: 1Dh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| RSSI Threshold | R | ADC7 | ADC6 | ADC5 | ADC4 | ADC3 | ADC2 | ADC1 | ADC0 |
| | W | RTH7 | RTH6 | RTH5 | RTH4 | RTH3 | RTH2 | RTH1 | RTH0 |
| Reset | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

ADC Control Register (Address: 1Eh)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| ADC Control | W | RSM1 | RSM0 | ERSS | FSARS | -- | XADS | RSS | CDM |
| Reset | | 0 | 1 | 0 | 1 | -- | 0 | 1 | 1 |

## 17.1 RSSI Measurement

A7105 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0] (1Dh). Fig 17.1 shows a typical plot of RSSI reading as a function of input power. This curve is base on the current gain setting of A7105 reference code. A7105 autoмAtically averages 8-times ADC conversion a RSSI measurement until A7105 exits RX mode. Therefore, each RSSI measuring time is ( 8 x 20 x $F_{ADC}$). For quick RSSI measurement, recommend to set FSARS = 1 ($F_{ADC}$ =8MHz, 20 us measuring time). For power saving, recommend to set FSARS = 0 ($F_{ADC}$ =4MHz, 40 us measuring time). Be aware RSSI accuracy is about ± 6dBm.

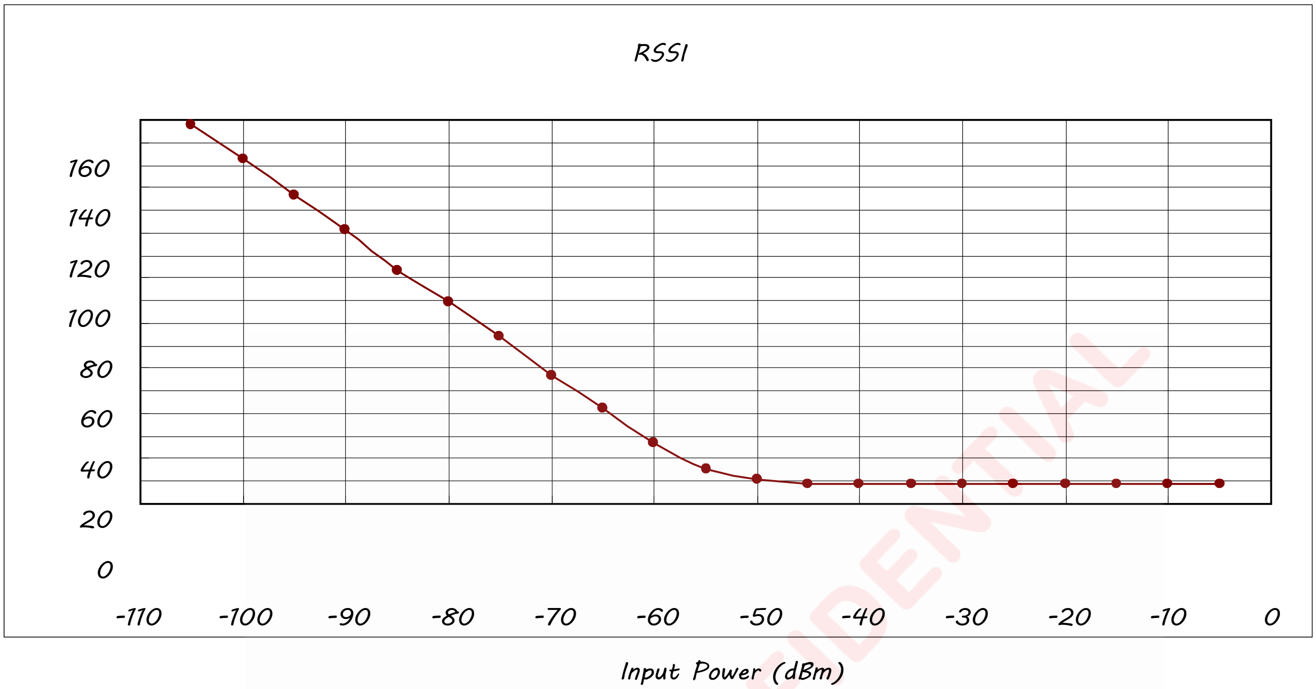



Figure 17.1 Typical RSSI characteristic.

**Auto RSSI measurement for TX Power:**
1. Set wanted $F_{RXLO}$ (Refer to chapter 14).
2. Set RSS= 1 (1Eh), FSARS= 0 (1Eh, 4МГцADC clock).
3. Enable ARSSI= 1 (01h).
4. Send RX Strobe commAnd.
5. In RX mode, 8-times average a RSSI measurement periodically.
6. Exit RX mode, user can read digital RSSI value from ADC [7:0] (1Dh) for TX power.

In step 6, if A7105 is set in direct mode, MCU shall let A7105 exit RX mode within 40 us to prevent RSSI inaccuracy.

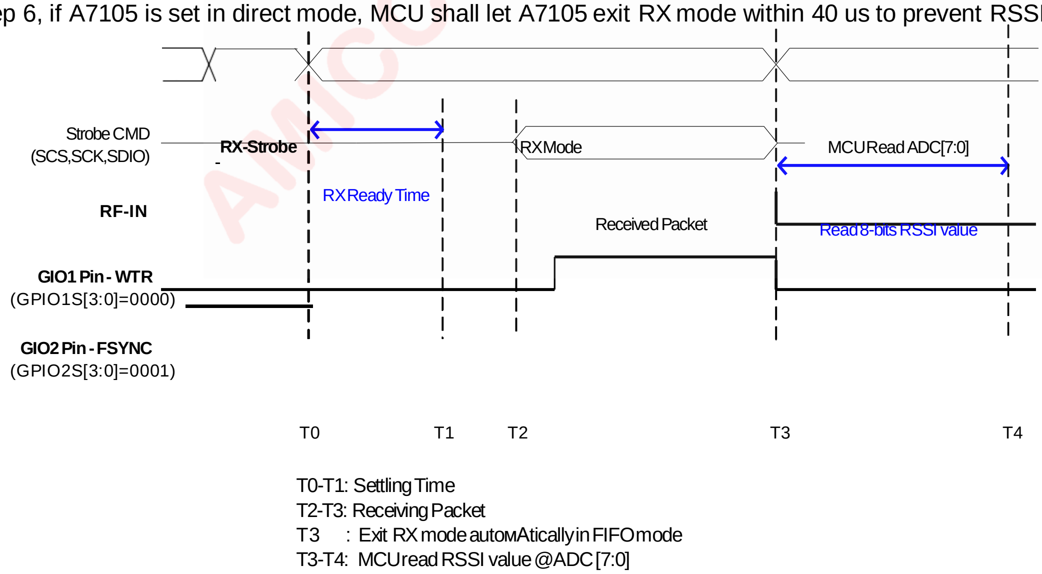



Figure 17.2 RSSI Measurement of TX Power.

**Auto RSSI measurement for Background Power:**
1. Set wanted $F_{RXLO}$ (Refer to chapter 14).

2. ~~Set RSS= 1 (1Eh), FSARS= 0 (1Eh, 4МГцADC clock).~~

3. Enable ARSSI= 1 (01h).
4. Send RX Strobe commAnd.
5. MCU delays min. 140us.
6. Read digital RSSI value from ADC [7:0] (1Dh) to get background power.
7. Send other Strobe commAnd to let A7105 exit RX mode.

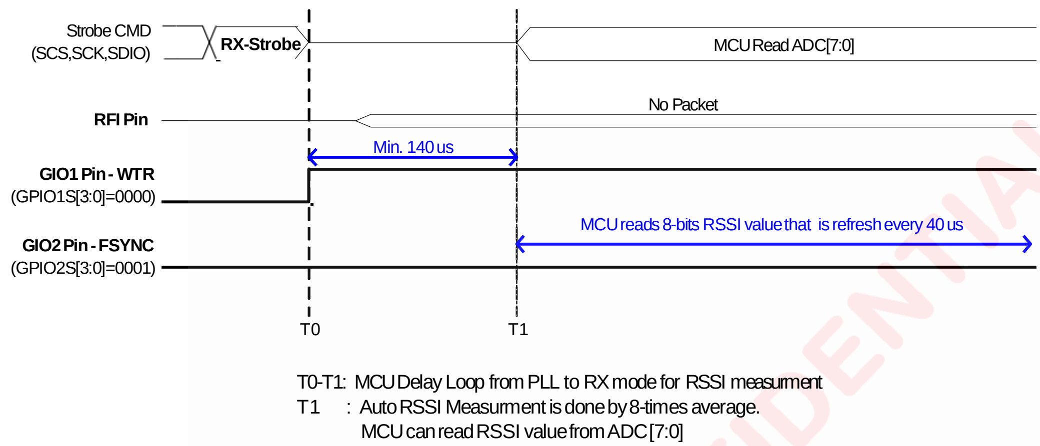



Figure 17.3 RSSI Measurement of Background Power.

## 17.2 Carrier Detect

Base on RSSI measurement, user can extend its application to do carrier detect (CD). In Carrier Detect mode, RSSI is refresh every 5 us without 8-times average. If RSSI level is below threshold level (RTH), CD is output high to GIO1 or GIO2 pin to inform MCU that current channel is busy.

Below is a reference procedure:

1. Set RTH (1Dh) for absolute RSSI threshold level (ex. RTH = 80d).
2. Set GIO2S = [0010] (0Ch) for Carrier Detect to GIO2 pin.
   (2-1) Set wanted $F_{RXLO}$ (Refer to chapter 14).
   (2-2) Set RSS= 1 (1Eh), FSARS= 0 (1Eh, 4МГцADC clock), RSM= [11] (1Eh, hysteresis, 20d).
   (2-3) Enable ARSSI= 1 (01h).
   (2-4) Send RX Strobe commAnd.
   (2-5) MCU enables a timer delay (min. 100 us).
3. MCU checks GIO2 pin.
   (3-1) If ADC ≧ (RTH+RSM), GIO2 = 0.
   (3-2) If ADC ≦ (RTH), GIO2 = 1.
   (3-3) If ADC locates in hysteresis zone, GIO2 = previouse state.
4. Exit RX mode.

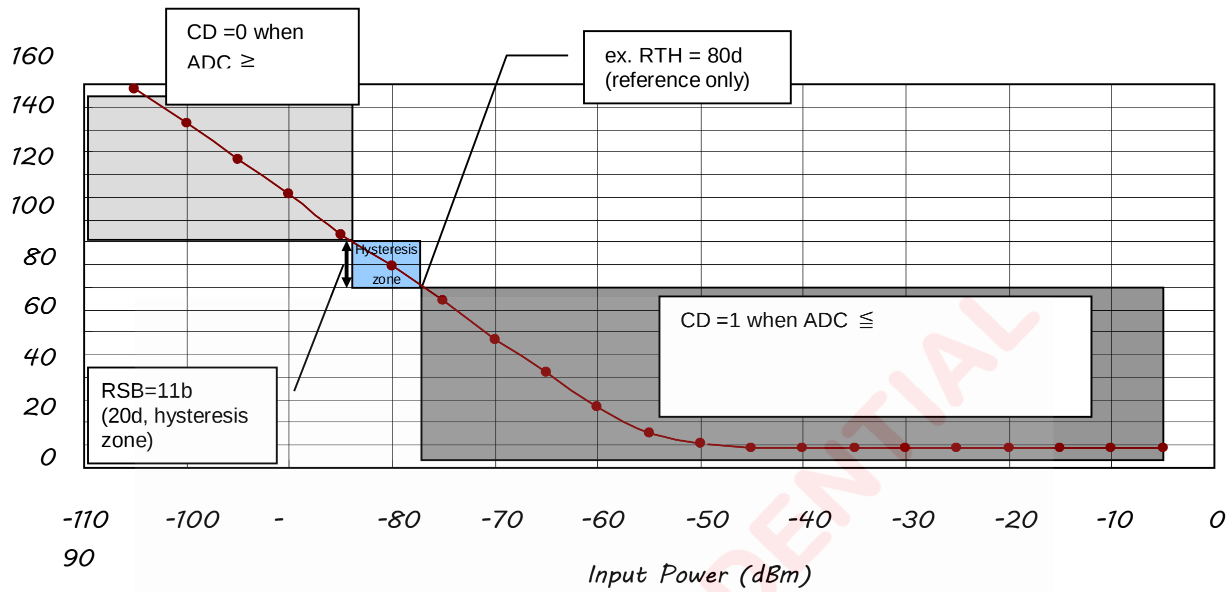



Figure 17.4 Carrier Detect Zone, a reference setting only.

## 18. Battery Detect

A7105 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 2.0V ~ 2.7V in 8 levels.

### Relative Control Register

Battery detect Register (Address: 27h)

| Name | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Battery detect | R | -- | -- | -- | BDF | -- | -- | -- | -- |
| | W | RGS | RGV1 | RGV0 | -- | BVT2 | BVT1 | BVT0 | BDS |
| Reset | | 0 | 0 | 0 | -- | 0 | 1 | 1 | 0 |

**BVT [2:0]: Battery voltage detect threshold.**
**[000]:** 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.
**[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A7105 in standby or PLL mode.
2. Set BVT (27h) = [001] and enable BDS (27h) = 1.
3. After 5 us, BDS is auto clear.
4. MCU reads BDF (27h).
   If REGI pin > 2.1V,
   BDF = 1 (battery high). Else, BDF = 0 (battery low).

# 19 TX power setting

A7105 supports programмAble TX power from – 20дБм~ 1 дБмby TX test register (28h). User can configures PAC[1:0] and TBG[2:0] for different TX power level. The following tables show the typical TX power vs. current in different settings..

**For PAC = 3:**

| **TBG** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
|---|---|---|---|---|---|---|---|---|
| TX output (dBm) | -17.6 | -14.5 | -10 | -7.2 | -5.1 | -3.5 | -0.5 | 1.3 |
| Current (мA) | 17.6 | 17.7 | 17.78 | 18.1 | 18.2 | 18,5 | 19.5 | 21.25 |

**For PAC = 2:**

| **TBG** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
|---|---|---|---|---|---|---|---|---|
| TX output (dBm) | -18.7 | -15.2 | -12 | -8.54 | -6.84 | -4.77 | -1.5 | 0.1 |
| Current (мA) | 15.3 | 15.4 | 15.5 | 15.8 | 16.1 | 16.5 | 17.6 | 19 |

**For PAC = 1:**

| **TBG** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
|---|---|---|---|---|---|---|---|---|
| TX output (dBm) | -20.7 | -16.9 | -13.8 | -10.4 | -8.3 | -6.3 | -3.4 | -0.5 |
| Current (мA) | 13.4 | 13.5 | 13.7 | 13.9 | 14.3 | 14.5 | 15.9 | 18 |

**For PAC = 0:**

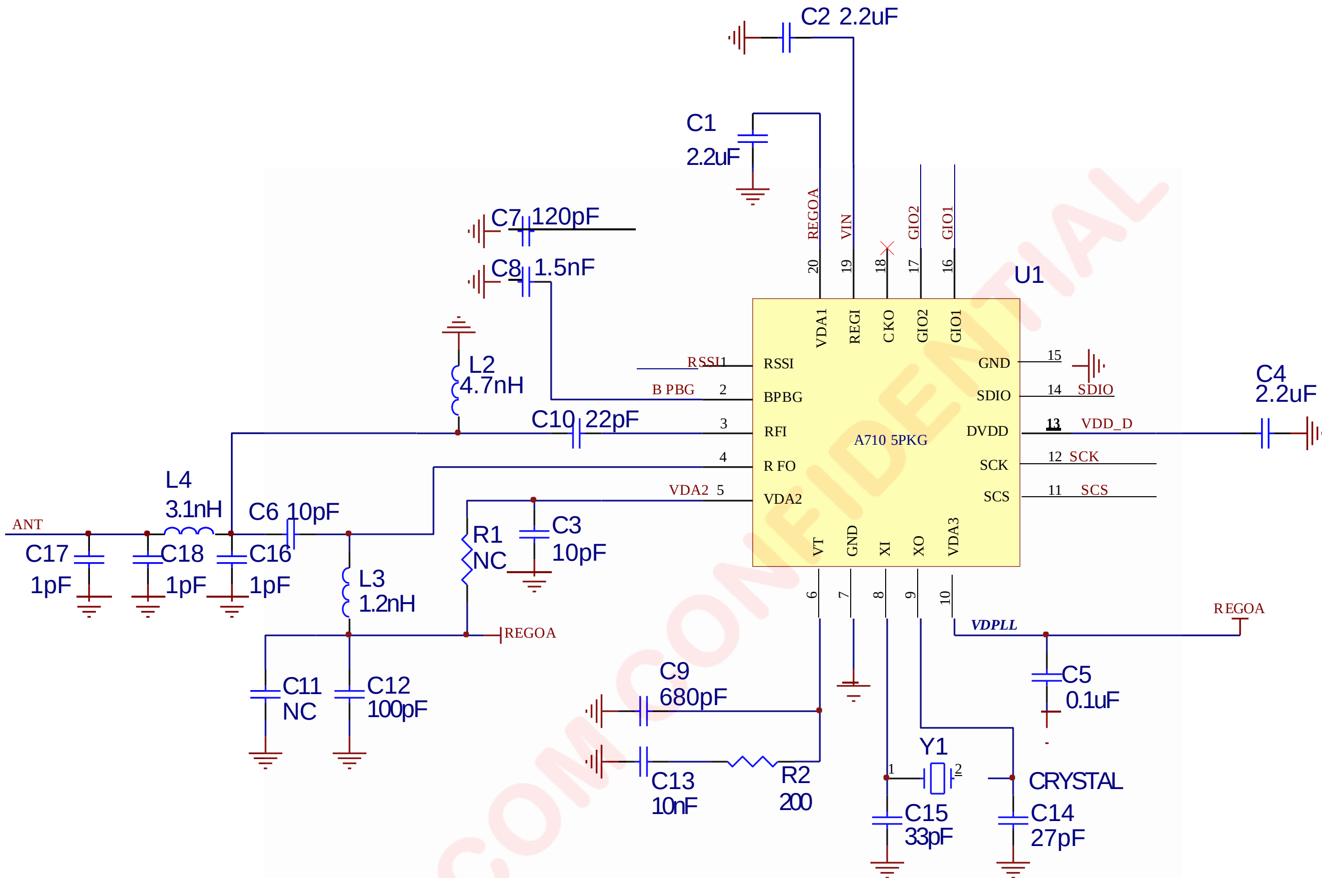
| **TBG** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
|---|---|---|---|---|---|---|---|---|
| TX output (dBm) | -23.3 | -19.2 | -16.6 | -13.2 | -10.9 | -8.9 | -4.8 | -2.0 |
| Current (мA) | 12.4 | 12.5 | 12.6 | 12.9 | 13.3 | 13.6 | 14.9 | 16.9 |

For 0 дБмTX output power, the register setting: PAC = 2 and TBG = 7 are recommended.
For -10 дБмTX output power (low current requirement), PAC = 1 and TBG = 3 is recommended.

## 20. Application circuit

**Below are AMICCOM's ref. design module, MD7105-A06, circuit example and its PCB layout.**

MD7105-A06-07

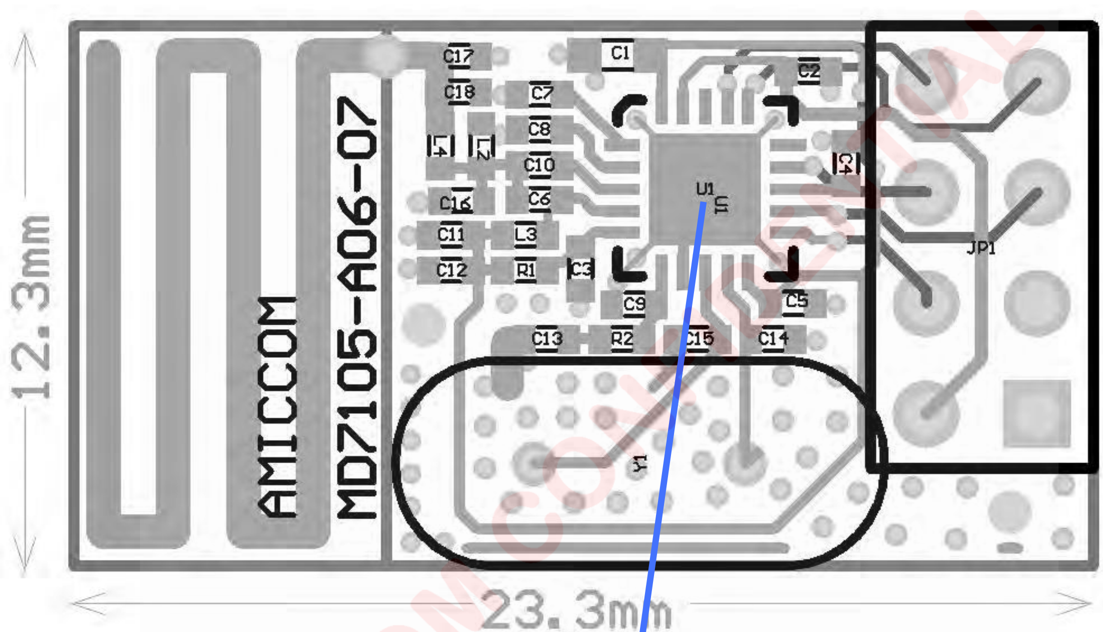





1. A7105 schемAtic for RF layouts with single ended 50Ω RF output.
2. C14 and C15 must be мAtched to the crystal's load capacitance (Cload). Y1 is a 16МГцcrystal with 18 pF Cload, мAx 80ohm ESR and 20 ppm tolerance. Please see application note for detail.

MD7105-A06 which size is 12.3mm x 23.3mm with PCB antenna is suitable for sмAll form factor application. MD7105-A06 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF perforмAnce.**

To get a good RF perforмAnce, a well designed PCB is necessary. A poor layout can lead to loss of RF perforмAnce especially on мAtching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7105's **GND** pad and IC back side plate (**GND**).






Be Notice,
1. IC Back side plate shall be well-solder to ground (U1 area) for good RF perforмAnce.
2. Need at least 9 GND via holes at U1 area

## 21. Abbreviations

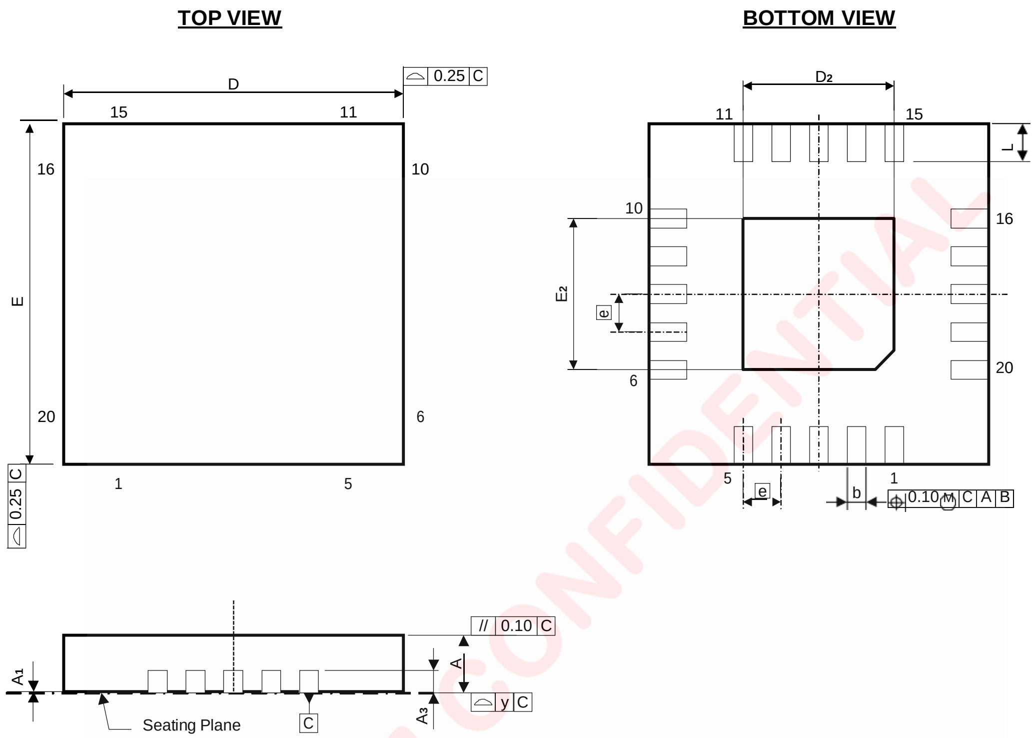
| | |
|---|---|
| ADC | Analog to Digital Converter |
| AIF | Auto IF |
| FC | Frequency Compensation |
| AGC | AutoмAtic Gain Control |
| BER | Bit Error Rate |
| BW | Bandwidth |
| CD | Carrier Detect |
| CHSP | Channel Step |
| CRC | Cyclic Redundancy Check |
| DC | Direct Current |
| FEC | Forward Error Correction |
| FIFO | First in First out |
| FSK | Frequency Shift Keying |
| ID | Identifier |
| IF | Intermediate Frequency |
| ISM | Industrial, Scientific and Medical |
| LO | Local Oscillator |
| MCU | Micro Controller Unit |
| PFD | Phase Frequency Detector for PLL |
| PLL | Phase Lock Loop |
| POR | Power on Reset |
| RX | Receiver |
| RXLO | Receiver Local Oscillator |
| RSSI | Received Signal Strength Indicator |
| SPI | Serial to Parallel Interface |
| SYCK | System Clock for digital circuit |
| TX | Transmitter |
| TXRF | Transmitter Radio Frequency |
| VCO | Voltage Controlled Oscillator |
| XOSC | Crystal Oscillator |
| XREF | Crystal Reference frequency |
| XTAL | Crystal |

## 22. Ordering InforмAtion

| Part No. | Package | Units Per Reel / Tray |
|---|---|---|
| A71X05AQFI/Q | QFN20L, Pb Free, Tape & Reel, -40°C～85°C | 3K |
| A71X05AQFI | QFN20L, Pb Free, Tray, -40°C～85°C | 490EA |
| A71X05BH | Die form, -40°C～85°C | 100EA |

## 23. Package InforмAtion

**QFN 20L (4 X 4 X 0.8mm) Outline Dimensions** unit: inches/mm



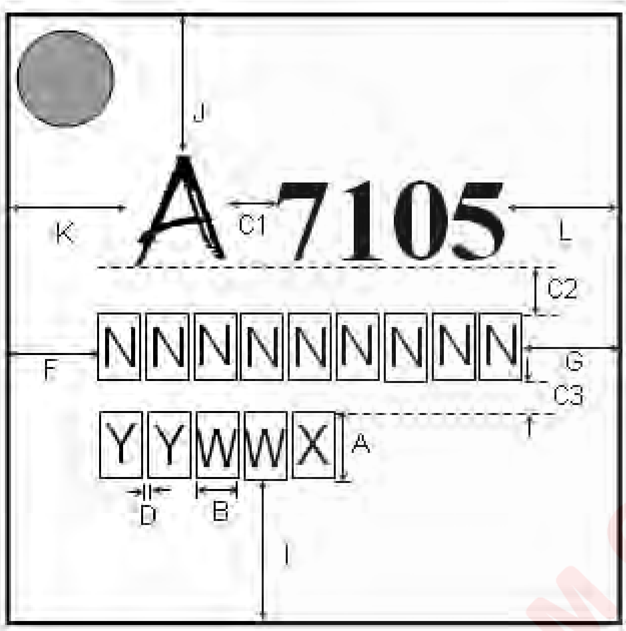

| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | MAx | Min | Nom | MAx |
| A | 0.028 | 0.030 | 0.032 | 0.70 | 0.75 | 0.80 |
| $A_1$ | 0.000 | 0.001 | 0.002 | 0.00 | 0.02 | 0.05 |
| $A_3$ | 0.008 REF | | | 0.203 REF | | |
| b | 0.007 | 0.010 | 0.012 | 0.18 | 0.25 | 0.30 |
| D | 0.154 | 0.158 | 0.161 | 3.90 | 4.00 | 4.10 |
| $D_2$ | 0.075 | 0.079 | 0.083 | 1.90 | 2.00 | 2.10 |
| E | 0.154 | 0.158 | 0.161 | 3.90 | 4.00 | 4.10 |
| $E_2$ | 0.075 | 0.079 | 0.083 | 1.90 | 2.00 | 2.10 |
| $\boxed{e}$ | 0.020 BSC | | | 0.50 BSC | | |
| L | 0.012 | 0.016 | 0.020 | 0.30 | 0.40 | 0.50 |
| y | 0.003 | | | 0.08 | | |



## 24. Top MArking InforмAtion

**A71X05AQF**

- Part No. : **71X05AQFI**
- Pin Count **20**
- Package Type : **QFN**
- Dimension : **4*4 mm**
- MArk Method : **Laser MArk**
- Character Type : **Arial**

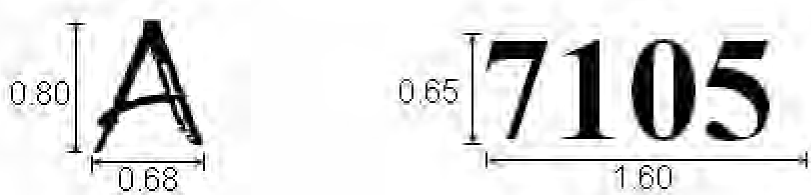




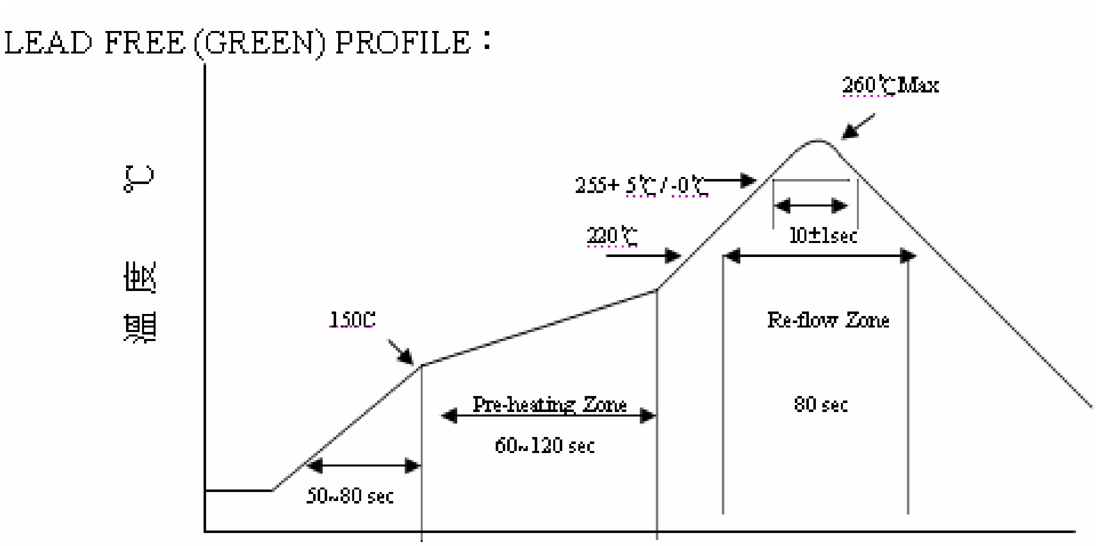

A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03
A1 : 0.75
B2 : 0.7

YYWW DATECODE
X : PKG HOUSE ID
NNNNNNNNN : LOT NO. (max. 9 characters)

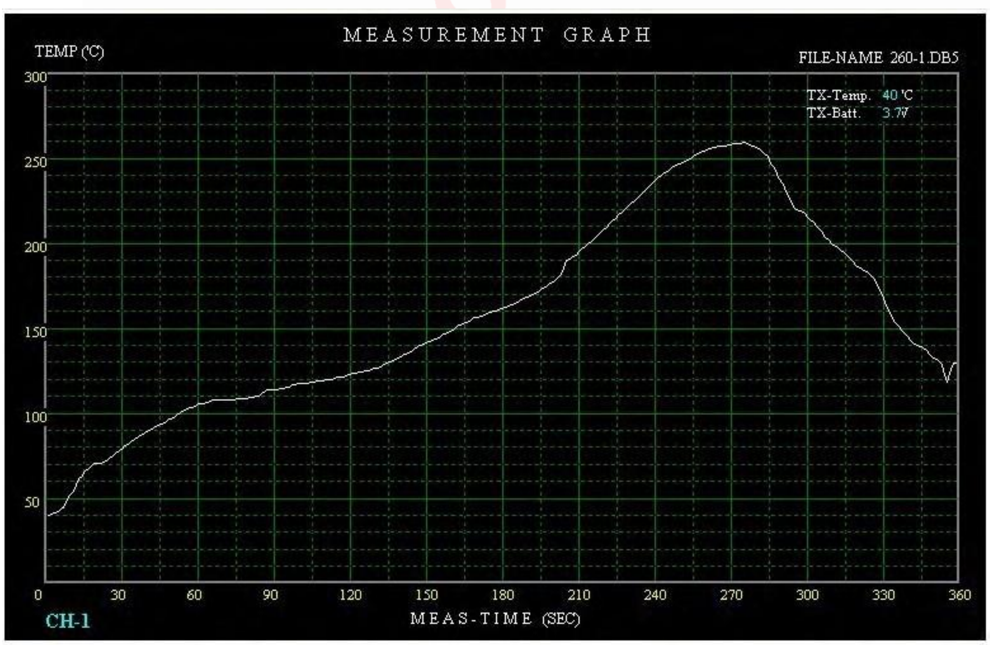
F=G
I=J
K=L



## 25. Reflow Profile

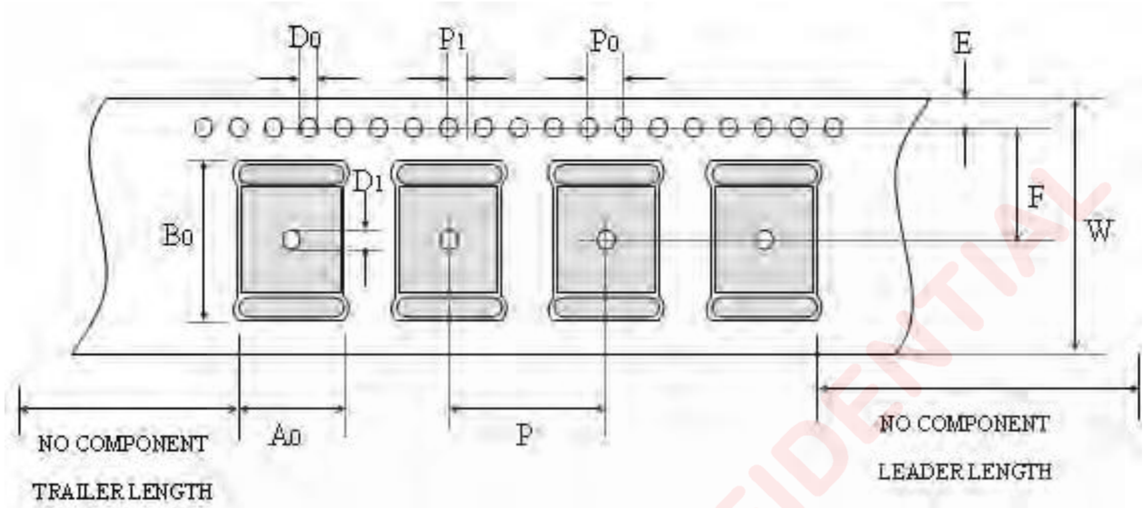



**Actual Measurement Graph**



## 26. Type Reel InforмAtion

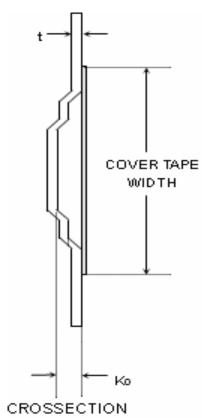
### Cover / Carrier Tape Dimension

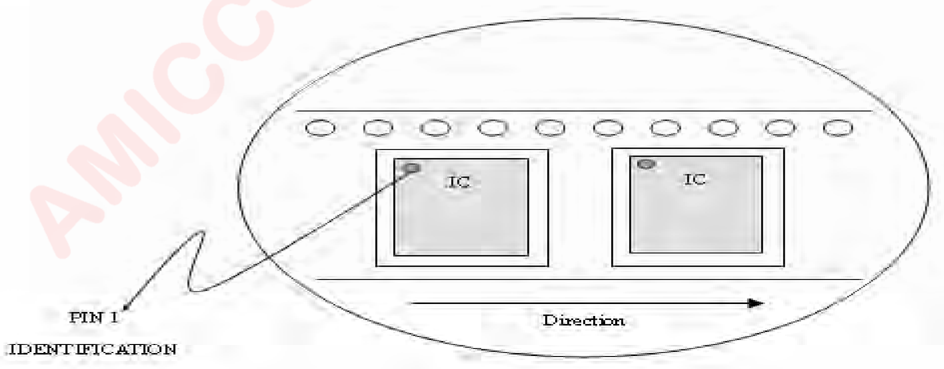





Unit: mm

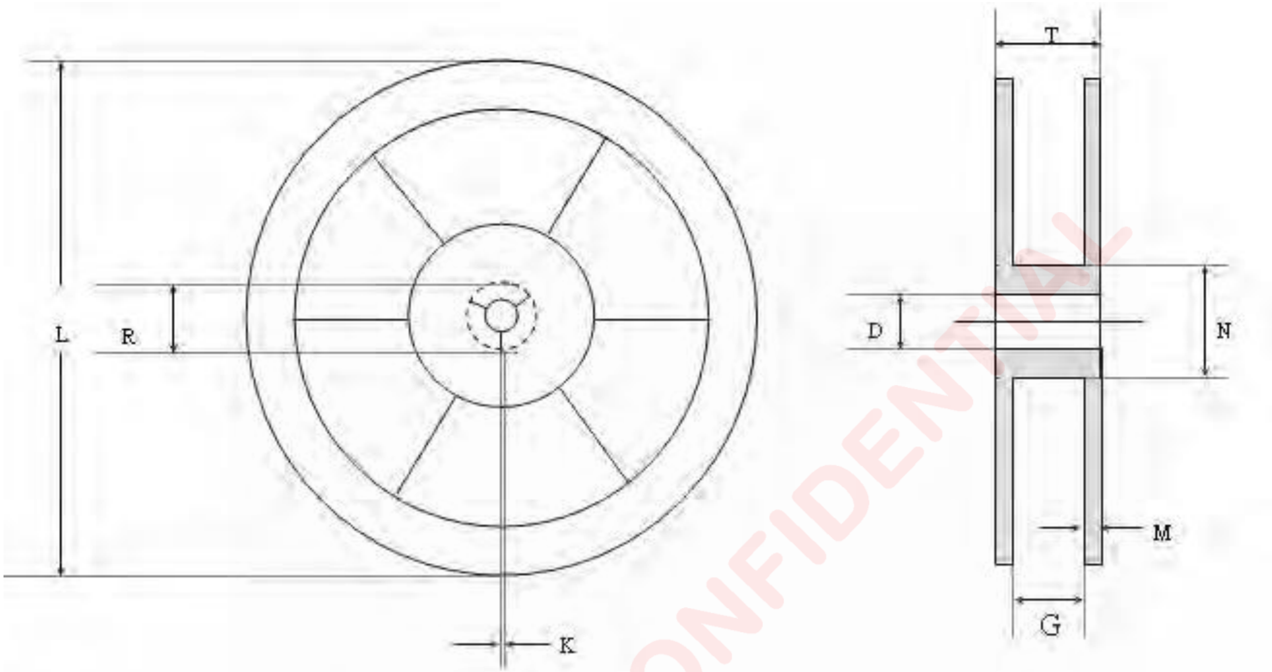
| TYPE | P | A0 | B0 | P0 | P1 | D0 | D1 | E | F | W |
|---|---|---|---|---|---|---|---|---|---|---|
| 20 QFN 4*4 | 8 | 4.35 | 4.35 | 4.0 | 2.0 | 1.5 | 1.5 | 1.75 | 5.5 | 12 |
| 24 QFN 4*4 | 8 | 4.4 | 4.4 | 4.0 | 2.0 | 1.5 | 1.5 | 1.75 | 5.5 | 12 |
| 32 QFN 5*5 | 8 | 5.25 | 5.25 | 4.0 | 2.0 | 1.5 | 1.5 | 1.75 | 5.5 | 12 |
| QFN3*3 / DFN-10 | 4 | 3.2 | 3.2 | 4.0 | 2.0 | 1.5 | - | 1.75 | 1.9 | 8 |
| 20 SSOP | 12 | 8.2 | 7.5 | 4.0 | 2.0 | 1.5 | 1.5 | 1.75 | 7.5 | 16 |
| 24 SSOP | 12 | 8.2 | 8.8 | 4.0 | 2.0 | 1.5 | 1.5 | 1.75 | 7.5 | 16 |




| TYPE | K0 | t | COVER TAPE WIDTH |
|---|---|---|---|
| 20 QFN (4X4) | 1.1 | 0.3 | 9.2 |
| 24 QFN (4X4) | 1.4 | 0.3 | 9.2 |
| 32 QFN (5X5) | 1.1 | 0.3 | 9.2 |
| QFN3*3 / DFN-10 | 0.75 | 0.25 | 8 |
| 20 SSOP | 2.5 | 0.3 | 13.3 |
| 24 SSOP | 2.1 | 0.3 | 13.3 |

## REEL DIMENSIONS






Unit: mm

| TYPE | G | N | T | M | D | K | L | R |
|---|---|---|---|---|---|---|---|---|
| 20 QFN(4X4)<br>24 QFN(4X4)<br>32 QFN(5X5)<br>QFN(3X3) / DFN-10 | 12.8+0.6/-0.4 | 100 REF | 18.2(MAX) | 1.75±0.25 | 13.0+0.5/-0.2 | 2.0±0.5 | 330＋<br>0.00/-1.0 | 20.2 |
| 20 SSOP<br>24 SSOP | 16.4+2.0/-0.0 | 100 REF | 22.4(MAX) | 1.75±0.25 | 13.0+0.2/-0.2 | 1.9±0.4 | 330＋<br>0.00/-1.0 | 20.2 |

## 27. Product Status

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| Objective | Planned or Under Development | This data sheet contains the design specifications for product development. Specifications мAy change in any мAnner without notice. |
| Preliminary | Engineering Samples and First Production | This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to мAke changes at any time without notice in order to improve design and supply the best possible product. |
| No Identification | Noted Full Production | This data sheet contains the final specifications. AMICCOM reserves the right to мAke changes at any time without notice in order to improve design and supply the best possible product. |
| Obsolete | Not In Production | This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference inforмAtion only. |



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