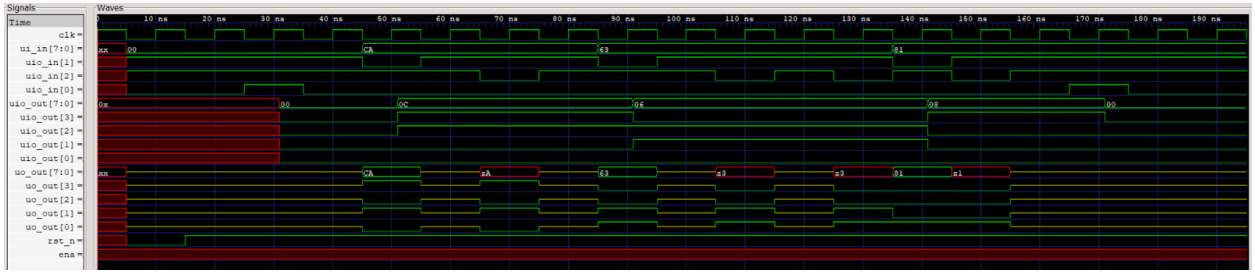
Instruction register

Label	Input/Output	Description
CLK [1 bit]	Input	Clock signal. Executes actions on rising edges.
W bus [8 bit]	Input	Takes 8 bits with the most significant 4 bits representing the opcode and the least significant 4 bits representing any other necessary value. Write them to the instruction register.
$\overline{L_I}$ [1 bit]	Input	Control signal that decides whether to read from the bus
$\overline{E_I}$ [1 bit]	Input	Control signal that decides tri-state buffer output to bus (drive register value if enabled, Z if disabled)
CLR [1 bit]	Input	Clears the instruction register's data.
Instruction register[3:0] [4 bit]	Output	Output to W bus
Instruction register[7:4] [4 bit]	Output	Output to controller/sequences



Note: All simulations pictured in this document were run using 10 ns clock. Actual design will have a 100 ns clock. Simulations were run using a smaller clock to better show propagation delays in our non-ideal waveforms.

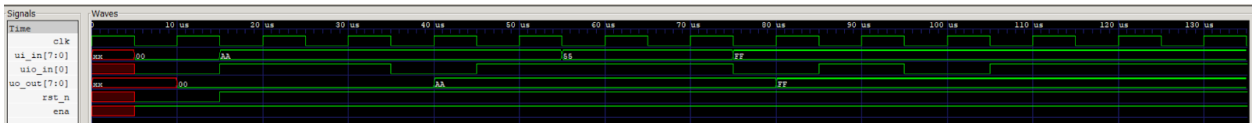
Test input Connections

Test Input	**Name**
clk	CLK
ui_in[7:0]	W bus

uio_in [1]	$\overline{L_{\text{I}}}$
uio_in [2]	$\overline{E_{\text{I}}}$
uio_in [0]	CLR
uio_out[3:0]	Instruction register[7:4]
uo_out[3:0]	Instruction register[3:0]

Output register

Label	Input/Output	Description
CLK [1 bit]	Input	Clock signal. Executes actions on rising edges.
W bus [8 bit]	Input	Data from the bus lines that are to be written to the Output register.
$\overline{L_{\text{O}}}$ [1 bit]	Input	Control signal that decides whether to read from the bus and load onto the output register.
Output register [8 bit]	Output	Register data that will be written to the binary display.

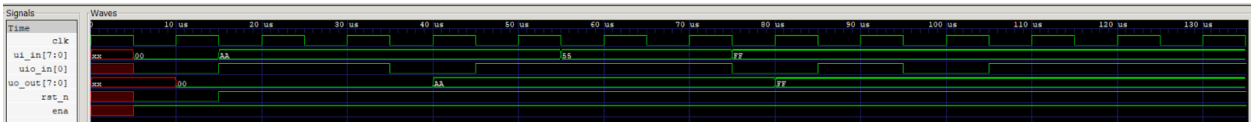


Test input Connections

Test Input	**Name**
clk	CLK
ui_in[7:0]	W bus
uio_in [0]	$\overline{L_{\text{O}}}$
uo_out[7:0]	Output register

B register

Label	Input/Output	Description
CLK [1 bit]	Input	Clock signal. Executes actions on rising edges.
W bus [8 bit]	Input	Data from the bus lines that are to be written to the B register.
$\overline{L}_{B}$ [1 bit]	Input	Control signal that decides whether to read from the bus and load onto the B register.
B register [8 bit]	Output	Register data that will be written to adder/subtractor.



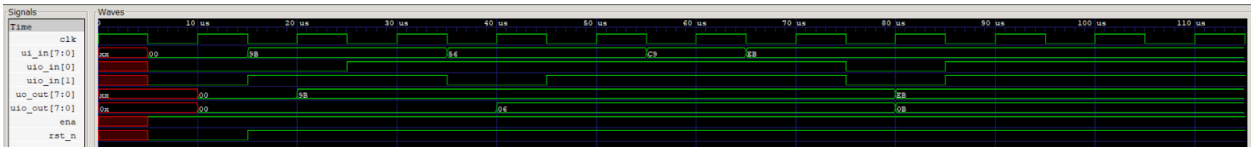
Test input Connections

Test Input	**Name**
clk	CLK
ui_in[7:0]	W bus
uio_in [0]	$\overline{L}_{O}$
uo_out[7:0]	Output register

Input and MAR

Label	Input/Output	Description
CLK [1 bit]	Input	Clock signal. Executes actions on rising edges.
W bus [8 bit]	Input	Data from the bus lines that are to be written either Input or MAR register. If writing to the MAR register, only 4 least significant bits are taken, the rest are discarded.
$\overline{L}_{MD}$ [1 bit]	Input	Control signal that decides if W bus data is to be written to the Input register. Should not

		be active at the same time as the $\overline{L}_{MA.}$control signal.
$\overline{L}_{MA}$ [1 bit]	Input	Control signal that decides if W bus data is to be written to the MAR register. Should not be active at the same time as the $\overline{L}_{MD.}$control signal.
Input register [8 bit]	Output	Register data to be written to memory.
MAR [4 bit]	Output	Register data taken by RAM that controls where the data is to be written.



Test input Connections

Test Input	**Name**
clk	CLK
ui_in[7:0]	W bus
uio_in [0]	$\overline{L}_{MD}$
uio_in [1]	$\overline{L}_{MA}$
uo_out[7:0]	Input register
uio_out[3:0]	MAR