ECE 411 MP4 Design

### An Out-of-Order Implementation of the RV32I Processor

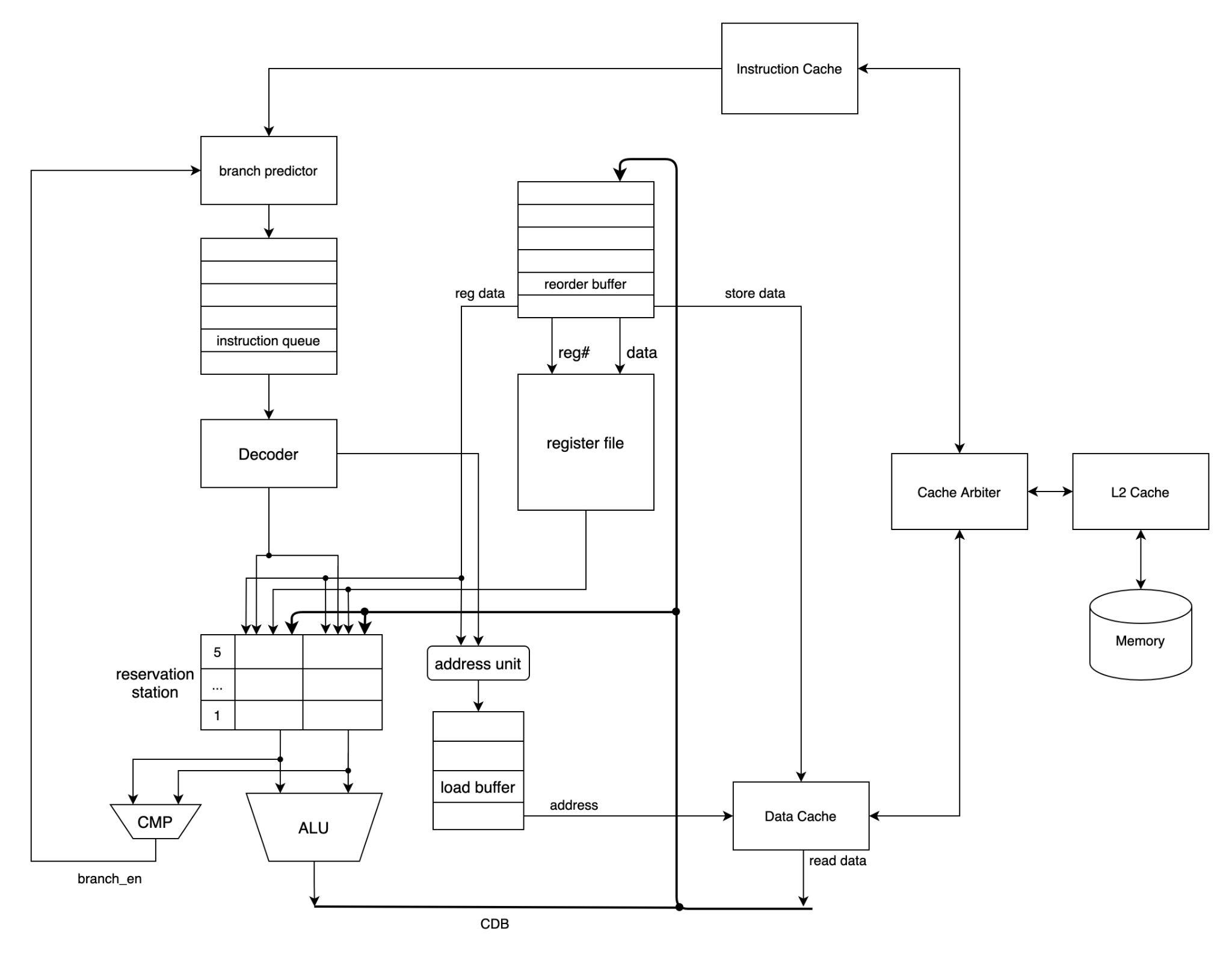
Zeduo Yu, Xiwei Wang, Pengyang Zhou

TA: Abishek Venkit

### October 20, 2021

We propose to design and implement an Out-of-Order CPU based on the revised Tomasulo algorithm supporting speculation.

1. **Datapath**

****

1. **Complex Components:**

**Instruction unit:**

Description: Implemented as a queue. If not full, read instructions from the instruction cache passing the branch predictor. Each cycle if the reservation station and reorder buffer is not full, pop an instruction.

Input: instruction (32 bits), PC (32 bits), branch enable (1 bit)

Output: instruction (32 bits), PC (32 bits)

**Decoder:**

Description: Decode the instruction, check if it is the load/store instruction, branch instruction, or register operation.

Input: instruction (32 bits), PC (32 bits)

Output: operation code (7 bits), operand1 (32 bits), operand2 (32 bits), destination register (5 bits).

**Reorder Buffer:**

Description: Used to store the instructions already executed but not committed.

Input: instruction type (7 bits), the destination field (5 bits), the value field (32 bits), branch result (1 bit)

Output: register value (32 bits), ROB entry number (3 bits)

**Reservation Station:**

Description: Store the operations and the value of operands. Write the result and the corresponding ROB entry number to CDB if the operation is complete.

Input: ROB entry number (3 bits), operation to perform in the unit (7 bits), value of source1 (32 bits), value of source2 (32 bits).

Output: operation code and values of operands to the ALU and CMP.

**Cache:**

Description: Data cache and Instruction cache are separated. We plan to use the L2 cache.

Input: memory address (32 bits), write data (32 bits), memory read (1 bit), memory write (1 bit)

Output: read data (32 bits), memory response (1 bit)

**Register files:**

Description: Contain the values of registers. Each entry is attached with a ROB entry number.

Input: register number (5 bits), register value (32 bits), ROB entry number (3 bits)

Output: register value (32 bits)

1. **Proposed Timeline**

Checkpoint1(October 27):

Create all the modules and connect the signals. Set up the test mechanism.

Checkpoint2(November 10):

Have a working machine except for branch prediction and integration of cache.

Checkpoint3(December 1):

Finish the implementation of Out-of-Order. Handle edge cases.

Checkpoint4(December 6):

Try to optimize and implement superscalar.