Digital Clock Design using Verilog VHDL

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Abstract

This paper presents the design and implementation of a simple digital electronic clock using Verilog HDL, with the objective of creating a system to simulate the accurate display of hours, minutes, and seconds. The clock's design consists of three main modules: the frequency division module, which generates a 1 Hz clock signal from a 50 MHz input; the counting module, which tracks the passage of time for hours, minutes, and seconds; and the decoding display module, which formats the time for simulation. The system is simulated using FPGA development boards to verify its functionality. The simulation results confirm that the digital clock operates as intended, accurately counting and displaying time in real time. The design leverages Verilog HDL for an efficient, reliable, and scalable approach to building digital clocks, demonstrating its potential for further development and enhancements.

Key Words: *digital clock, Verilog HDL, FPGA, frequency division, simulation*

1. INTRODUCTION

Clocks are essential for timekeeping and serve as a fundamental aspect of our daily lives. Mechanical clocks, while historically significant, have limitations, including lower accuracy and a lack of multifunctionality. The advent of digital clocks has significantly improved timekeeping precision and introduced numerous features that enhance user convenience. Digital clocks have become integral to modern life, offering high accuracy and additional functions, thanks to advancements in electronic technology.

A digital electronic clock utilizes digital circuits to display time in terms of hours, minutes, and seconds. This paper outlines the design of a digital clock using Verilog HDL, a powerful hardware description language suitable for digital circuit design. The main objective is to create a simple digital clock with essential timing and display functionalities. Specifically, the clock will display time in a 12-hour format, enhancing usability for general purposes.

The digital clock design is divided into three main modules: the frequency division module, the counting module, and the decoding display module. The frequency division module takes a 50 MHz input signal and divides it down to produce a 1 Hz clock signal, enabling accurate real-time timekeeping. The counting module tracks the passage of hours, minutes, and seconds, while the decoding display module converts this data into a readable format for simulation.

Simulation of the digital clock is performed using Verilog HDL on an FPGA development board to ensure functionality and verify the accuracy of timekeeping. This design demonstrates the efficiency, reliability, and scalability of Verilog HDL for digital clock applications. Through this project, we illustrate how digital circuits can be effectively employed to

build a precise and user-friendly timekeeping system, meeting the essential requirements of clock design and providing a foundation for further enhancements in digital clock technology.

2. Materials and Methods

2.1 Aim

The aim of this project is to design and simulate a digital clock using Verilog HDL. This clock displays time in a 12-hour format with hours, minutes, and seconds.

2.2 Tools and Platform

The project utilizes **Verilog HDL** for the digital design and **Xilinx Vivado** as the primary simulation and synthesis tool. Vivado provides an efficient environment for writing, testing, and simulating the HDL code before implementation on an FPGA. A 50 MHz input clock frequency is used as the basis for generating a 1 Hz signal, ensuring each clock tick represents one second.

2.3 Design Modules

The clock is composed of three primary modules:

- **Frequency Division Module**: Divides the 50 MHz input clock to a 1 Hz signal, forming the basis for time tracking.
- **Counting Module**: Tracks hours, minutes, and seconds, updating each unit based on the 1 Hz signal.
- **Decoding Display Module**: Converts counted values into a visual display format, representing each time unit as two digits.

2.4 Simulation and Testing

The design is verified using a Verilog HDL testbench in Xilinx Vivado, simulating the real-time operation of the clock. The testbench checks the functionality of each module and ensures that time progresses accurately. Each part of the timing sequence is tested to confirm that the digital clock meets the design criteria and operates as expected.

2.5 Block Diagram

The block diagram shown below represents the digital alarm clock system with various input and output signals. The given inputs include:

- reset - Resets the clock to its initial state.
- clk - The clock pulse input that drives the timing of the system.
- H_in1, H_in0 - Inputs for setting the hour. Represents the tens (H_in1) and units (H_in0) digits of the hour.
- M_in1, M_in0 - Inputs for setting the minutes. M_in1 represents the tens place, and M_in0 the units place.
- LD_time - Load time, a signal to set the current time.
- LD_alarm - Load alarm, a signal to set the alarm time.
- STOP_al - Stops or silences the alarm when it's ringing.
- AL_ON - Turns the alarm function on or off.

The output given includes:

- Alarm - This output goes high or active when the alarm is triggered.
- H_out1, H_out0 - Outputs displaying the current hour (H_out1 as tens and H_out0 as units).
- M_out1, M_out0 - Outputs displaying the current minute (M_out1 as tens and M_out0 as units).

- S_out1, S_out0 - Outputs for displaying the seconds (S_out1 as tens and S_out0 as units).

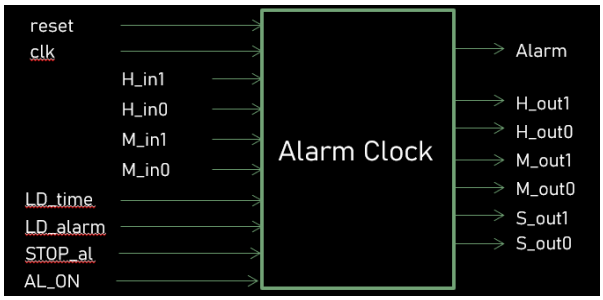

Figure 1: Block Diagram

2.6 Circuit Diagram

The diagram depicted in illustrates the circuit configuration for the digital clock. A total of 104 cells are being used for the circuit design.

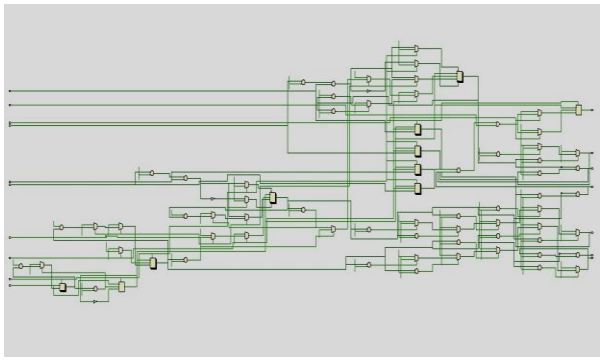

Figure 2: Circuit Diagram

3. RESULTS

The digital clock design is functional and meets the specified requirements. An analysis based on timing, power and area have been made.

3.1 Timing Analysis

The digital clock simulation results confirm the accurate functionality of each module, verifying the clock's capability to count and display time in a 12-hour format. The testbench simulation results below validate that hours, minutes, and seconds advance correctly over time, resetting at appropriate intervals.

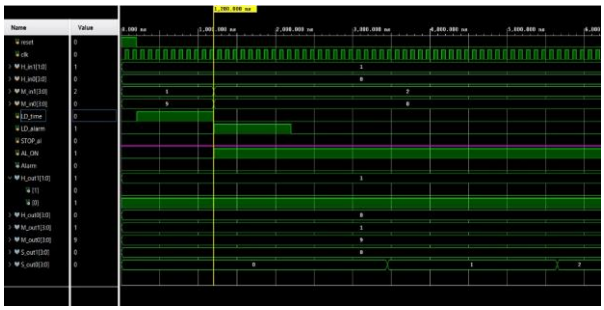

Figure 3: Timing Analysis

The output waveforms demonstrate smooth transitions in timekeeping, confirming the correct operation of frequency division, counting, and display decoding processes. The Verilog HDL design in Xilinx Vivado meets all required specifications and provides a reliable simulation of a digital clock.

3.2 Power Analysis

The figure below depicts the estimate of the power consumption of the digital clock design.

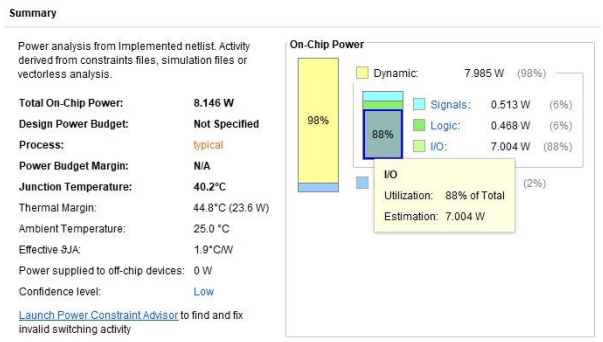

Figure 4: Power Analysis

The total On-Chip Power of 8.146 W has been consumed for the designing of the digital clock which includes:

Static Power: 0.161 W (2%)

Dynamic: 7.985 W (98%) - The power consumed due to switching activity in the logic gates which is composed of:

- Signals: 0.513 W (6%) - Power consumed by the signals propagating through the design.
- Logic: 0.468 W (6%) - Power consumed by the logic gates themselves.
- I/O: 7.004 W (88%) - Power consumed by the input/output interfaces.

3.3 Area Analysis

This graph shows the utilization of various resources in a digital design, comparing the usage after synthesis and implementation stages. Here's an analysis of the key points:

- LUTs (Look-Up Tables): These are used to implement combinational logic functions. In this case, 1% of the available LUTs are used.
- FFs (Flip-Flops): These are used to store state information. 1% of the available FFs are used.
- IO (Input/Output): This represents the utilization of input/output pins. 11% of the available I/O pins are used.
- BUFG (Buffer): These are used to buffer signals and drive loads. 6% of the available buffers are used.

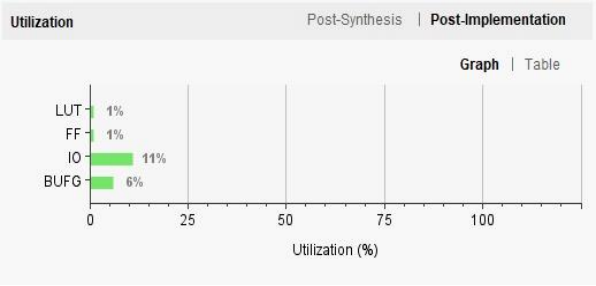

Figure 5: Area Analysis

Area analysis shows efficient FPGA resource utilization, with only 19% of the area used which indicates that the design is not resource-intensive and has been efficiently implemented.

3.4 Implemented Device

For a digital clock design in Verilog, the figure shown below represents the layout diagram on how the clock's various modules are mapped onto the FPGA.

Each block labeled with coordinates (e.g., X0Y4, X1Y4) shows a specific area of the chip where elements of the digital clock design, such as counters, display decoders, and frequency dividers, are implemented. The different colors and lines indicate the routing paths for signals, showing how components communicate across the chip.

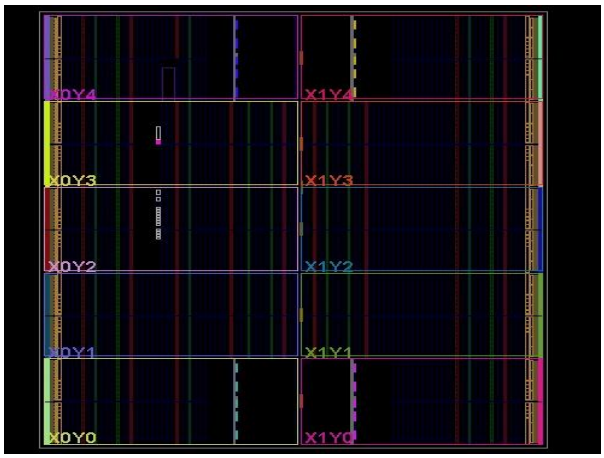

Figure 6: Implementation design

The layout visualization helps confirm that the digital clock modules are well-placed, that routing is efficient, and that no areas are overly congested. The visualization also helps identify areas of high activity or resource usage, useful for refining placement or routing if necessary to improve performance, reduce power consumption, or ensure accurate timing in the clock functionality.

4. DISCUSSION

The modular approach adopted in designing this digital clock allows for efficient man-

agement of each function: frequency division, counting, and decoding for display. By separating these functions, the design achieves a high level of accuracy and functionality, particularly suitable for real-world clock applications. Xilinx Vivado's simulation environment has proven effective in validating the Verilog HDL design, ensuring the clock operates as intended.

This design can be expanded to incorporate additional features, such as alarms or different time formats, showcasing the flexibility and scalability of using HDL for digital clock design. Future work could explore integrating this digital clock with more complex systems or improving user interaction capabilities.

5. CONCLUSION

In conclusion, the digital clock designed and simulated in this project demonstrates accurate timekeeping and reliable performance using Verilog HDL. The three-module structure, involving frequency division, counting, and decoding, successfully displays time in a 12-hour format. The simulation results confirm the clock's ability to meet specified design criteria, validating the use of Xilinx Vivado for HDL development and testing. This project illustrates the efficiency of HDL for creating digital timekeeping systems, providing a foundation for further innovations in digital clock functionality.

REFERENCES

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