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Abstract

This paper describes the design, simulation, and analysis of an SR latch in 45nm CMOS technology, concentrating on its pre-layout and post-layout performance. The SR latch which is the basic memory circuit is built using two NMOS and PMOS cross-coupled NAN gates. Design includes schematic, pre-layout simulation, layout design and post layout simulation. Functional checks are carried out in the form of Design Rule Check (DRC) and Layout vs. Schematic (LVS) verifications. The results indicate a noteworthy post layout performance drop where static and dynamic power dissipation increases and rise, fall and delay times lengthen due to layout introduced parasitic effects. These results contribute towards the understanding of the effects of parasitic elements on the power and timing performance of the circuit and advocate for the integration of layout optimization techniques towards improved efficiency in practical use.

Introductions:

Sequential logic is a fundamental aspect of modern digital systems, forming the backbone of memory elements and various electronic circuits. A basic component of digital memory, the SR (Set-Reset) latch stores a single bit of data and keeps the output steady even if the input signals are deleted. It is necessary for the creation of more complex storage components like D and T flip-flops and needs two inputs, Set (S) and Reset (R). The SR latch is a crucial component of sequential logic circuits and is traditionally implemented using cross-coupled transistors. As semiconductor technologies develop, research is being done to improve the latch's performance, dependability, and power efficiency. Improving the performance of these memory components in digital devices requires efforts to reduce clock power and lessen the impact of manufacturing changes.

With the advance developments in photonics which has resulted in the rise of much interest on optical logic. This also includes all optical SR latch which is actuated based on interferometric and mirroring resonators. Besides this, these optical components have VLSI benefits such as being faster and higher integration density which can greatly improve digital systems. This paper presents the design and simulation of an SR latch using 45nm CMOS technology and explores the conceptual design of a digital electro-optic SR NAND latch based on silicon mirroring resonators.

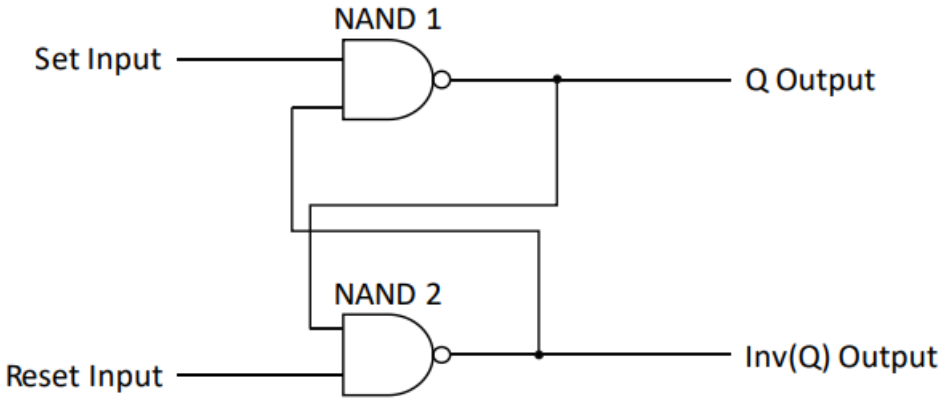


Figure 1: Design of SR latch using NAND gate

Aim:

To design and simulate an SR latch using NMOS and PMOS transistors in 45nm technology with Cadence software.

Objectives:

1. Create the schematic and layout of the SR latch using NMOS and PMOS transistors.
2. Complete Design Rule Check (DRC) and Layout vs. Schematic (LVS) verification.
3. Verify SR latch's ability to store one bit based on set (S) and reset (R) inputs.
4. Study the behavior of the cross-coupled inverter configuration in maintaining the latch state.

Procedure to Design of SR latch

1. Schematic Design

- Create Schematic: Use two NAND gates constructed from NMOS and PMOS transistors to construct the SR latch.

- Connect Inputs and Outputs: Connect the outputs as Q and Q' and label the inputs as Set (S) and Reset (R).

- Check Design: Run a Design Rule Check (DRC) to ensure no errors.

2. Pre-Layout Simulation

- Set Up Test Bench: Connect inputs (S, R) and load outputs (Q, Q').

- Run Simulation: Perform transient and DC analysis to verify output behavior for each input combination.

- Verify Results: Confirm output matches SR latch truth table.

3. Layout Design

- Place Components: Arrange NMOS/PMOS transistors for each NAND gate.

- Interconnect: Wire up according to the schematic, add Vdd and GND rails.

- DRC & LVS: Run DRC for layout rules and LVS to match schematic with layout.

4. Post-Layout Simulation

- Extract Parasitic: Generate an extracted view with parasitic.

- Re-run Simulation: Simulate with extracted layout and check performance.

- Compare Results: Analyze any changes from pre-layout due to parasitic.

Design of SR – Latch

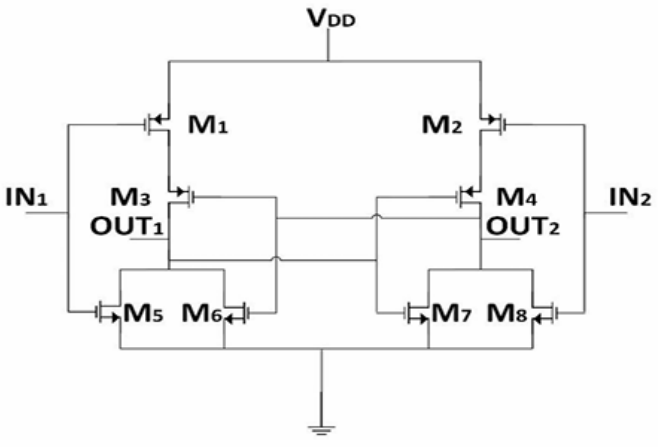


Figure 2:Transistor level SR latch design

Description of Design

It can be implemented using two cross-connected NAND gates. A NAND gate, a fundamental logic gate, can be implemented at the transistor level using a combination of NMOS and PMOS transistors. NMOS transistors act as switches that are turned on when their gate voltage is high, while PMOS transistors act as switches that are turned on when their gate voltage is low.

An SR latch is a basic memory element that can store one bit of information. It can be implemented using two cross-connected NAND gates. The inputs S and R control the latch's state. When S is high and R is low, the latch is set. When S is low and R is high, the latch is reset. When both inputs are low, the latch retains its previous state. Both inputs high is an undefined state and should be avoided.

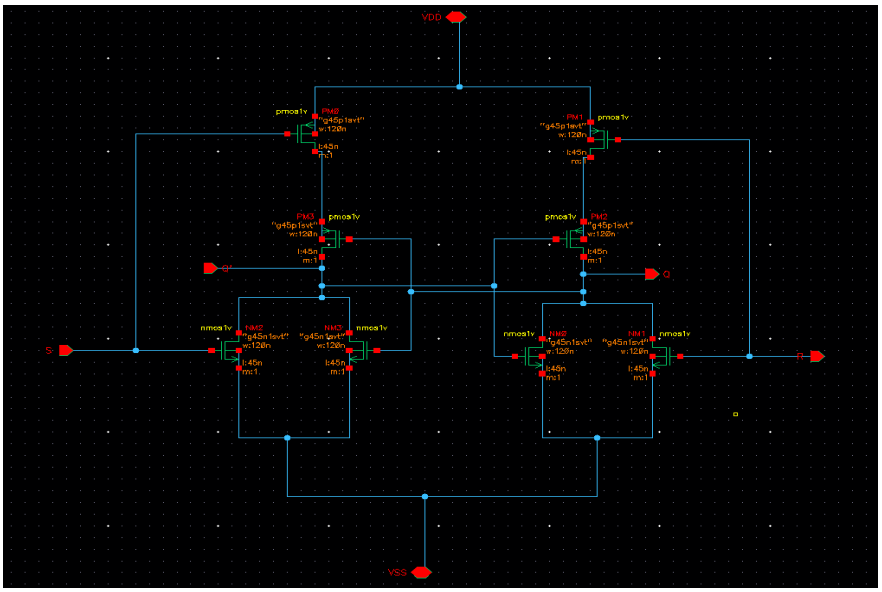


Figure 3: Schematic Diagram of SR latch

Description of the Schematic:

The provided schematic illustrates an 8-transistor differential amplifier, a fundamental building block in analog integrated circuit design. This circuit comprises two input transistors (M1 and M2) configured as a differential pair, two current source transistors (M3 and M4) to provide a constant current bias, and four output transistors (M5-M8) in a common-emitter configuration.

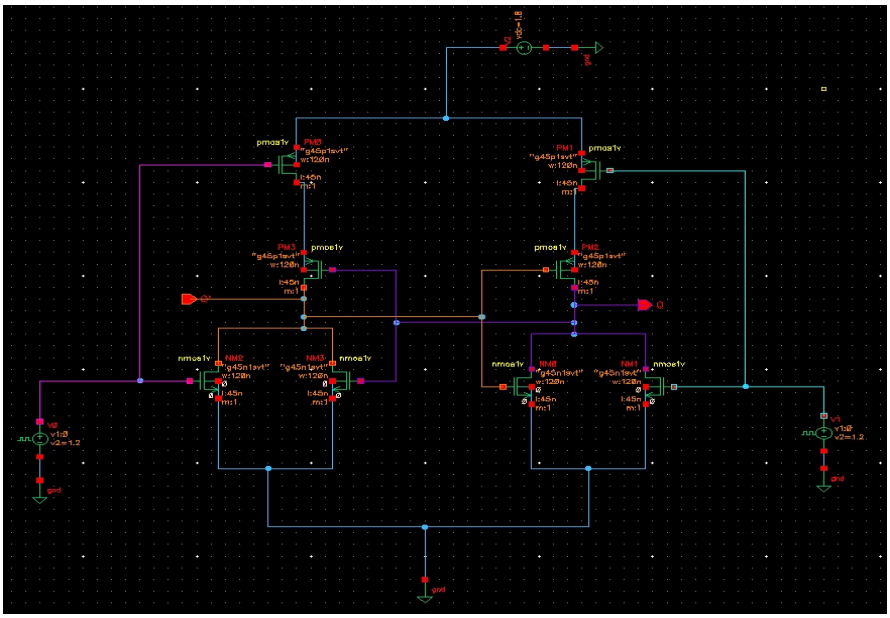


Figure 4: Test bench for SR lacth

The schematic shows a test bench for an SR latch, a fundamental digital circuit capable of storing one bit of data. It comprises two cross-coupled NOR gates with inputs S (Set) and R (Reset), and outputs Q and Q'. The test bench includes voltage sources, input signals (S and R), and output monitoring points (Q and Q'). By simulating various input conditions, the test bench verifies the SR latch's correct operation.

- Common test cases include:
  - Set operation (S=1, R=0)
  - Reset operation (S=0, R=1)
  - Hold operation (S=0, R=0)
  - Invalid state (S=1, R=1)

Simulation Result

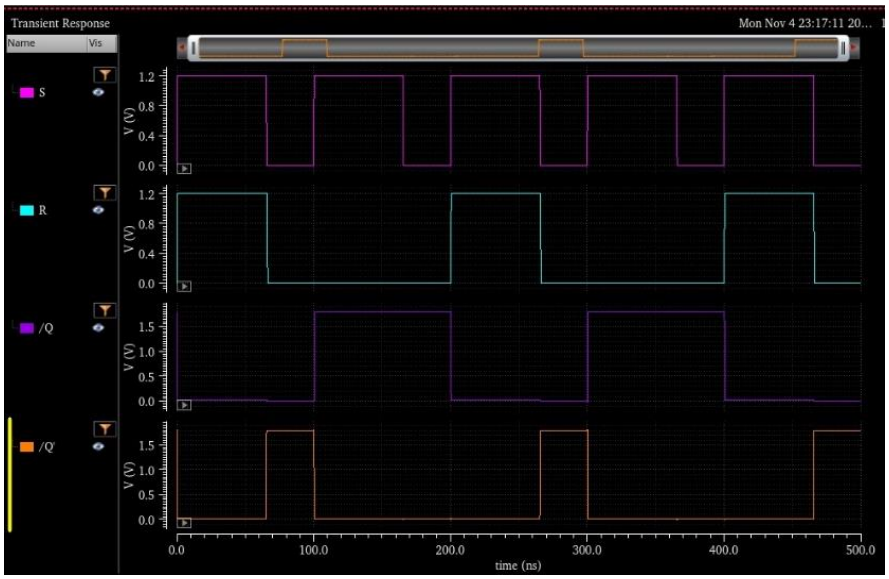
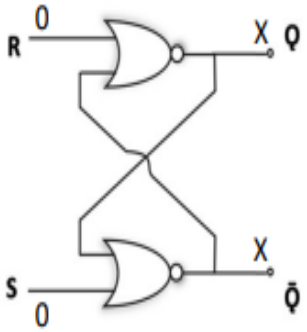


Figure 6: Transient Response

The plot shows the simulation results of an SR latch. The input signals (S and R) control the output signals (Q and Q'). The SR latch operates as expected, changing its state based on the input conditions. The transient response is verified using the truth table of the SR latch.

RS Latch



R	S	Q	Q'	State
0	1	1	0	Set
0	0	1	0	No Change
1	0	0	1	Reset
0	0	0	1	No Change
1	1	0	0	Invalid
0	0	X	X	RACE

Figure 5: Truth Table of SR Latch

Layout:

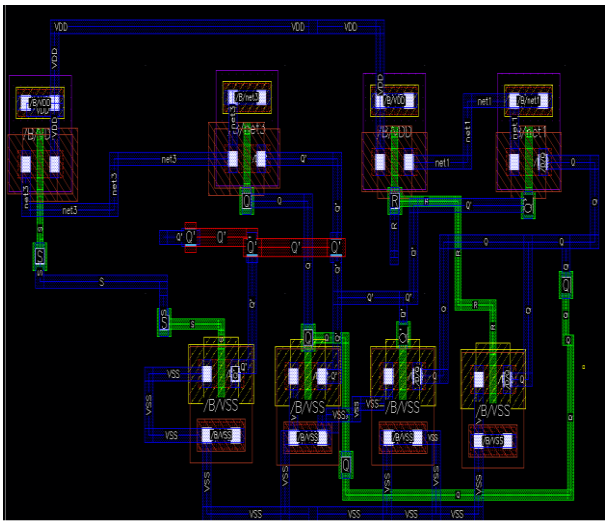


Figure 7: Initial Layout of SR Latch

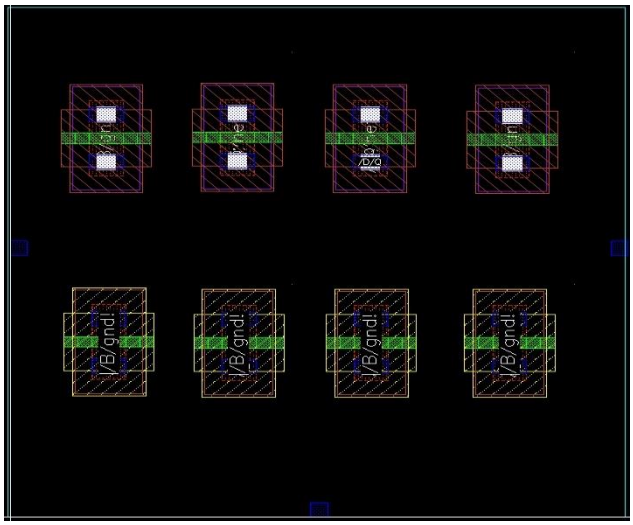


Figure 8: Final making of SR Layout

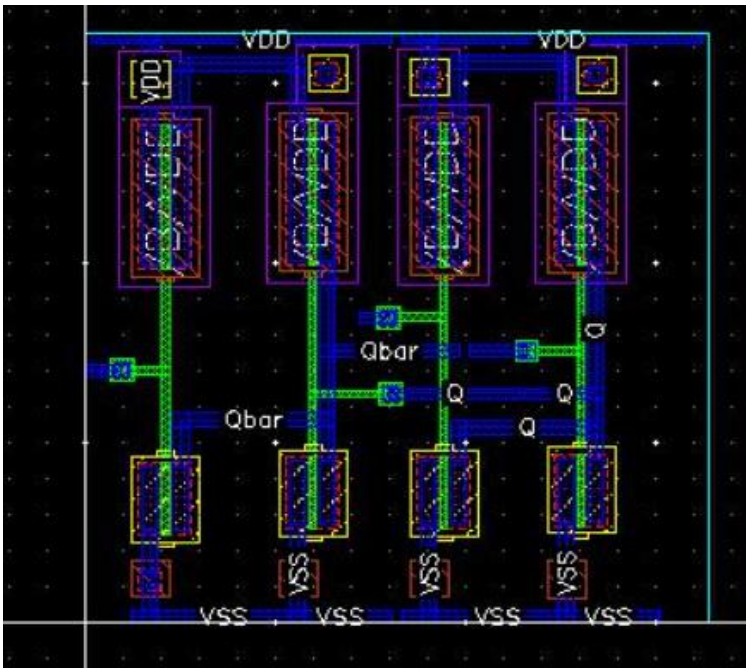


Figure 9:SR Latch Layout

The SR latch layout in CMOS involves placing NMOS and PMOS transistors to form two cross-coupled NAND gates, with connections labeled as Set (S), Reset (R), and outputs Q and Q'. Power rails (Vdd and GND) are added to supply power to the circuit. After placing and wiring the transistors, a Design Rule Check (DRC) ensures compliance with fabrication guidelines, and a Layout vs. Schematic (LVS) test confirms the layout matches the schematic, verifying functional accuracy.

DRC and LVS test:

- *DRC (Design Rule Check):* Ensures the SR latch layout follows fabrication rules, such as minimum spacing and layer widths, to ensure it can be manufactured without issues.
- *LVS (Layout vs. Schematic):* Confirms the layout matches the SR latch schematic by verifying that all connections and components (e.g., NAND gates) align, ensuring functional accuracy.
- Passing both tests confirms the latch layout is both manufacturable and true to the design.

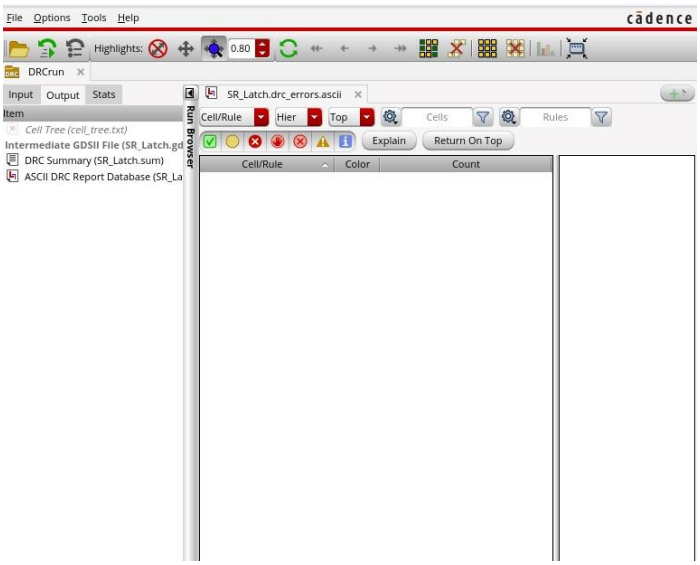


Figure 11: DRC test

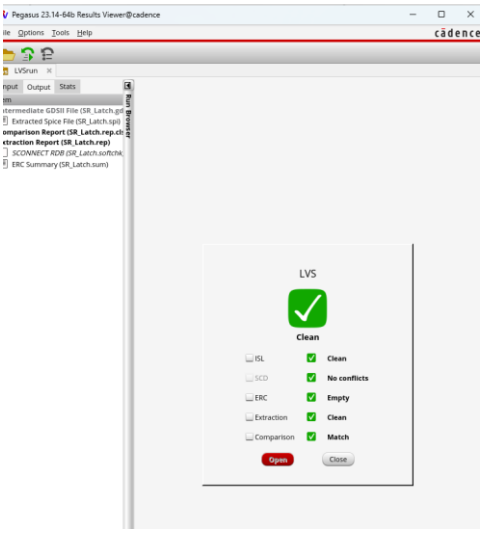


Figure 10: LVS test

Parasitic Extraction of Layout

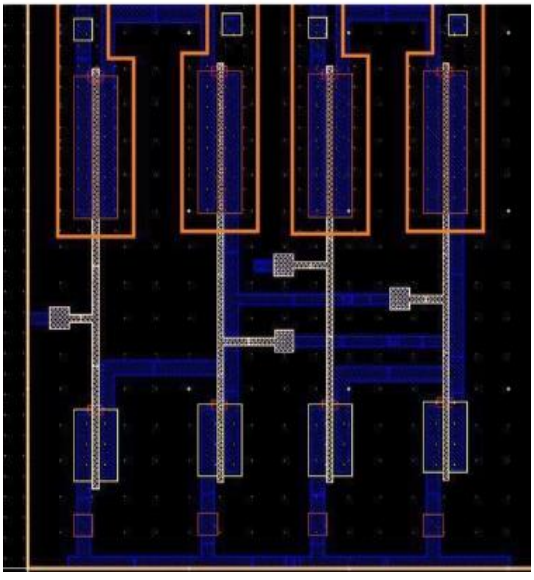


Figure 12: AV_extraction of SR Latch

In AV extraction using Quantus, a layout's parasitic resistances and capacitances are extracted to create an accurate, real-world model of the circuit. Once a small cell layout is complete, Quantus calculates parasitic elements like interconnect resistance and coupling capacitance, based on geometry and spacing in the design. This process generates an "AV-extracted" view, where parasitic are integrated into the original netlist, providing a more realistic circuit model. This view is then used for post-layout simulations, allowing designers to verify performance and ensure that the circuit will behave reliably under actual conditions.

Result and Analysis

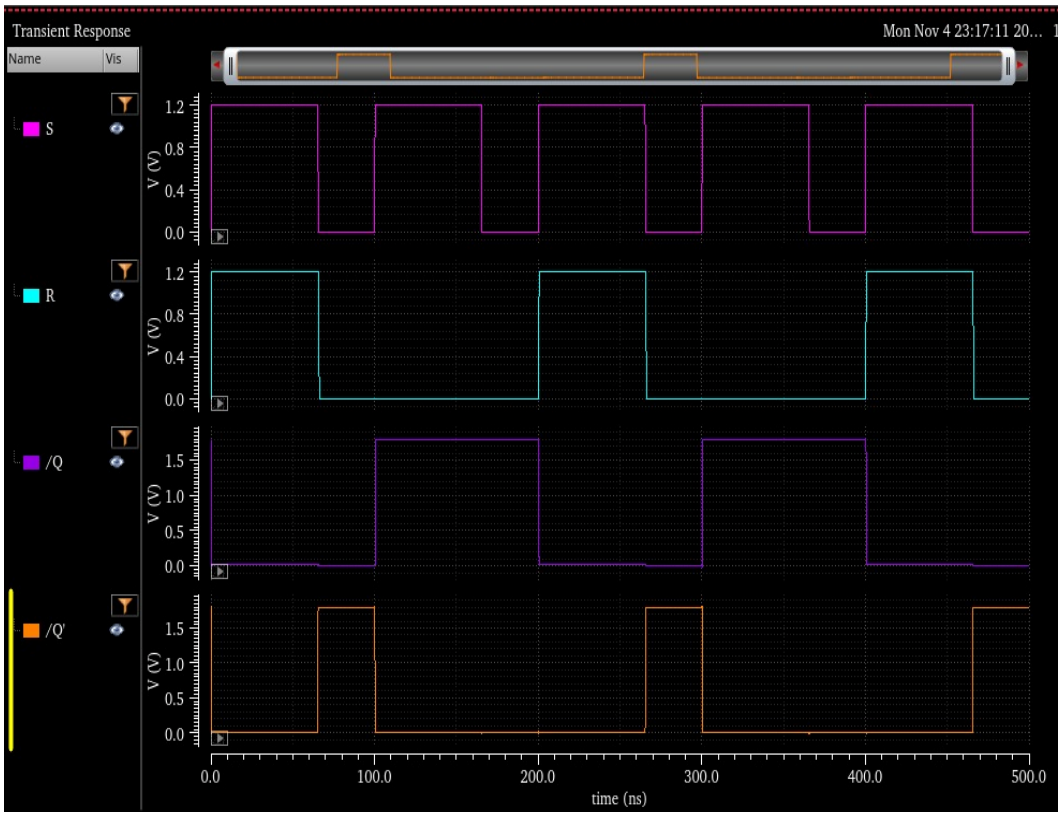


Figure 13: Post Layout Transient Analysis

The transient response of an SR latch describes how its output (Q) changes over time in response to varying Set (S) and Reset (R) inputs. It includes key factors like rise time, fall time, settling time, and propagation delay. This response helps evaluate how the latch behaves during input transitions, including any delays or overshoot, and is crucial for ensuring correct operation in real circuits.

Comparison between the result of Pre-Layout and Post Layout Simulations:

Type	**Static Power (nW)**	**Dynamic Power (uW)**	**Rise time (psec)**	**Fall time (psec)**	**Delay (psec)**
Pre-Layout Simulation	25.66	0.34	15.11	25	35
Post-Layout Simulation	52.55	0.71	25.32	37	60

The post-layout simulation results show a significant degradation in performance compared to the pre-layout simulation. Static power consumption increases from 25.66 nW to 52.55 nW, and dynamic power rises from 0.34 µW to 0.71 µW. This increase in power consumption can be attributed to the parasitic capacitances and resistances introduced during the layout process, which lead to higher leakage currents and more power being consumed during switching. Additionally, the timing characteristics also worsen after layout, with the rise time increasing from 15.11 psec to 25.32 psec, the fall time increasing from 25 psec to 37 psec, and the overall delay growing from 35 psec to 60 psec. These delays are primarily caused by the additional parasitic elements slowing down the signal transitions. Overall, the post-layout simulation highlights the impact of parasitic effects on both power consumption and timing performance, emphasizing the need for layout optimization to mitigate these issues and ensure efficient operation in real-world applications.

Conclusion

The design and simulation of the SR latch using 45nm CMOS technology revealed significant performance degradation after layout implementation. While the pre-layout simulation showed optimal static power of 25.66 nW, dynamic power of 0.34 µW, and reasonable timing characteristics (rise time of 15.11 psec, fall time of 25 psec, and delay of 35 psec), the post-layout results indicated an increase in static power to 52.55 nW, dynamic power to 0.71 µW, and worsened timing with rise time at 25.32 psec, fall time at 37 psec, and delay at 60 psec. This performance decline can be attributed to the parasitic resistances and capacitances introduced during the layout process, which caused higher leakage currents and slower signal transitions. These findings emphasize the need for layout optimization to mitigate parasitic effects and improve both power efficiency and timing performance in practical applications.

Reference

Study Materials. (2018, August 30). *Layout Tutorial in Cadence Tool- SR Latch* [Video]. YouTube. https://www.youtube.com/watch?v=fUJL5SEGki0

He, Y. and Yuan, G. (2022). A 1.2 V high-speed low-power preamplifier latch-based comparator. *Electronics Letters*, 58(24), pp.896–898. *doi:https://doi.org/10.1049/ell2.12636.*