Advanced Micro and Nanofabrication Technologies

Engineering Physics – Ingegneria Fisica - Cod. 055559

a.a. 2024/2025

Matteo Cantoni
Dipartimento di Fisica
Politecnico di Milano and Polifab
Ed. 30 - Via G. Colombo 81 – Milano
https://cantoni.faculty.polimi.it/

Lecture 1
Introduction

prof. Matteo Cantoni

matteo.cantoni@polimi.it

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eFES

How to fabricate a device?

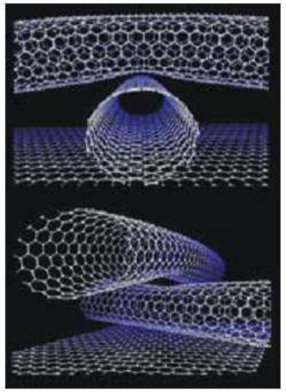
Top-down: adding or removing material from macroscopic systems to make micro-scale objects

Growth of macroscopic heterostructures

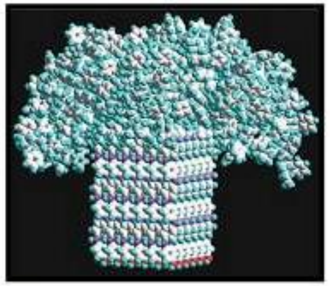
+

patterning by lithography of micro (nano) structured devices

Bottom-up: assemble nanoscale objects starting from smaller units (e.g., atoms or molecules)



Carbon nanotubes synthesis



Supramolecular rodcoil "mushrooms"

Example: a (spin) photodiode

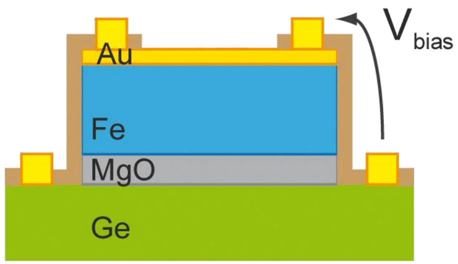
Top-down: adding or removing material from macroscopic systems to make micro-scale objects

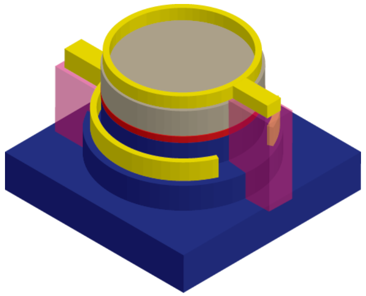
Growth of macroscopic heterostructures

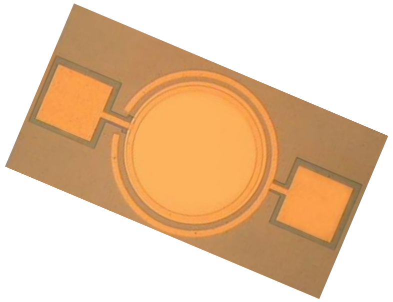
+

patterning by lithography of micro (nano) structured devices

Example: **Fabrication a photodiode for integrated detection of light polarization**







L-NESS

C. Rinaldi, M. Cantoni, et al., Adv. Mat. 24, 3037 (2012)

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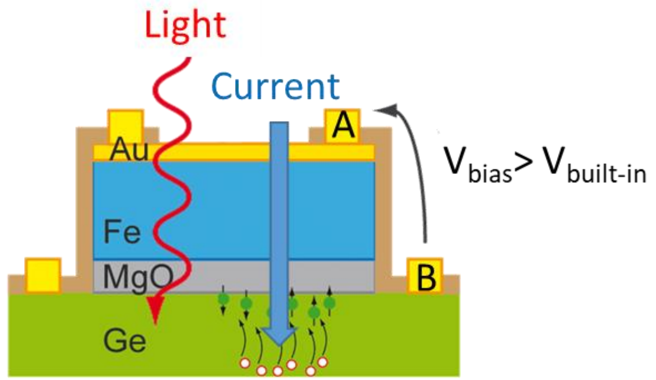
From the working idea…

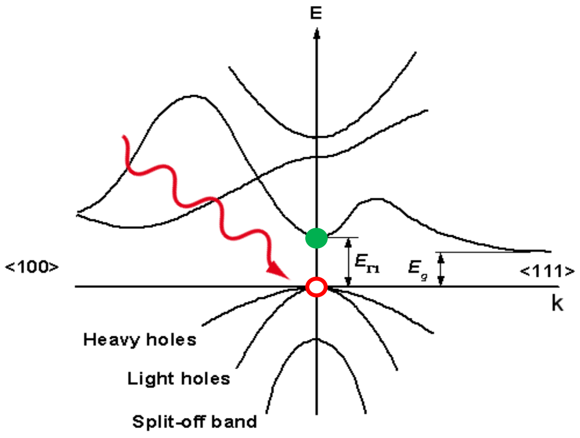


What the photodiode must do?

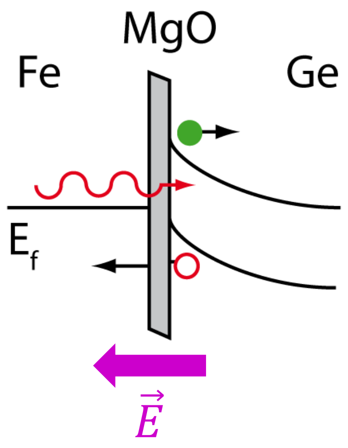
- **Collect** light
- **Convert** light into a related electrical signal
- Make the signal **available** to be measurement

What we basically need?

- A **semiconductor** (e.g Ge) where the absorption of a light with photon energy equal or larger than the gap (0.66 eV, corresponding to a wavelength λ=1.88 μm, in the IR range) promotes an electron in the conduction band, leaving an hole in the valence band.
- This electron-hole pair is physically separated by an electrical field providing a current flowing across the layer.



Physics of semiconductors, optoelectronics, material science, …



… to the device fabrication

What the photodiode must do?

- **Collect** light
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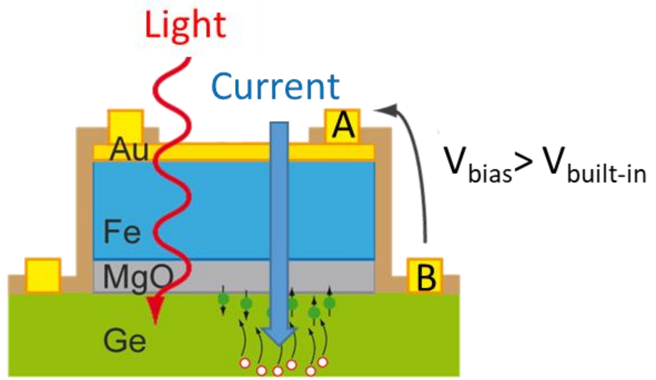


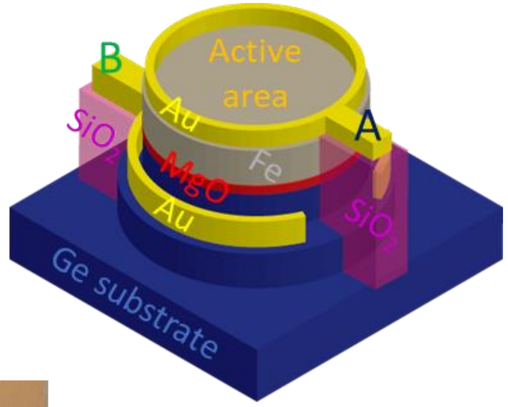
*How to **use** the heterostructure as a **device**?*

✓ **Active area** for photodetection – the thickness of the material above Ge must be *as small as possible* to reduce light attenuation

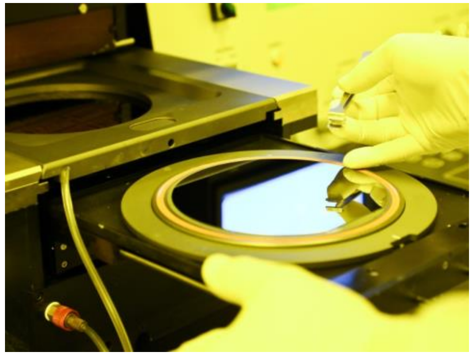
✓ **Electrode A** in electrical contact with the Au/Fe layer – and *insulated* (using silicon dioxide - SiO_2) from the Ge substrate to avoid short circuits

✓ **Electrode B** in electrical contact with the Ge substrate – and *insulated* (using silicon dioxide - SiO_2) from the Au/Fe layer to avoid short circuits

Device patterning by lithography



First: deposition



From what we start?

- Substrate: Ge(001) wafer

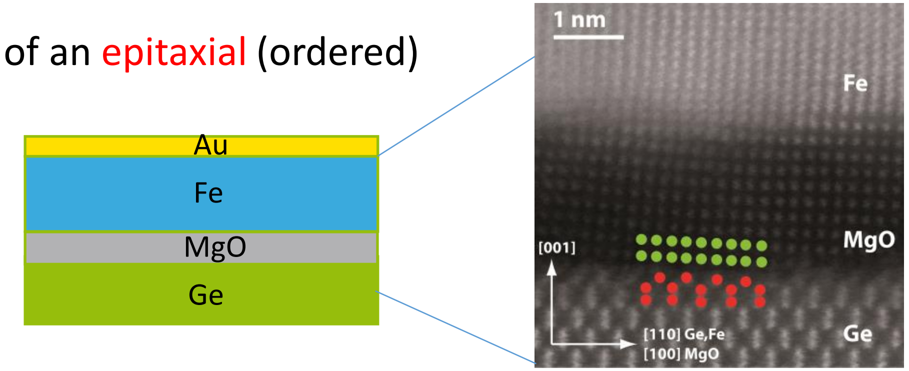
… but the surface will be contaminated (C, O) and oxidized (GeO, GeO_2)

- Cleaning (i) ex-situ (by chemical agents, e.g. HF) in clean room

  (ii) in-situ (by annealing at ~600°C) in high vacuum conditions

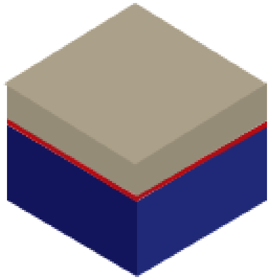
What's next?

- Layers growth (MgO, Fe, Au) by Molecular Beam Epitaxy (MBE) ⇒ realization of an epitaxial (ordered) structure
- Post-growth characterization
  - in-situ (XPS, XPD, LEED, RHEED, MOKE, …)
  - ex-situ (AFM, TEM, …)

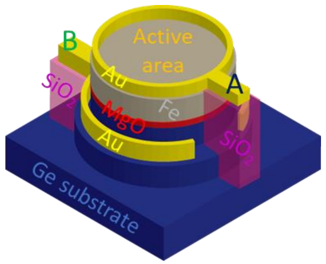


TEM (Transmission Electron Microscope)
[D. Petti et al., Journal of Applied Physics 109, 084909 (2011)]

Second: patterning



patterning



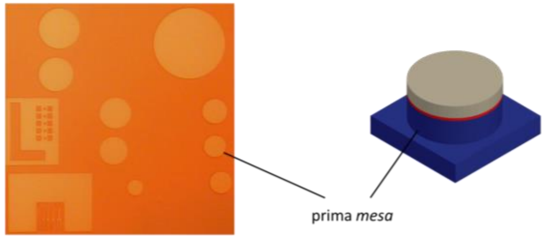
From heterostructure …

… to device

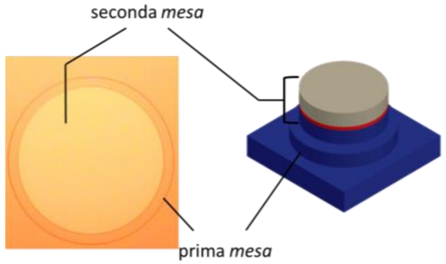
4 steps involving:

- ✓ Optical **lithography** by physical masks (all steps) to define suitable areas in the heterostructure stack
- ✓ Material removal by physical (ion beam) **etching** (steps 1-2)
- ✓ Material deposition by e-beam **evaporation** (steps 3-4)

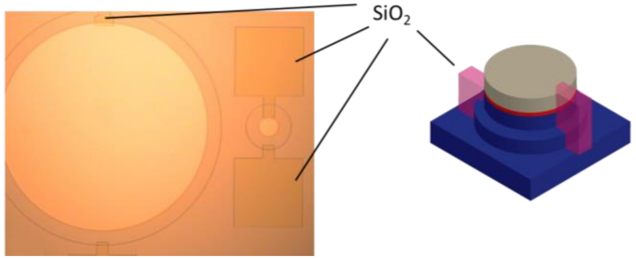
Step 1:
definition of the **device area**



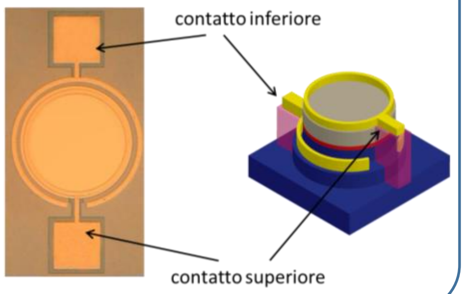
Step 2:
definition of the active area for photodetection



Step 3:
deposition of SiO_2 to **insulate** bottom (Ge) from top (Au/Fe) layers

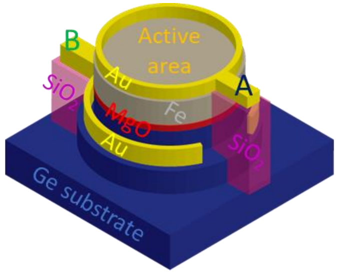


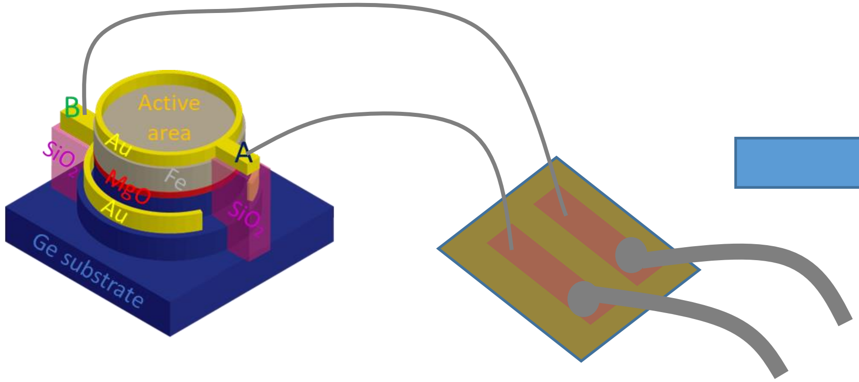
Step 4: deposition of Au **contacts** on bottom (Ge) and top (Au/Fe) layers

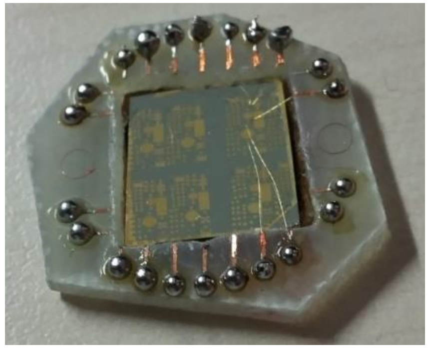


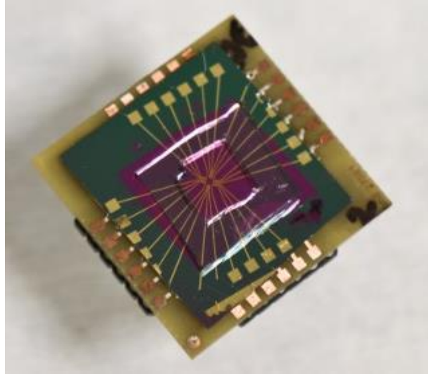
Third: electrical contacts

The device must be **electrically accessible**





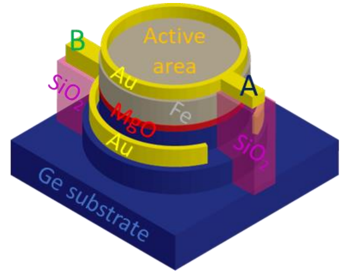




- ✓ **Thin wires** (12.5-500 μm diameter) of Au or Al are used to connect the **device electrodes** to an **external board** with **metallic pads**, suitable for conventional **tin soldering**
- ✓ Ultrasonic wire bonder can be used to locally heat the **wire tip** until its fusion on the electrode area

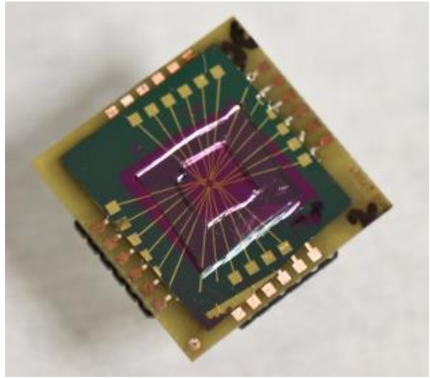
Finally: packaging, testing etc.

The device must be **inserted in a suitable packaging** to manage it without being scientist…



Packaging

Chip holder with device contacts wire bonded by gold wire to copper pads



Testing … **Protyping** … **Release to market** …

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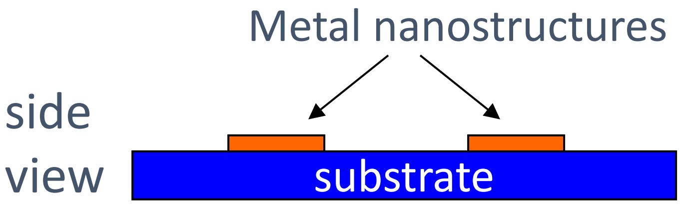
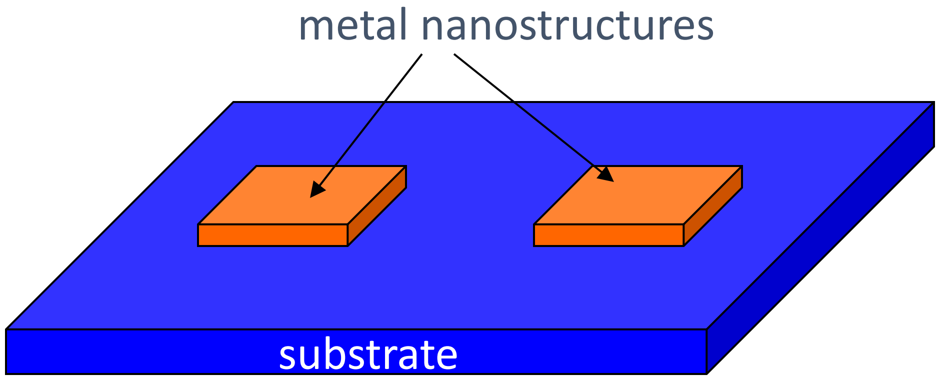
Electrical access to electrodes A and B by coaxial connector

Light access to active area

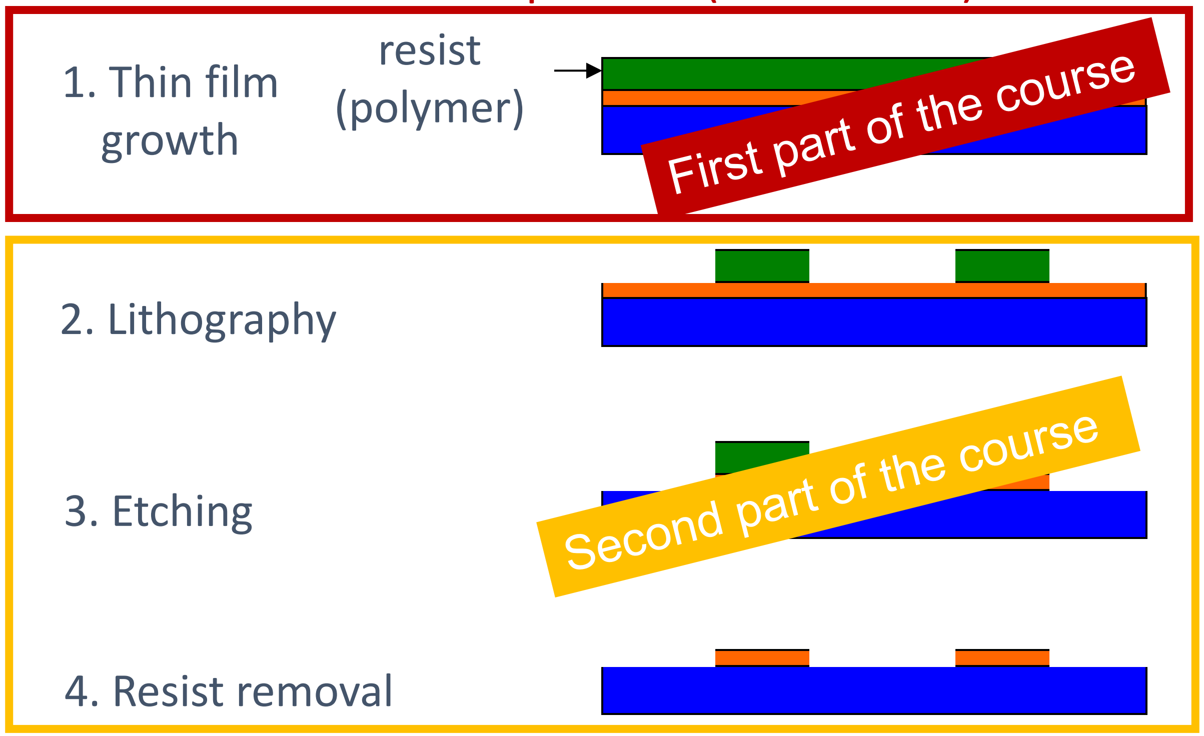
Example of wafer manufacturing

Credits: Bo Cui, University of Waterloo

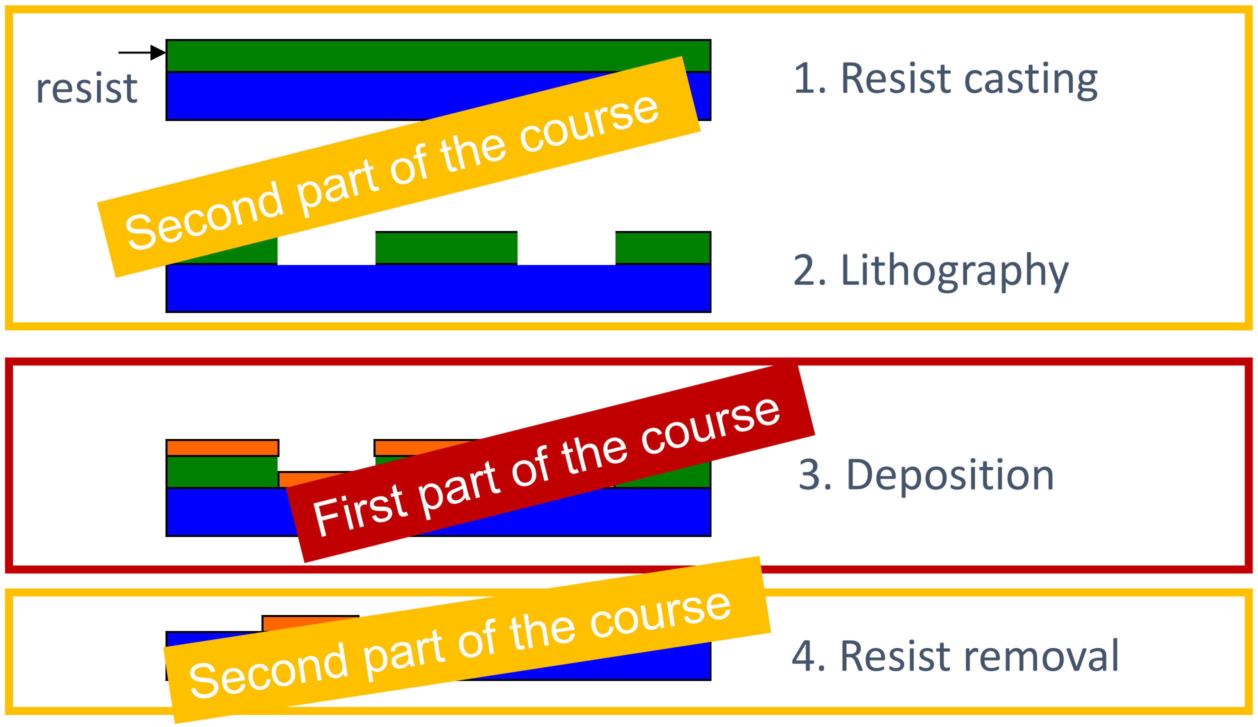




Direct etch process (subtractive)



Liftoff process (additive)



Which problems deposition addresses?

- Material: metals/insulators/semiconductors/oxides…
- Stoichiometry: elementals/alloys (binary/ternary/quaternary…)
- Surface: flat/rough
- Order: crystalline/amorphous
- Thickness: thick/(ultra)thin
- Uniformity: high/low
- Substrate: conductive/insulating; flat/rough
- Process step: patterned/unpatterned…
- Applications: FM, FE, SC, …

There is not a unique solution

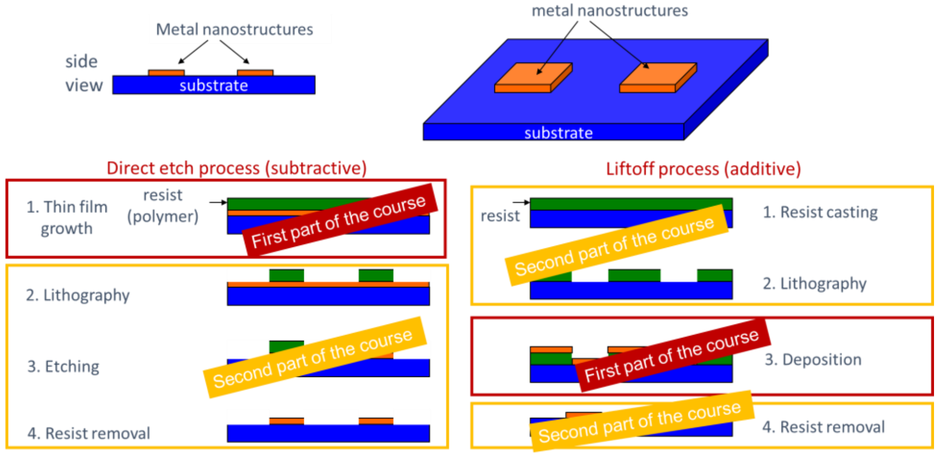
$\Downarrow$

different techniques to the same scope

$\Updownarrow$

different scopes for the same technique

Film and heterostructure deposition



- **Where** we will grow? **Vacuum**
- **On what** we will grow? **Surfaces**
- **Which kind** of films we will grow? **Epitaxy**
- **How** we will grow?
  - **Physical techniques (PVD)**
    - **Evaporation**
    - **Sputtering**
  - **Chemical techniques (CVD)**
- **How** we will check the growth? **Characterization**

Reference book: M. Ohring, Materials Science of Thin films, Academic Press
+ slides, exercises, recording