

Assignment

COEN 311
Computer Organization and Software
Assignment #2

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“I certify that this submission is my original work and meets the
Faculty’s Expectations of Originality”

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February 15, 2022

Short answer questions

Question 1

1- How large is a memory segment in 8086 architecture?

Each memory segment is 64KB.

Question 2

2- What is the function of Instruction Pointer?

The instruction pointer stores the offset address, with respect to the code segment, of the next instruction in memory to be executed.

Question 3

3- What two address elements are combined to form a physical address?

To form the physical address, we add the base address, shifted to the left by 4 bits, with the offset address.


Question 4

4- A data is going to be stored in a memory cell, which registers are required to calculate the memory address that data is stored into?

To calculate the memory address that we'll store the data in, we use the data segment register (DS) to get the base address.

Question 5

5- What kind of information is stored in pointer and index registers?

Address/Memory locations are stored in pointer and index registers. 

Question 6

6- What happens to the value of IP each time an instruction is executed?

The instruction pointer is incremented by the size of the instruction that was executed. This places its current value at the location of the next instruction to execute.

Question 7

7- In the previous question, assume that the instruction is 2 bytes, what happens for IP after the instruction execution?

$IP = IP + 0002$

Question 8

8- What is the purpose of segment registers in 8086 register?

The segment registers hold the lowest/base address of a segment.

Question 9

9- Which of the following architectures are found in the 8086 microprocessor?

Why? (6 points)

- Harvard architecture
- Von-Neuman architecture
- RISC Instruction architecture
- CISC Instruction architecture



Harvard architecture since memory is broken up into segments meaning we have a section for data memory (the data segment) and a section for instruction memory (the code segment). These segments can be used individually.

Its also a CISC because its instruction set is simpler. One instruction can perform multiple operations with only one instruction.

Computational Questions

Question 10

10-How many bits are required to address the Memory space of 8086 processor? Why? Show your work. (8 points)

Since the 8086 processor can have a memory capacity of 1Mb and it is byte organized,

$$C = 2^k * \frac{8}{8} \text{ bytes}$$

$$1Mb = 2^k$$

$$2^{20} = 2^k$$

$k = 20$ bits are required to address the memory space

Question 11

11-Calculate the value of each physical addresses that follows. Assume all numbers are hexadecimal:

- a) 1000:1234
- b) 0100:ABCD
- c) A200:12CF

Shift the base address to the left by 4 bits, then add the offset address to get the physical address.

a)

Base Address: 1000 → shifted by 4 bits → 10000

Offset address: 1234

$$\begin{array}{r} 10000 \\ + 1234 \\ \hline 11234 \end{array}$$

Physical address: \$11234

b)

Base Address: 0100 → shifted by 4 bits → 01000

Offset address: ABCD

$$\begin{array}{r} 01000 \\ + \quad ABCD \\ \hline 0BB CD \end{array}$$

Physical Address: \$0BBCD

c)

Base Address: A200 → shifted by 4 bits → A2000

Offset address: 12CF

$$\begin{array}{r} A2000 \\ + \quad 12CF \\ \hline A32CF \end{array}$$

Physical Address: \$A32CF**Question 12**

12-Find the unknown value for each of the following physical addresses?

a) A000 : ? = A0123

b) ? : 14DA = 235DA

c) D765 : ? = DABCD

a)

Physical Address: A0123

Base Address: A000 → shifted by 4 bits → A0000

Offset Address = physical address - base address

$$\begin{array}{r} A0123 \\ - A0000 \\ \hline 00123 \end{array} \quad \text{but only 16 bits are used for offset address.}$$

Offset Address: **\$0123**

b)

Offset address: 14DA

Physical Address: 235DA

Base address = physical address – offset address

$$\begin{array}{r} 235DA \\ - 14DA \\ \hline 22100 \end{array}$$

but, this is the shifted base address. So we shift by 4 bits to the right.

Base Address: \$2210

c)

Physical Address: DABCO

Base Address: D765 → shifted by 4 bits → D7650

Offset Address = physical address – base address

$$\begin{array}{r} DABCO \\ - D7650 \\ \hline 03570 \end{array}$$

Offset Address: \$3570

Addressing Mode Questions

Question 13

13-In the following instructions identify the addressing mode used for the source and destination operand:

- a) MOV AL, BL
- b) MOV AX, 0FFH
- c) MOV [DI], AX
- d) MOV DI, [SI]
- e) MOV [BX]+ 0400H, CX

a)

Source: register mode

Destination: register mode

b)

Source: immediate

Destination: register mode

c)

Source: register mode

Destination: indexed

d)

Source: indexed mode

Destination: register mode

e)

Source: register mode

Destination: based mode

Question 14

14-Compute the **physical address** for the specified operand in each of the instructions below.

Assume the register contents are as follows:

(CS) = 0A00 H, (DS) = 0B00 H, (SI) = 0100 H, (DI) = 0200 H, (BX)=0300 H

- a) Destination operand of **MOV [DI], AX**
- b) Source operand of instruction **MOV DI, [SI]**
- c) Destination operand of the instruction in **MOV [BX]+ 0400H, CX**

a)

Base Address is DS: \$0B00 → shifted by 4 bits → \$0B000

Offset Address: \$0200

$$\begin{array}{r} 0B000 \\ + 0200 \\ \hline 0B200 \end{array}$$

Physical Address: \$0B200

b)

Base Address is DS: \$0B00 → shifted by 4 bits → \$0B000

Offset Address: \$0100

$$\begin{array}{r} 0B000 \\ + 0100 \\ \hline 0B100 \end{array}$$

Physical Address: \$0B100

c)

Base Address is DS: \$0B00 → shifted by 4 bits → \$0B000

Offset: \$0300 + \$0400 = \$0700

$$\begin{array}{r} 0B000 \\ + 0700 \\ \hline 0B700 \end{array}$$

Physical Address: \$0B700