

## COEN 311 Section W (Computer Organization and Software)

### Assignment 2

Due Friday October 6, 2023

**Note: Please submit only one PDF file through Moodle.**

In this assignment we want to design and measure the performance of a new processor (CPU) with 16 general purpose Registers (R0, ..., R15), 16-bit data bus and 16-bit address bus.

Note: Memory is by default byte organized.

#### Question 1)

Draw the internal organization of this CPU by showing the widths of all registers as well as all external and internal buses. Also show the byte organized memory and its interface to the CPU.

#### Question 2)

Write an assembly program to evaluate the following expression for this CPU. Ignore the remainder part of the division process and assume the multiplication result is 16 bit instead of 32 bit.

$$x = ((a + b) / (a + c)) * (100 * a)$$

The instruction set of this processor consists of the following instructions:

```
ADD  Ri, Rj, Rk    ; add Rj to Rk and put result in Ri
MUL  Ri, Rj, Rk    ; multiply Rj by Rk and put result in Ri
DIV  Ri, Rj, Rk    ; divide Rj by Rk and put result in Ri
MOVE Ri, #100      ; move constant value #100 in Ri
LOAD Ri, M[X]      ; load (copy) content of Memory at address
                   ; X into Ri
STORE M[X], Ri     ; store (copy) Ri into Memory location at
                   ; address X
```

Note that in the equation above  $a = M[A]$ . It represents content of memory location at address A. Same applies for B, C, X.

#### Question 3)

How many bits (in binary) would be required to encode instructions for this processor? Explain how.

#### Question 4)

Using encoding bits from Question 3) above, provide possible binary encoding for the following instructions:

- a) ADD R5, R1, R2
- b) MOVE R4, #100
- c) LOAD R3, M[C] (where C is memory address 2004)

**Question 5)**

Provide micro-instructions in the form of detailed flowchart for the execution of the instructions in Question 4).

- a) ADD R5, R1, R2
- b) MOVE R4, #100
- c) LOAD R3, M[C] (where C is memory address 2004)

**Question 6)**

Assuming an execution on a 2 GHz CPU, where every step requires a number of clock cycles (cc) as shown below, calculate the execution time (in ns) for every instruction in the instruction set as given in Question 5).

Internal Register Transfers	1 cc
PC Increment	2 cc
Decoding	1 cc
Memory Access	10 cc
Addition	3 cc
Multiplication	5 cc
Division	5 cc