Concordia University

Lab 4

Clocked Processes and registers in VHDL

COEN 313

Lab Section: FK-X

Digital System Design II

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I certify that this submission is my original work and meets the Faculty’s Expectations of Originality

# Objective:

This laboratory session focuses on enhancing the understanding and practical application of clocked processes and registers using VHDL (VHSIC Hardware Description Language). The lab involves designing a system comprising four 4-bit registers, which collectively function as a shift register file. These registers are interconnected in a way that allows the storage and shifting of data values with each clock cycle. Additionally, the lab introduces a combinational logic block that determines the maximum and minimum values from the shift registers. Output registers are then used to store and display these values, providing real-time insights into the workings of the digital system.

# Procedure (Methods):

1. **Design VHDL component:**
   1. **Shift Register Design:**

A register component to store the value pass into our system per cloak signal. It take an input, a cloak and reset signal and return its current value. They are initialised to “1000” on reset signals.

* 1. **Output Registers Implementation:**

A register component to store the value of the biggest or smallest register that is pass into our system per cloak signal. It take an input, a cloak and load signal and return its current value. They are initialised to “1000” on reset signals and change based on the next.

* 1. **Selection Multiplexer implementation:**

A MUX component to select and display the value of any shift register that is in our system. It takes an input, a selection signal and 4 4-bits registers and return the 4-bit registers value that correspond to the selection .

1. **Design component logic**:
   1. **Use of Combinational Processes:**

This will direct the updating process of our min and max output register to make sure that they display the biggest and smallest entered registers.

* 1. **Shifting value on cloak signal:**

This will direct the shifting register to take in an new value on each clock signal.

* 1. **Mux shift register and selector:**

This will adjust our mux to display any value displayed by our selection signal.

1. **Simulation and Verification:**
   1. **Modelsim Simulation:**

Simulate the entire design using the Modelsim simulator. Pass multiple values to the registers and look for the output.

1. **Synthesis and FPGA Programming:**
   1. **Synthesis with Xilinx Vivado:**

Synthesize the VHDL code using Xilinx Vivado. Pay attention to the synthesis reports and ensure that the logic is implemented as intended.

* 1. **RTL Schematic Diagram:**

Obtain the RTL schematic diagram from the synthesis and implementation tool to visualize the synthesized circuit.

1. **FPGA Board Programming and Demonstration:**
   1. **Programming the FPGA Board:**

Program the Nexys A7 FPGA board using Xilinx Vivado with the synthesized code.

* 1. **Demonstration:**

Demonstrate the operation of the design by downloading the synthesized code to the FPGA demonstration board. Use input switches for the entity ports and LEDs for output visualization.

# Result:

We ran a simulation for my code and here was the resulting wave:



We synthesise and implemented the code and here was the resulting schematic diagram

This diagram represents the implementation of my VHDL code. A set of more detailed diagram is available in the appendices section for each component.

## Questions:

1. To which signals should a clocked process be sensitive to if the register is to have a synchronous reset?

* The process should only be sensitive to the clock signal, and the reset logic should be checked inside the clock edge detection condition. Here is an example of my code reimplemented.

process(clk)

begin

if rising\_edge(clk) then

if reset = '1' then

reg\_out <= "1000";

else

reg\_out <= din;

end if;

end if;

end process;

1. What will happen if the following VHDL code is simulated?

library IEEE;  
use IEEE.std\_logic\_1164.all;  
use IEEE.std\_logic\_unsigned.all;

entity registers is  
port(

din1, din2 : in std\_logic\_vector(3 downto 0);  
 reset : in std\_logic;  
 clk : in std\_logic;  
 mick,keith : out std\_logic\_vector(3 downto 0)

);

end registers ;

architecture rtl of registers is

begin

process(clk, reset)  
 begin  
 if reset = ’1’ then  
 mick <= "0000";  
 keith <= "0000";  
 elsif clk’event and clk = ’1’ then  
 mick <= din1;  
 end if;  
 end process;

process(clk, reset)  
 begin  
 if reset = ’1’ then  
 mick <= "0000";  
 keith <= "0000";  
 elsif clk’event and clk = ’1’ then  
 keith <= din2;  
 end if;  
 end process;  
end rtl;

* The code implements the same process twice with a slight nuance. The processes are meant to reset the values of mick and keith to “0000” twice and individually pass new values to mick and keith when the clock value change. The main issue is that there seems to be no difference in the reset process which might lead to an unexpected value.

# Conclusions:

The laboratory successfully culminated in a comprehensive learning experience for students in the realm of digital system design using VHDL. The primary objective of designing a shift register file integrated with max/min logic was achieved with a hands-on approach. The process began with the theoretical design of the system, followed by practical implementation using VHDL. Students gained valuable insights into how shift registers operate and how data is processed in a digital system. The skills and concepts learned here will be fundamental to their future endeavors in the field of digital electronics and circuit design.

# Appendices:

## Here is my detailed schematic:







## Here is my main VHDL code:

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_unsigned.all;

entity registers\_min\_max is

port( din : in std\_logic\_vector(3 downto 0);

reset : in std\_logic;

clk : in std\_logic;

sel : in std\_logic\_vector(1 downto 0);

max\_out : out std\_logic\_vector(3 downto 0);

min\_out : out std\_logic\_vector(3 downto 0);

reg\_out : out std\_logic\_vector(3 downto 0)

);

end registers\_min\_max ;

architecture true\_outputs of registers\_min\_max is

component registers is

port( din : in std\_logic\_vector(3 downto 0);

reset : in std\_logic;

clk : in std\_logic;

reg\_out : out std\_logic\_vector(3 downto 0)

);

end component;

component fbMUX is

port( reg3 : in std\_logic\_vector(3 downto 0);

reg2 : in std\_logic\_vector(3 downto 0);

reg1 : in std\_logic\_vector(3 downto 0);

reg0 : in std\_logic\_vector(3 downto 0);

sel : in std\_logic\_vector(1 downto 0);

muxout : out std\_logic\_vector(3 downto 0)

);

end component;

component minMaxComb is

port( reg3 : in std\_logic\_vector(3 downto 0);

reg2 : in std\_logic\_vector(3 downto 0);

reg1 : in std\_logic\_vector(3 downto 0);

reg0 : in std\_logic\_vector(3 downto 0);

minout : out std\_logic\_vector(3 downto 0);

maxout : out std\_logic\_vector(3 downto 0)

);

end component;

component max\_reg is

port( din : in std\_logic\_vector(3 downto 0);

clk : in std\_logic;

maxout : out std\_logic\_vector(3 downto 0)

);

end component;

component min\_reg is

port( din : in std\_logic\_vector(3 downto 0);

clk : in std\_logic;

minout : out std\_logic\_vector(3 downto 0)

);

end component;

signal r0, r1, r2, r3, min\_comb, max\_comb : std\_logic\_vector(3 downto 0);

for all : registers use entity work.registers(true\_outputs);

for mux : fbMUX use entity work.fbMUX(true\_outputs);

for Max\_led : max\_reg use entity work.max\_reg(true\_outputs);

for Min\_led : min\_reg use entity work.min\_reg(true\_outputs);

for Max\_Min\_comb\_logic : minMaxComb use entity work.minMaxComb(true\_outputs);

begin

register0 : registers port map(din => din, reset => reset , clk => clk ,reg\_out => r0);

register1 : registers port map(din => r0, reset => reset , clk => clk ,reg\_out => r1);

register2 : registers port map(din => r1, reset => reset , clk => clk ,reg\_out => r2);

register3 : registers port map(din => r2, reset => reset , clk => clk ,reg\_out => r3);

mux : fbMUX port map(reg3 => r3, reg2 => r2, reg1 => r1, reg0 => r0, sel => sel, muxout => reg\_out);

Max\_Min\_comb\_logic : minMaxComb port map(reg3 => r3, reg2 => r2, reg1 => r1, reg0 => r0, minout => min\_comb, maxout => max\_comb);

Max\_led : max\_reg port map(din => max\_comb, clk => clk, maxout => max\_out);

Min\_led : min\_reg port map(din => min\_comb, clk => clk, minout => min\_out);

end architecture;

## Here is my register.vhd code :

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_unsigned.all;

entity registers is

port( din : in std\_logic\_vector(3 downto 0);

reset : in std\_logic;

clk : in std\_logic;

reg\_out : out std\_logic\_vector(3 downto 0)

);

end registers ;

architecture true\_outputs of registers is

begin

process(clk, reset)

begin

if reset = '1' then

reg\_out <= "1000";

elsif rising\_edge(clk) then

reg\_out <= din;

end if;

end process;

end true\_outputs;

## Here is my minMaxComb.vhd code :

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_unsigned.all;

entity minMaxComb is

port( reg3 : in std\_logic\_vector(3 downto 0);

reg2 : in std\_logic\_vector(3 downto 0);

reg1 : in std\_logic\_vector(3 downto 0);

reg0 : in std\_logic\_vector(3 downto 0);

minout : out std\_logic\_vector(3 downto 0);

maxout : out std\_logic\_vector(3 downto 0)

);

end minMaxComb;

architecture true\_outputs of minMaxComb is

begin

minout <= reg0 when reg0 < reg1 and reg0 < reg2 and reg0 < reg3 else

reg1 when reg1 < reg0 and reg1 < reg2 and reg1 < reg3 else

reg2 when reg2 < reg0 and reg2 < reg1 and reg2 < reg3 else

reg3;

maxout <= reg0 when reg0 > reg1 and reg0 > reg2 and reg0 > reg3 else

reg1 when reg1 > reg0 and reg1 > reg2 and reg1 > reg3 else

reg2 when reg2 > reg0 and reg2 > reg1 and reg2 > reg3 else

reg3;

end true\_outputs;

## Here is my min\_reg.vhd code :

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_unsigned.all;

use IEEE.numeric\_std.all;

entity min\_reg is

port( din : in std\_logic\_vector(3 downto 0);

clk : in std\_logic;

minout : out std\_logic\_vector(3 downto 0)

);

end min\_reg;

architecture true\_outputs of min\_reg is

signal minout\_reg : std\_logic\_vector(3 downto 0):="1000";

begin

process(clk)

begin

if rising\_edge(clk) then

if unsigned(din) < unsigned(minout\_reg) then

minout\_reg <= din;

end if;

end if;

end process;

minout <=minout\_reg;

end true\_outputs;

## Here is my max\_reg.vhd code :

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_unsigned.all;

use IEEE.numeric\_std.all;

entity max\_reg is

port( din : in std\_logic\_vector(3 downto 0);

clk : in std\_logic;

maxout : out std\_logic\_vector(3 downto 0)

);

end max\_reg;

architecture true\_outputs of max\_reg is

signal maxout\_reg : std\_logic\_vector(3 downto 0):="1000";

begin

process(clk)

begin

if rising\_edge(clk) then

if unsigned(din) > unsigned(maxout\_reg) then

maxout\_reg <= din;

end if;

end if;

end process;

maxout <= maxout\_reg;

end true\_outputs;

## Here is my fbMUX.vhd code :

library IEEE;

use IEEE.std\_logic\_1164.all;

use IEEE.std\_logic\_unsigned.all;

entity fbMUX is

port( reg3 : in std\_logic\_vector(3 downto 0);

reg2 : in std\_logic\_vector(3 downto 0);

reg1 : in std\_logic\_vector(3 downto 0);

reg0 : in std\_logic\_vector(3 downto 0);

sel : in std\_logic\_vector(1 downto 0);

muxout : out std\_logic\_vector(3 downto 0)

);

end fbMUX;

architecture true\_outputs of fbMUX is

begin

process (reg3, reg2, reg1, reg0, sel)

begin

case sel is

when "00" => muxout <= reg0;

when "01" => muxout <= reg1;

when "10" => muxout <= reg2;

when "11" => muxout <= reg3;

when others => muxout <= "0000";

end case;

end process;

end true\_outputs;

## Here is my vivado log :

\*\*\* Running vivado

with args -log registers\_min\_max.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source registers\_min\_max.tcl -notrace

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source registers\_min\_max.tcl -notrace

Command: link\_design -top registers\_min\_max -part xc7a100tcsg324-1

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 8 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/constrs\_1/imports/lab4/constraint\_lab4.xdc]

Finished Parsing XDC File [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/constrs\_1/imports/lab4/constraint\_lab4.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link\_design completed successfully

link\_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:31 . Memory (MB): peak = 1652.371 ; gain = 344.242 ; free physical = 8780 ; free virtual = 20993

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command opt\_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1742.398 ; gain = 90.027 ; free physical = 8771 ; free virtual = 20984

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: 110f4107b

Time (s): cpu = 00:00:09 ; elapsed = 00:00:36 . Memory (MB): peak = 2196.898 ; gain = 454.500 ; free physical = 8355 ; free virtual = 20568

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 110f4107b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 110f4107b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 110f4107b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 110f4107b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 110f4107b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 110f4107b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

Ending Logic Optimization Task | Checksum: 110f4107b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 110f4107b

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 110f4107b

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2196.898 ; gain = 0.000 ; free physical = 8412 ; free virtual = 20625

INFO: [Common 17-83] Releasing license: Implementation

23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:11 ; elapsed = 00:00:39 . Memory (MB): peak = 2196.898 ; gain = 544.527 ; free physical = 8412 ; free virtual = 20625

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2228.914 ; gain = 0.004 ; free physical = 8409 ; free virtual = 20622

INFO: [Common 17-1381] The checkpoint '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/impl\_1/registers\_min\_max\_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file registers\_min\_max\_drc\_opted.rpt -pb registers\_min\_max\_drc\_opted.pb -rpx registers\_min\_max\_drc\_opted.rpx

Command: report\_drc -file registers\_min\_max\_drc\_opted.rpt -pb registers\_min\_max\_drc\_opted.pb -rpx registers\_min\_max\_drc\_opted.rpx

INFO: [IP\_Flow 19-234] Refreshing IP repositories

INFO: [IP\_Flow 19-1704] No user IP repositories specified

INFO: [IP\_Flow 19-2313] Loaded Vivado IP repository '/CMC/tools/xilinx/Vivado\_2018.2/Vivado/2018.2/data/ip'.

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/impl\_1/registers\_min\_max\_drc\_opted.rpt.

report\_drc completed successfully

report\_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 2316.957 ; gain = 88.035 ; free physical = 8352 ; free virtual = 20565

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8350 ; free virtual = 20564

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: bdc4c663

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.02 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8350 ; free virtual = 20563

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8350 ; free virtual = 20563

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

WARNING: [Place 30-574] Poor placement for routing between an IO pin and BUFG. This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y58

clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: befa488c

Time (s): cpu = 00:00:00.89 ; elapsed = 00:00:00.42 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8349 ; free virtual = 20562

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: d3527899

Time (s): cpu = 00:00:00.95 ; elapsed = 00:00:00.44 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8349 ; free virtual = 20562

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: d3527899

Time (s): cpu = 00:00:00.95 ; elapsed = 00:00:00.45 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8349 ; free virtual = 20562

Phase 1 Placer Initialization | Checksum: d3527899

Time (s): cpu = 00:00:00.95 ; elapsed = 00:00:00.45 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8349 ; free virtual = 20562

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: d3527899

Time (s): cpu = 00:00:00.98 ; elapsed = 00:00:00.46 . Memory (MB): peak = 2316.957 ; gain = 0.000 ; free physical = 8348 ; free virtual = 20561

WARNING: [Place 46-29] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: ed4dae5f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8328 ; free virtual = 20541

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: ed4dae5f

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.81 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8328 ; free virtual = 20541

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 159e0b2d5

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.83 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8328 ; free virtual = 20541

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: e26a1a8a

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.84 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8328 ; free virtual = 20541

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: e26a1a8a

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.84 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8328 ; free virtual = 20541

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.94 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8323 ; free virtual = 20537

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.95 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8323 ; free virtual = 20537

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.95 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8323 ; free virtual = 20537

Phase 3 Detail Placement | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.95 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8323 ; free virtual = 20537

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.95 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8323 ; free virtual = 20537

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.96 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8325 ; free virtual = 20538

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.96 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8325 ; free virtual = 20538

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.96 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8325 ; free virtual = 20538

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 1fe3d50e1

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.96 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8325 ; free virtual = 20538

Ending Placer Task | Checksum: 17d34acbb

Time (s): cpu = 00:00:03 ; elapsed = 00:00:00.96 . Memory (MB): peak = 2370.977 ; gain = 54.020 ; free physical = 8342 ; free virtual = 20555

INFO: [Common 17-83] Releasing license: Implementation

41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.11 . Memory (MB): peak = 2370.977 ; gain = 0.000 ; free physical = 8341 ; free virtual = 20555

INFO: [Common 17-1381] The checkpoint '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/impl\_1/registers\_min\_max\_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_io -file registers\_min\_max\_io\_placed.rpt

report\_io: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.10 . Memory (MB): peak = 2370.977 ; gain = 0.000 ; free physical = 8336 ; free virtual = 20550

INFO: [runtcl-4] Executing : report\_utilization -file registers\_min\_max\_utilization\_placed.rpt -pb registers\_min\_max\_utilization\_placed.pb

report\_utilization: Time (s): cpu = 00:00:00.03 ; elapsed = 00:00:00.06 . Memory (MB): peak = 2370.977 ; gain = 0.000 ; free physical = 8343 ; free virtual = 20557

INFO: [runtcl-4] Executing : report\_control\_sets -verbose -file registers\_min\_max\_control\_sets\_placed.rpt

report\_control\_sets: Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.04 . Memory (MB): peak = 2370.977 ; gain = 0.000 ; free physical = 8343 ; free virtual = 20556

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command route\_design

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing between an IO pin and BUFG.

Resolution: Poor placement of an IO pin and a BUFG has resulted in the router using a non-dedicated path between the two. There are several things that could trigger this DRC, each of which can cause unpredictable clock insertion delays that result in poor timing. This DRC could be caused by any of the following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the BUFG has not been placed in the same half of the device or SLR as the CCIO-pin (c) a single ended clock has been placed on the N-Side of a differential pair CCIO-pin.

This is normally an ERROR but the CLOCK\_DEDICATED\_ROUTE constraint is set to FALSE allowing your design to continue. The use of this override is highly discouraged as it may lead to very poor timing results. It is recommended that this error condition be corrected in the design.

clk\_IBUF\_inst (IBUF.O) is locked to IOB\_X0Y58

clk\_IBUF\_BUFG\_inst (BUFG.I) is provisionally placed by clockplacer on BUFGCTRL\_X0Y0

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 8 CPUs

Checksum: PlaceDB: e55f0f0b ConstDB: 0 ShapeSum: 97d59db0 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 1087c9a54

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2402.973 ; gain = 31.996 ; free physical = 8190 ; free virtual = 20404

Post Restoration Checksum: NetGraph: 1c4f80cc NumContArr: ec2d1988 Constraints: 0 Timing: 0

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: 1087c9a54

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2408.961 ; gain = 37.984 ; free physical = 8159 ; free virtual = 20372

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: 1087c9a54

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2408.961 ; gain = 37.984 ; free physical = 8159 ; free virtual = 20372

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: 63524c82

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8149 ; free virtual = 20363

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 12cf687b8

Time (s): cpu = 00:00:16 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8149 ; free virtual = 20363

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 5

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8151 ; free virtual = 20364

Phase 4 Rip-up And Reroute | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8151 ; free virtual = 20364

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8151 ; free virtual = 20364

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8151 ; free virtual = 20364

Phase 6 Post Hold Fix | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8151 ; free virtual = 20364

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.0164077 %

Global Horizontal Routing Utilization = 0.0137113 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 19.8198%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 16.2162%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 13.2353%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 17.6471%, No Congested Regions.

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Reporting congestion hotspots

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Direction: North

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Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: South

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: East

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Direction: West

----------------

Congested clusters found at Level 0

Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2418.227 ; gain = 47.250 ; free physical = 8151 ; free virtual = 20364

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: bfec3cd2

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2420.227 ; gain = 49.250 ; free physical = 8150 ; free virtual = 20363

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 11c2e0e53

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2420.227 ; gain = 49.250 ; free physical = 8150 ; free virtual = 20363

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:17 ; elapsed = 00:00:13 . Memory (MB): peak = 2420.227 ; gain = 49.250 ; free physical = 8183 ; free virtual = 20397

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:18 ; elapsed = 00:00:16 . Memory (MB): peak = 2420.230 ; gain = 49.254 ; free physical = 8183 ; free virtual = 20397

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00.15 ; elapsed = 00:00:00.15 . Memory (MB): peak = 2420.230 ; gain = 0.000 ; free physical = 8184 ; free virtual = 20399

INFO: [Common 17-1381] The checkpoint '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/impl\_1/registers\_min\_max\_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_drc -file registers\_min\_max\_drc\_routed.rpt -pb registers\_min\_max\_drc\_routed.pb -rpx registers\_min\_max\_drc\_routed.rpx

Command: report\_drc -file registers\_min\_max\_drc\_routed.rpt -pb registers\_min\_max\_drc\_routed.pb -rpx registers\_min\_max\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 8 threads

INFO: [Coretcl 2-168] The results of DRC are in file /nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/impl\_1/registers\_min\_max\_drc\_routed.rpt.

report\_drc completed successfully

INFO: [runtcl-4] Executing : report\_methodology -file registers\_min\_max\_methodology\_drc\_routed.rpt -pb registers\_min\_max\_methodology\_drc\_routed.pb -rpx registers\_min\_max\_methodology\_drc\_routed.rpx

Command: report\_methodology -file registers\_min\_max\_methodology\_drc\_routed.rpt -pb registers\_min\_max\_methodology\_drc\_routed.pb -rpx registers\_min\_max\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 8 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file /nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/impl\_1/registers\_min\_max\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

INFO: [runtcl-4] Executing : report\_power -file registers\_min\_max\_power\_routed.rpt -pb registers\_min\_max\_power\_summary\_routed.pb -rpx registers\_min\_max\_power\_routed.rpx

Command: report\_power -file registers\_min\_max\_power\_routed.rpt -pb registers\_min\_max\_power\_summary\_routed.pb -rpx registers\_min\_max\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [runtcl-4] Executing : report\_route\_status -file registers\_min\_max\_route\_status.rpt -pb registers\_min\_max\_route\_status.pb

INFO: [runtcl-4] Executing : report\_timing\_summary -max\_paths 10 -file registers\_min\_max\_timing\_summary\_routed.rpt -pb registers\_min\_max\_timing\_summary\_routed.pb -rpx registers\_min\_max\_timing\_summary\_routed.rpx -warn\_on\_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

INFO: [runtcl-4] Executing : report\_incremental\_reuse -file registers\_min\_max\_incremental\_reuse\_routed.rpt

INFO: [Vivado\_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

INFO: [runtcl-4] Executing : report\_clock\_utilization -file registers\_min\_max\_clock\_utilization\_routed.rpt

INFO: [runtcl-4] Executing : report\_bus\_skew -warn\_on\_violation -file registers\_min\_max\_bus\_skew\_routed.rpt -pb registers\_min\_max\_bus\_skew\_routed.pb -rpx registers\_min\_max\_bus\_skew\_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max, Timing Stage: Requireds.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

Command: write\_bitstream -force registers\_min\_max.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t'

Running DRC as a precondition to command write\_bitstream

INFO: [DRC 23-27] Running DRC with 8 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Designutils 20-2272] Running write\_bitstream with 8 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./registers\_min\_max.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Common 17-83] Releasing license: Implementation

83 Infos, 6 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 2764.145 ; gain = 239.840 ; free physical = 8169 ; free virtual = 20387

INFO: [Common 17-206] Exiting Vivado at Fri Nov 17 16:41:11 2023...

\*\*\* Running vivado

with args -log registers\_min\_max.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source registers\_min\_max.tcl

\*\*\*\*\*\* Vivado v2018.2 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source registers\_min\_max.tcl -notrace

Command: synth\_design -top registers\_min\_max -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 31126

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Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:03 . Memory (MB): peak = 1401.582 ; gain = 85.805 ; free physical = 8960 ; free virtual = 21173

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INFO: [Synth 8-638] synthesizing module 'registers\_min\_max' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:16]

INFO: [Synth 8-3491] module 'registers' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/registers.vhd:5' bound to instance 'register0' of component 'registers' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:70]

INFO: [Synth 8-638] synthesizing module 'registers' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/registers.vhd:13]

INFO: [Synth 8-256] done synthesizing module 'registers' (1#1) [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/registers.vhd:13]

INFO: [Synth 8-3491] module 'registers' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/registers.vhd:5' bound to instance 'register1' of component 'registers' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:71]

INFO: [Synth 8-3491] module 'registers' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/registers.vhd:5' bound to instance 'register2' of component 'registers' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:72]

INFO: [Synth 8-3491] module 'registers' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/registers.vhd:5' bound to instance 'register3' of component 'registers' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:73]

INFO: [Synth 8-3491] module 'fbMUX' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/fbMUX.vhd:5' bound to instance 'mux' of component 'fbMUX' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:75]

INFO: [Synth 8-638] synthesizing module 'fbMUX' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/fbMUX.vhd:15]

INFO: [Synth 8-226] default block is never used [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/fbMUX.vhd:19]

INFO: [Synth 8-256] done synthesizing module 'fbMUX' (2#1) [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/fbMUX.vhd:15]

INFO: [Synth 8-3491] module 'minMaxComb' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/minMaxComb.vhd:5' bound to instance 'Max\_Min\_comb\_logic' of component 'minMaxComb' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:77]

INFO: [Synth 8-638] synthesizing module 'minMaxComb' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/minMaxComb.vhd:15]

INFO: [Synth 8-256] done synthesizing module 'minMaxComb' (3#1) [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/minMaxComb.vhd:15]

INFO: [Synth 8-3491] module 'max\_reg' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/max\_reg.vhd:6' bound to instance 'Max\_led' of component 'max\_reg' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:79]

INFO: [Synth 8-638] synthesizing module 'max\_reg' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/max\_reg.vhd:13]

INFO: [Synth 8-256] done synthesizing module 'max\_reg' (4#1) [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/max\_reg.vhd:13]

INFO: [Synth 8-3491] module 'min\_reg' declared at '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/min\_reg.vhd:6' bound to instance 'Min\_led' of component 'min\_reg' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:80]

INFO: [Synth 8-638] synthesizing module 'min\_reg' [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/min\_reg.vhd:13]

INFO: [Synth 8-256] done synthesizing module 'min\_reg' (5#1) [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/min\_reg.vhd:13]

INFO: [Synth 8-256] done synthesizing module 'registers\_min\_max' (6#1) [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/sources\_1/imports/lab4/register\_min\_max.vhd:16]

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Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.223 ; gain = 130.445 ; free physical = 8955 ; free virtual = 21168

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.223 ; gain = 130.445 ; free physical = 8954 ; free virtual = 21168

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.223 ; gain = 130.445 ; free physical = 8954 ; free virtual = 21168

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INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/constrs\_1/imports/lab4/constraint\_lab4.xdc]

Finished Parsing XDC File [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/constrs\_1/imports/lab4/constraint\_lab4.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.srcs/constrs\_1/imports/lab4/constraint\_lab4.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/registers\_min\_max\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/registers\_min\_max\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 1833.508 ; gain = 0.000 ; free physical = 8658 ; free virtual = 20871

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Finished Constraint Validation : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8764 ; free virtual = 20977

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8764 ; free virtual = 20977

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8766 ; free virtual = 20979

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8757 ; free virtual = 20970

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Registers :

4 Bit Registers := 6

+---Muxes :

4 Input 4 Bit Muxes := 1

2 Input 4 Bit Muxes := 6

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Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module registers

Detailed RTL Component Info :

+---Registers :

4 Bit Registers := 1

Module fbMUX

Detailed RTL Component Info :

+---Muxes :

4 Input 4 Bit Muxes := 1

Module minMaxComb

Detailed RTL Component Info :

+---Muxes :

2 Input 4 Bit Muxes := 6

Module max\_reg

Detailed RTL Component Info :

+---Registers :

4 Bit Registers := 1

Module min\_reg

Detailed RTL Component Info :

+---Registers :

4 Bit Registers := 1

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:10 ; elapsed = 00:00:38 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8744 ; free virtual = 20959

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8640 ; free virtual = 20855

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8640 ; free virtual = 20855

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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---------------------------------------------------------------------------------

Finished Final Netlist Cleanup

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Finished IO Insertion : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-----+------+

| |Cell |Count |

+------+-----+------+

|1 |BUFG | 1|

|2 |LUT3 | 6|

|3 |LUT4 | 6|

|4 |LUT5 | 14|

|5 |LUT6 | 22|

|6 |FDCE | 12|

|7 |FDPE | 4|

|8 |FDRE | 8|

|9 |IBUF | 8|

|10 |OBUF | 12|

+------+-----+------+

Report Instance Areas:

+------+------------+------------+------+

| |Instance |Module |Cells |

+------+------------+------------+------+

|1 |top | | 93|

|2 | Max\_led |max\_reg | 4|

|3 | Min\_led |min\_reg | 6|

|4 | register0 |registers | 17|

|5 | register1 |registers\_0 | 16|

|6 | register2 |registers\_1 | 14|

|7 | register3 |registers\_2 | 15|

+------+------------+------------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8638 ; free virtual = 20853

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:18 . Memory (MB): peak = 1833.508 ; gain = 130.445 ; free physical = 8693 ; free virtual = 20908

Synthesis Optimization Complete : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1833.508 ; gain = 517.730 ; free physical = 8703 ; free virtual = 20918

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 8 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

33 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1833.512 ; gain = 530.383 ; free physical = 8690 ; free virtual = 20904

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint '/nfs/home/p/p\_thibe/COEN313/Modelsim/Code/lab4/Lab\_4.1/Lab\_4.1.runs/synth\_1/registers\_min\_max.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file registers\_min\_max\_utilization\_synth.rpt -pb registers\_min\_max\_utilization\_synth.pb

report\_utilization: Time (s): cpu = 00:00:00.06 ; elapsed = 00:00:00.15 . Memory (MB): peak = 1857.531 ; gain = 0.000 ; free physical = 8691 ; free virtual = 20906

INFO: [Common 17-206] Exiting Vivado at Fri Nov 17 16:39:07 2023...