Concordia University

Lab 4

Clocked Processes and registers in VHDL

COEN 313

Lab Section: FK-X

Digital System Design II

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I certify that this submission is my original work and meets the Faculty’s Expectations of Originality

# Objective:

The primary objective of this laboratory exercise is to develop system taking a 4-bit input, representing a signed integer in sign-magnitude notation, and converting it into its corresponding 4-bit two's complement representation. Through this process, students will engage in a detailed exploration of VHDL coding techniques, deepen their understanding of digital logic concepts, and acquire hands-on experience in the synthesis and simulation of digital circuits.

# Procedure (Methods):

1. **Design VHDL component:**
   1. **Shift Register Design:**

A register component to store the value pass into our system per cloak signal. It take an input, a cloak and reset signal and return its current value. They are initialised to “1000” on reset signals.

* 1. **Output Registers Implementation:**

A register component to store the value of the biggest or smallest register that is pass into our system per cloak signal. It take an input, a cloak and load signal and return its current value. They are initialised to “1000” on reset signals and change based on the next.

* 1. **Selection Multiplexer implementation:**

A MUX component to select and display the value of any shift register that is in our system. It takes an input, a selection signal and 4 4-bits registers and return the 4-bit registers value that correspond to the selection .

1. **Design component logic**:
   1. **Use of Combinational Processes:**

This will direct the updating process of our min and max output register to make sure that they display the biggest and smallest entered registers.

* 1. **Shifting value on cloak signal:**

This will direct the shifting register to take in an new value on each clock signal.

* 1. **Mux shift register and selector:**

This will adjust our mux to display any value displayed by our selection signal.

1. **Simulation and Verification:**
   1. **Modelsim Simulation:**

Simulate the entire design using the Modelsim simulator. Pass multiple values to the registers and look for the output.

1. **Synthesis and FPGA Programming:**
   1. Synthesis with Xilinx Vivado:

Synthesize the VHDL code using Xilinx Vivado. Pay attention to the synthesis reports and ensure that the logic is implemented as intended.

* 1. RTL Schematic Diagram: Obtain the RTL schematic diagram from the synthesis tool to visualize the synthesized circuit.

1. **FPGA Board Programming and Demonstration:**
   1. Programming the FPGA Board: Program the Nexys A7 FPGA board using Xilinx Vivado with the synthesized code.
   2. Demonstration: Demonstrate the operation of the design by downloading the synthesized code to the FPGA demonstration board. Use input switches for the entity ports and LEDs for output visualization.
2. **Implementation Notes:**
   1. Port Mapping: Map all the entity ports to the appropriate input switches or LEDs on the Nexys A7 FPGA board.
   2. Reset Logic: Implement an asynchronous reset for the shift register and decide on the initial values for the max\_out and min\_out registers. The shift register should reset to "1000" to facilitate effective testing of the max/min logic.

## Questions:

**1.**

# Conclusions:

# Apendices: