Concordia University

Digital Design Project

Designing a Combinational Sign-Magnitude to Two's Complement Converter

COEN 313

Digital System Design II

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I certify that this submission is my original work and meets the Faculty’s Expectations of Originality

# Abstract:

This project focuses on the design and simulation of a digital system to monitor the occupancy of a room. The system is developed using digital design principles learned throughout the semester such as VHDL programing, simulation, testing, synthesis and implementation . The core of the system is a set of photocells at the entrance and exit doors, which detect room entrance and exit and return a binary signal. A predefined maximum occupancy threshold is set at 63 and the system alerts when this threshold is reached. The system's performance is simulated and implemented and analysed in terms of FPGA resource utilization, with a detailed analysis provided in the simulation and synthesis results.

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# Introduction:

The designed system will utilise 2 photocell setup at the entrance and exit points, which triggers binary signals based on the interruption of light. The occupancy count is maintained and compared against a maximum threshold of 63 individuals. Upon reaching or exceeding this threshold, a conspicuous red indicator light is activated, signaling that the room has reached its capacity.

The project leverages the VHDL (VHSIC Hardware Description Language) for modeling the circuit and simulating it .

A diagram of a computer system

Description automatically generated

### Figure 1: Circuit conceptual diagram

The design incorporates essential digital components like Adjuster, comparator and registers to manage the occupancy data efficiently. Furthermore, a reset mechanism is included to enable the system to revert to its initial state, facilitating continuous and accurate occupancy tracking.

The simulation and synthesis predictions and results are presented in the report, providing insights into the efficiency and effectiveness of the design.

# Procedure (Methods):

## Conceptual Design of the Digital System:

* **Block Diagram Creation:**

Utilizing digital design principles, a conceptual diagram was developed. This included identifying and arranging essential components choose to count occupancy, adapt its value to room entrance and exits and control the LED state.

## VHDL Circuit Design :

* **Components design:**

The components of the block diagram was modeled using VHDL.

* **Components interactions:**

This involved writing code to simulate the desired behavior of our digital components well as the logic for occupancy tracking and threshold alert.

## Testbench Development:

* **Scenario Planning:**

Various scenarios were outlined to test the system thoroughly, including normal occupancy tracking, threshold reaching, and reset mechanism activation.

* **VHDL Testbench Writing:**

A testbench was written in VHDL to simulate these scenarios, ensuring the system's functionality under different conditions.

## Simulation and Synthesis:

* **Modelsim:**

The VHDL model was compiled and simulated using Modalism to display a wave with the testbench.

* **Verilog Data Collection:**

This step did not involve physical implementation, but focused on the software synthesis and implementation of the design.

## Analysis of Results:

* **Schematic Evaluation:**

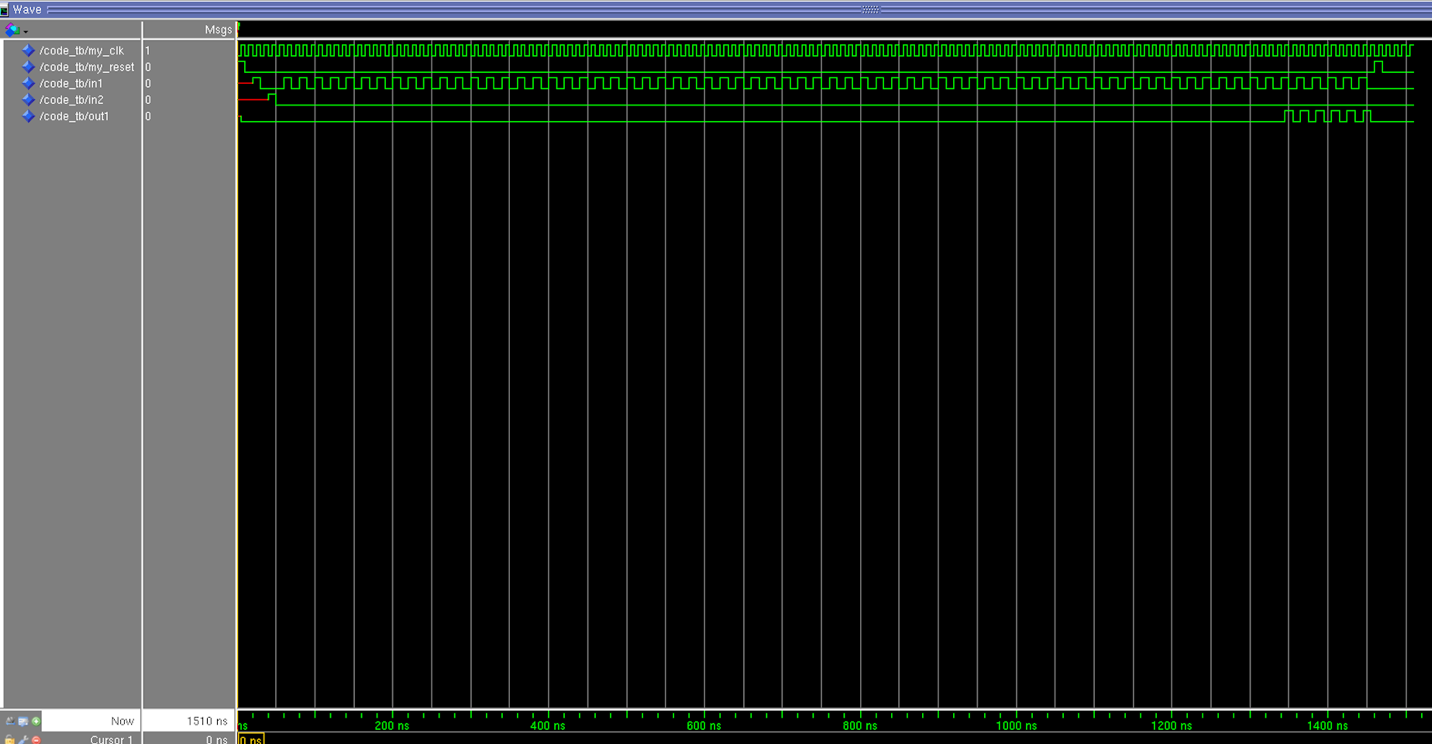
The collected schematic was analyzed to evaluate that the design was properly implemented.

* **Vivado Log File Documentation:**

All findings, including simulation and synthesis results, were documented, with the Vivado log file included in the report.

# Results :

After successfully implementing our conceptual circuit into an VHDL code, we had to write a test bench to simulate a little set of scenarios. The scenarios involved normal occupancy trackingfor regular values from 0 to 63, threshold reaching for values over 63 and the reset mechanism activation that allow to restart the tracking at any stage. Here was the simulation result.



### Figure 2: Modelsim testbench results

The 3 scenarios are tested here. We can notice that the out1 signal is activated after the in1 signal has been activated 65 times and in2 has been activated one time. This result imply that our system handles normal occupancy tracking and occupancy passed the threshold. We can also notice that after the reset signal, the out1 goes down to zero. Which imply that our light goes of since our system was reinitialised.

We also implemented our VHDL code using Verilog to verify that the proper design was implemented. Here was the implementation result.

A computer screen shot of a computer

Description automatically generated

### Figure 3: Verilog Schematic diagram

The diagram implemented correspond to the conceptual diagram and a more detailed diagram is available in the appendixes section.

# Conclusions:

In conclusion, this project successfully achieved its aim of designing a digital system for room occupancy monitoring. The methodologies applied from VHDL modeling to simulation and schematic analysis, were effective in evaluating a system functionality and design. The results from the various tests conducted validate the system's reliability and responsiveness, making it a viable solution for occupancy tracking in real-world applications.

# Appendixes:



### Figure 4: Detailed Verilog Schematic diagram