Digital System Design

Latches and Flip-Flops

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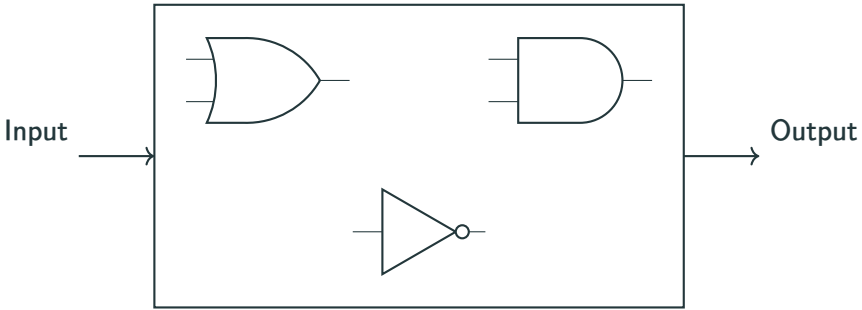
Combinational Systems

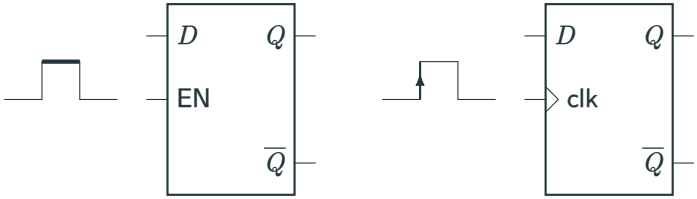
Combinational circuits are an interconnection of OR, AND, and NOT gates.

Examples of combinational systems are Encoder/Decoder, MUX/DEMUX, Adders, Multipliers, among others.



On the other side, in sequential circuits, there are two new blocks, called **latch** and **flip-flop**.

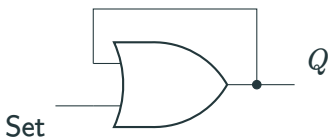
Latches are storage elements that operate with signal levels, whereas flip-flops are controlled by a clock transition.



Contents

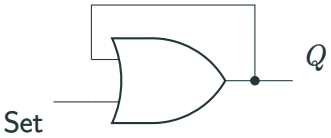
Simple Latch

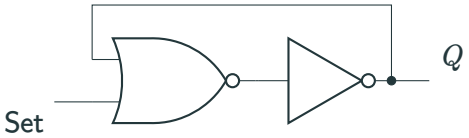
A simple latch can be designed using an OR gate with feedback.

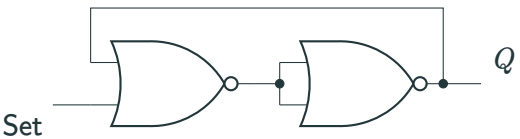


Set	Q	Q_+
0	Q	Q
1	X	1

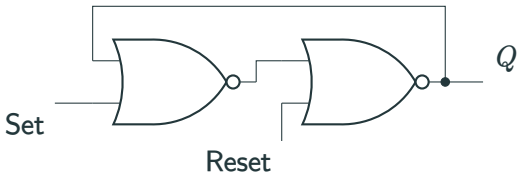
Equivalent Simple Latch

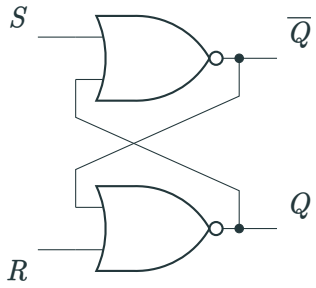






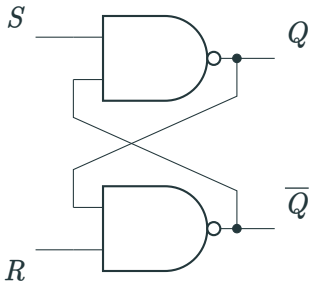
SR Latch (Improved Simple Latch)





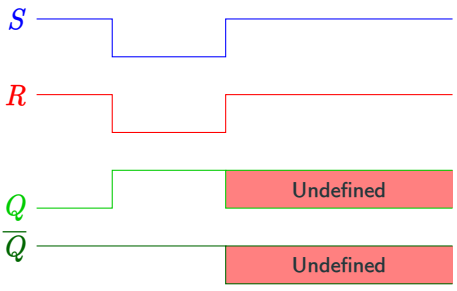
S	R	Q_+	$\overline{Q}_+$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0 (forbidden)

SR Latch with NAND Gates

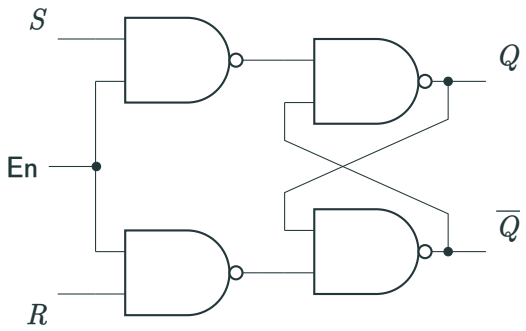


S	R	Q_+	$\overline{Q}_+$	
0	0	1	1	(forbidden)
0	1	1	0	
1	0	0	1	
1	1	Q	$\overline{Q}$	

Critical Race

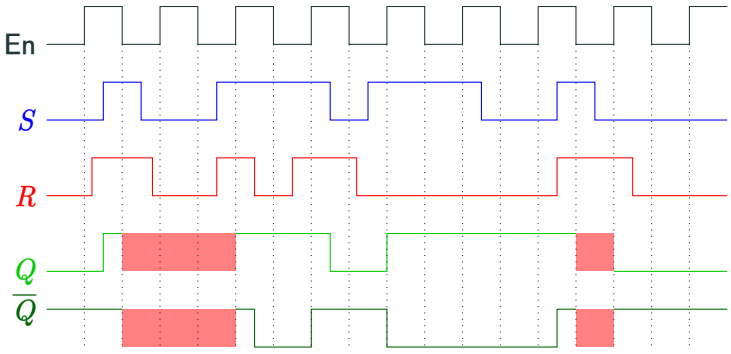


SR Latch with Control Input



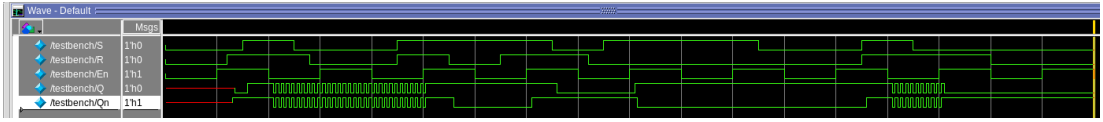
En	S	R	Q_+	$\overline{Q}_+$
0	X	X	Q	$\overline{Q}$
1	0	0	Q	$\overline{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1 (forbidden)

SR Latch with Control Input: Timing Diagram

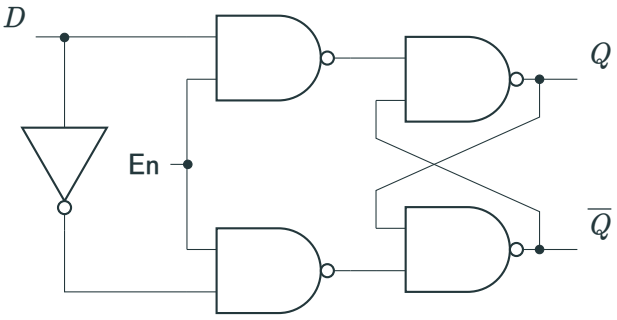


SR Latch with Control Input: Questa Simulation

In this simulation, we consider that the propagation delay t_d in NAND gates is $0.025T$, where T is the time period of the clock signal.

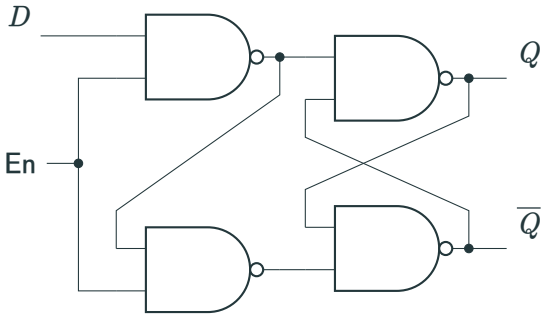


D Latch (Transparent Latch) with Control Input



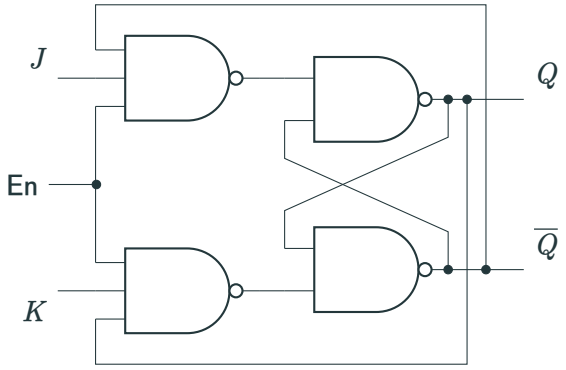
En	D	Q_+	$\overline{Q}_+$
0	X	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Improved D Latch with Control Input



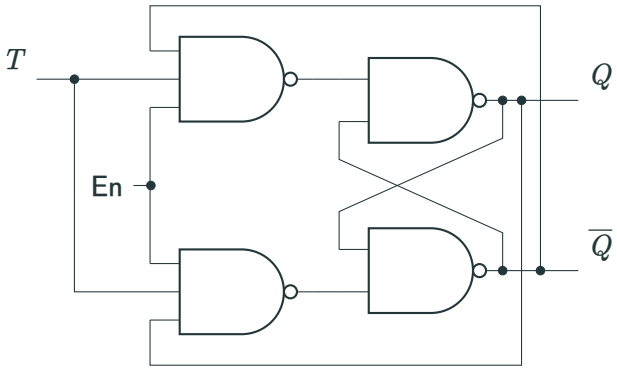
En	D	Q_+	$\overline{Q}_+$
0	X	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

JK Latch with Control Input



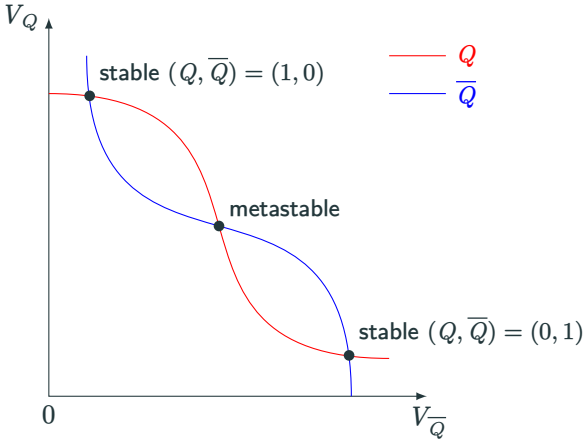
En	J	K	Q_+	$\overline{Q}_+$
0	X	X	Q	$\overline{Q}$
1	0	0	Q	$\overline{Q}$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\overline{Q}$	Q

T Latch with Control Input



En	T	Q_+	$\overline{Q}_+$
0	X	Q	$\overline{Q}$
1	0	Q	$\overline{Q}$
1	1	$\overline{Q}$	Q

Bistable Multivibrator Element



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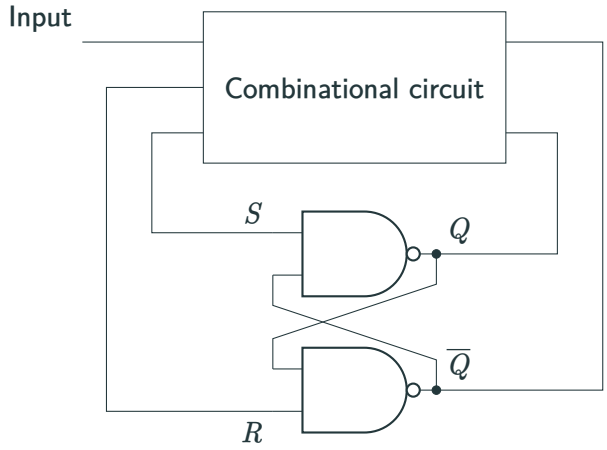
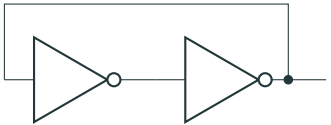
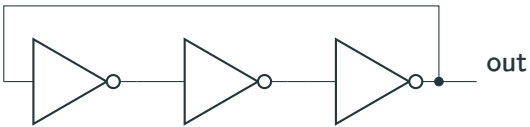
SR Latch and Feedback

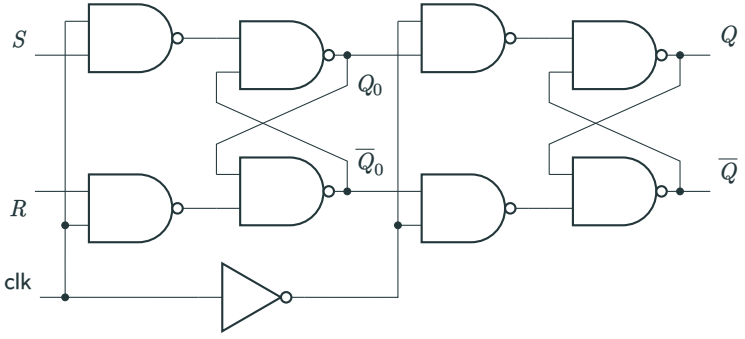


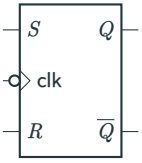
Stable and Unstable Feedback



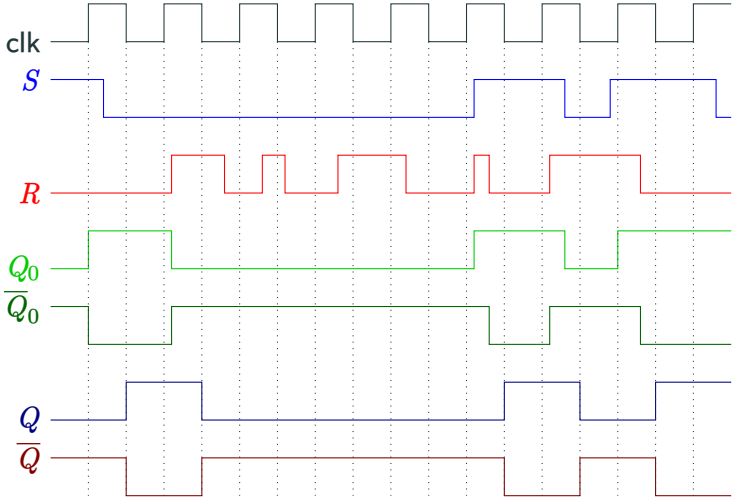


Master-Slave SR Flip-Flop





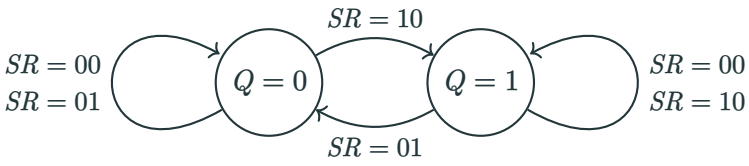
Timing Diagram – Part I



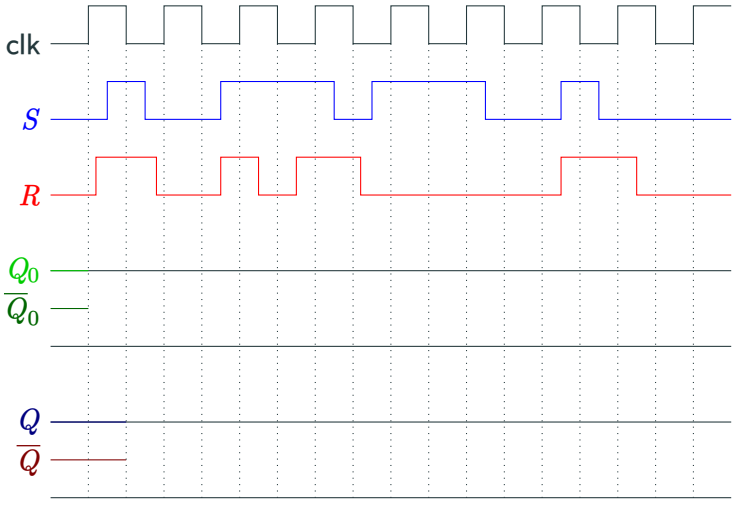
SR Flip-flop: Characteristic Table, Characteristic Equation, and State Diagram

clk	S	R	Q_+
↓	0	0	Q
↓	0	1	0
↓	1	0	1
↓	1	1	–

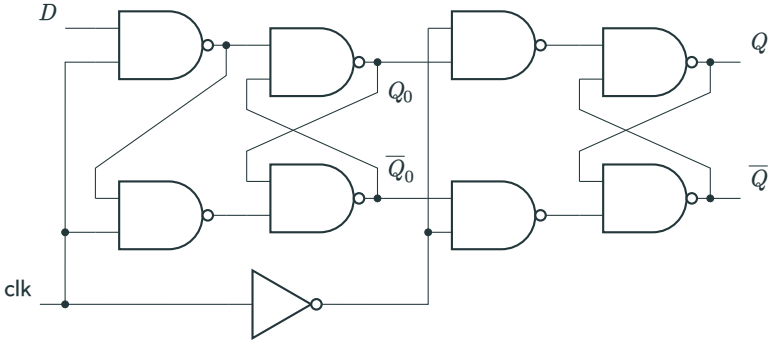
$$Q_+ = S + \overline{R}Q$$

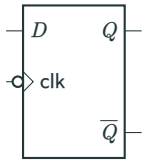


Timing Diagram – Part II

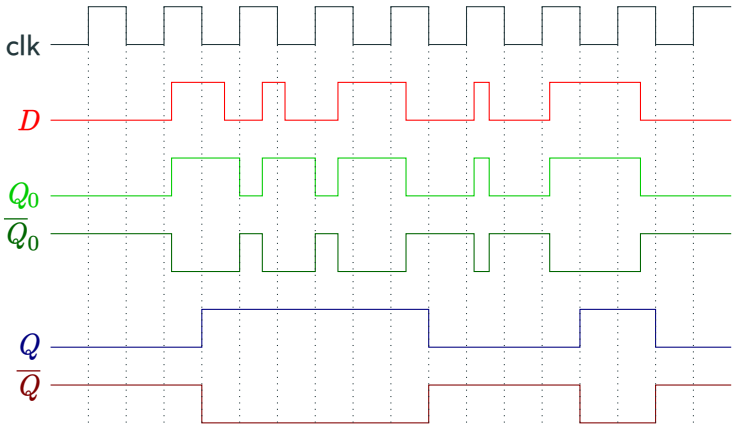


Master-Slave D Flip-Flop





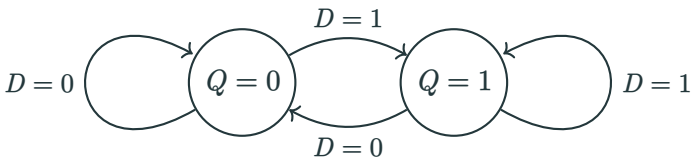
Timing Diagram



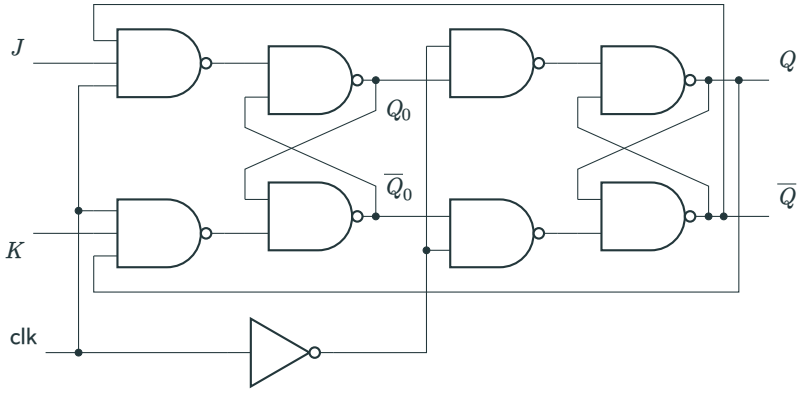
D Flip-flop: Characteristic Table, Characteristic Equation, and State Diagram

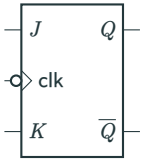
clk	D	Q_+
↓	0	0
↓	1	1

$$Q_+ = D$$

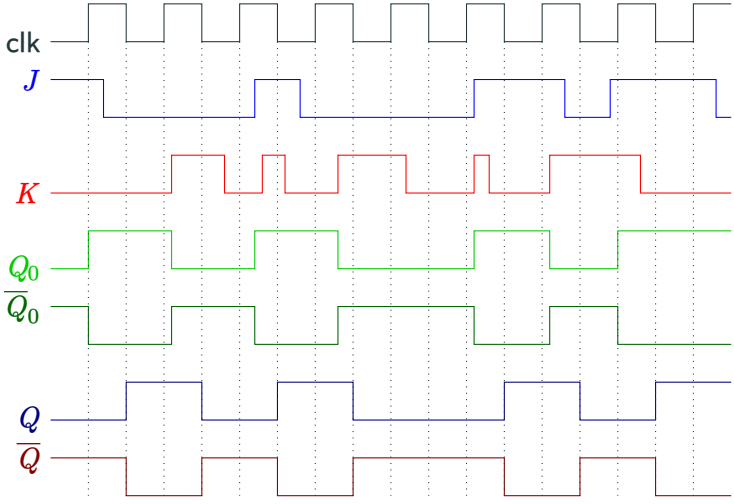


Master-Slave JK Flip-Flop





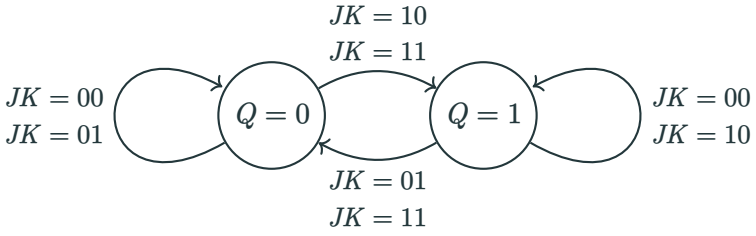
Timing Diagram



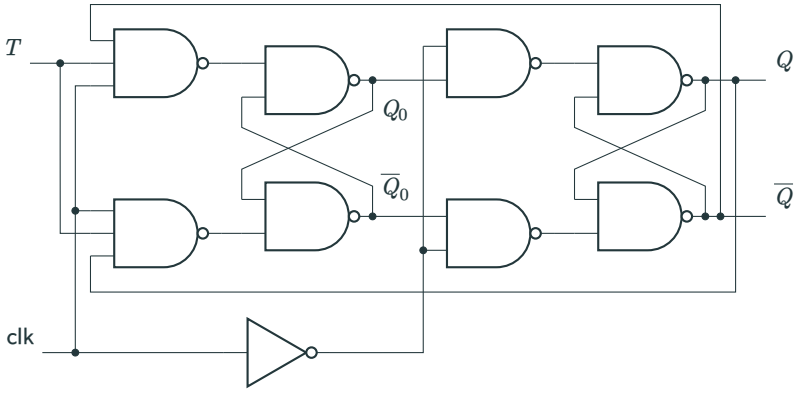
JK Flip-flop: Characteristic Table, Characteristic Equation, and State Diagram

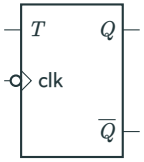
clk	J	K	Q_+
↓	0	0	Q
↓	0	1	0
↓	1	0	1
↓	1	1	$\overline{Q}$

$$Q_+ = J\overline{Q} + \overline{K}Q$$

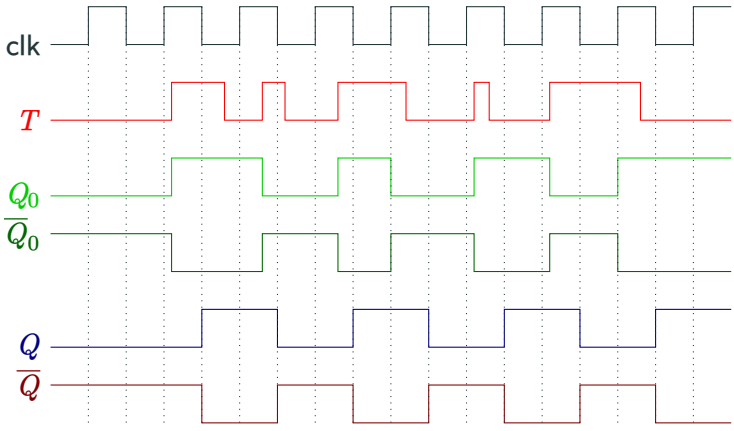


Master-Slave T Flip-Flop





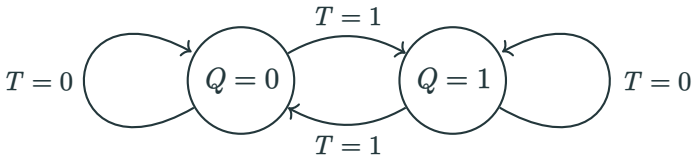
Timing Diagram



T Flip-flop: Characteristic Table, Characteristic Equation, and State Diagram

clk	T	Q_+
↓	0	Q
↓	1	$\overline{Q}$

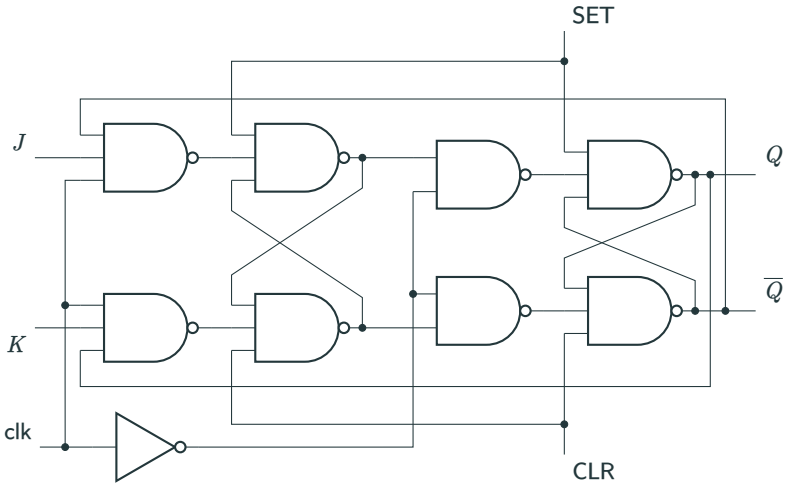
$$Q_+ = T \oplus Q$$

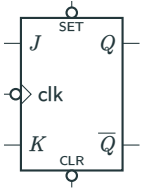


Key Observation

Master-slave flip-flops depend on the stability of the inputs when the clock pulse is high.

Master-Slave JK Flip-Flop with Asynchronous Set and Clear

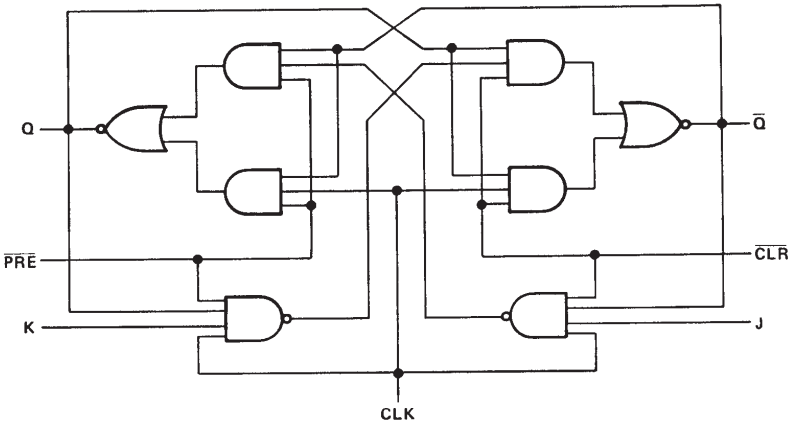




Characteristic Table

SET	CLR	clk	J	K	Q_+	$\overline{Q}_+$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1	↓	0	0	Q	$\overline{Q}$
1	1	↓	0	1	0	1
1	1	↓	1	0	1	0
1	1	↓	1	1	$\overline{Q}$	Q

Texas Instruments: 74LS76A—Master-Slave JK Flip-Flop



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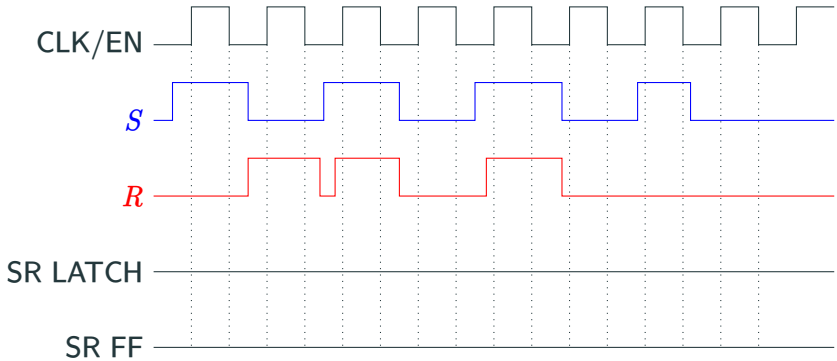
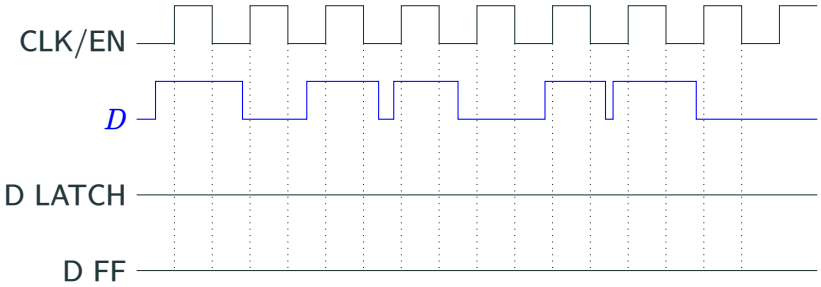
SR



D



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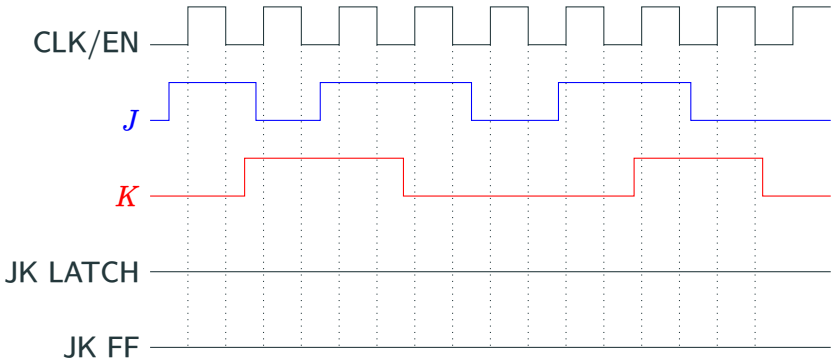

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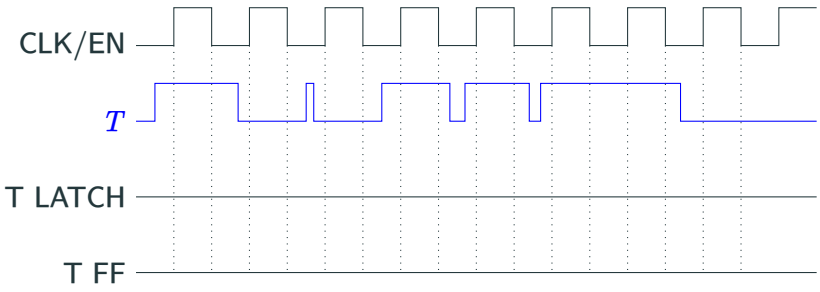

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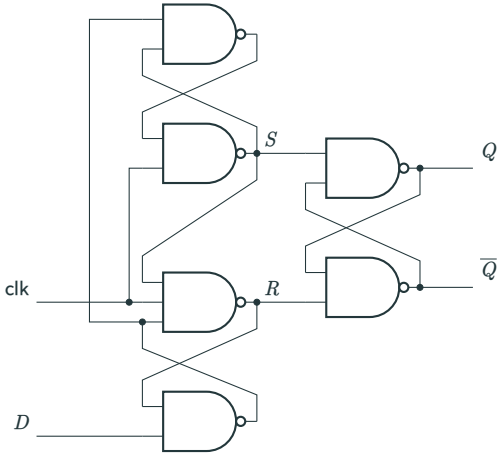
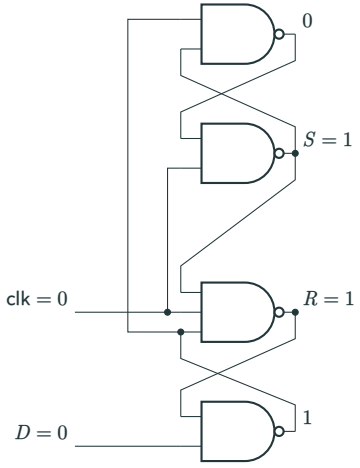
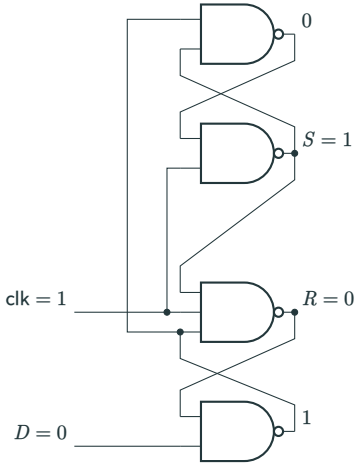
Edge-Triggered D Flip-Flop

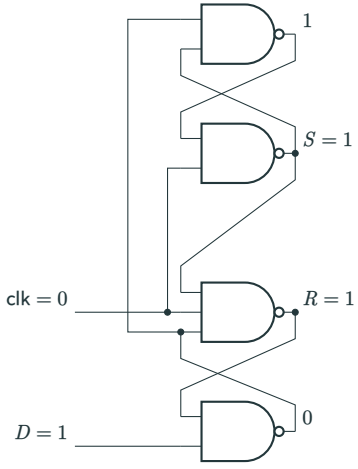


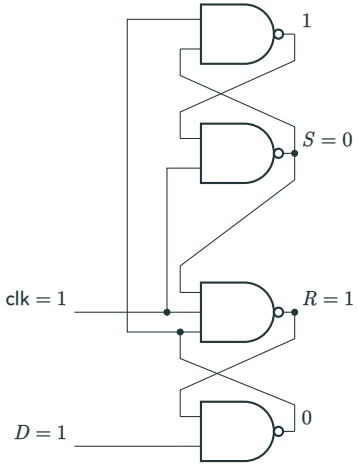
Edge-Triggered D Flip-Flop: Details ($D = 0$)



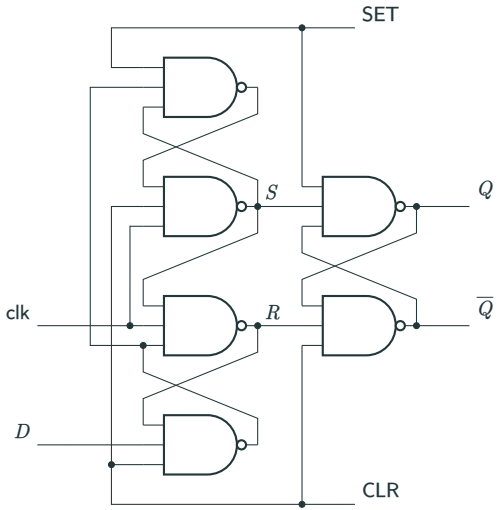


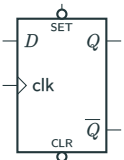
Edge-Triggered D Flip-Flop: Details ($D = 1$)



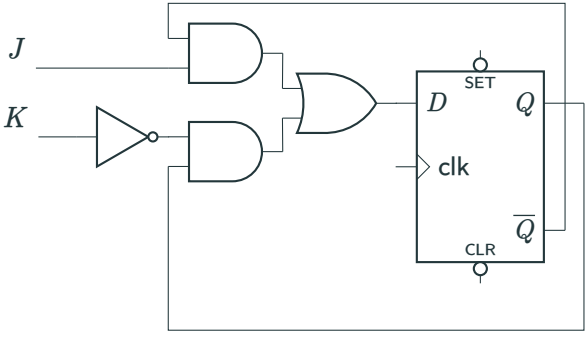


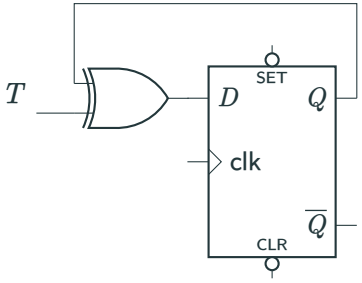
Edge-Triggered D Flip-Flops with Asynchronous Set and Clear





Edge-Triggered JK and T Flip-Flops





Texas Instruments: SN7474—Edge-Triggered D Flip-Flop