Digital System Design

Design of Synchronous Counters

Alfonso Fernandez

Ingeniería en Inteligencia Artificial
Academia de Sistemas Digitales
Escuela Superior de Cómputo, ESCOM
Instutito Politécnico Nacional, IPN

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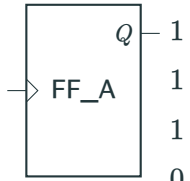
Flip-flop Sequence Example



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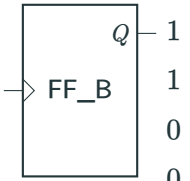

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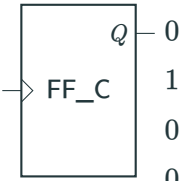
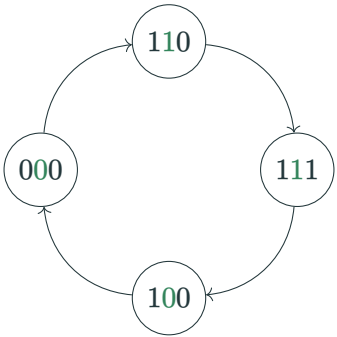


0 1 0 0 0 1

State Diagram



State Table

Present State			Next State		
A	B	C	A_+	B_+	C_+
0	0	0	1	1	0
0	0	1	X	X	X
0	1	0	X	X	X
0	1	1	X	X	X
1	0	0	0	0	0
1	0	1	X	X	X
1	1	0	1	1	1
1	1	1	1	0	0

Karnaugh Maps and State Equations

A_+

A \ BC	00	01	11	10
0	1	X	X	X
1	0	X	1	1

$$A_+ = \overline{A} + B$$

B_+

A \ BC	00	01	11	10
0	1	X	X	X
1	0	X	0	1

$$B_+ = \overline{A} + B\overline{C}$$

C_+

A \ BC	00	01	11	10
0	0	X	X	X
1	0	X	0	1

$$C_+ = B\overline{C}$$

Transition mappings

- $\alpha : 0 \to 1$
- $\beta : 1 \to 0$
- $1 : 1 \to 1$
- $0 : 0 \to 0$
- $\mathsf{X} : \mathsf{X} \to \mathsf{X}$

Transition Table

Present State			Next State			Transitions		
A	B	C	A_+	B_+	C_+	I_A	I_B	I_C
0	0	0	1	1	0	α	α	0
0	0	1	X	X	X	X	X	X
0	1	0	X	X	X	X	X	X
0	1	1	X	X	X	X	X	X
1	0	0	0	0	0	β	0	0
1	0	1	X	X	X	X	X	X
1	1	0	1	1	1	1	1	α
1	1	1	1	0	0	1	β	β

Karnaugh Maps for Transition Table

I_A

A \ BC	00	01	11	10
0	α	X	X	X
1	β	X	1	1

I_B

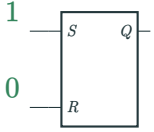
A \ BC	00	01	11	10
0	α	X	X	X
1	0	X	β	1

I_C

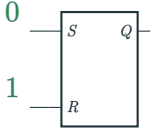
A \ BC	00	01	11	10
0	0	X	X	X
1	0	X	β	α

SR Flip-Flop: Excitation Equations

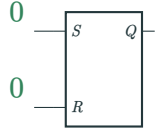
- $\alpha : 0 \to 1$

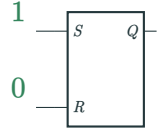


- $\beta : 1 \to 0$

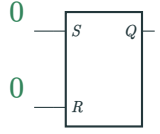


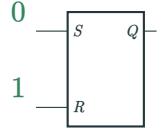
- $1 : 1 \to 1$





- $0 : 0 \to 0$





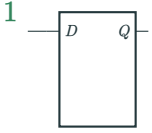
Excitation equations:

$$S = \{\alpha\} + \text{D.C.}\{1, \text{X}\}$$

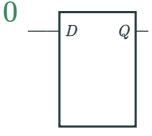
$$R = \{\beta\} + \text{D.C.}\{0, \text{X}\}$$

D Flip-Flop: Excitation Equations

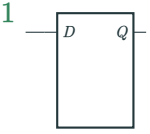
- $\alpha: 0 \to 1$



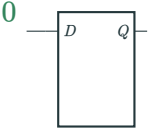
- $\beta: 1 \to 0$



- $1: 1 \to 1$



- $0: 0 \to 0$

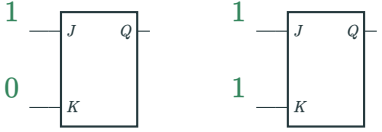


Excitation equations:

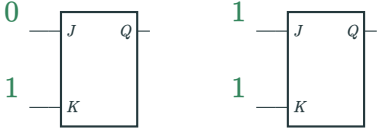
$$D = \{\alpha, 1\} + \text{D.C.}\{X\}$$

JK Flip-Flop: Excitation Equations

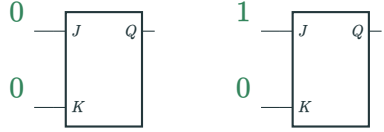
- $\alpha : 0 \to 1$



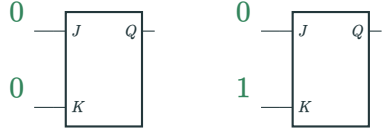
- $\beta : 1 \to 0$



- $1 : 1 \to 1$



- $0 : 0 \to 0$



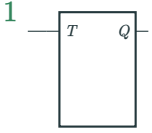
Excitation equations:

$$J = \{\alpha\} + \text{D.C.}\{1, \beta, \text{X}\}$$

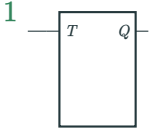
$$K = \{\beta\} + \text{D.C.}\{0, \alpha, \text{X}\}$$

T Flip-Flop: Excitation Equations

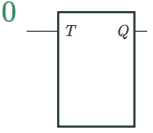
- $\alpha: 0 \to 1$



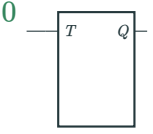
- $\beta: 1 \to 0$



- $1: 1 \to 1$



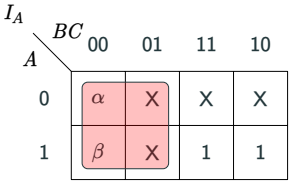
- $0: 0 \to 0$



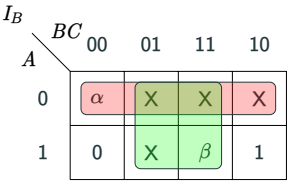
Excitation equations:

$$T = \{\alpha, \beta\} + \text{D.C.}\{\text{X}\}$$

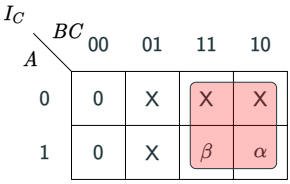
Design with T Flip-Flops



$$T_A = \overline{B}$$

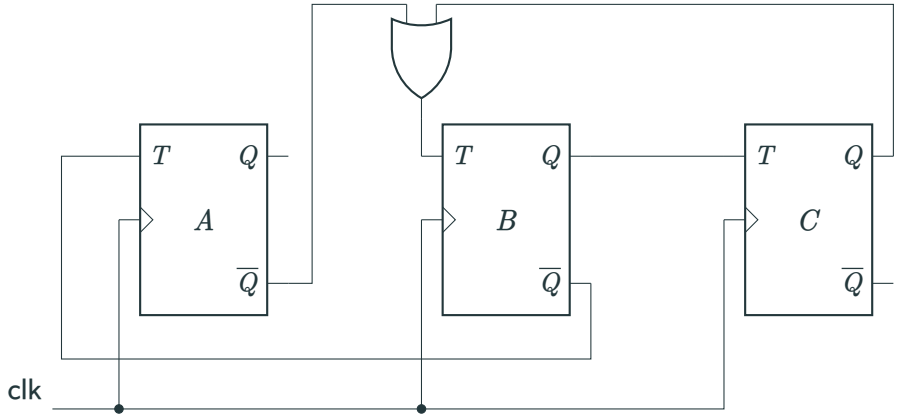


$$T_B = \overline{A} + C$$



$$T_C = B$$

Circuit Diagram



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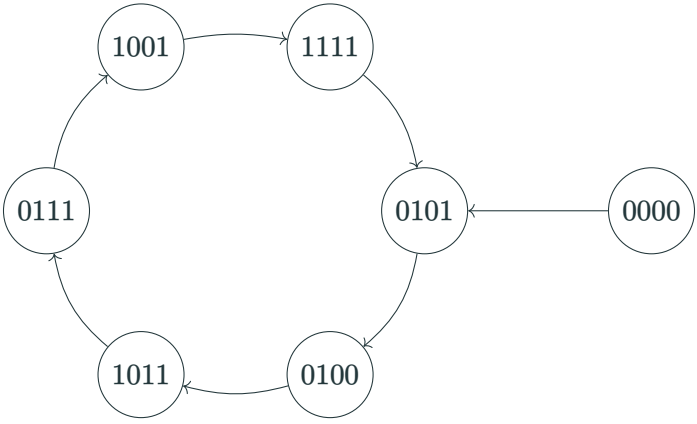
Algorithm

- From the State Diagram, obtain the State Table and Transtion Table.
- Construct the Karnaugh maps using the Transition Table.
- Select the flip-flop to be used in the design.
- Using the Karnaugh maps derive the optimum input equations for the selected flip-flops.

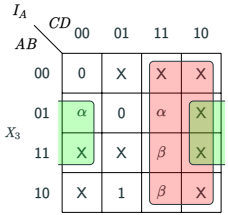
Example



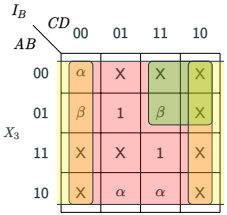
State Table and Transition Table

Present State				Next State				Transitions			
A	B	C	D	A_+	B_+	C_+	D_+	I_A	I_B	I_C	I_D
0	0	0	0	0	1	0	1	0	α	0	α
0	1	0	0	1	0	1	1	α	β	α	α
0	1	0	1	0	1	0	0	0	1	0	β
0	1	1	1	1	0	0	1	α	β	β	1
1	0	0	1	1	1	1	1	1	α	α	1
1	0	1	1	0	1	1	1	β	α	1	1
1	1	1	1	0	1	0	1	β	1	β	1

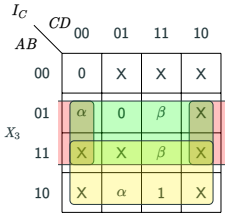
Design with JK Flip-Flops



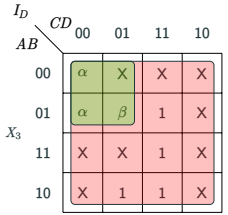
$$J_A = C + B\overline{D}$$
$$K_A = C$$



$$J_B = 1$$
$$K_B = \overline{D} + \overline{A}C$$

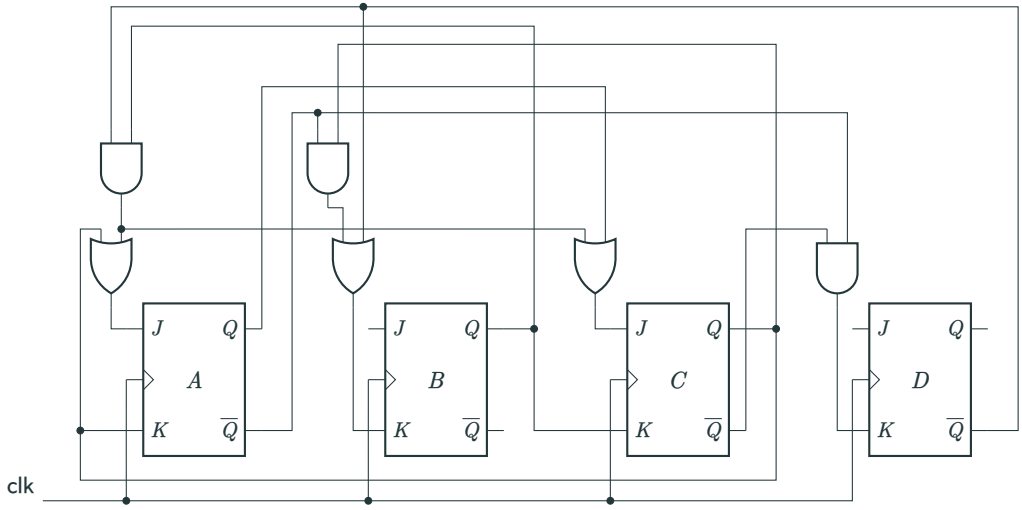


$$J_C = A + B\overline{D}$$
$$K_C = B$$



$$J_D = 1$$
$$K_D = \overline{A}\,\overline{C}$$

Circuit Diagram



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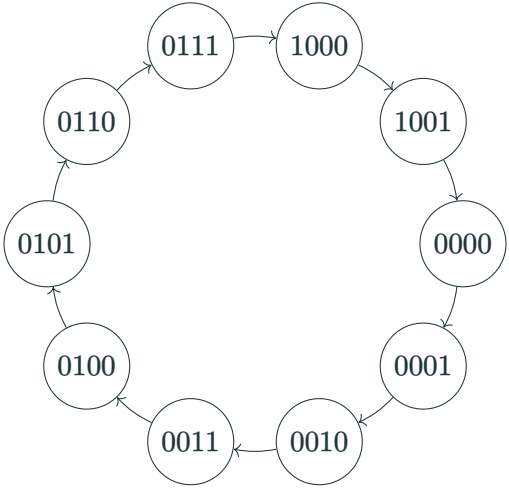
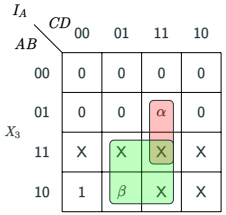
State diagram



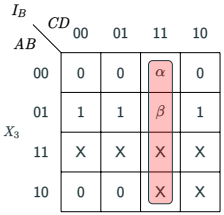
State Table and Transition Table

Present State				Next State				Transitions			
A	B	C	D	A_+	B_+	C_+	D_+	I_A	I_B	I_C	I_D
0	0	0	0	0	0	0	1	0	0	0	α
0	0	0	1	0	0	1	0	0	0	α	β
0	0	1	0	0	0	1	1	0	0	1	α
0	0	1	1	0	1	0	0	0	α	β	β
0	1	0	0	0	1	0	1	0	1	0	α
0	1	0	1	0	1	1	0	0	1	α	β
0	1	1	0	0	1	1	1	0	1	1	α
0	1	1	1	1	0	0	0	α	β	β	β
1	0	0	0	1	0	0	1	1	0	0	α
1	0	0	1	0	0	0	0	β	0	0	β

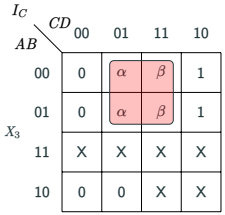
Design with T Flip-Flops



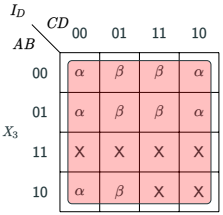
$T_A = BCD + AD$



$T_B = CD$

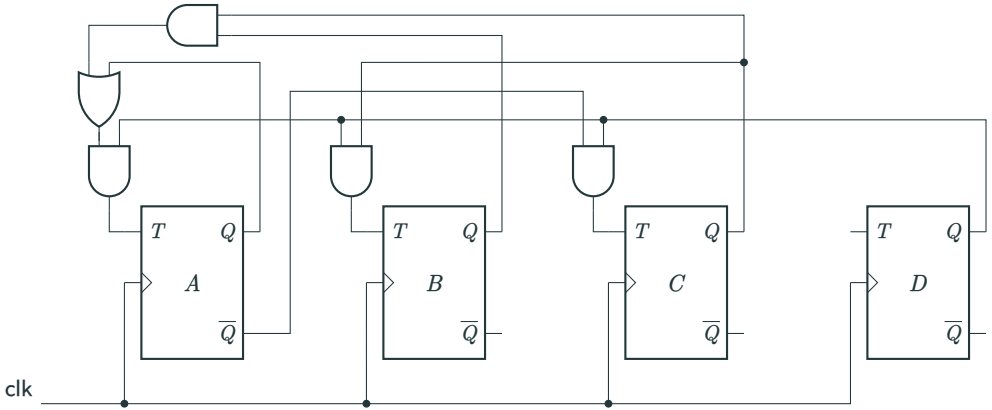


$T_C = \overline{A}D$

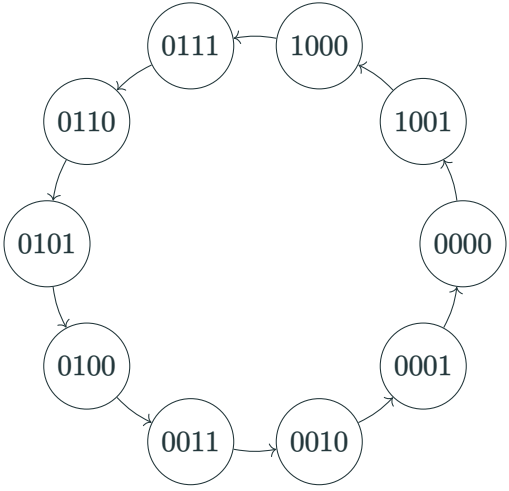


$T_D = 1$

Circuit Diagram



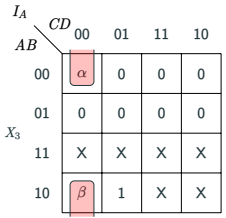
State diagram (Down Counter)

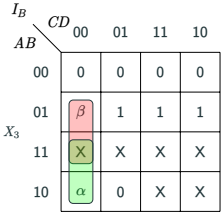


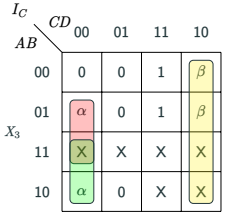
State Table and Transition Table

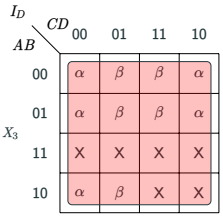
Present State				Next State				Transitions			
A	B	C	D	A_+	B_+	C_+	D_+	I_A	I_B	I_C	I_D
0	0	0	0	1	0	0	1	α	0	0	α
0	0	0	1	0	0	0	0	0	0	0	β
0	0	1	0	0	0	0	1	0	0	β	α
0	0	1	1	0	0	1	0	0	0	1	β
0	1	0	0	0	0	1	1	0	β	α	α
0	1	0	1	0	1	0	0	0	1	0	β
0	1	1	0	0	1	0	1	0	1	β	α
0	1	1	1	0	1	1	0	0	1	1	β
1	0	0	0	0	1	1	1	β	α	α	α
1	0	0	1	1	0	0	0	1	0	0	β

Design with T Flip-Flops









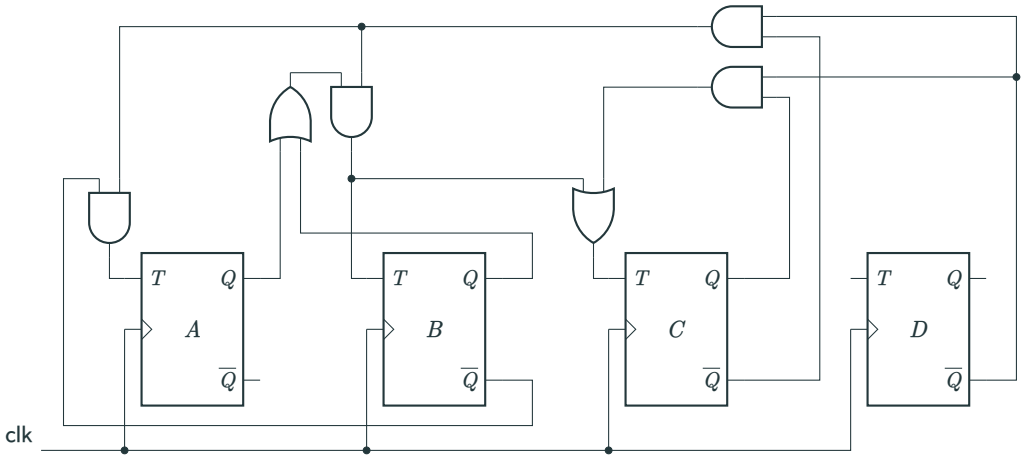
$$T_A = \overline{B}\,\overline{C}\,\overline{D}$$

$$T_B = (A+B)\overline{C}\,\overline{D}$$

$$T_C = (A+B)\overline{C}\,\overline{D} + C\overline{D}$$

$$T_D = 1$$

Circuit Diagram



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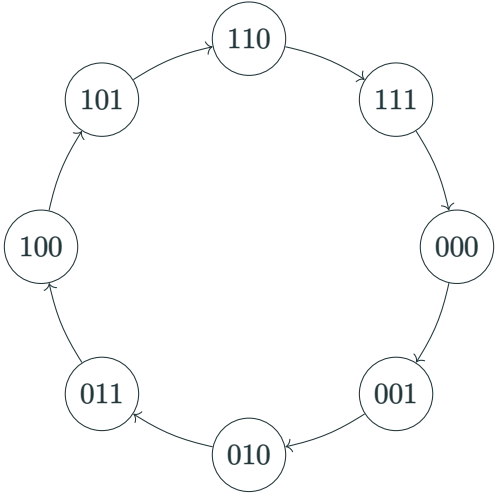
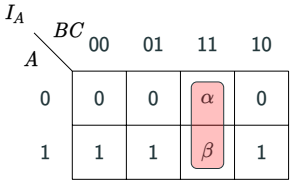
State diagram



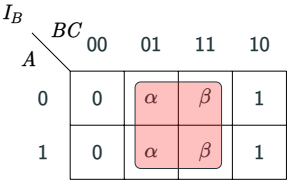
State Table and Transition Table

Present State			Next State			Transitions		
A	B	C	A_+	B_+	C_+	I_A	I_B	I_C
0	0	0	0	0	1	0	0	α
0	0	1	0	1	0	0	α	β
0	1	0	0	1	1	0	1	α
0	1	1	1	0	0	α	β	β
1	0	0	1	0	1	1	0	α
1	0	1	1	1	0	1	α	β
1	1	0	1	1	1	1	1	α
1	1	1	0	0	0	β	β	β

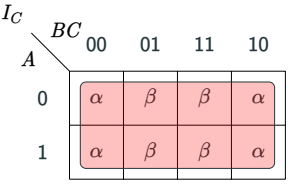
Design with JK Flip-Flops



$$J_A = BC$$
$$K_A = BC$$

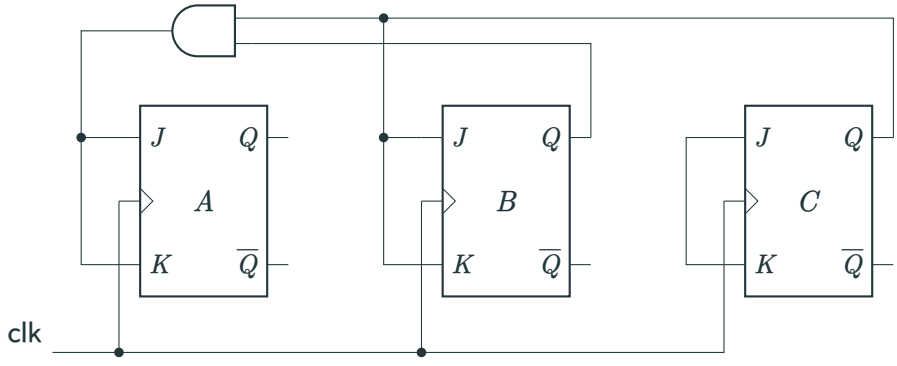


$$J_B = C$$
$$K_B = C$$



$$J_C = 1$$
$$K_C = 1$$

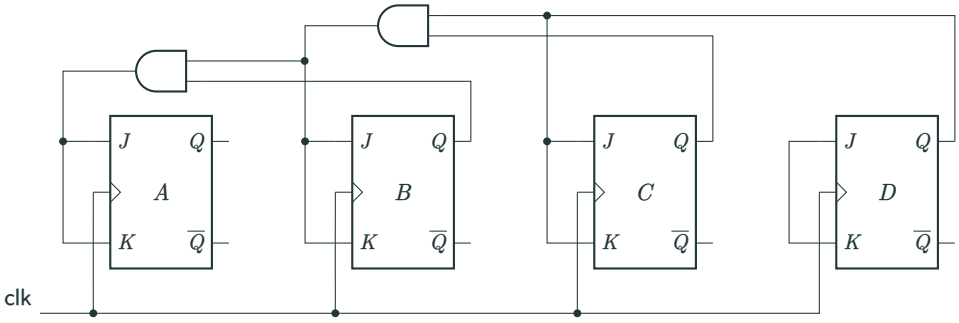
Circuit Diagram



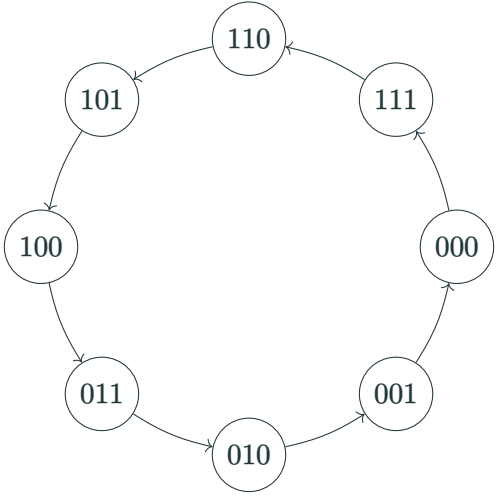
4-Bit Binary Counter, ABCD

$$J_A = BCD \qquad J_B = CD \qquad J_C = D \qquad J_D = 1$$
$$K_A = BCD \qquad K_B = CD \qquad K_C = D \qquad K_D = 1$$

Circuit Diagram



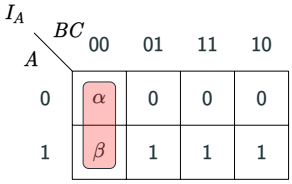
State diagram (Down Counter)

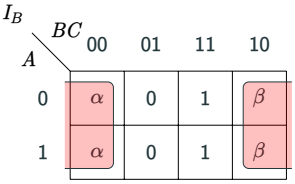


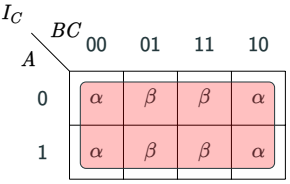
State Table and Transition Table

Present State			Next State			Transitions		
A	B	C	A_+	B_+	C_+	I_A	I_B	I_C
0	0	0	1	1	1	α	α	α
0	0	1	0	0	0	0	0	β
0	1	0	0	0	1	0	β	α
0	1	1	0	1	0	0	1	β
1	0	0	0	1	1	β	α	α
1	0	1	1	0	0	1	0	β
1	1	0	1	0	1	1	β	α
1	1	1	1	1	0	1	1	β

Design with JK Flip-Flops





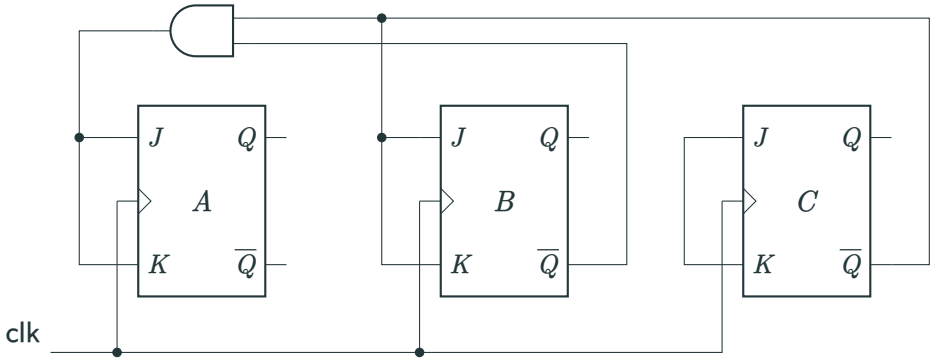


$$J_A = \overline{B}\,\overline{C}$$
$$K_A = \overline{B}\,\overline{C}$$

$$J_B = \overline{C}$$
$$K_B = \overline{C}$$

$$J_C = 1$$
$$K_C = 1$$

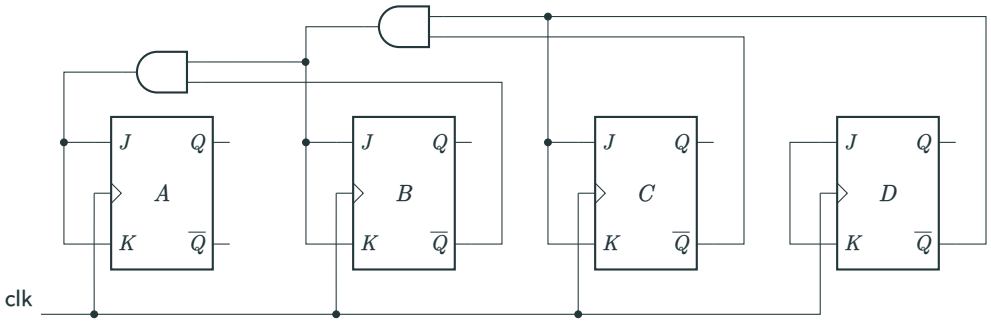
Circuit Diagram



4-Bit Binary Down Counter, ABCD

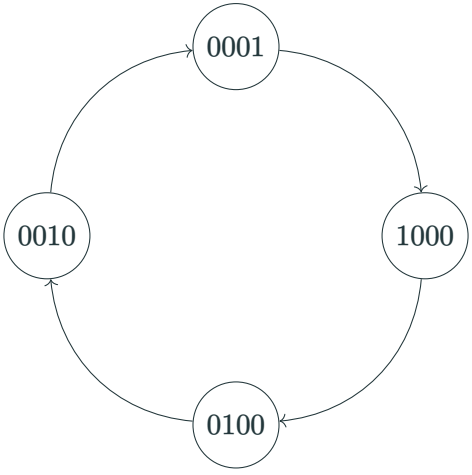
$$J_A = \overline{B}\,\overline{C}\,\overline{D} \qquad J_B = \overline{C}\,\overline{D} \qquad J_C = \overline{D} \qquad J_D = 1$$
$$K_A = \overline{B}\,\overline{C}\,\overline{D} \qquad K_B = \overline{C}\,\overline{D} \qquad K_C = \overline{D} \qquad K_D = 1$$

Circuit Diagram

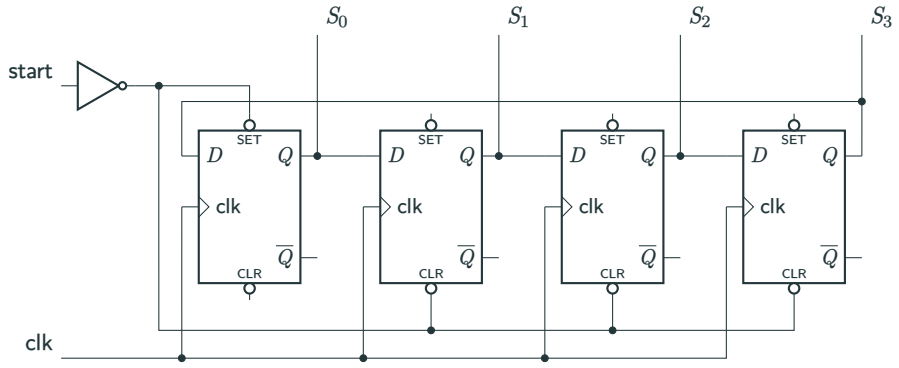


Contents

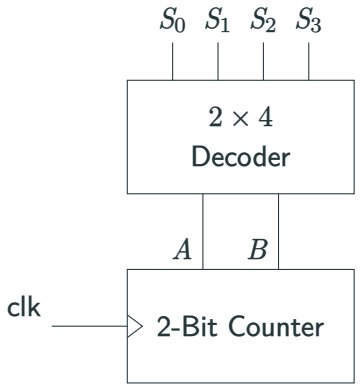
Four States Ring Counter



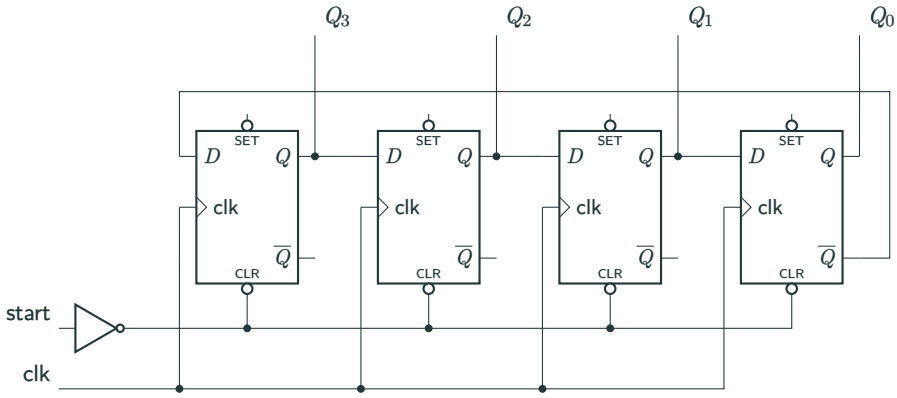
4-Bit Ring Counter



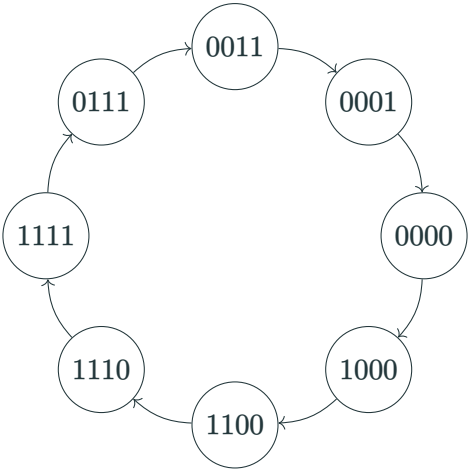
4-Bit Ring Counter: 2-Bit Counter Implementation



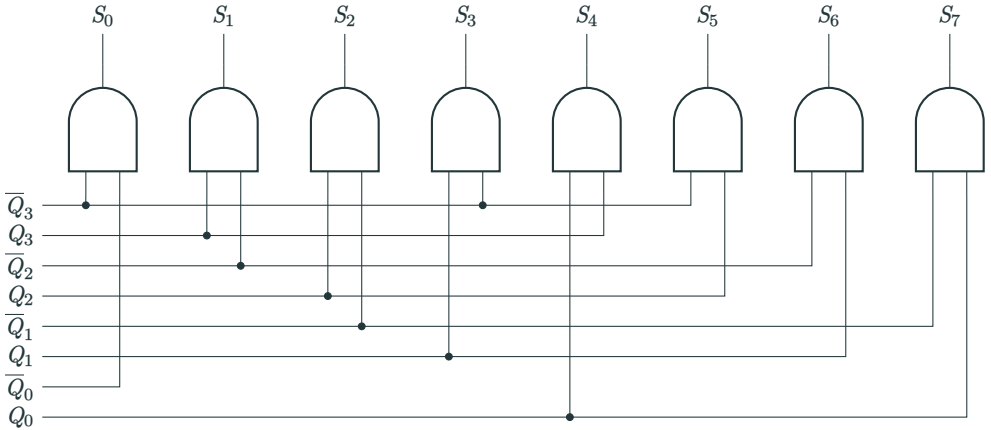
Switch-tail Ring Counter



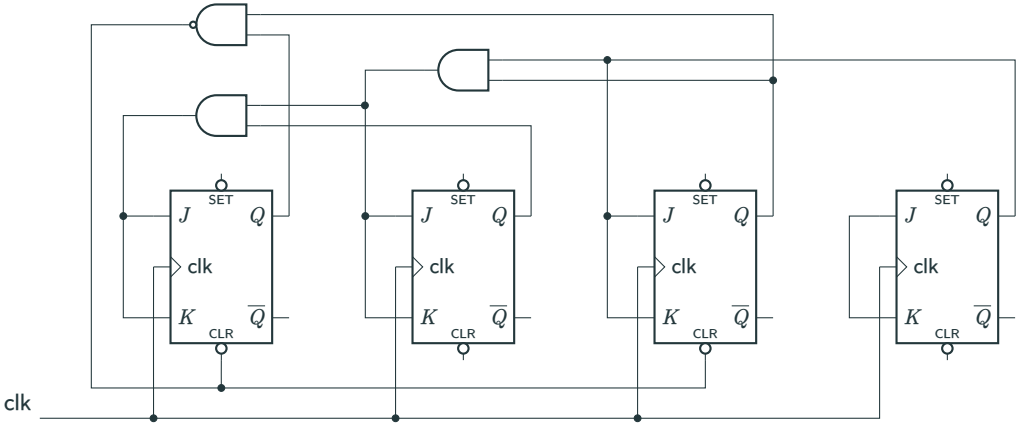
State Diagram



Eight States Ring Counter: Johnson Counter



BCD Counter Using a Binary Counter and CLR Flip-Flop Inputs



BCD Down Counter Using a Binary Counter and CLR Flip-Flop Inputs