Digital System Design

Design of Mealy and Moore Finite State Machines

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Finite Automata

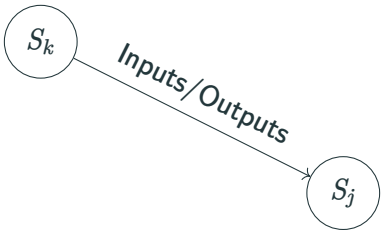
Finite automata are abstract computing devices or **machines**, which are useful model for important hardware and software applications.

Finite automata are composed by discrete inputs, outputs, states and set of transitions, which depend on input symbols, from state to state. They are defined by the 5-tuples $M = (Q, \Sigma, \delta, q_0, F)$, where

- Q is a finite state set
- Σ is a finite alphabet set
- $\delta\colon Q \times \Sigma \to Q$ is the transition function
- $q_0 \in Q$ is the initial state
- $F \subset Q$ is the set of accepted states

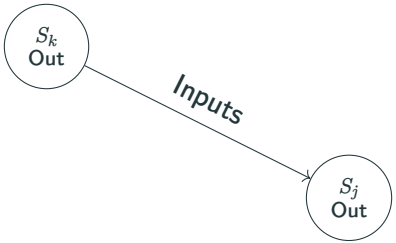
Mealy Machines

- Next state depends on present state and inputs
- Output is a function of present state and inputs



Moore Machines

- Next state depends on present state and inputs
- Output is a function of present state



Algorithm

- From the State Diagram, obtain the State Table and Transition Table.
- Construct the Karnaugh maps using the Transition Table.
- Select the flip-flop to be used in the design.
- Using the Karnaugh maps derive the optimum input equations for the selected flip-flops.

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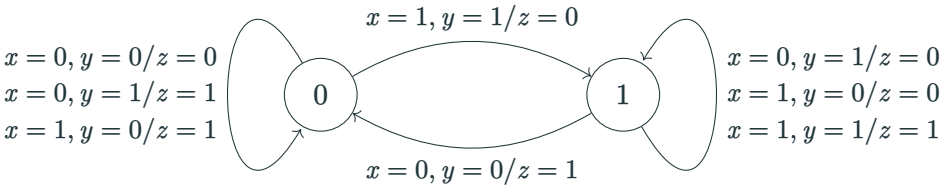
Example 1: Serial Adder



State Table and Transition Table

Present State	Inputs		Next State	Output	Transition
A	x	y	A_+	z	f_A
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	α
1	0	0	0	1	β
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	1	1

Design with JK Flip-Flops

f_A

A \ $x\,y$	00	01	11	10
0	0	0	α	0
1	β	1	1	1

z

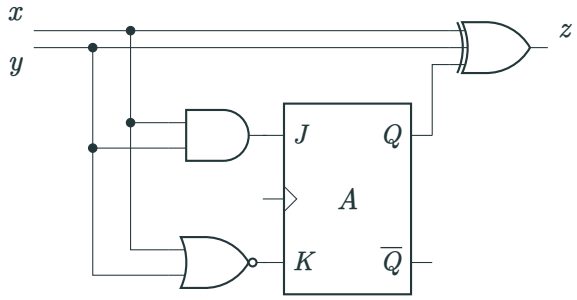
A \ $x\,y$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$J_A = x\,y$$

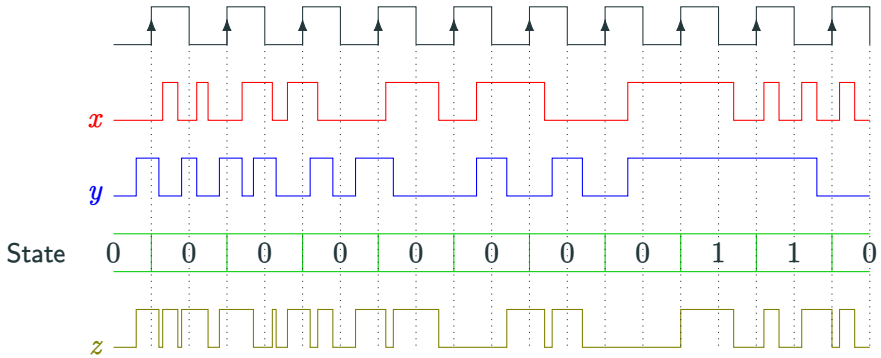
$$K_A = \overline{x}\,\overline{y} = \overline{x + y}$$

$$z = A \oplus x \oplus y$$

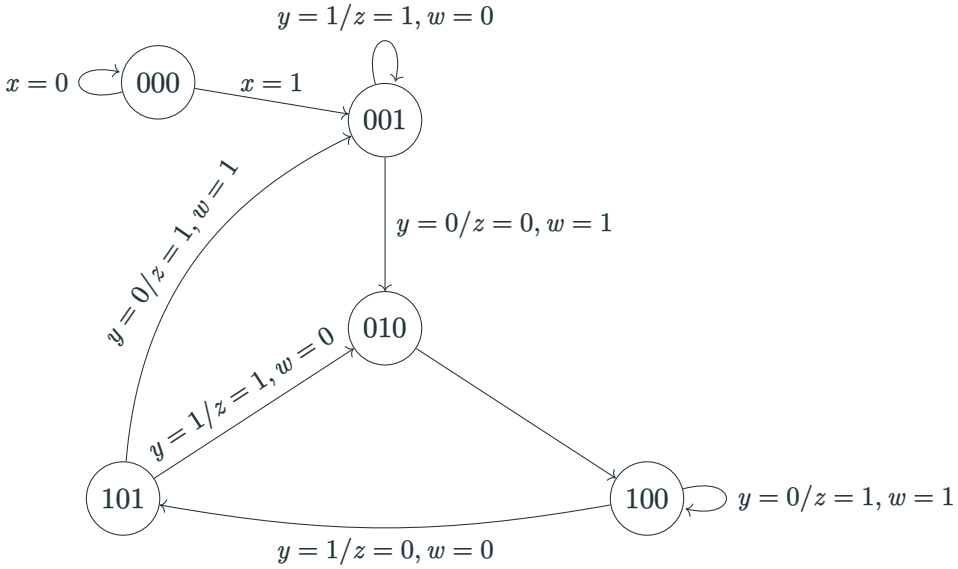
Circuit Diagram



Timing Diagram



Example 2: State Diagram



State Table and Transition Table

Present State			Inputs		Next State			Outputs		Transitions		
A	B	C	x	y	A_+	B_+	C_+	z	w	f_A	f_B	f_C
0	0	0	0	X	0	0	0	X	X	0	0	0
0	0	0	1	X	0	0	1	X	X	0	0	α
0	0	1	X	0	0	1	0	0	1	0	α	β
0	0	1	X	1	0	0	1	1	0	0	0	1
0	1	0	X	X	1	0	0	X	X	α	β	0
1	0	0	X	0	1	0	0	1	1	1	0	0
1	0	0	X	1	1	0	1	0	0	1	0	α
1	0	1	X	0	0	0	1	1	1	β	0	1
1	0	1	X	1	0	1	0	1	0	β	α	β

Karnaugh Maps for z and w

z / xy \ ABC	000	001	011	010	110	111	101	100
00	X	0	X	X	X	X	1	1
01	X	1	X	X	X	X	1	0
11	X	1	X	X	X	X	1	0
10	X	0	X	X	X	X	1	1

$$z = yC + \overline{y}A$$

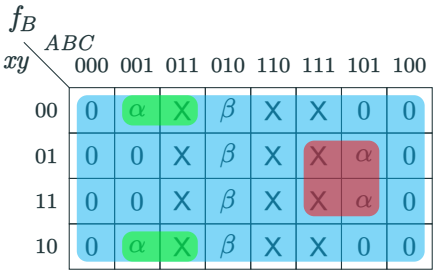
w / xy \ ABC	000	001	011	010	110	111	101	100
00	X	1	X	X	X	X	1	1
01	X	0	X	X	X	X	0	0
11	X	0	X	X	X	X	0	0
10	X	1	X	X	X	X	1	1

$$w = \overline{y}$$

Karnaugh Maps for f_A and f_B

$$J_A = B$$

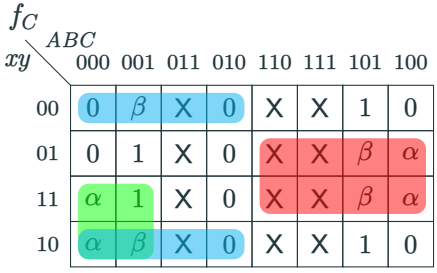
$$K_A = C$$



$$J_B = (y \odot A)C$$

$$K_B = 1$$

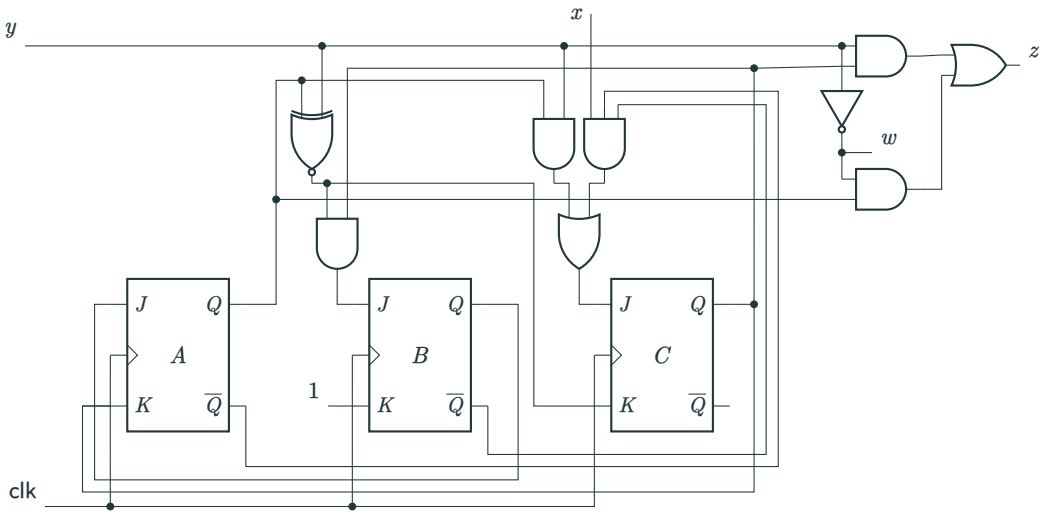
Karnaugh Map for f_C



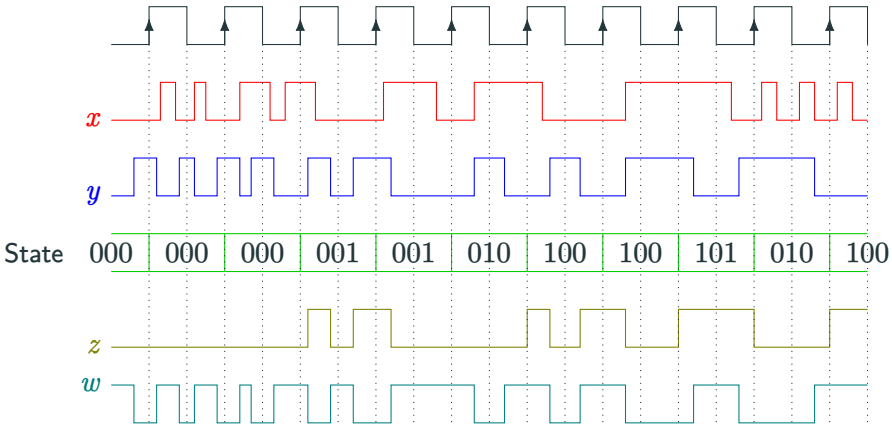
$$J_C = yA + x\overline{A}\,\overline{B}$$

$$K_C = y \odot A$$

Circuit Diagram



Timing Diagram



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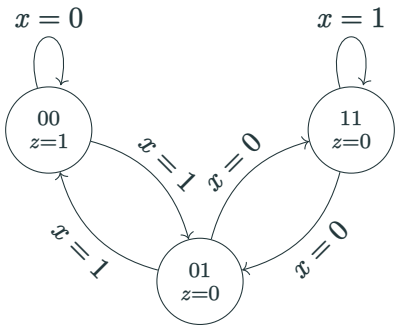
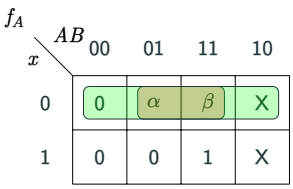
Example 1: Divisible by Three Detector



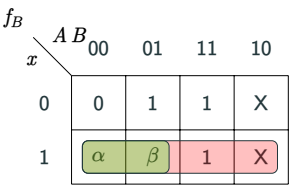
State Table and Transition Table

Present State		Input	Next State		Output	Transitions	
A	B	x	A_+	B_+	z	f_A	f_B
0	0	0	0	0	1	0	0
0	0	1	0	1		0	α
0	1	0	1	1	0	α	1
0	1	1	0	0		0	β
1	1	0	0	1	0	β	1
1	1	1	1	1		1	1

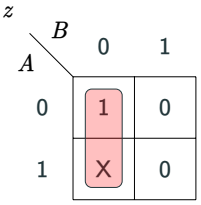
Design with JK Flip-Flops



$$J_A = B\,\overline{x}$$
$$K_A = \overline{x}$$

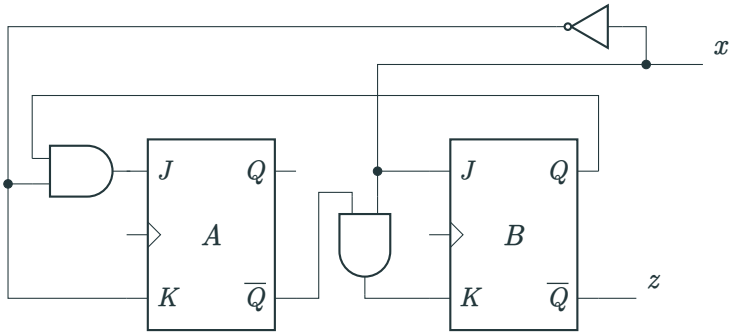


$$J_A = x$$
$$K_B = \overline{A}\,x$$

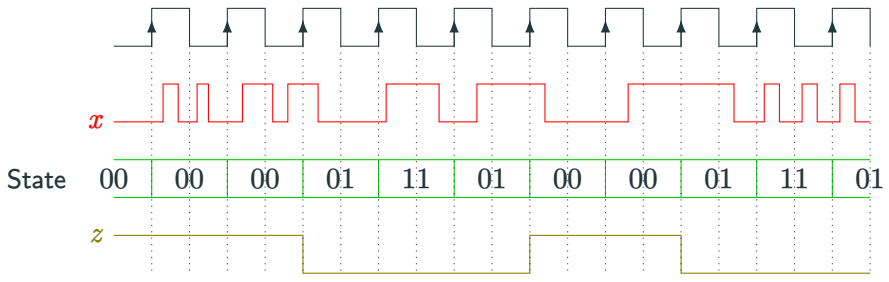


$$z = \overline{B}$$

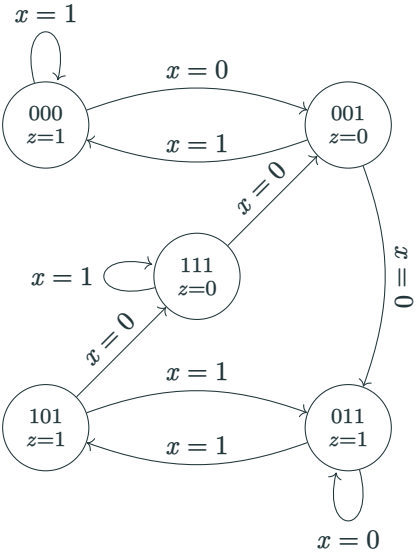
Circuit Diagram



Timing Diagram



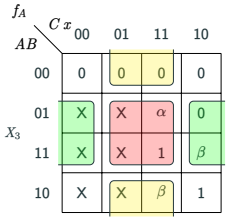
Example 2: State Diagram



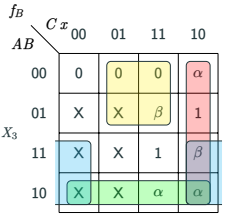
State Table and Transition Table

Present State			Input	Next State			Output	Transitions		
A	B	C	x	A_+	B_+	C_+	z	f_A	f_B	f_C
0	0	0	0	0	0	1	1	0	0	α
0	0	0	1	0	0	0		0	0	0
0	0	1	0	0	1	1	0	0	α	1
0	0	1	1	0	0	0		0	0	β
0	1	1	0	0	1	1	1	0	1	1
0	1	1	1	1	0	1		α	β	1
1	0	1	0	1	1	1	1	1	α	1
1	0	1	1	0	1	1		β	α	1
1	1	1	0	0	0	1	0	β	β	1
1	1	1	1	1	1	1		1	1	1

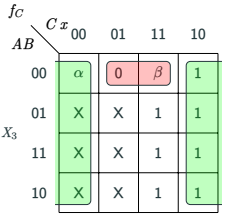
Design with JK Flip-Flops



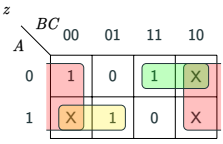
$$J_A = B\,x$$
$$K_A = B \oplus x$$



$$J_B = C\,\overline{x} + A\,\overline{B}$$
$$K_B = A \oplus x$$

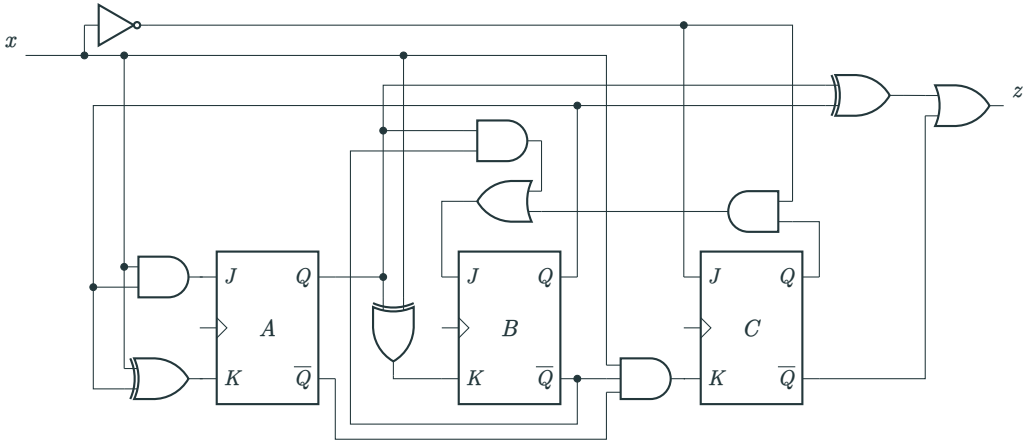


$$J_C = \overline{x}$$
$$K_C = \overline{A}\,\overline{B}\,x$$



$$z = \overline{C} + A \oplus B$$

Circuit Diagram



Timing Diagram