

Digital System Design

Design of Ripple Counters

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Introduction

Design of Ripple Counters

Design of BCD Ripple Counters

Design of Binary Ripple Counters

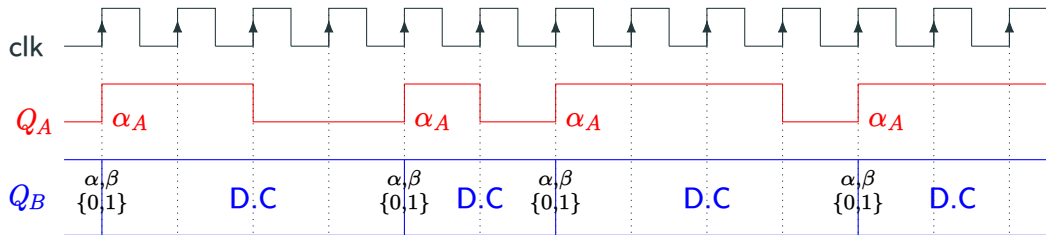
Introduction

Design of Ripple Counters

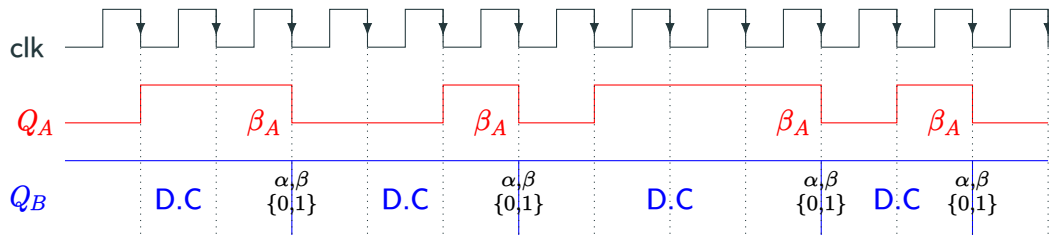
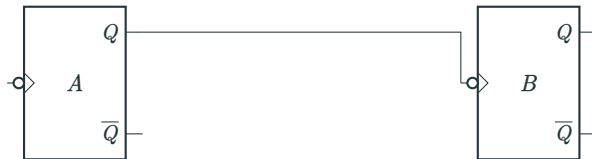
Design of BCD Ripple Counters

Design of Binary Ripple Counters

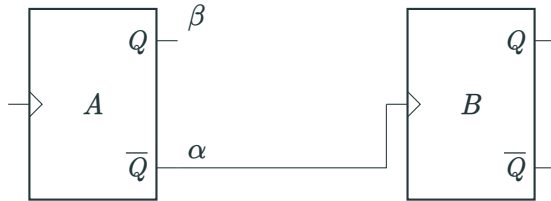
α Transitions



β Transitions



β Transitions in Positive Edge Triggered Flip-Flops



Algorithm

- From the State Diagram, obtain the State Table and Transition Table.
- Identify the flip-flop '**Z**' that can be clocked by the output of flip-flop '**Y**'. To do that, check if α transitions (or β transitions) in flip-flop **Y** cover all α and β transitions in flip-flop **Z**.
- Modify the transitions of flip-flop **Z** according to the following: for each flip-flop **Z** transition different from α transition (or β transition, respectively) change any '0' and '1' transitions in flip-flop **Z** with don't care transition ('X').
- Construct the Karnaugh maps using the Transition Table.
- Select the flip-flop to be used in the design.
- Using the Karnaugh maps derive the optimum input equations for the selected flip-flops.

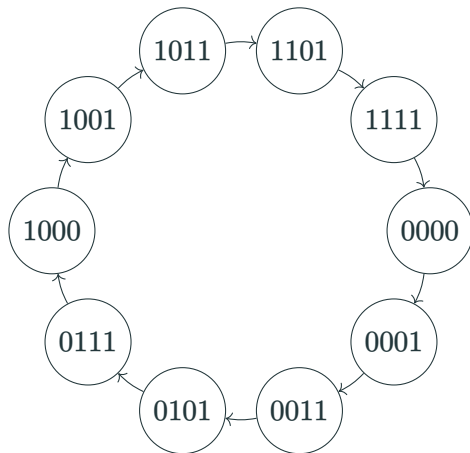
Introduction

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State Diagram



State Table and Transition Table

Present State				Next State				Transitions											
A	B	C	D	A_+	B_+	C_+	D_+	I_A	I_B	I_C	I_D	I'_A	I'_B	I'_C	I'_D	I''_A	I''_B	I''_C	I''_D
0	0	0	0	0	0	0	1	0	0	0	α	X	X	0	α	X	X	0	α
0	0	0	1	0	0	1	1	0	0	α	1	X	X	α	1	X	X	α	1
0	0	1	1	0	1	0	1	0	α	β	1	X	α	β	1	0	α	β	1
0	1	0	1	0	1	1	1	0	1	α	1	X	X	α	1	X	X	α	1
0	1	1	1	1	0	0	0	α	β	β	β	α	β	β	β	α	β	β	β
1	0	0	0	1	0	0	1	1	0	0	α	X	X	0	α	X	X	0	α
1	0	0	1	1	0	1	1	1	0	α	1	X	X	α	1	X	X	α	1
1	0	1	1	1	1	0	1	1	α	β	1	X	α	β	1	1	α	β	1
1	1	0	1	1	1	1	1	1	1	α	1	X	X	α	1	X	X	α	1
1	1	1	1	0	0	0	0	β	β	β	β	β	β	β	β	β	β	β	β

Karnaugh Maps for $\{I'_A, I'_B, I'_C, I'_D\}$

		I'_A			
		CD			
X_3	AB	00	01	11	10
	00	X	X	X	X
	01	X	X	α	X
	11	X	X	β	X
	10	X	X	X	X

$$J_A = 1$$

$$K_A = 1$$

		I'_B			
		CD			
X_3	AB	00	01	11	10
	00	X	X	α	X
	01	X	X	β	X
	11	X	X	β	X
	10	X	X	α	X

$$J_B = 1$$

$$K_B = 1$$

		I'_C			
		CD			
X_3	AB	00	01	11	10
	00	0	α	β	X
	01	X	α	β	X
	11	X	α	β	X
	10	0	α	β	X

$$J_C = D$$

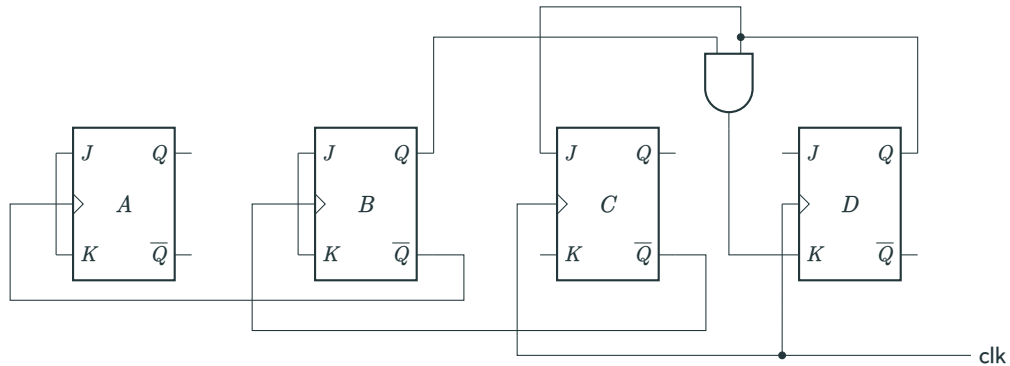
$$K_C = 1$$

		I'_D			
		CD			
X_3	AB	00	01	11	10
	00	α	1	1	X
	01	X	1	β	X
	11	X	1	β	X
	10	α	1	1	X

$$J_D = 1$$

$$K_D = BC$$

Circuit Diagram



Karnaugh Maps for $\{I''_A, I''_B, I''_C, I''_D\}$

		I''_A			
		CD			
AB	X_3	00	01	11	10
		00	01	11	10
	00	X	X	0	X
	01	X	X	α	X
	11	X	X	β	X
	10	X	X	1	X

$$J_A = B$$

$$K_A = B$$

		I''_B			
		CD			
AB	X_3	00	01	11	10
		00	01	11	10
	00	X	X	α	X
	01	X	X	β	X
	11	X	X	β	X
	10	X	X	α	X

$$J_B = 1$$

$$K_B = 1$$

		I''_C			
		CD			
AB	X_3	00	01	11	10
		00	01	11	10
	00	0	α	β	X
	01	X	α	β	X
	11	X	α	β	X
	10	0	α	β	X

$$J_C = D$$

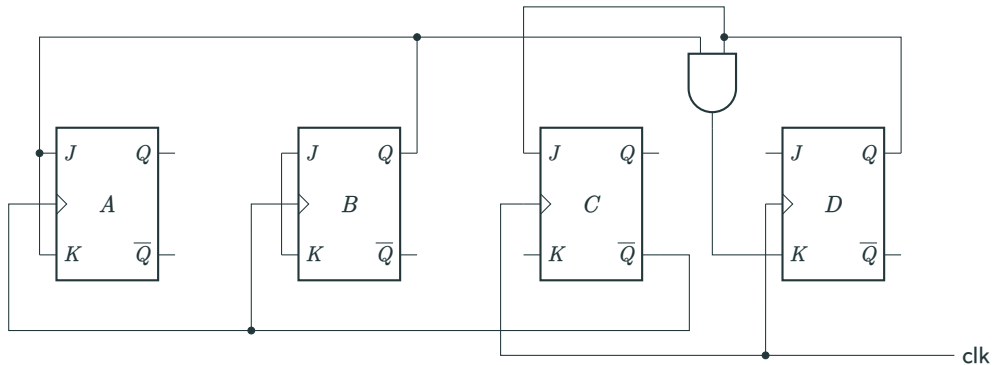
$$K_C = 1$$

		I''_D			
		CD			
AB	X_3	00	01	11	10
		00	01	11	10
	00	α	1	1	X
	01	X	1	β	X
	11	X	1	β	X
	10	α	1	1	X

$$J_D = 1$$

$$K_D = BC$$

Circuit Diagram



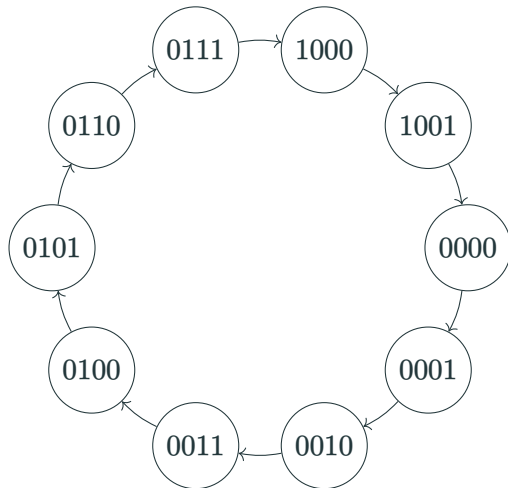
Introduction

Design of Ripple Counters

Design of BCD Ripple Counters

Design of Binary Ripple Counters

State diagram



State Table and Transition Table

Present State				Next State				Transitions							
A	B	C	D	A_+	B_+	C_+	D_+	I_A	I_B	I_C	I_D	I'_A	I'_B	I'_C	I'_D
0	0	0	0	0	0	0	1	0	0	0	α	X	X	X	α
0	0	0	1	0	0	1	0	0	0	α	β	0	X	α	β
0	0	1	0	0	0	1	1	0	0	1	α	X	X	X	α
0	0	1	1	0	1	0	0	0	α	β	β	0	α	β	β
0	1	0	0	0	1	0	1	0	1	0	α	X	X	X	α
0	1	0	1	0	1	1	0	0	1	α	β	0	X	α	β
0	1	1	0	0	1	1	1	0	1	1	α	X	X	X	α
0	1	1	1	1	0	0	0	α	β	β	β	α	β	β	β
1	0	0	0	1	0	0	1	1	0	0	α	X	X	X	α
1	0	0	1	0	0	0	0	β	0	0	β	β	X	0	β

Design with JK Flip-Flops

		I'_A			
		CD			
X_3	AB	00	01	11	10
	00	X	0	0	X
01	00	X	0	α	X
11	00	X	X	X	X
10	00	X	β	X	X

$$J_A = BC$$

$$K_A = 1$$

		I'_B			
		CD			
X_3	AB	00	01	11	10
	00	X	X	α	X
01	00	X	X	β	X
11	00	X	X	X	X
10	00	X	X	X	X

$$J_B = 1$$

$$K_B = 1$$

		I'_C			
		CD			
X_3	AB	00	01	11	10
	00	X	α	β	X
01	00	X	α	β	X
11	00	X	X	X	X
10	00	X	0	X	X

$$J_C = \bar{A}$$

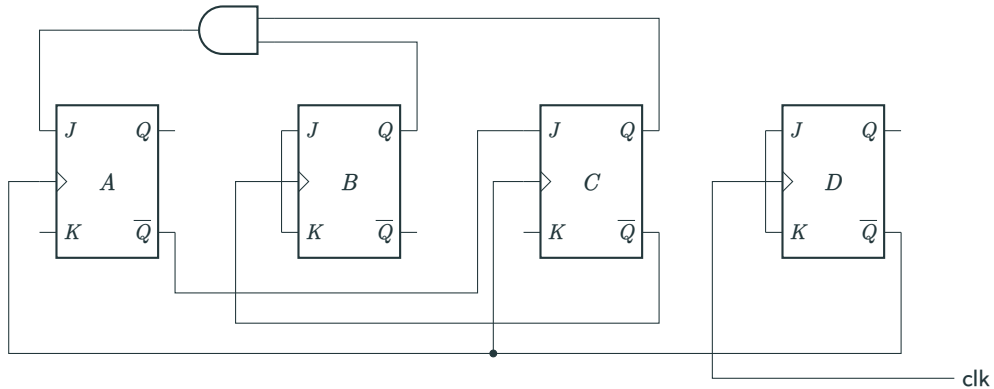
$$K_C = 1$$

		I'_D			
		CD			
X_3	AB	00	01	11	10
	00	α	β	β	α
01	00	α	β	β	α
11	00	X	X	X	X
10	00	α	β	X	X

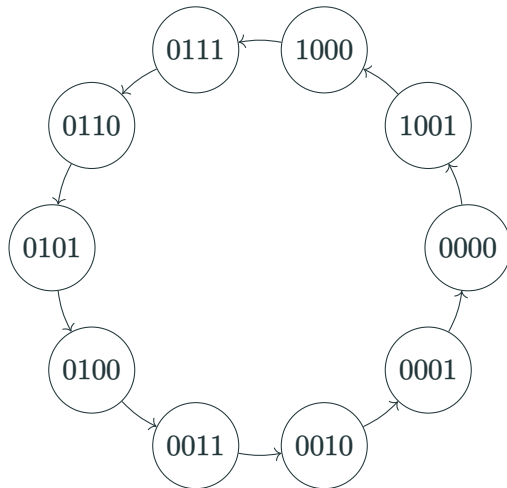
$$J_D = 1$$

$$K_D = 1$$

Circuit Diagram



State diagram (Down Counter)



State Table and Transition Table

Present State				Next State				Transitions							
A	B	C	D	A_+	B_+	C_+	D_+	I_A	I_B	I_C	I_D	I'_A	I'_B	I'_C	I'_D
0	0	0	0	1	0	0	1	α	0	0	α	α	X	0	α
0	0	0	1	0	0	0	0	0	0	0	β	X	X	X	β
0	0	1	0	0	0	0	1	0	0	β	α	0	X	β	α
0	0	1	1	0	0	1	0	0	0	1	β	X	X	X	β
0	1	0	0	0	0	1	1	0	β	α	α	0	β	α	α
0	1	0	1	0	1	0	0	0	1	0	β	X	X	X	β
0	1	1	0	0	1	0	1	0	1	β	α	0	X	β	α
0	1	1	1	0	1	1	0	0	1	1	β	X	X	X	β
1	0	0	0	0	1	1	1	β	α	α	α	β	α	α	α
1	0	0	1	1	0	0	0	1	0	0	β	X	X	X	β

Design with JK Flip-Flops

I'_A

$AB \backslash CD$	00	01	11	10
00	α	X	X	0
01	0	X	X	0
11	X	X	X	X
10	β	X	X	X

X_3

$$J_A = \overline{B} \overline{C}$$

$$K_A = 1$$

I'_B

$AB \backslash CD$	00	01	11	10
00	X	X	X	X
01	β	X	X	X
11	X	X	X	X
10	α	X	X	X

X_3

$$J_B = 1$$

$$K_B = 1$$

I'_C

$AB \backslash CD$	00	01	11	10
00	0	X	X	β
01	α	X	X	β
11	X	X	X	X
10	α	X	X	X

X_3

$$J_C = A + B$$

$$K_C = 1$$

I'_D

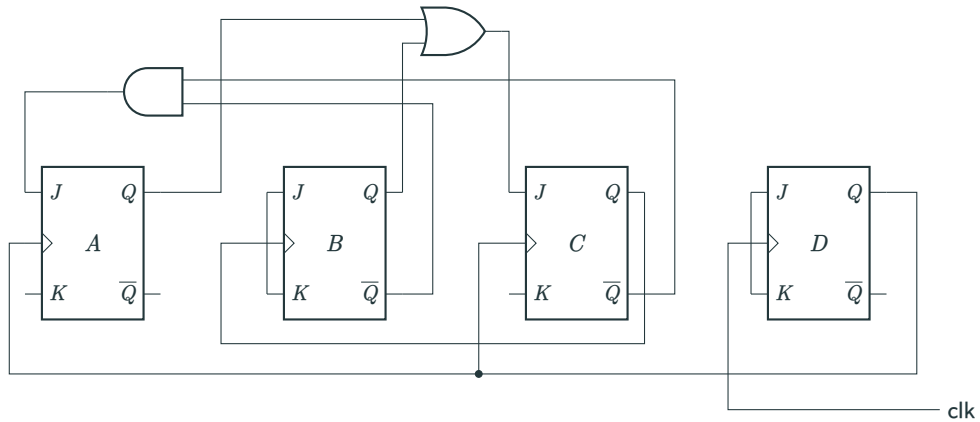
$AB \backslash CD$	00	01	11	10
00	α	β	β	α
01	α	β	β	α
11	X	X	X	X
10	α	β	X	X

X_3

$$J_D = 1$$

$$K_D = 1$$

Circuit Diagram



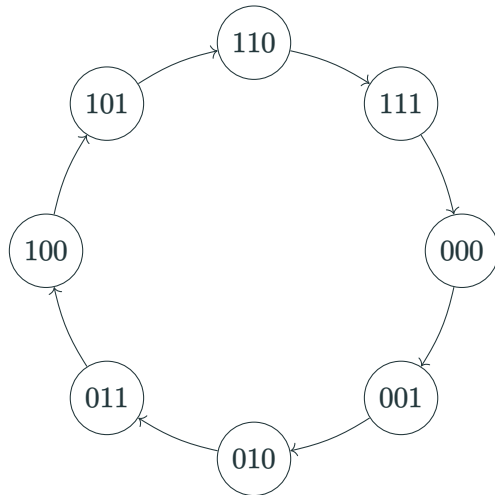
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State diagram



State Table and Transition Table

Present State			Next State			Transitions					
A	B	C	A_+	B_+	C_+	I_A	I_B	I_C	I'_A	I'_B	I'_C
0	0	0	0	0	1	0	0	α	X	X	α
0	0	1	0	1	0	0	α	β	X	α	β
0	1	0	0	1	1	0	1	α	X	X	α
0	1	1	1	0	0	α	β	β	α	β	β
1	0	0	1	0	1	1	0	α	X	X	α
1	0	1	1	1	0	1	α	β	X	α	β
1	1	0	1	1	1	1	1	α	X	X	α
1	1	1	0	0	0	β	β	β	β	β	β

Design with T Flip-Flops

Truth table for $T_A = 1$:

I'_A	A	BC			
		00	01	11	10
0		X	X	α	X
1		X	X	β	X

$$T_A = 1$$

Truth table for $T_B = 1$:

I'_B	A	BC			
		00	01	11	10
0		X	α	β	X
1		X	α	β	X

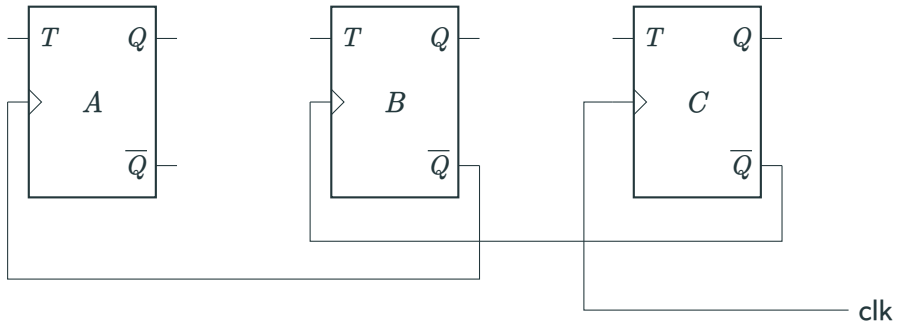
$$T_B = 1$$

Truth table for $T_C = 1$:

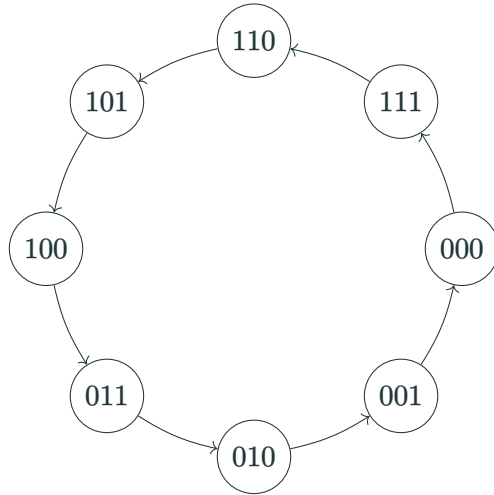
I'_C	A	BC			
		00	01	11	10
0		α	β	β	α
1		α	β	β	α

$$T_C = 1$$

Circuit Diagram



State diagram (Down Counter)



State Table and Transition Table

Present State			Next State			Transitions					
A	B	C	A_+	B_+	C_+	I_A	I_B	I_C	I'_A	I'_B	I'_C
0	0	0	1	1	1	α	α	α	α	α	α
0	0	1	0	0	0	0	0	β	X	X	β
0	1	0	0	0	1	0	β	α	X	β	α
0	1	1	0	1	0	0	1	β	X	X	β
1	0	0	0	1	1	β	α	α	β	α	α
1	0	1	1	0	0	1	0	β	X	X	β
1	1	0	1	0	1	1	β	α	X	β	α
1	1	1	1	1	0	1	1	β	X	X	β

Design with T Flip-Flops

Truth table for $T_A = 1$:

I'_A	A	BC			
		00	01	11	10
0		α	X	X	X
1		β	X	X	X

$$T_A = 1$$

Truth table for $T_B = 1$:

I'_B	A	BC			
		00	01	11	10
0		α	X	X	β
1		α	X	X	β

$$T_B = 1$$

Truth table for $T_C = 1$:

I'_C	A	BC			
		00	01	11	10
0		α	β	β	α
1		α	β	β	α

$$T_C = 1$$

Circuit Diagram

