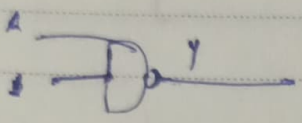
16010123325
E2

NOTES DATE

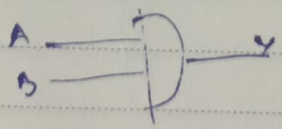
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overline{A} \cdot \overline{B}$



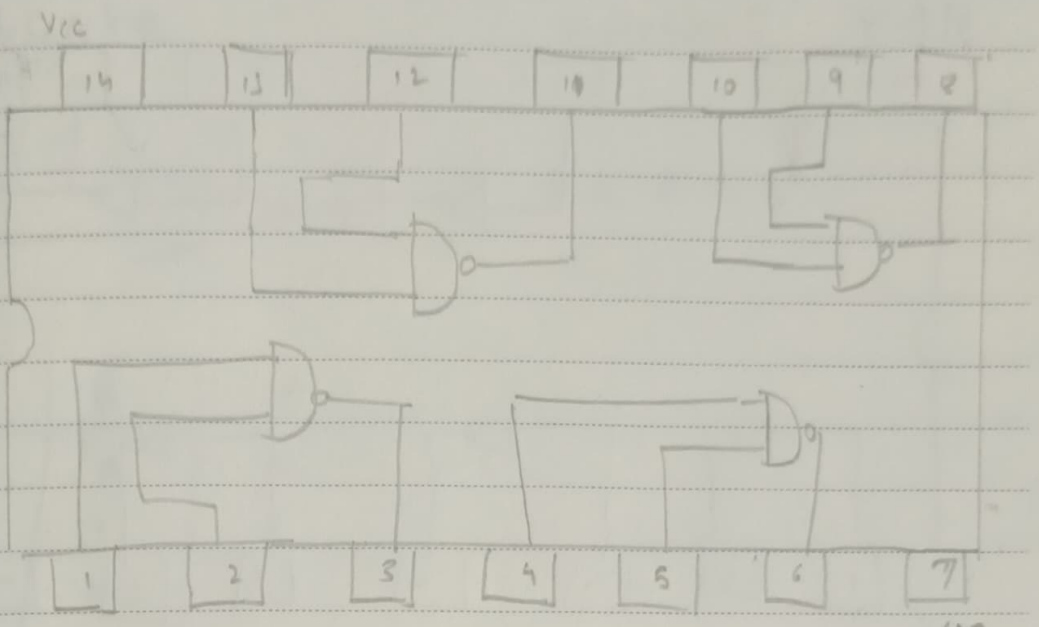
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = A \cdot B$

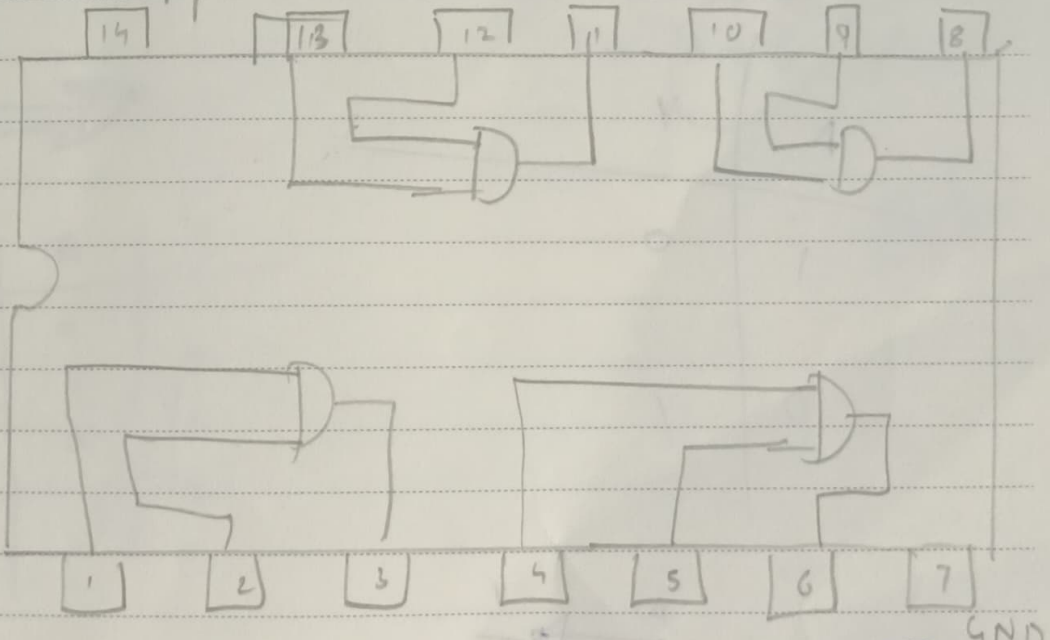


Quad 2-Input NANDGATE

NOTES DATE



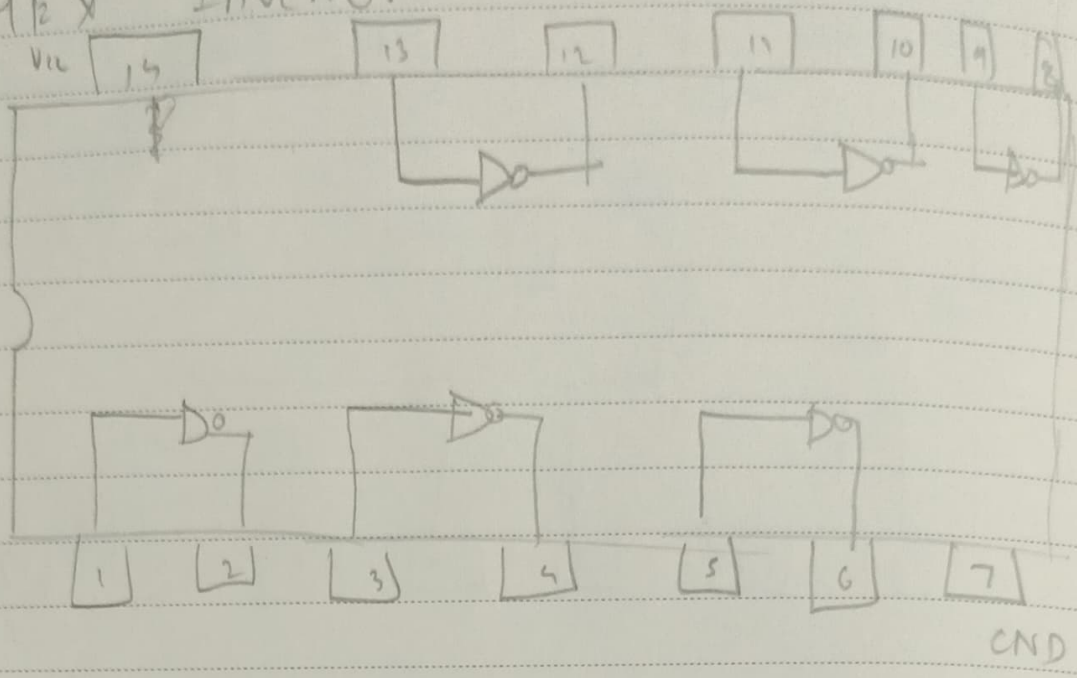
Quad 2-Input AND GATE



NOTES

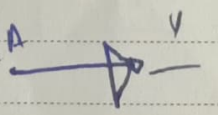
DATE

HEX Inverter



$Y = \bar{A}$

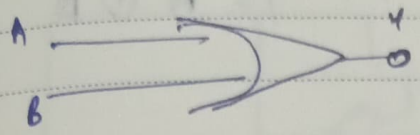
A	Y
1	0
0	1



A'B + B'A

NOTES DATE

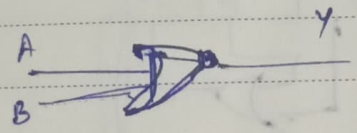
OR Gate



$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOR Gate



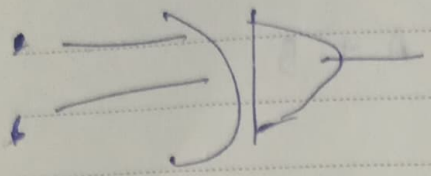
$Y = \overline{A + B}$ $\overline{A+B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOTES DATE

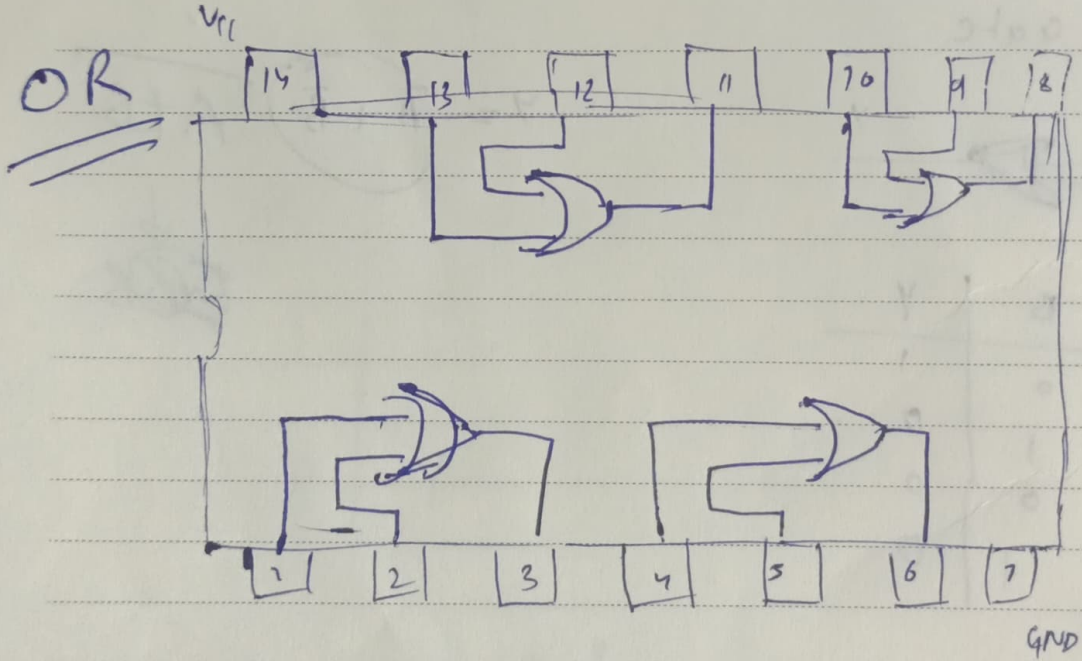
XOR

$Y = A \oplus B$

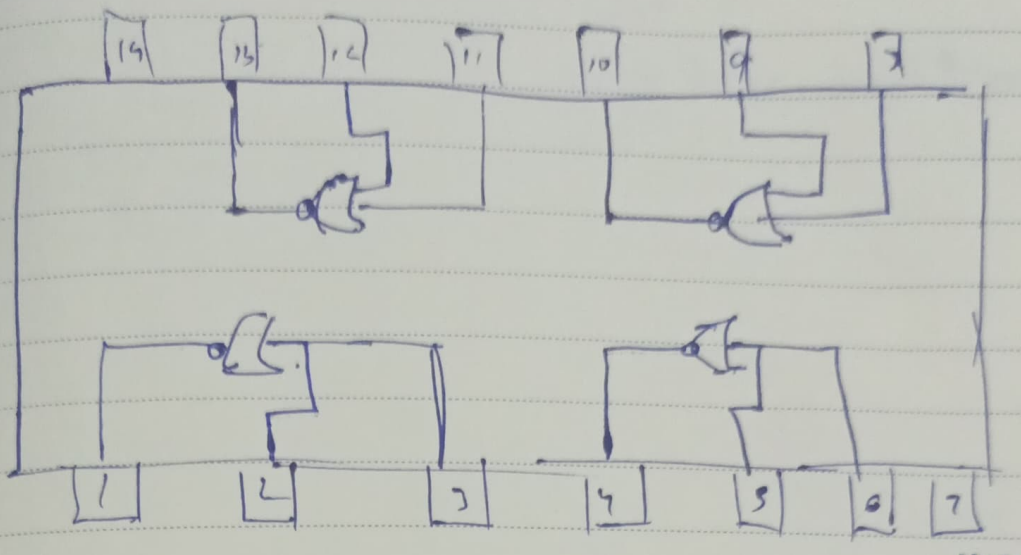


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

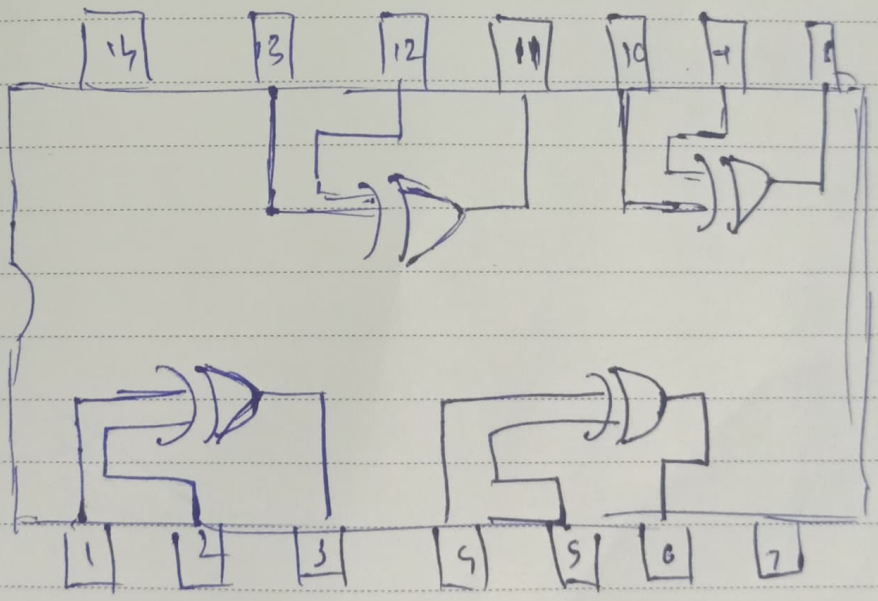
OR



NOR



XOR



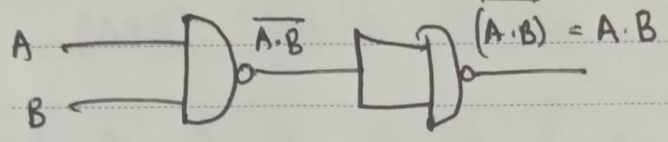
EZ 160101 23325

NOTES DATE

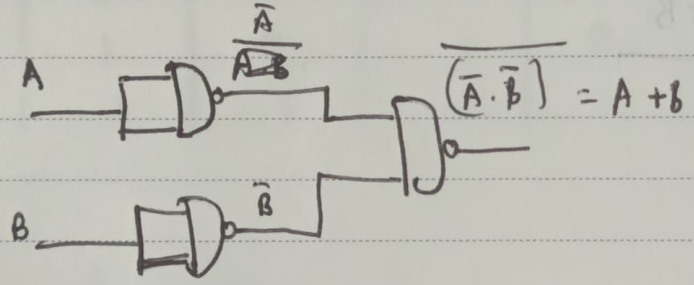
Basic Gates using Universal Gates

NAND : Y =

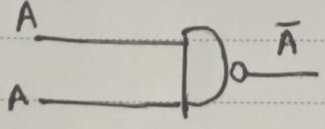
→ AND (Y = AB)



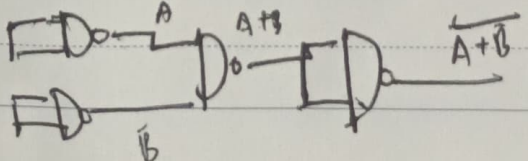
→ OR (Y = A+B)



→ NOT ($Y = \bar{A}$)

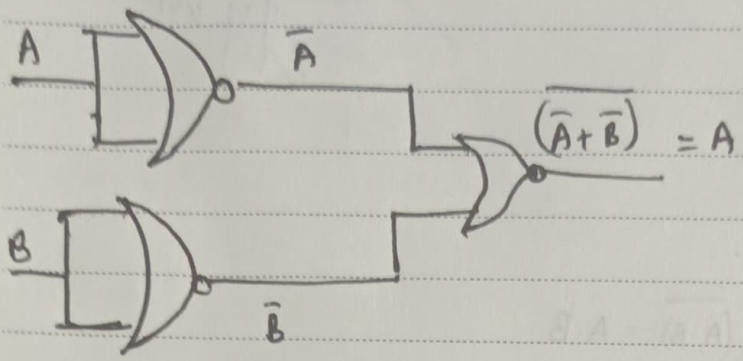


NOR ($Y = \overline{A+B}$)

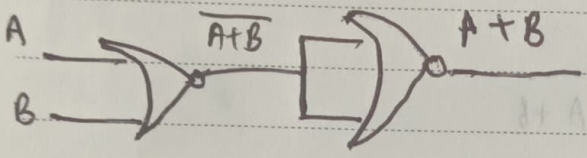


2] NOR

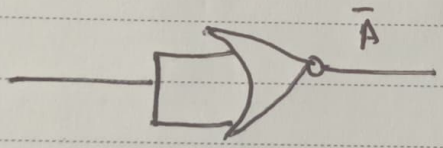
→ AND (Y = AB)



→ OR (Y = A+B)



→ NOT ($Y = \bar{A}$)



→ NAND