COMPUTER ORGANIZATION AND ARCHITECTURE

SYLLABUS and SCHEME

Course Code	Name of the Course			
216U01C304	Computer Organization and Architecture			
Teaching Scheme (Hrs./Week)	TH	P	TUT	Total
	03	-	-	03
Credits Assigned	03	-	-	03

Evaluation Scheme	Marks				
	LAB/TUT CA	CA (TH)		ESE	Total
		IA	ISE		
	-	20	30	50	100

Course pre-requisites: Basic concepts of computers and their applications.

Course Objectives: Students will try to:

1. Conceptualize the basics of organization and architecture of a digital computer and the detailed working of the ALU
2. Learn the function of each element of a memory hierarchy and detailed working of the control unit
3. Study various input output techniques and their applications

Course Outcomes (CO):

CO 1	Describe and define the structure of a computer with buses structure and detail working of the arithmetic logic unit and its sub modules
CO 2	Understand the Central processing unit with addressing modes and working of control unit in depth.
CO 3	Learn and evaluate memory organization and cache structure
CO 4	Summarize Input output techniques and multiprocessor configurations

Detailed Curriculum

Module No.	Unit No.	Contents	No of Hrs.	CO
———				
	1.1	Introduction of computer system and its sub modules, Basic organization of computer and block level description of the functional units. Von Neumann model, difference between computer architecture and computer organization.		
	1.2	Introduction to buses, bus types, and connection I/O devices to CPU and memory, PCI and SCSI		
2	**Arithmetic and Logic Unit**			
	2.1	Booth's Recoding and Booth's algorithm for signed multiplication, Restoring division and non-restoring division algorithms.	10	CO1
	2.2	IEEE floating point number representation and operations: Addition. Subtraction, Multiplication and Division. IEEE standards for Floating point representations :Single Precision and Double precision Format		
3	**Central Processing Unit**			
	3.1	CPU architecture, Register organization, Instruction formats and addressing modes(Intel processor).,Basic instruction cycle. Control unit Operation ,Micro operations : Fetch, Indirect, Interrupt , Execute cycle Control of the processor, Functioning of micro programmed control unit, Micro instruction Execution and Sequencing, Applications of Micro programming.	10	CO2
	3.2	RISC v/s CISC processors, RISC pipelining		
		Self learning: RISC and CISC Architecture, Case study on SPARC		

4	**Memory Organization**			
	4.1	Characteristics of memory system and hierarchy, Main memory, Cache memory principles , Elements of Cache Design.	**10**	**CO3**
	4.2	ROM, Types of ROM, RAM, SRAM, DRAM, Flash memory, High speed memories		
	4.3	Cache Memory Organization: Address mapping, Replacement Algorithms, Cache Coherence, MESI protocol, Interleaved and associative memories, Introduction to: Virtual memory, Main memory allocation, Segmentation ,Paging: demand paging and thrashing. Secondary storage, RAID levels		
5	**I/O Organization**		**03**	**CO4**
	5.1	External Devices, I/ O Modules		
	5.2	Programmed I/O, Interrupt driven I/O, DMA		

Module No.	Unit No.	Contents	No of Hrs.	CO
6	**Multiprocessor Configurations**		08	CO4
	6.1	Flynn's classification, Parallel processing systems and concepts, Introduction to pipeline processing and pipeline hazards.		
	6.2	Design issues of pipeline architecture, Instruction pipelining: Six Stage instruction pipeline.		
	6.3	8086 Instruction set (Arithmetic Instructions, Logical Instructions, Data transfer instructions), Assembly language programming.		

Sr. No.	Name/s of Author/s	Title of Book	Name of Publisher with country	Edition and Year of Publication
1.	W.Stallings William	Computer Organization and Architecture: Designing for Performance	Pearson Prentice Hall Publication	7th Edition
2.	Hamacher, V. Zvonko, S. Zaky	Computer Organization	Tata McGraw Hill Publication	5th Edition
3.	Hwang and Briggs	Computer Architecture and Parallel Processing	Tata McGraw Hill Publication	
4.	A. Tanenbaum	Structured Computer Organization	Prentice Hall Publication	4th Edition.
5.	John Uffenbeck	8086/8088 families: Design Programming and Interfacing	Pearson Education	
6.	Douglas Hall	Microprocessor and Interfacing	TMH Publication	

William Stallings
Computer Organization and Architecture

Chapter 1
Introduction

Architecture & Organization

- **Architecture** is those attributes **visible** to the programmer
  - Instruction set, number of bits used for data representation, I/O mechanisms, addressing techniques.

- **Organization** is **how** features are implemented
  - Control signals, interfaces, memory technology.
  - e.g. Is there a hardware multiply unit or is it done by repeated addition?

COMPUTER ARCHITECTURE	COMPUTER ORGANIZATION
Way hardware components are connected together to form a computer system.	**Structure and behaviour** of a computer system as **seen by the user**.
It acts as the interface between hardware and software.	It deals with the components of a connection in a system.
Helps us to understand the **functionalities** of a system.	How exactly all the **units in the system are arranged and interconnected.**
A programmer can **view architecture** in terms of **instructions, addressing modes and registers**.	Whereas Organization expresses the **realization of architecture.**
While **designing** a computer system **architecture is considered first**.	An organization is done on the basis of architecture.
Computer Architecture deals with high-level design issues.	Computer Organization deals with low-level design issues.
Architecture involves **Logic** (Instruction sets, Addressing modes, Data types, Cache optimization)	Organization involves **Physical Components** (Circuit design, Adders, Signals, Peripherals)

Architecture & Organization

- All **Intel x86** family share the same basic **architecture**
- The **IBM System/370** family share the same basic **architecture**
- This gives **code compatibility**
  - At least backwards
- **Organization** differs between different versions

S.NO	Processor	Clock Speed	Bus Width	MIPS	Power	Price
1	**Intel Pentium 111**	The clock speed of Intel Pentium 111 processor is 1GHz	The bus width of Intel Pentium 111 processor is 32	A million instructions per second of Intel Pentium 111 processor is ~900	The power of this processor is 97 W	$900
2	**IBM PowerPC 750X**	The clock speed of the IBM PowerPC 750X processor is 550 MHz	The bus width of the IBM PowerPC 750X processor is 32/64	A million instructions per second of IBM PowerPC 750X processor is ~1300	The power of this processor is 5 W	#900
3	MIPS R5000	The clock speed of the MIPS R5000 processor is 250 MHz	The bus width of the MIPS R5000 processor is 32/64	NA	NA	NA
4	StrongARM SA-110	The clock speed of StrongARM SA-110 processor is 233 MHz	The bus width of StrongARM SA-110processor is 32	The million instructions per second of StrongARM SA-110processor is 268	The power of this processor is 1 W	NA

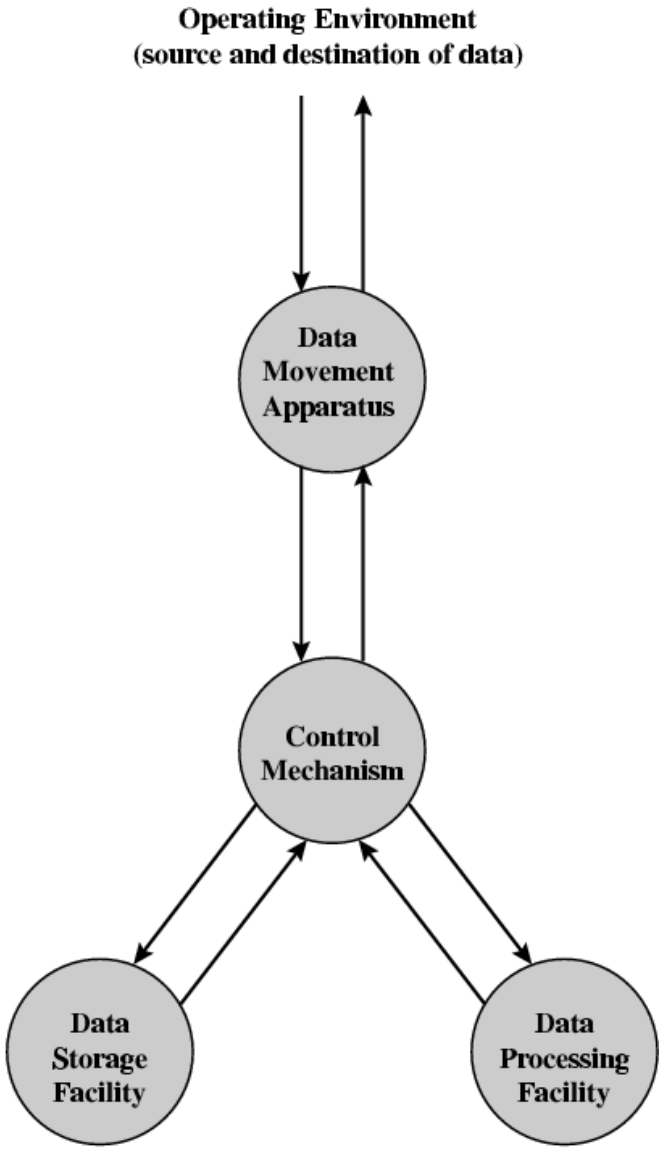
Structure & Function

- **Structure** is the way in which components relate to each other
- **Function** is the operation of individual components as part of the structure

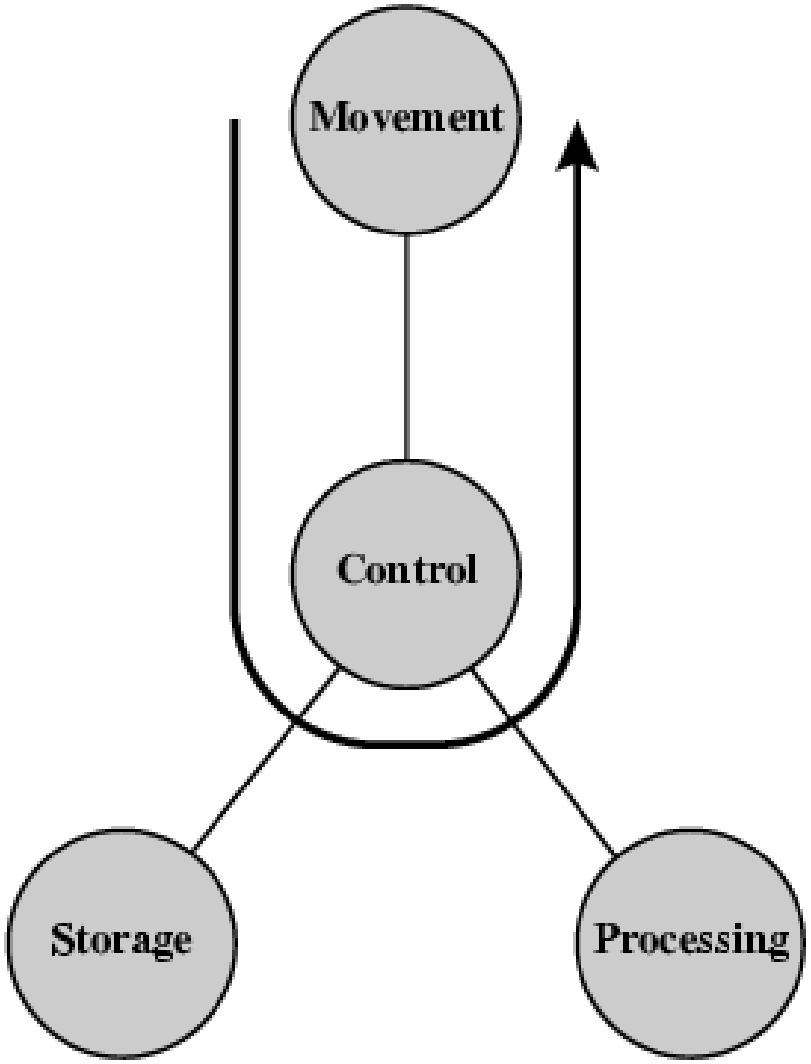
Function

- All computer **functions** are:
  - Data processing
  - Data storage
  - Data movement
  - Control

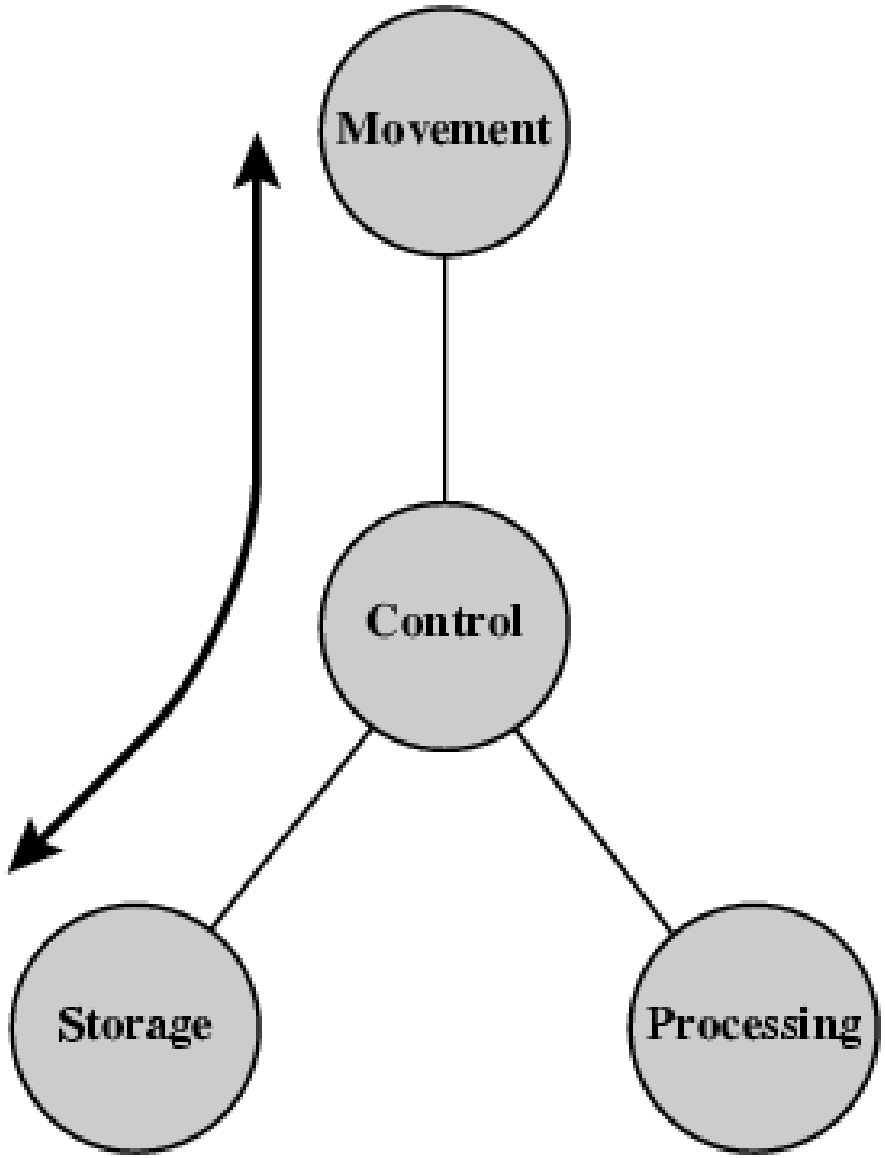
Functional View



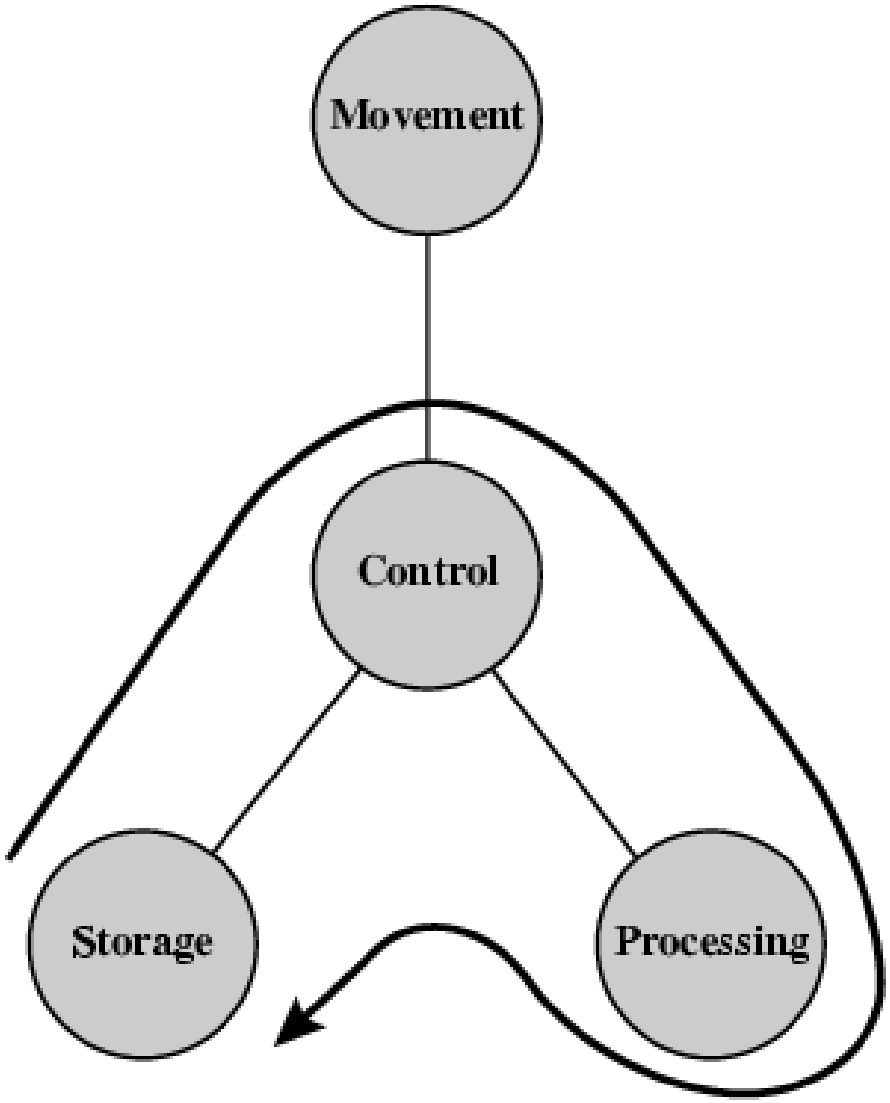
Operations (a) Data movement



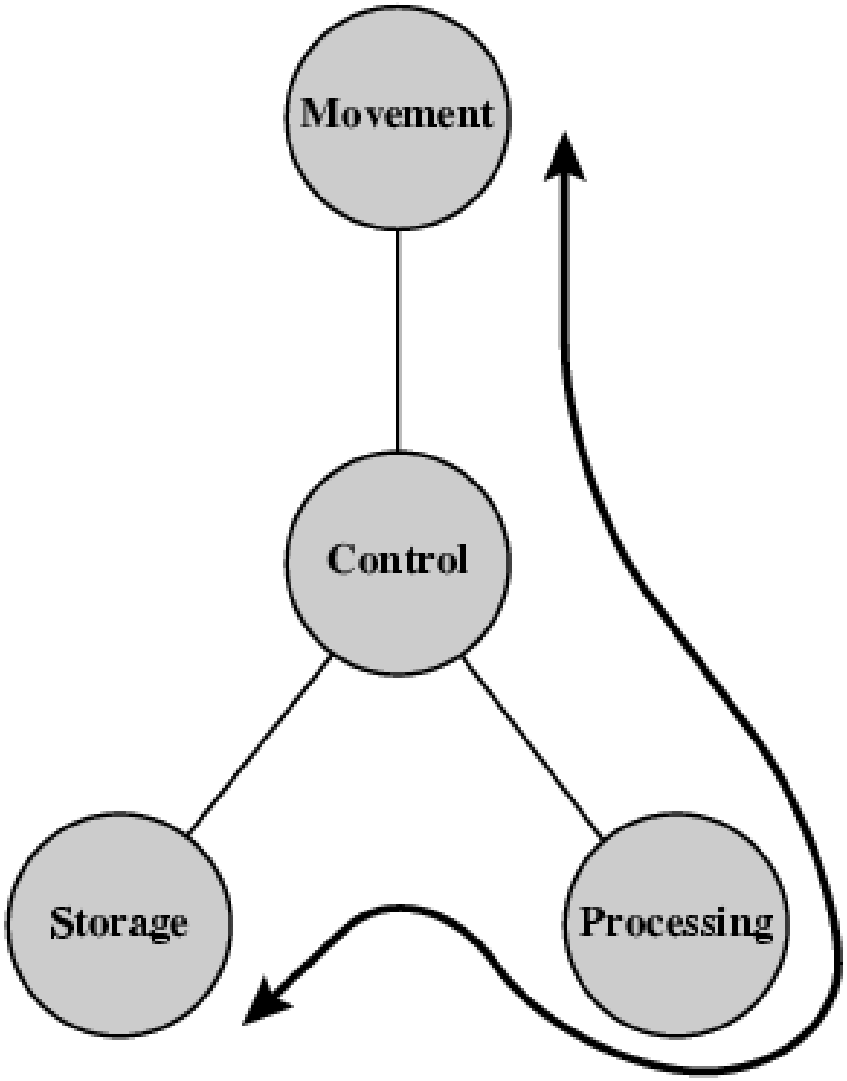
Operations (b) Storage



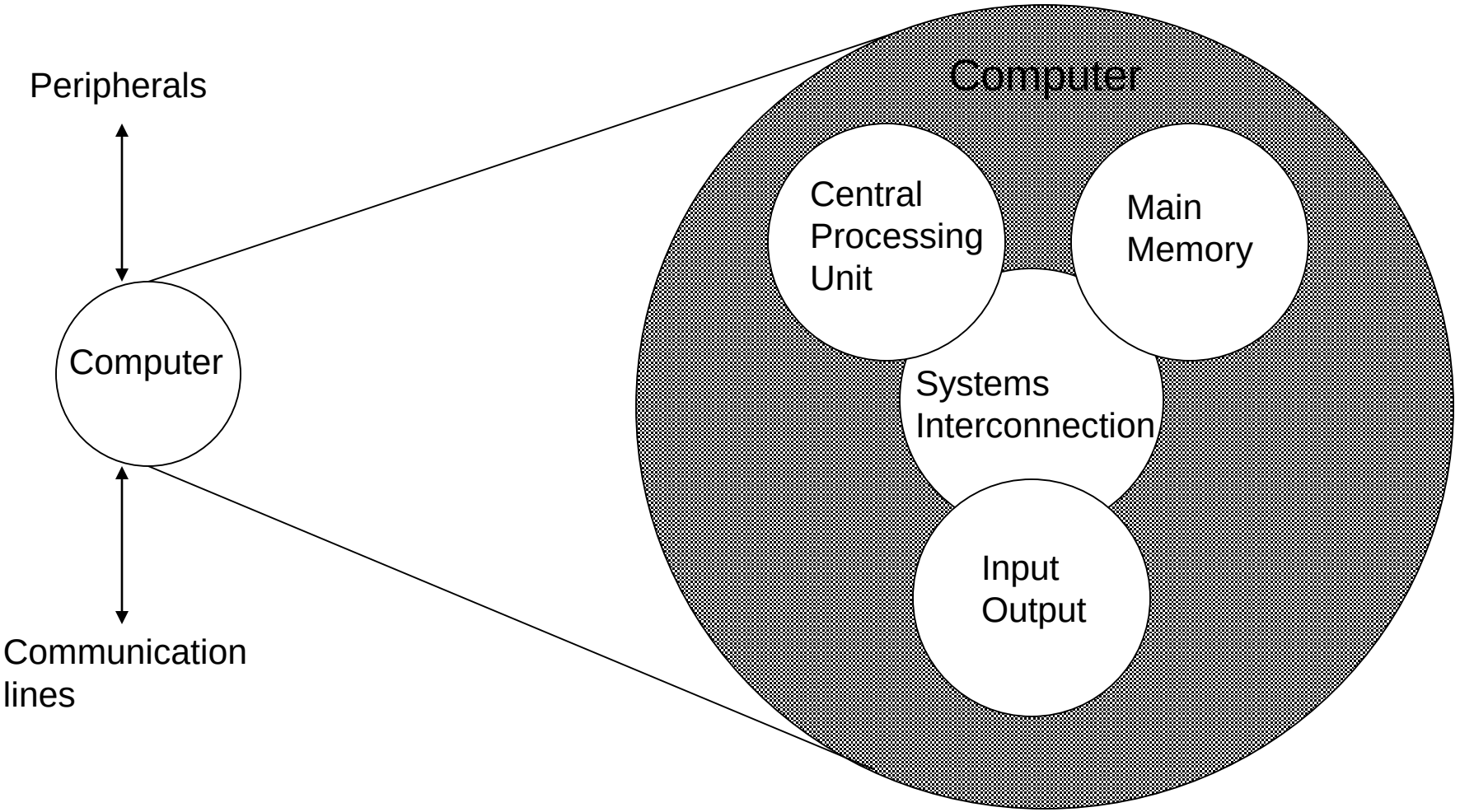
Operation (c) Processing from/to storage



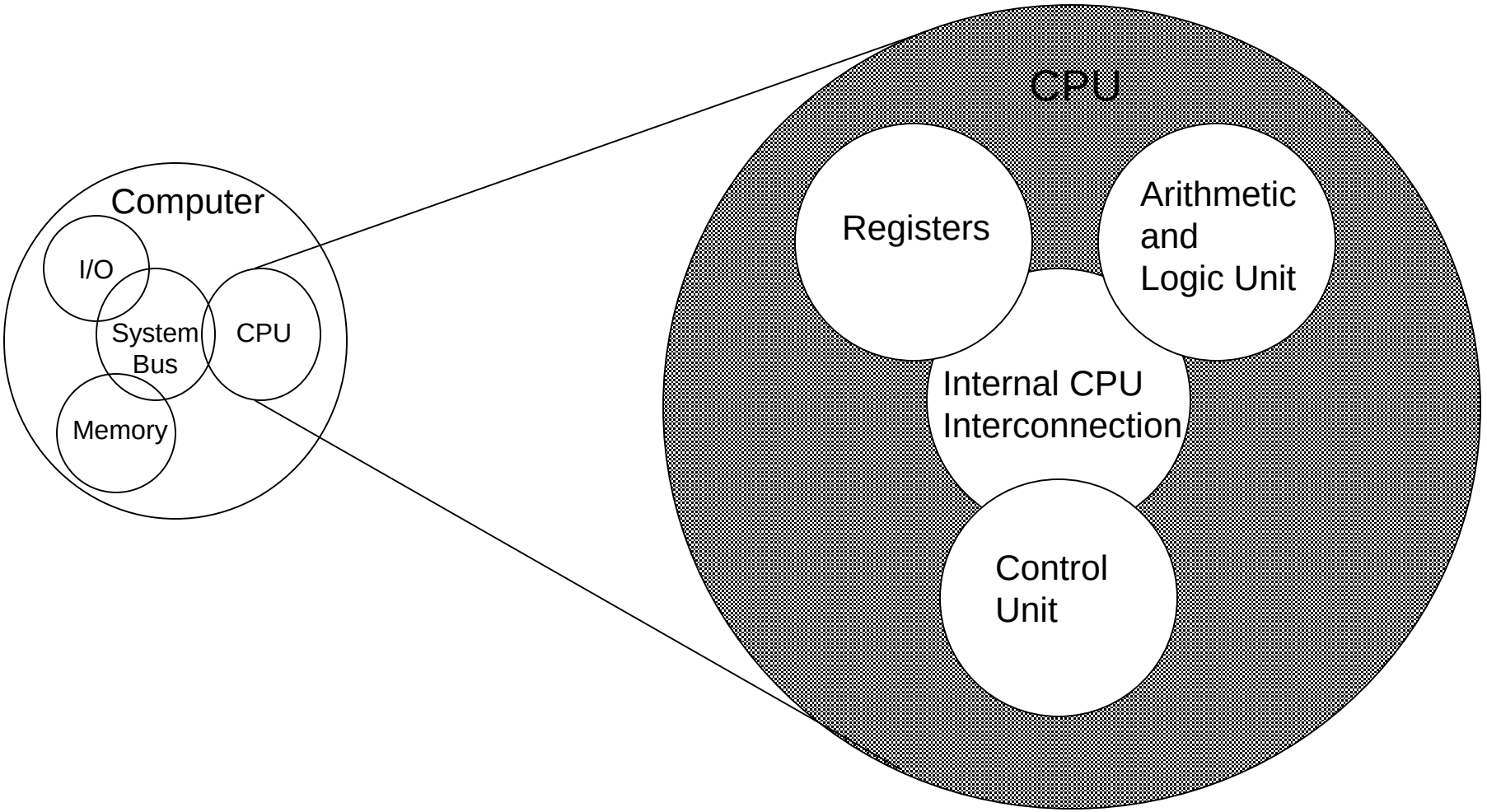
Operation (d)
Processing from storage to I/O



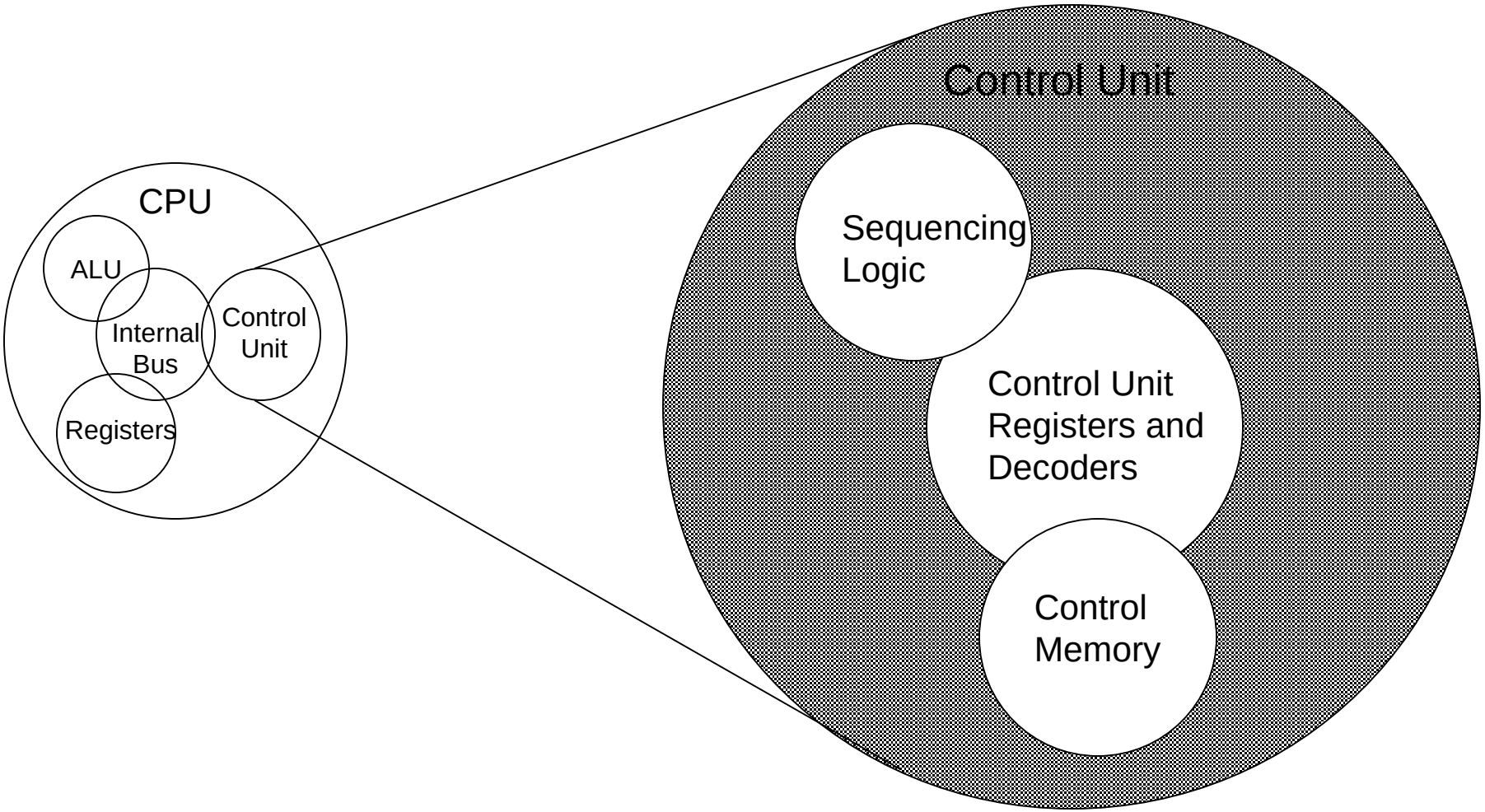
Structure - Top Level



Structure - The CPU



Structure - The Control Unit



William Stallings Computer Organization and Architecture 8th Edition

Chapter 2

Computer Evolution and Performance

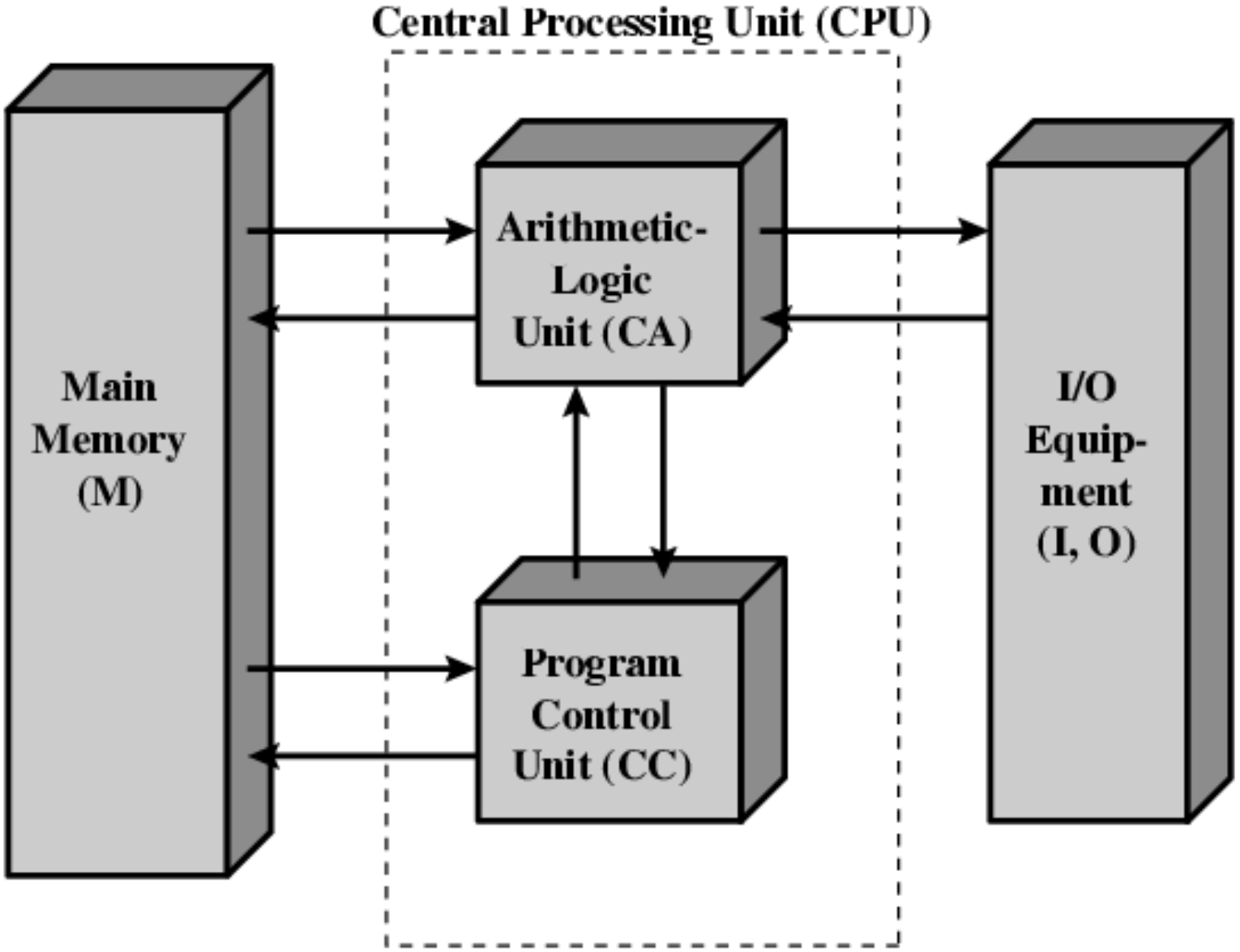
Von Neumann

- **Stored Program concept**

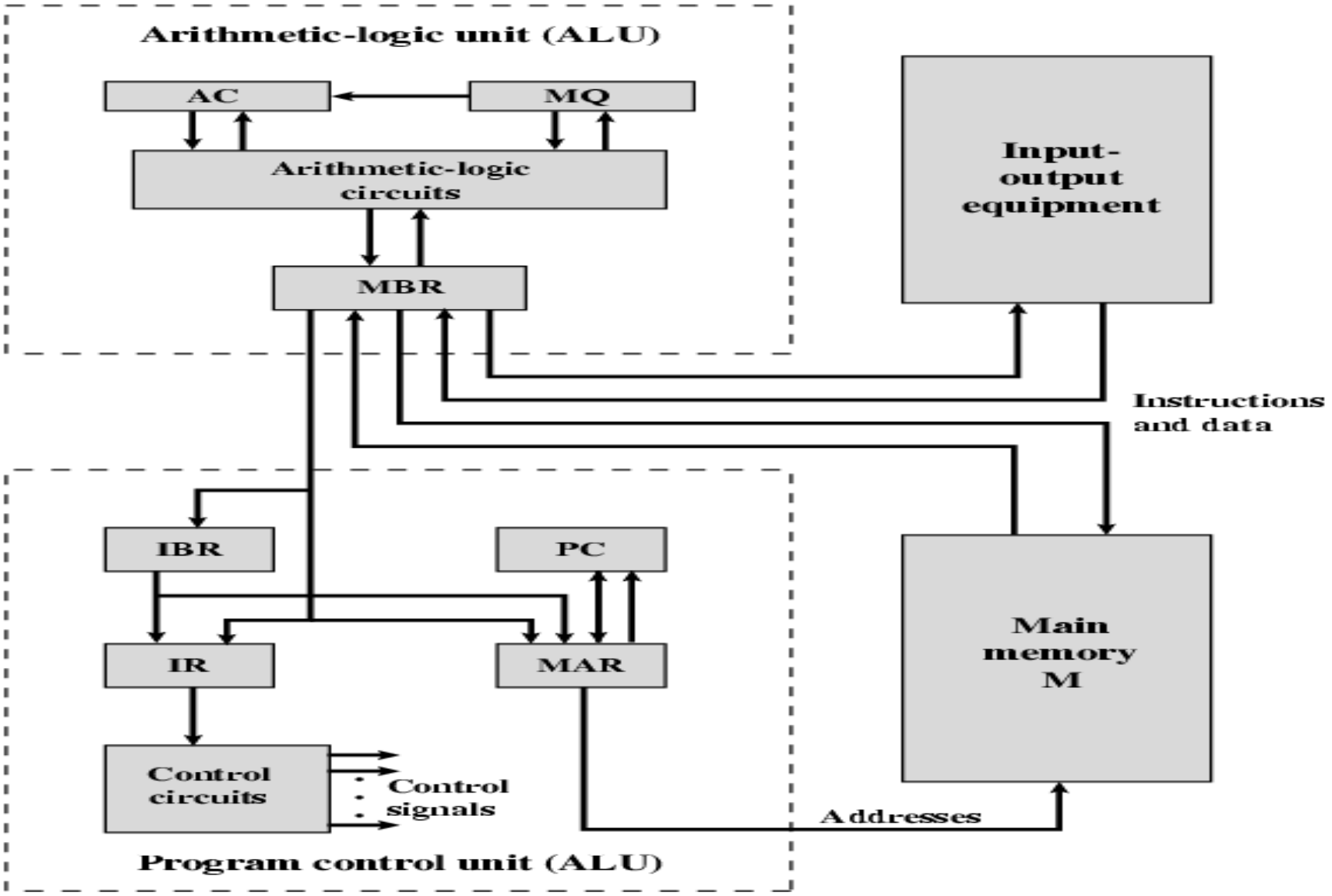
- **Main memory** storing programs and data
- **ALU** operating on binary data
- **Control unit** interpreting instructions from memory and executing
- **Input and output** equipment operated by control unit

- Princeton Institute for Advanced Studies
  - IAS
- Completed 1952

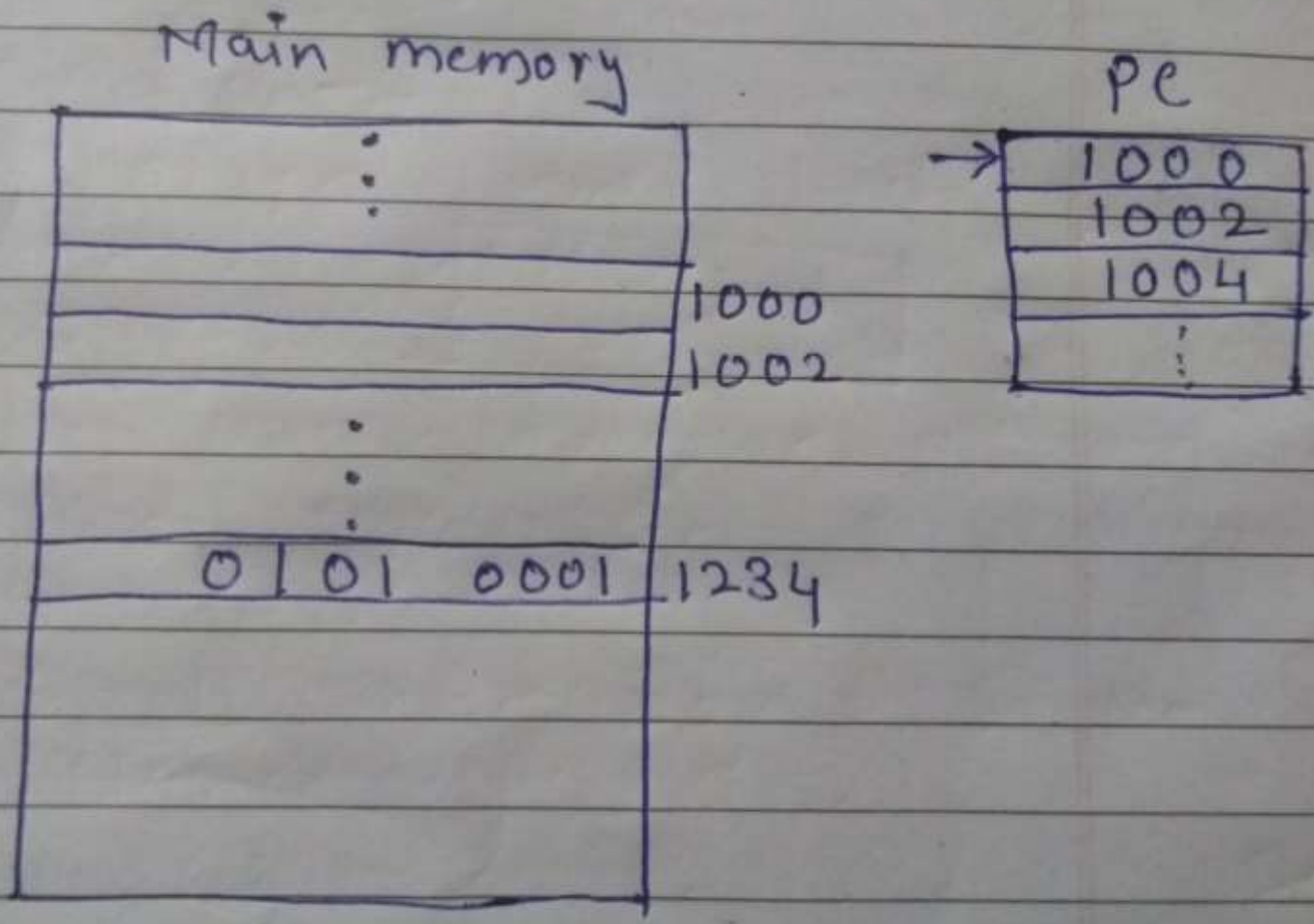
Structure of Von Neumann machine



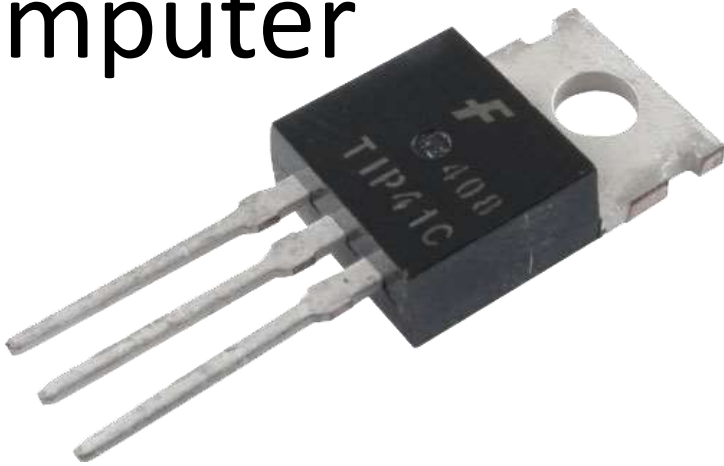
Structure of IAS – detail



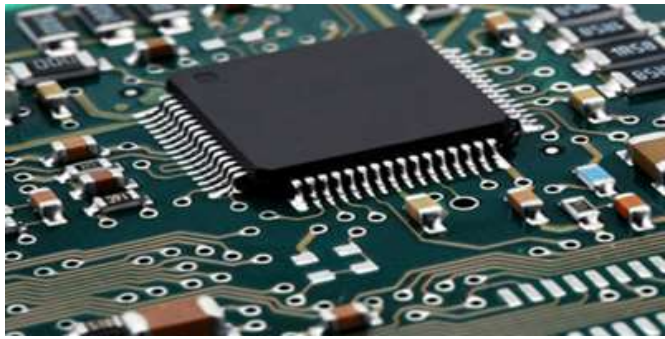
Add AX, BX
Add [1234], AX



Generations of Computer



- Vacuum tube - 1946-1957
- Transistor - 1958-1964
- Small scale integration - 1965
  - Up to 100 devices on a chip
- Medium scale integration - to 1971
  - 100-3,000 devices on a chip
- Large scale integration - 1971-1977
  - 3,000 - 100,000 devices on a chip



- Very large scale integration - 1978 -1991
  - 100,000 - 100,000,000 devices on a chip
- Ultra large scale integration – 1991 -Over 100,000,000 devices on a chip

Vacuum Tube

Transistors

Integrated Circuit

Microprocessor

Quantum Computer

1st Generation Computer

2nd Generation Computer

3rd Generation Computer

4th Generation Computer

5th Generation Computer

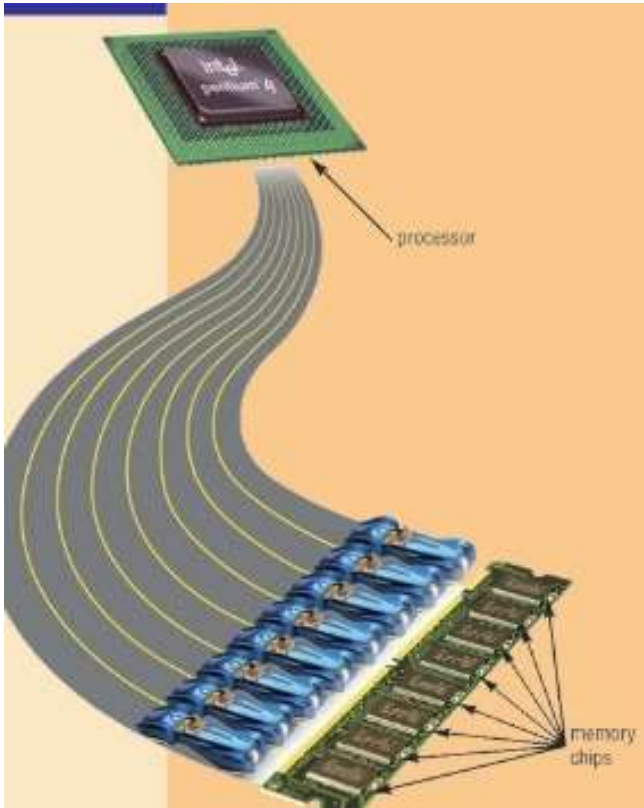
Subject	1st generation	2nd generation	3rd generation	4th generation	5th generation
Period	1940-1956	1956-1963	1964-1971	1971-present	present & beyond
Circuitry	Vacuum tube	Transistor	Integrated chips (IC)	Microprocessor (VLSI)	ULSI (Ultra Large Scale Integration) technology
Memory Capacity	20 KB	128KB	1MB	Magnetic core memory, LSI and VLSI. High Capacity	ULSI
Processing Speed	300 IPS instructions Per sec.	300 IPS	1MIPS (1 million inst. Per sec.)	Faster than 3rd generation	Very fast
Programming Language	Machine, Language	Assembly language & early high-level languages(FORTRAN, COBOL, ALGOL)	C,C++	Higher level languages,C,C++,Java	All the Higher level languages,,Neural networks,
Example of computers	UNIVAC, EDVAC	IBM 1401, IBM 7094, CDC 3600,D UNIVAC 1108	IBM 360 series, 1900 series	Pentium series,Multimedia,	Artificial Intelligence, Robotics

What is a Bus?

- A **communication pathway** connecting two or more devices
- Data connection between 2 or more devices connected to the computer
- Usually **broadcast** ,Often grouped
  - For Ex: A bus enables a computer processor to communicate with the memory or video card to communicate with the memory
  - e.g. 32 bit data bus is 32 separate single bit channels
- Power lines may not be shown

Buses

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus (PC)
- e.g. Unibus (DEC-PDP)



Functions of Buses in Computers

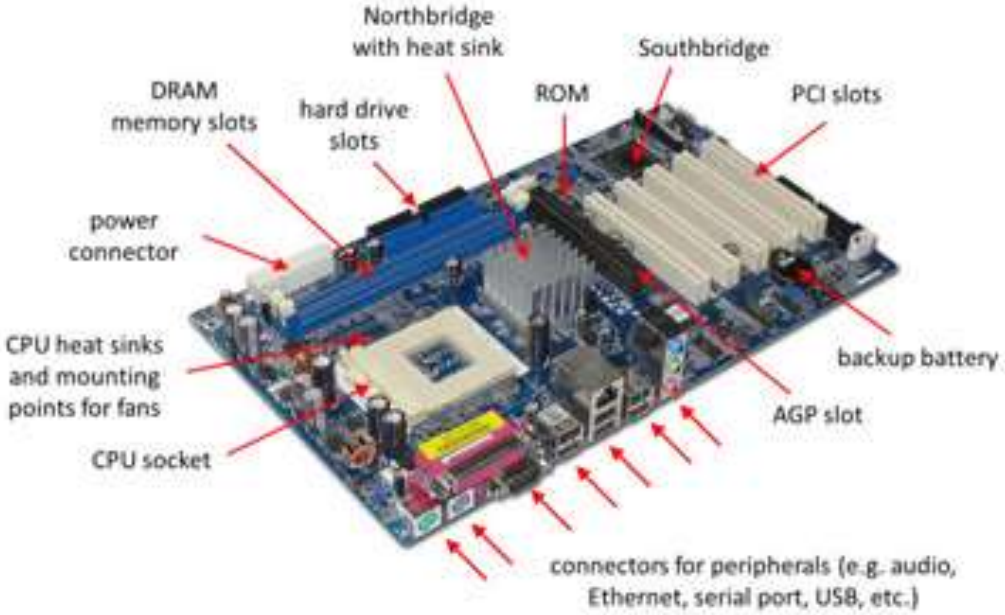
Data sharing - Serial/Parallel, 8-bit, 16-bit, 32-bit or even 64-bit buses.

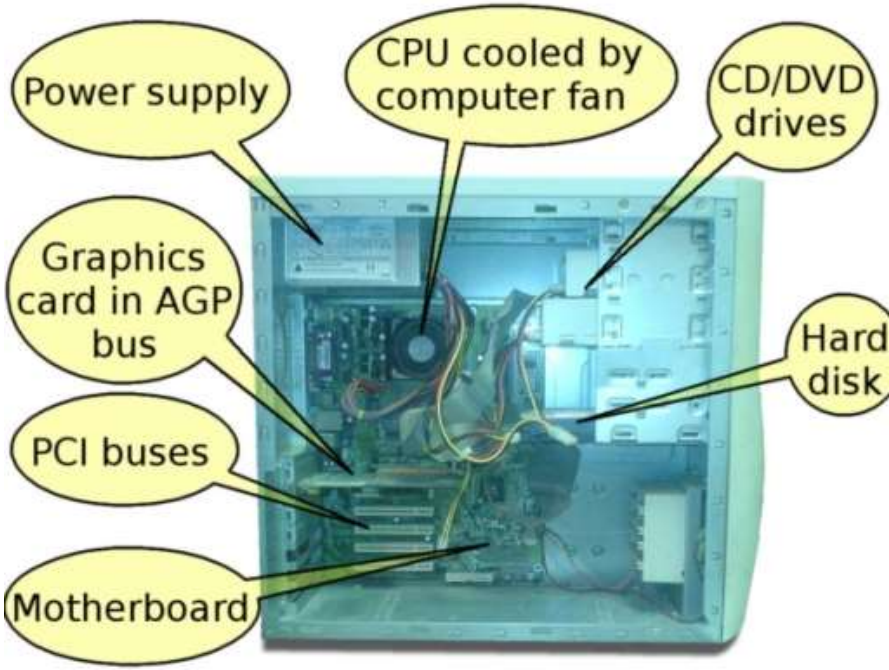
Addressing - A bus has address lines which allows data to be sent to or from specific memory locations.

Power - A bus supplies power to various peripherals connected to it.

Timing - System clock-**s**ynchronize the peripherals attached to it with the rest of the system.

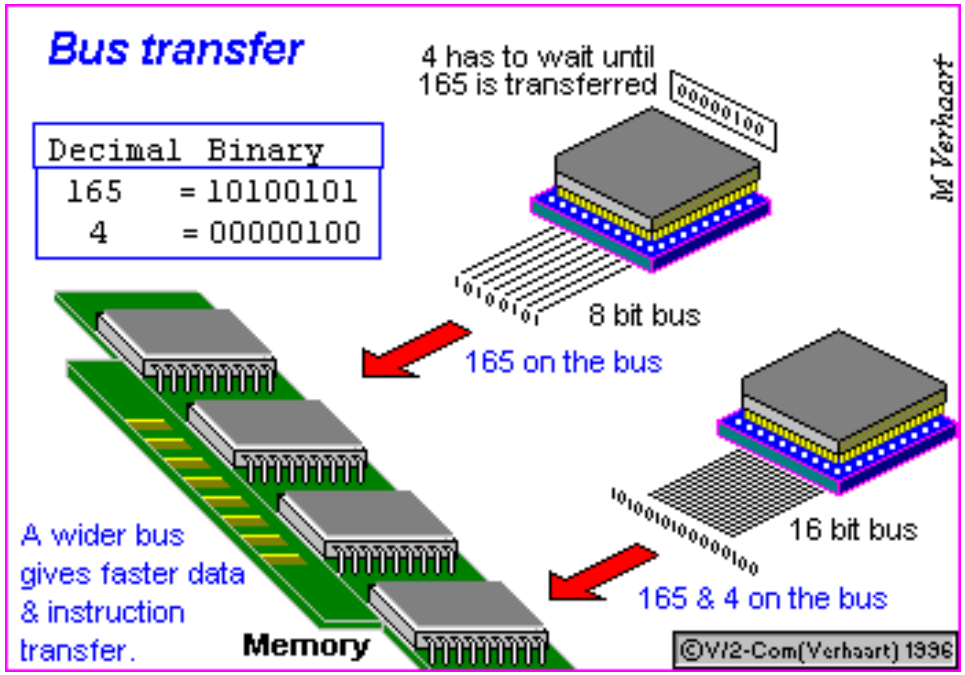
Eg: The expansion bus facilitates easy connection of more or additional components and devices on a computer such as a TV card or sound card.

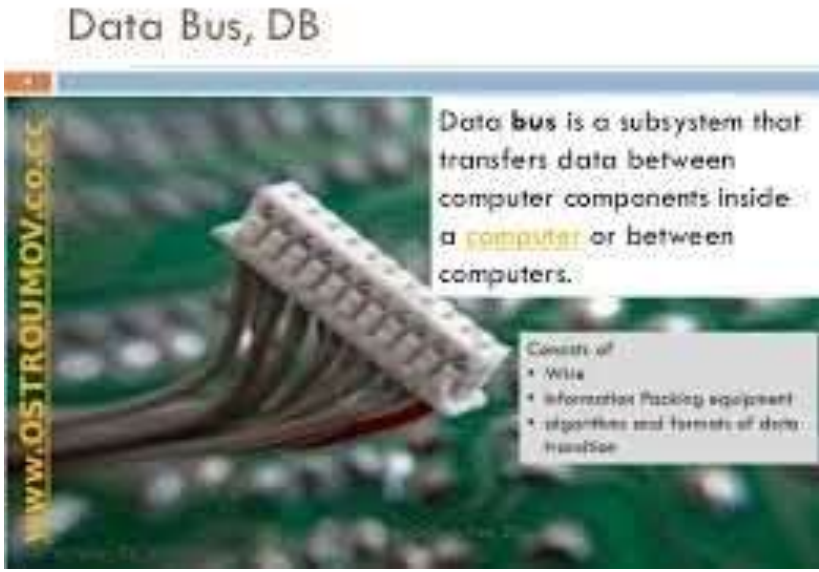

Northbridge
with heat sink
Southbridge
DRAM
memory slots
hard drive
slots
ROM
PCI slots
power
connector
CPU heat sinks
and mounting
points for fans
backup battery
AGP slot
CPU socket
connectors for peripherals (e.g. audio,
Ethernet, serial port, USB, etc.)


Power supply
CPU cooled by
computer fan
CD/DVD
drives
Graphics
card in AGP
bus
Hard
disk
PCI buses
Motherboard

Data Bus

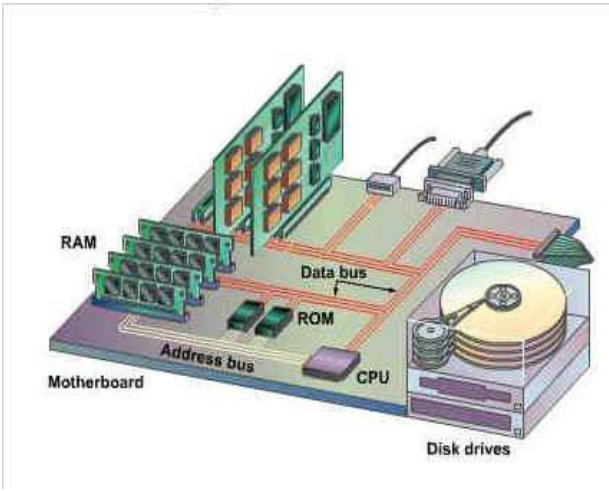
- Carries **data**
  - Remember that there is no difference between “data” and “instruction” at this level
- **Width** is a key determinant of performance
  - 8, 16, 32, 64 bit

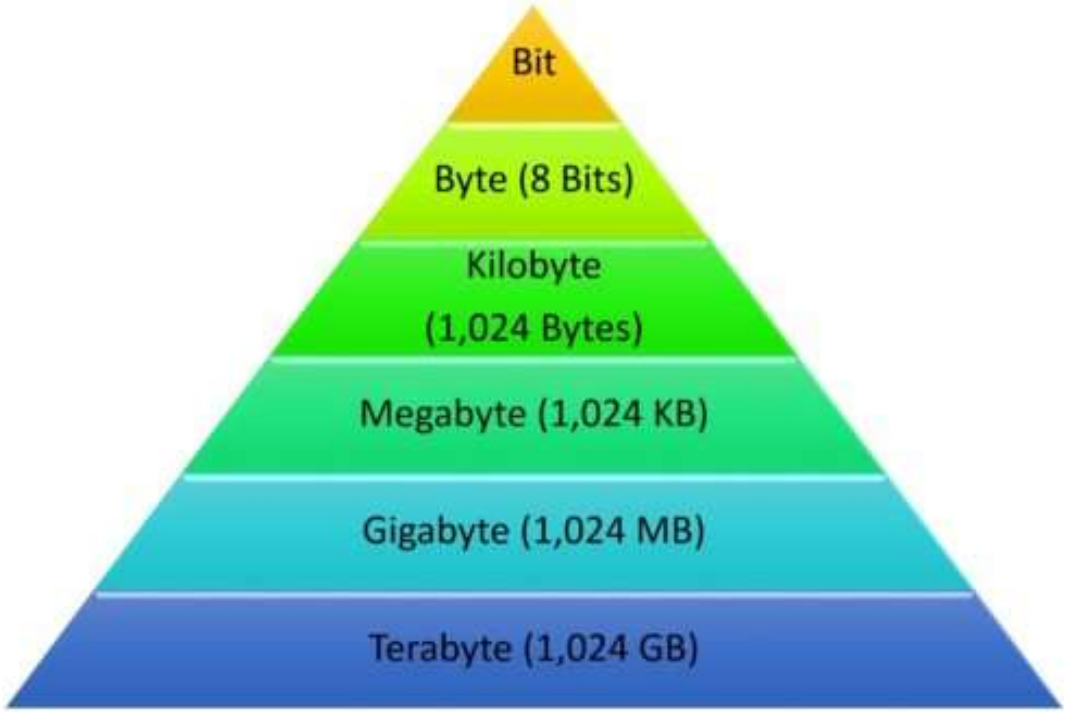




Address bus

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity of system
- 2 ^nos of address lines=Memory Capacity
  - e.g. 8080 has 16 bit address bus giving 64k address space
  - 32 bit?64bit ? 2 ^
  - (16.777216 million terabyte)



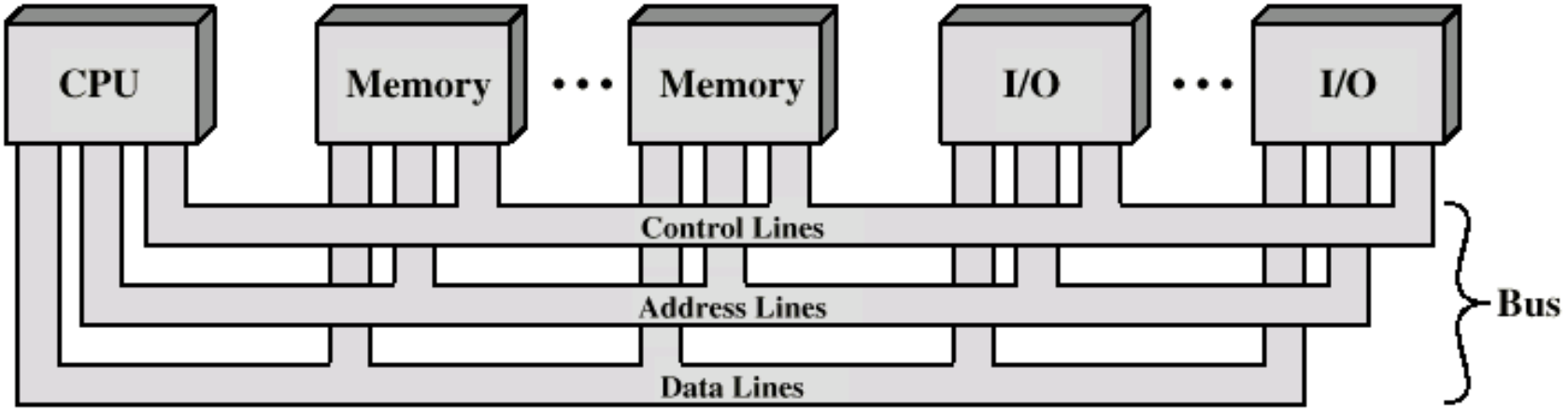


Megabyte	1,000,000 bytes
Gigabyte	1,000,000,000 bytes
Terabyte	1,000,000,000,000 bytes
Petabyte	1,000,000,000,000,000 bytes
Exabyte	1,000,000,000,000,000,000 bytes
Zettabyte	1,000,000,000,000,000,000,000 bytes
Yottabyte	1,000,000,000,000,000,000,000,000 bytes

Control Bus

- Controls activities of all units of a computer
- Main Function is to carry control signals generated by control unit
  - Ex: One line of control bus is used to indicate whether the CPU is reading/writing to the main memory
- Control and timing information
  - Memory read/write signal
  - Interrupt request
  - Clock signals

Bus Interconnection Scheme



Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
- Most systems use multiple buses to overcome these problems

Multiple Bus

problem can be countered to some extent by incr transfer demand rate that the bus can carry and by using wider buses.

Most computer systems enjoy the use of multiple buses. These buses ar rchy.

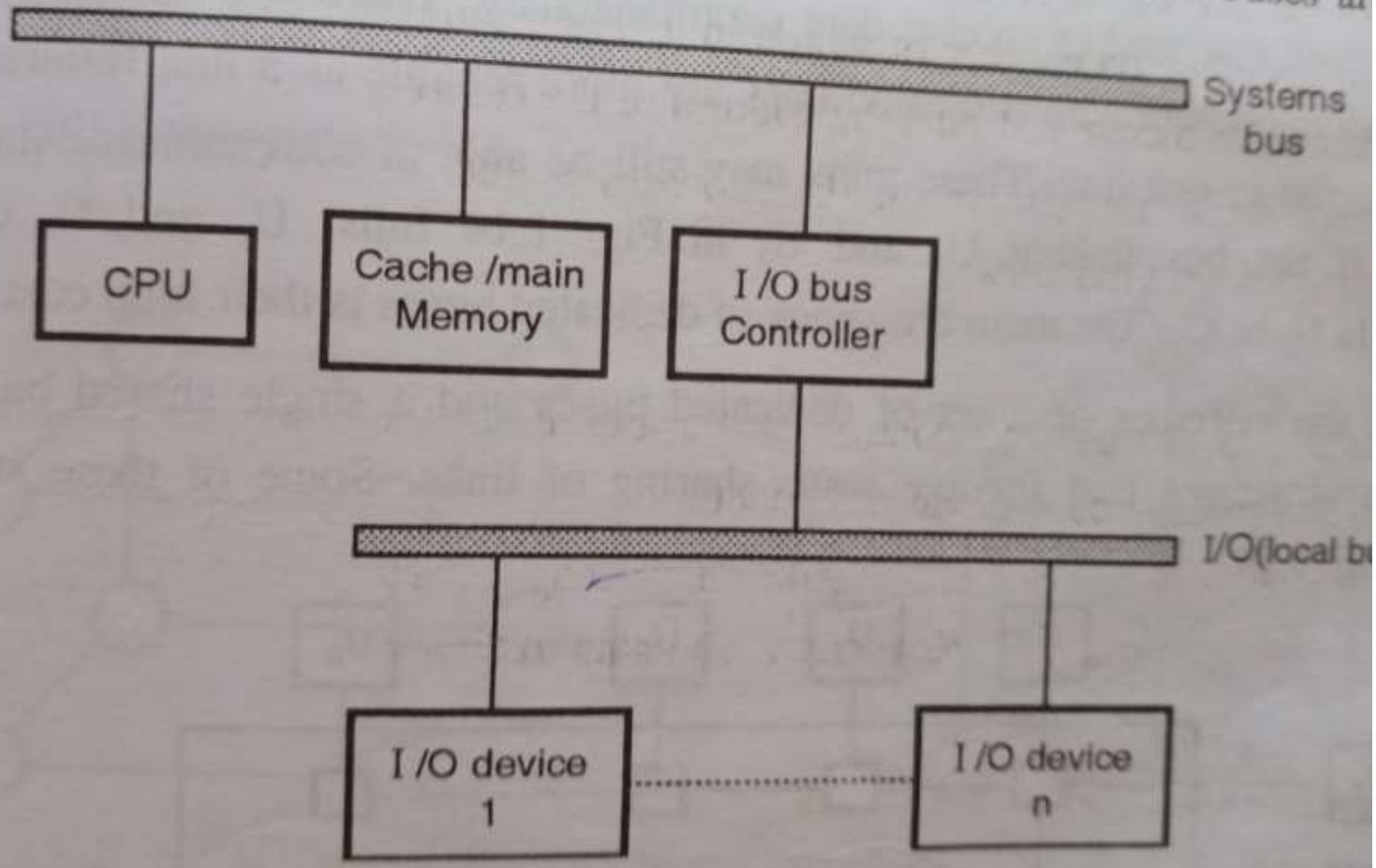


Fig. 1.12 : A multiple bus structure

Bus Types

- **Dedicated**
  - Separate data & address lines
- **Multiplexed**
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance

Bus Arbitration

- More than one module controlling the bus
- e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

Centralised or Distributed Arbitration

- Centralised
  - Single hardware device controlling bus access
    - Bus Controller
    - Arbiter
  - May be part of CPU or separate
- Distributed
  - Each module may claim the bus
  - Control logic on all modules

PCI Bus-Peripheral Component Interconnect

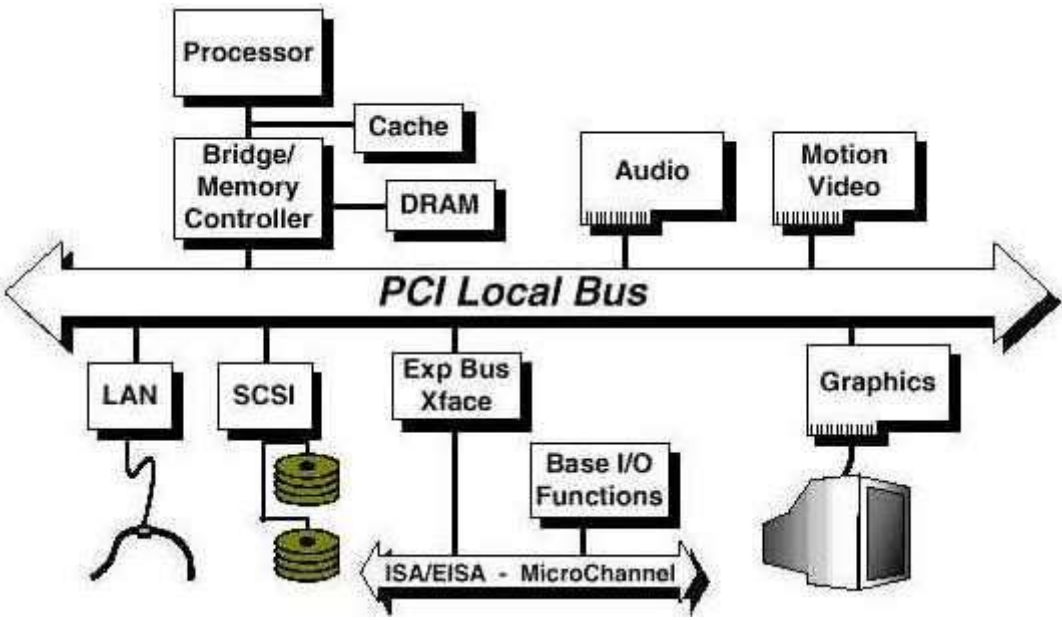
- Intel released to public domain-32 bit and 64 bit versions
- Plug and play facility.
- PCI bus connects the CPU and expansion boards
  - Examples of PCI devices
    - Modem
    - Network Card
    - Sound Card,Video Card,etc

PCI Bus-Peripheral Component Interconnect

- Coupling of the processor and expansion bus by means of a bridge
- 32-bit standard bus width with a maximum transfer rate of 133 Mbytes/s
- expansion to 64 bits with a maximum transfer rate of 266 Mbytes/s, – PCI-64/66 532 Mbytes/s,PCI-X 64/133 1064 Mbytes/s
- supporting of multi-processor systems
- burst transfers with arbitrary length
- supporting of 5 V and 3.3 V power supplies

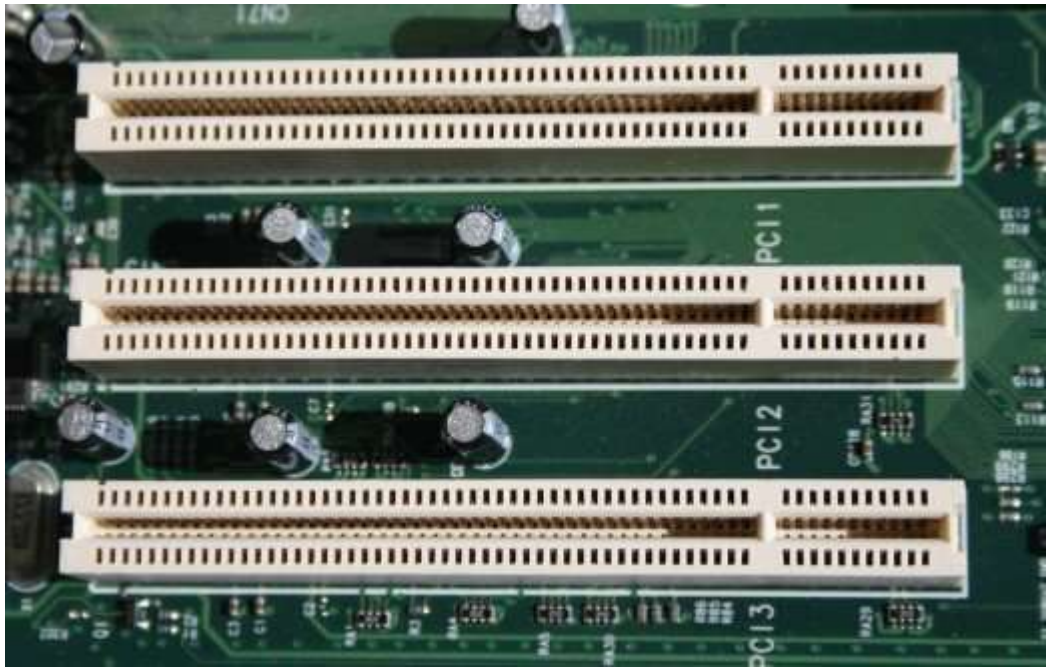
PCI Bus Lines (required)

- Systems lines
  - Including clock and reset
- Address & Data
  - 32 time mux lines for address/data
  - Interrupt & validate lines
- Interface Control
- Arbitration
  - Not shared
  - Direct connection to PC bus arbiter
- Error lines



PCI Bus Lines (Optional)

- Interrupt lines
  - Not shared
- Cache support
- 64-bit Bus Extension
  - Additional 32 lines
  - Time multiplexed
  - 2 lines to enable devices to agree to use 64-bit transfer



SCSI-Small Computer System Interface

- Set of standard electronic interfaces that allow personal computers **PC's to communicate with peripheral hardware** such as disk drives,tapes,CDs,Printers,scanners,etc
- Commonly used for hard disk drives and tape.
- Faster and more Flexibilty.
- SCSI standards are generally backward compatible
- SCSI interfaces have been replaced, for the most part, by Universal Serial Bus (USB)

SCSI-Small Computer System Interface

- It allows you to add up to 15 peripheral devices.
- SCSI is widely used in workstations, servers, and mainframes; it is less commonly used in desktop PCs.

SCSI-Small Computer System Interface

- **3 versions**

1. **8 bit 5 MB/s**
2. **16 bit 320 MB/s**
3. **32 bit 640 MB/s**

SCSI Bus

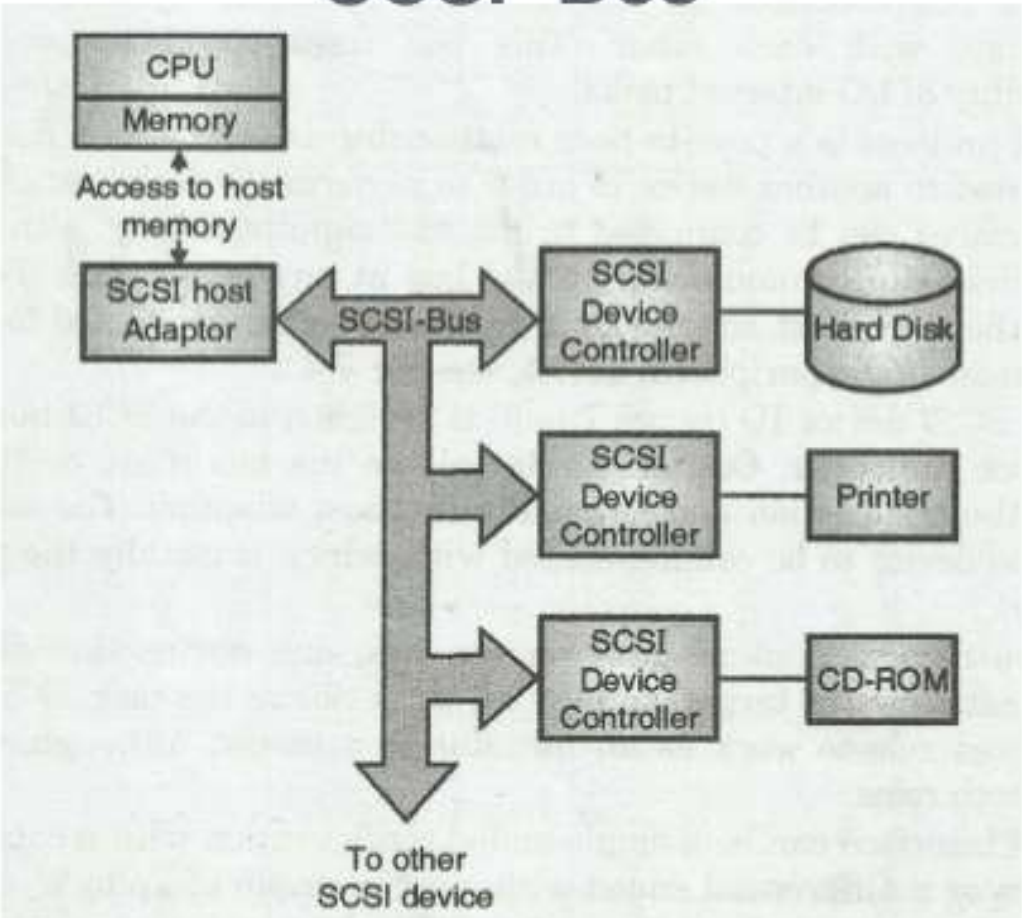
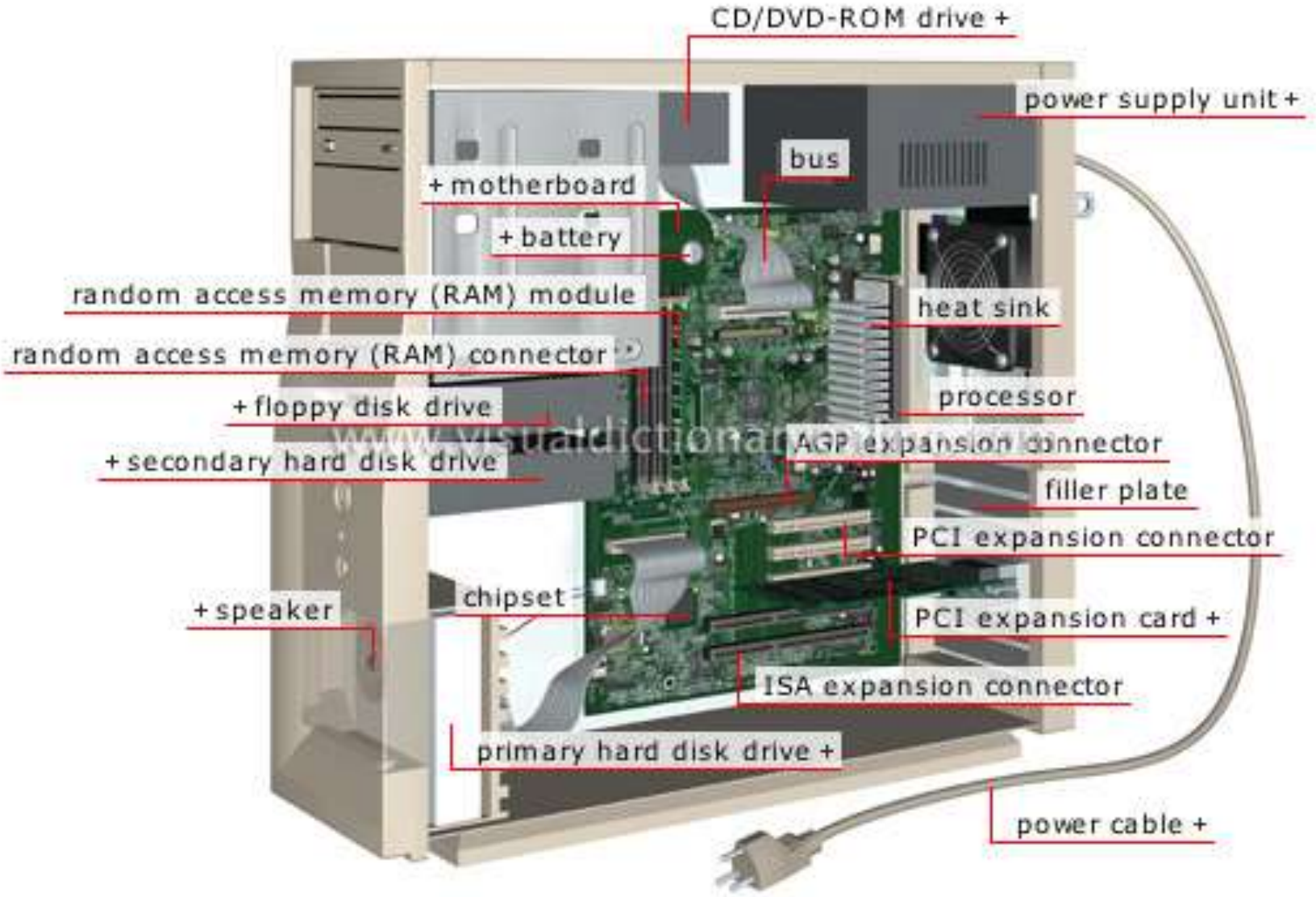


Fig. 7.4.2 : SCSI bus with host adapter and device controller


CD/DVD-ROM drive +
power supply unit +
bus
+ motherboard
+ battery
random access memory (RAM) module
heat sink
random access memory (RAM) connector
processor
+ floppy disk drive
AGP expansion connector
+ secondary hard disk drive
filler plate
PCI expansion connector
chipset
+ speaker
PCI expansion card +
ISA expansion connector
primary hard disk drive +
power cable +