BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

1

BIPOLAR JUNCTION TRANSISTORS

1.1 INTRODUCTION

In 1947, transistor was invented by Walter H. Brattain and John Bardeen at Bell laboratories. Transistor replaced vacuum tubes due to smaller size, light weight, less power consumption, lower operating voltages etc. Transistors can perform the function of current amplification and voltage amplification as well as power amplification. The amplification in transistor is obtained by passing the weak signal from low resistance region to high resistance region. Hence, the device is named as TRANSISTOR (TRANSsfer resISTOR).

1.2 TRANSISTOR CONSTRUCTION

A bipolar junction transistor is a three terminal semiconductor device containing two p-n junctions. When a p-type layer is placed between two n-type layers, an npn transistor is formed. Similarly when n-type layer is placed between two n-type layers, a pnp transistor is formed.

In each type of transistor, middle region is called base of the transistor and other two regions are called as emitter and collector. The physical size of the collector is greater than both emitter and base. The emitter is heavily doped while the base is lightly doped. The doping of collector is in between that of emitter and base. The pn junction joining the base region and the emitter region is called the emitter base junction. The pn junction joining the base region and the collector region is called collector base junction. The term bipolar refers to the use of both holes and electrons as charge carriers in the transistor structure.

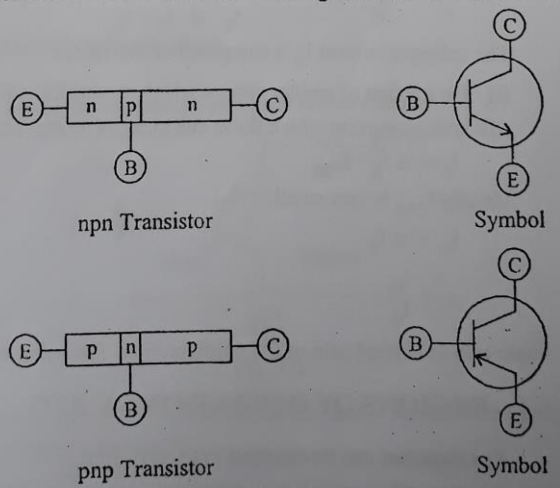

Fig. 1.1

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In the symbol shown, the arrowhead in the emitter shows the direction of conventional current which is opposite to the flow of electrons. In npn transistor, conventional current flows out of emitter while in pnp transistor, the conventional current flows into the emitter.

1.3 WORKING OF BJT

For proper working of BJT, emitter base junction is forward biased and collector base junction is reverse biased. The forward bias from base to emitter narrows the emitter base depletion region and the reverse bias from base to collector widens the collector base depletion region.

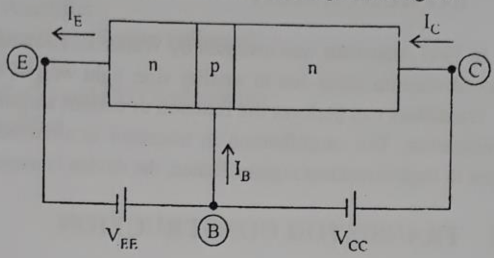

Fig. 1.2

When emitter base junction is forward biased, the majority carriers i.e. electrons from N-type emitter will get pushed towards the base junction. If the forward bias voltage is more than the knee voltage (0.7 V for silicon transistor and 0.3 V for germanium transistor), the electrons will flow into the base junction. Since the base region is very thin and lightly doped, very few of the electrons recombine with holes. This constitutes the base current(I_B).These diffused electrons are minority carriers in the base region. The minority carries can easily cross the junction. Hence most of the electrons diffuse to the reverse biased collector base junction and constitutes the collector current (I_C).

Applying Kirchhoff's current law to the transistor,

$$I_E = I_B + I_C$$

The collector current I_C is composed of two parts :

(i) the fraction of emitter current which reaches the collector,

(ii) leakage current which flows due to minority carriers.

$$I_C = \alpha I_E + I_{CBO}$$

Usually I_{CBO} is very small.

$$I_C = \alpha I_E$$

$$\alpha = \frac{I_C}{I_E}$$

where α is dc current gain of CB configuration. The value of α lies between 0.9 to 0.995.

1.4 REGIONS OF OPERATION OF BJT

Any transistor can be operated in three regions :

(i) Cut-off : In this region, both emitter base and collector base junctions are reverse biased.

(ii) Active : In this region, emitter base junction is forward biased and collector base junction is reverse biased.

(iii) Saturation : In this region, both emitter base and collector base junctions are forward biased.

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1.5 BJT CONFIGURATIONS

Depending upon common terminal, there are three possible configurations :

(i) Common Base (CB) configuration

(ii) Common Emitter (CE) configuration

(iii) Common Collector (CC) configuration

1.5.1 Common Base Configuration

In this configuration, the input is applied between emitter and base and output is taken from collector and base. Thus base is common to both input and output circuit.

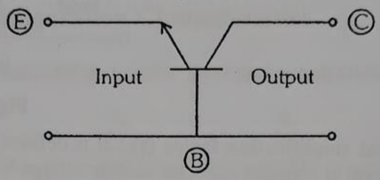

Fig. 1.3

Current amplification factor (α) : It is defined as the ratio of change in collector current to the change in emitter current at constant collector base voltage V_{CB}.

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$

If only dc values are considered,

$$\alpha_{dc} = \frac{I_C}{I_E}$$

1.5.2 Common Emitter Configuration

In this configuration, emitter is common to input and output circuit.

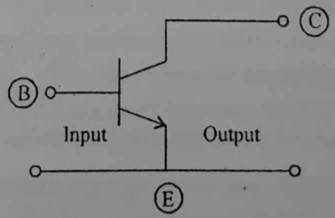

Fig. 1.4

Current amplification factor (β) : It is defined as the change in collector current to the change in base current at constant collector emitter voltage V_{CE}.

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

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If only dc values are considered,

$$\beta_{dc} = \frac{I_C}{I_B}$$

1.5.3 Common Collector Configuration

In this configuration, collector is common to input and output circuit.

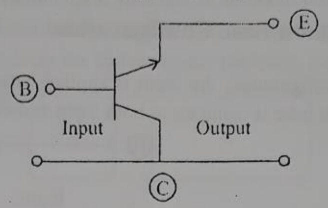

Fig. 1.5

Current amplification factor (γ) : It is defined as the ratio of change in emitter current to the change in base current at constant collector emitter voltage V_{CE}.

$$\gamma_{ac} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

If only dc values are considered,

$$\gamma_{dc} = \frac{I_E}{I_B}$$

1.6 RELATION BETWEEN α AND β

$$I_E = I_B + I_C$$

Also,

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$= \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

$$= \frac{\Delta I_C / \Delta I_E}{1 - \Delta I_C / \Delta I_E}$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \left(\alpha = \frac{\Delta I_C}{\Delta I_E}\right)$$

1.7 EXPRESSION FOR COLLECTOR CURRENT (I_C)

We know that,

$$I_E = I_B + I_C \qquad \ldots (1.1)$$

Also

$$I_C = \alpha I_E + I_{CBO} \qquad \ldots (1.2)$$

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Substituting I_E in equation (1.2),

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$= \beta I_B + (\beta + 1) I_{CBO}$$

1.8 TRANSISTOR CHARACTERISTICS

1.8.1 Common Base Configuration Characteristics

Fig. 1.6 shows the experimental set up to draw input and output characteristics in CB configuration.

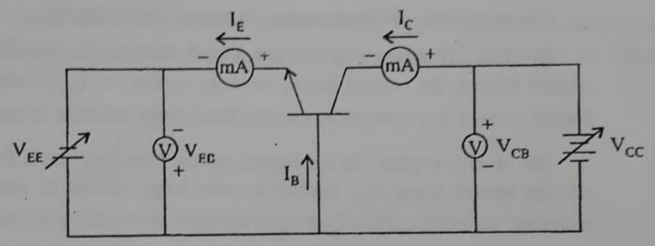

Fig. 1.6

Input characteristics

It is the graph of input current I_E versus input voltage V_{BE} when output voltage V_{CB} is kept constant.

For a given V_{CB}, the input characteristic resembles the characteristic of forward biased diode. Input current I_E increases as input voltage V_{BE} increases for fixed value of V_{CB}. For a given value of V_{BE}, I_E increases with increase in V_{CB} due to early effect.

As V_{CB} increases, width of the depletion layer in the base increases. Hence the width of the base available for conduction decreases. The reduction in the width of the base due to increase in reverse bias is known as **early effect**. Due to early effect, the chances of recombination of electrons with the holes in the base decreases. Therefore, base current decreases but more electrons can travel from emitter to collector terminal. Therefore, collector current increases with increase in emitter current I_E.

As reverse bias voltage V_{CB} further increases, at one stage the depletion region completely occupies the base at which collector base junction breaks down. This phenomenon is known as punch-through.

Dynamic input resistance $\quad r_i = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$

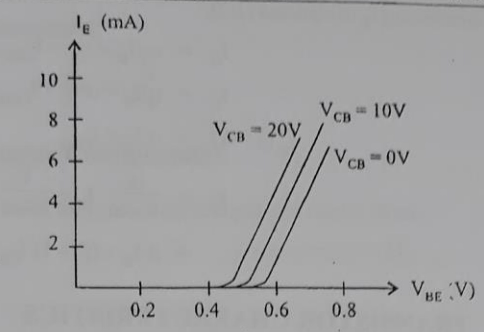

Fig. 1.7

Output characteristics

It is the graph of output current I_C versus output voltage V_{CB} for given values of I_E.

There are three different regions in output characteristics :

(i) Cut-off region : In this region, both the junctions are reverse biased. When emitter-base junction is reverse biased, the current due to majority carrier i.e. I_E is zero. Since collector-base junction is reverse biased, current due to minority carriers flows from collector to base which is represented as I_{CBO}.

(ii) Active region : In this region, emitter-base junction is forward biased and collector base junction is reverse biased. Once V_{CB} reaches a value large enough to ensure a large portion of electrons enter the collector, collector current I_C remains constant as shown by horizontal lines. As I_E increases, I_C increases.

(iii) Saturation region : In this region, both the junctions are forward biased. When V_{CB} is negative, collector base junction is actually forward biased. Thus the graphs are drawn on negative side of V_{CB}. In this region, there is large change in collector current with small increase in voltage V_{CB}.

Output resistance $\quad r_o = \left.\dfrac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}$

Current gain $\quad \alpha_{ac} = \left.\dfrac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$

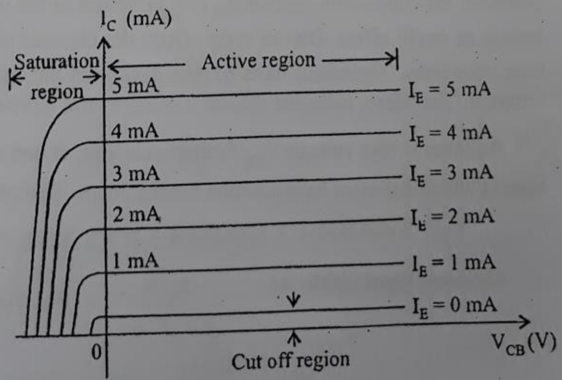

Fig. 1.8

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1.8.2 Common Emitter Configuration Characteristics

Fig 1.9 shows the experimental set up to draw input and output characteristics in CE configuration.

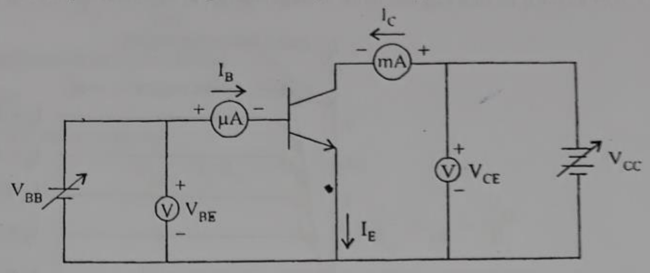

Fig. 1.9

Input characteristics

It is the graph of input current I_B versus input voltage V_{BE} at a constant output voltage V_{CE}. It resembles the characteristics of forward biased diode. Input current I_B increases as input voltage V_{BE} increases for fixed value of V_{CE}.

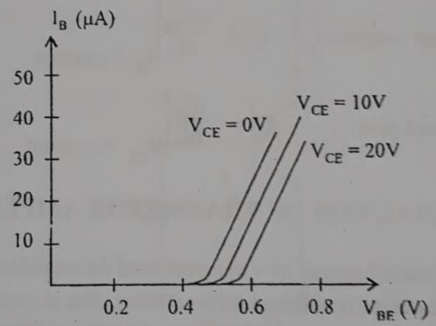

Fig. 1.10

As reverse bias voltage V_{CE} increases, depletion region in collector base increases. Hence the width of base available for conduction decreases. Hence I_B decreases due to early effect and graph shift towards X-axis.

$$\text{Dynamic input resistance} \quad r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

Output characteristics

It is the graph of output current I_C versus output voltage V_{CE} for given values of I_B. The output characteristics has three different regions :

(i) Cut-off region : In this region, both the junctions are reverse biased. When emitter base junction is reverse biased, the current due to majority carrier i.e. I_B is zero. Since collector-base junction is reverse biased, the current due to minority carriers flows from collector to emitter which is represented as I_{CEO}.

(ii) Active region : In this region, emitter base junction is forward biased and collector-base junction is reverse biased. As I_B is maintained constant, current I_C increases as reverse bias voltage V_{CE} increases.

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(iii) Saturation region : In this region, both the junctions are forward biased. When V_{CE} is reduced to a small value such as 0.2 V, collector base junction is actually forward biased ($V_{CB} = V_{CE} - V_{BE} = 0.2 - 0.7 = -0.5$ V). In this region, there is large change in collector current I_C with small change in V_{CE}.

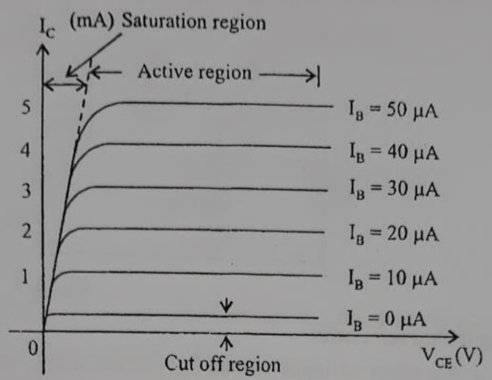

Fig. 1.11

Output resistance $\quad r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}$

Current gain $\quad \beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$

1.9 ANALYSIS OF TRANSISTOR AMPLIFIER (BJT as voltage amplifier)

The basic function of a transistor is to do amplification. The weak signal is given to the transistor and amplified output is obtained from collector. The process of raising the strength of weak signal without any change in its general shape is known as faithful amplification.

Fig. 1.12 shows basic CE amplifier. The battery V_{BB} forward biases emitter base junction and V_{CC} reverse biases collector base junction. R_B is current limiting resistor. Capacitor C_{C2} is used to couple ac output of the amplifier to load resistance R_L. Capacitor C_{C1} is dc blocking capacitor.

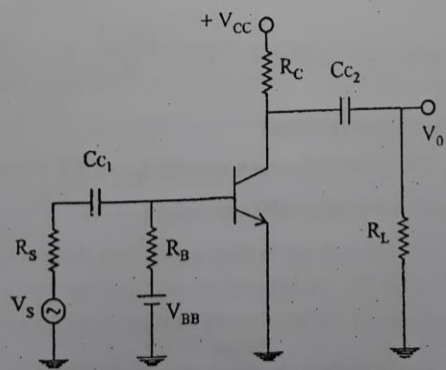

Fig. 1.12

DC analysis

For dc, $f = 0$

$$X_C = \frac{1}{2\pi fc} = \infty$$

Hence capacitors act as open circuits.

DC load line

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \ldots (1.3)$$

Equation (1.3) represents dc load line with slope of $-\frac{1}{R_C}$ and y-intercept of $\frac{V_{CC}}{R_C}$

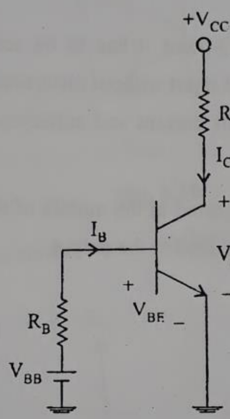

Fig. 1.13

Putting $I_C = 0$ in equation (1.3),

$$V_{CE} = V_{CC}$$

Putting $V_{CE} = 0$ in equation (1.3),

$$I_C = \frac{V_{CC}}{R_C}$$

Thus two end points are $(V_{CC}, 0)$ and $\left(0, \frac{V_{CC}}{R_C}\right)$. A line passing through these points is called dc load line as the slope of this line depends on the dc load R_C.

Quiescent point

Applying KVL to the input,

$$V_{BB} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{V_{BB}}{R_B} \quad (V_{BE} \text{ is very small})$$

This equation gives the value of base current. For this value of base current, output characteristic of the amplifier is plotted which intersects the dc load line at Q point. Hence Q point indicates quiescent (inactive, still) value of collector -emitter voltage V_{CE} and collector current I_C .

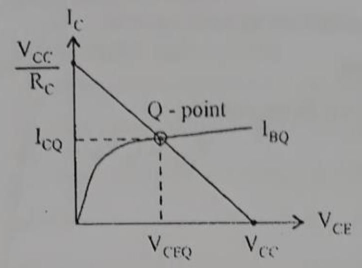

Fig. 1.14

While fixing the Q-point it has to be seen that the output of the amplifier is a proper sinusoidal waveform for sinusoidal input without distortion. By fixing the Q-point at different positions we can observe the variation in collector current and collector-emitter voltage corresponding to a given variation of base current.

When Q-point is located in the middle of the d.c. load line as shown in Fig. 1.15, sinusoidal waveform without distortion is obtained at the output.

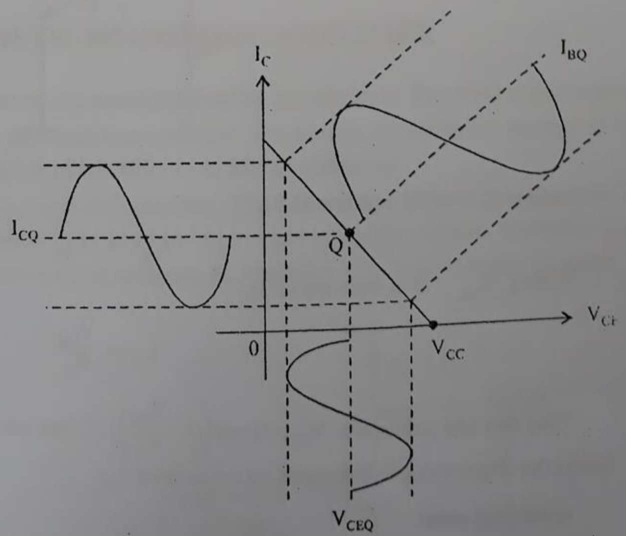

Fig. 1.15

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When Q-point is located near saturation region as shown in Fig. 1.16, the collector current is clipped at the positive half cycle.

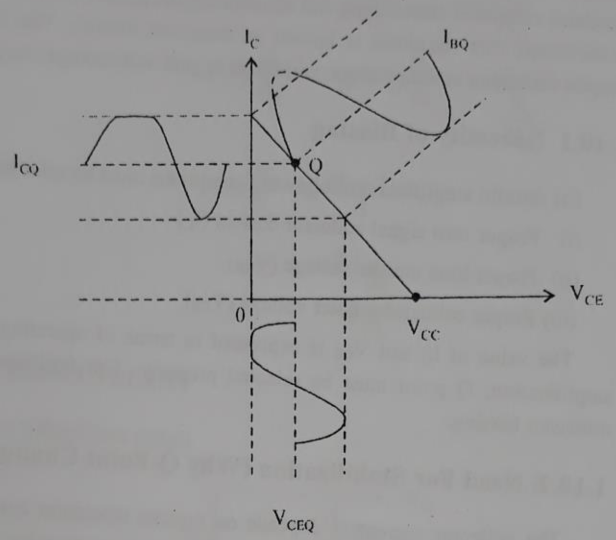

Fig. 1.16

When Q-point is located near the cut-off region, as shown in Fig.1.17, the collector current is clipped at the negative half cycle.

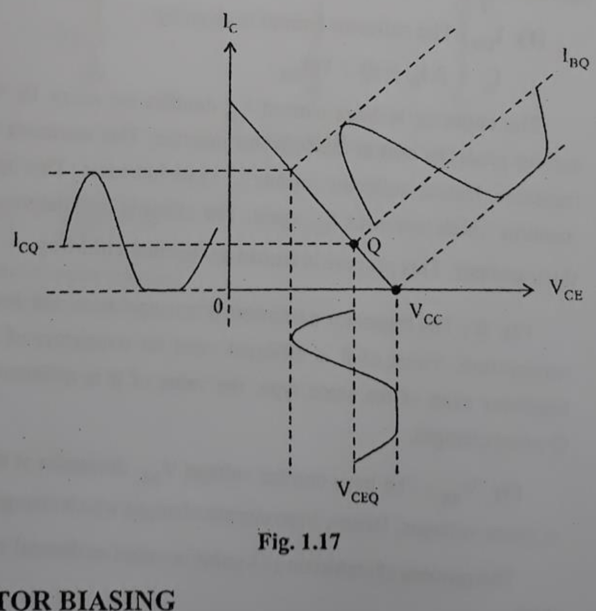

Fig. 1.17

1.10 TRANSISTOR BIASING

The basic function of a transistor is to do amplification. The weak signal is given to the transistor and amplified output is obtained from collector. The process of raising the strength of weak signal without any

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change in its general shape is known as faithful amplification. The basic problems involved in the design of transistor circuits is establishing and maintaining the proper collector to emitter voltage and collector current in the circuit.This condition is known as transistor biasing. The biasing conditions must be maintained despite variations in temperature, variations in gain and leakage current and variation in supply voltages.

1.10.1 Necessity of Biasing

For faithful amplification, following conditions must be satisfied:

(i) Proper zero signal collector current (I_C)

(ii) Proper base emitter voltage (V_{BE})

(iii) Proper collector-emitter voltage (V_{CE})

The value of I_C and V_{CE} is expressed in terms of operating point or quiescent point Q. For faithful amplification, Q point must be selected properly. The fulfillment of the above conditions is known as transistor biasing.

1.10.2 Need For Stabilization (Why Q-Point Changes)

The collector current I_c depends on reverse saturation current I_{CO}, current gain β and base emitter voltage V_{BE}. These parameters are temperature dependent i.e. as temperature changes, these parameters change. Hence collector current I_C changes. Due to this, Q point changes. Hence Q point has to be stabilized against temperature variation.

(pages 13 to 51 are not part of EEEE syllabus)

(1) I_{CO} : The collector current is given by

$$I_c = \beta I_B + (\beta + 1) I_{CO}$$

The collector leakage current I_{CO} doubles for every 10 °C rise in temperature. The flow of collector current produces heat at the collector junction. This increases the temperature, therefore leakage current I_{CO} increases. Hence, collector current I_C again increases. This increase in I_C increases temperature of collector junction which increases I_{CO} again. The effect is cumulative and at one stage I_C is so large which damages the transistor. This process is known as **thermal runaway**.

(2) β : The transistor parameter β is temperature and device dependent. β increases with the increase in temperature. Value of β is different even for transistors of same type. If transistor is replaced by another transistor even of the same type, the value of β is different. Hence, collector current changes. Therefore, Q-point changes.

(3) V_{BE} : The base emitter voltage V_{BE} decreases at the rate of 2.5 mV/°C i.e. device starts operating at lower voltages. Hence, base current changes which changes collector current and hence the Q-point.

The process of stabilizing Q-point is called as thermal stabilization.There are three methods to bias the BJT.

(1) Fixed bias

(2) Collector to base bias

(3) Voltage divider bias

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1.10.3 Stability Factor (S)

The rate of change of collector current w.r.t. collector leakage current I_{CO} at constant β and V_{BE} is called as stability factor.

$$\text{Stability factory } S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{\beta,\ V_{BE} = \text{constant}}$$

Expression for stability factor

We know that, $I_C = \beta I_B + (\beta + 1) I_{CO}$

Differentiating w.r.t. I_C,

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (\beta + 1)\frac{\partial I_{CO}}{\partial I_C}$$

$$1 - \beta\frac{\partial I_B}{\partial I_C} = (\beta + 1)\frac{\partial I_{CO}}{\partial I_C} = \frac{(\beta + 1)}{\frac{\partial I_C}{\partial I_{CO}}}$$

$$1 - \beta\frac{\partial I_B}{\partial I_C} = \frac{(\beta + 1)}{S}$$

$$S = \frac{\beta + 1}{1 - \beta\frac{\partial I_B}{\partial I_C}}$$

1.11 FIXED BIAS CIRCUIT

Fig 1.18 shows a fixed bias circuit.

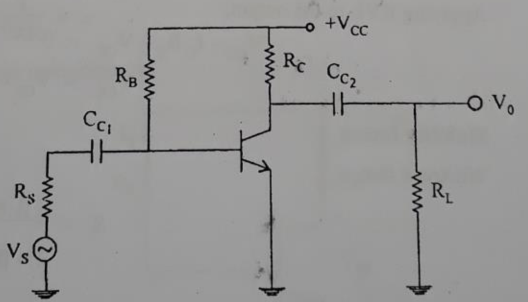

Fig. 1.18

DC analysis

For dc, $f = 0$, $X_C = \frac{1}{2\pi fC} = \infty$

Hence capacitors act as open circuits.

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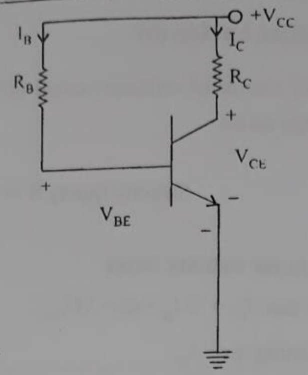


Fig. 1.19

Collector current I_C

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CC} > V_{BE} \qquad (V_{BE} = 0.7V)$$

$$I_B = \frac{V_{CC}}{R_B}$$

When V_{CC} and R_B is selected for a circuit, I_B is fixed. Hence, the circuit is called as fixed bias circuit.

$$I_C = \beta I_B$$

Collector-emitter voltage V_{CE}

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Stability factor

We know that,

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Differentiating w.r.t. I_C,

$$0 - R_B \frac{\partial I_B}{\partial I_C} - 0 = 0$$

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

$$\frac{\partial I_B}{\partial I_C} = 0$$

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}} = \beta + 1$$

If $\beta = 100$, then $S = 101$.

i.e. If I_{CO} changes by 1 %, I_C will change by 101% i.e. very large change in collector current occurs even for small changes in I_{CO}. Thus stability of the circuit is very poor.

1.12 FIXED EMITTER BIAS CIRCUIT

Fig 1.20 shows a fixed emitter bias circuit. Here R_E is connected between emitter and ground. Hence stability of the fixed bias circuit improves.

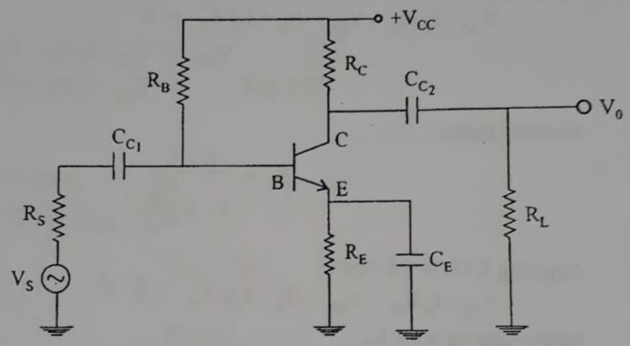


Fig. 1.20

DC analysis

For dc, $f = 0$, $X_C = \frac{1}{2\pi fc} = \infty$

Hence capacitors act as open circuits.

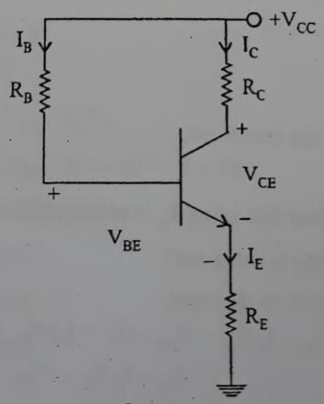


Fig. 1.21

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

Collector current I_C

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + \beta I_B) R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_C = \beta I_B$$

Collector-emitter voltage V_{CE}

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

$$= V_{CC} - I_C (R_C + R_E) - I_B R_E$$

Stability factor

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

Differentiating w.r.t. I_C,

$$0 - R_B \frac{\partial I_B}{\partial I_C} - 0 - R_E \frac{\partial I_B}{\partial I_C} - R_E = 0$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E}$$

Negative sign indicates that I_C increases with decrease in I_B and vice-versa.

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}} = \frac{\beta + 1}{1 + \beta \frac{R_E}{R_B + R_E}}$$

when R_E is not connected,

$$S = \beta + 1$$

Thus it is clear that when R_E is added, stability factor reduces i.e. stability of Q-point increases.

How stability is achieved?

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - I_C R_E - V_{BE} = I_B (R_B + R_E)$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E}$$

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

If temperature increases, collector current I_C tends to increase. As a result voltage drop across R_E increases which decreases base current I_B. As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. Hence variation in I_C with temperature is minimized and stability of Q-point is achieved.

Example 1.1 For the circuit shown in Fig.1.22, find I_C, V_{CE} and S.

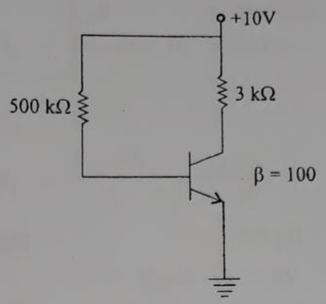


Fig. 1.22

Solution :

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{500 \times 10^3} = 18.6\ \mu A$$

$$I_C = \beta I_B = 100 \times 18.6 \times 10^{-6} = 1.86\ mA$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 1.86 \times 10^{-3} \times 3 \times 10^3 = 4.42\ V$$

$$S = \beta + 1 = 100 + 1 = 101$$

Example 1.2 Design a fixed bias circuit with $I_C = 2$ mA, $V_{CE} = 6$ V, $V_{CC} = 12$ V, $\beta = 100$.

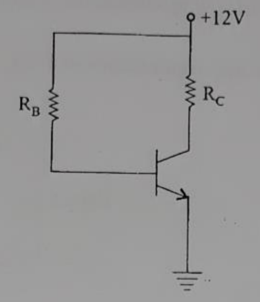


Fig. 1.23

Solution :

$$I_B = \frac{I_C}{\beta} = \frac{2\times10^{-3}}{100} = 20\ \mu A$$

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{12 - 0.7}{20\times10^{-6}} = 566\ k\Omega$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$= \frac{12 - 6}{2\times10^{-3}} = 3\ k\Omega$$

Example 1.3 For fixed bias circuit shown in Fig. 1.24, determine I_C, R_C, R_B and V_{CE} where V_{CC}=12V, $V_C = 6$ V, $\beta = 80$ and $I_B = 30\ \mu$A.

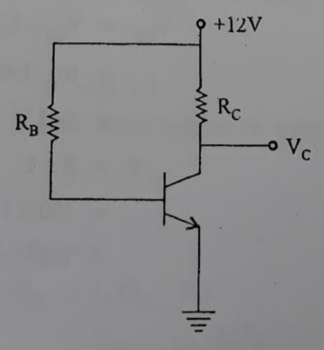


Fig. 1.24

Solution :

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{40 \times 10^{-6}}$$

$$= 282.5 \text{ k}\Omega$$

$$I_C = \beta I_B = 80 \times 40 \times 10^{-6} = 3.2 \text{ mA}$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_C = 0$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12 - 6}{32 \times 10^{-3}}$$

$$= 1.875 \text{ k}\Omega$$

$$V_{CE} = V_C = 6\text{V}$$

Example 1.4 Using CE amplifier with fixed bias where $I_B = 20\mu A$, $I_E = 4$ mA, $V_{CE} = 7.2V$ and $R_C = 2.2$ kΩ, determine I_C, V_{CC}, β and R_B.

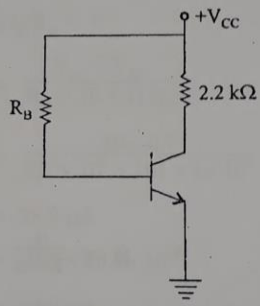


Fig. 1.25

Solution :

We know that,

$$I_E = I_B + I_C$$

$$I_C = I_E - I_B = 4 \times 10^{-3} - 20 \times 10^{-6}$$

$$= 3.98 \text{ mA}$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} = I_C R_C + V_{CE}$$

$$= 3.98 \times 10^{-3} \times 2.2 \times 10^3 + 7.2$$

$$= 15.96 \text{ V}$$

$$\beta = \frac{I_C}{I_B} = \frac{3.98 \times 10^{-3}}{20 \times 10^{-6}} = 199$$

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{15.96 - 0.7}{20 \times 10^{-6}} = 762.8\ k\Omega$$

Example 1.5 For the fixed bias circuit, $\alpha = 0.98$, $I_{CBO} = 10\ \mu A$, $R_C = 4\ k\Omega$, $R_B = 820\ k\Omega$, $V_{CC} = 12\ V$, Find I_C and V_{CE}.

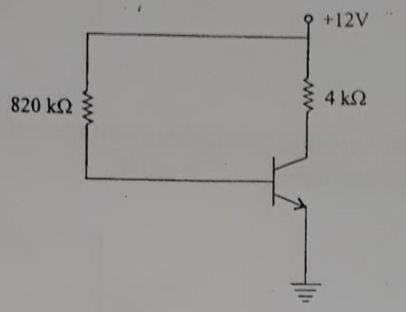


Fig. 1.26

Solution :

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{820 \times 10^3}$$

$$= 13.78\ \mu A$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$= 49 \times 13.78 \times 10^{-6} + (49 + 1) \times 10 \times 10^{-6}$$

$$= 1.17\ mA$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12 - 1.17 \times 10^{-3} \times 4 \times 10^3$$

$$= 7.3\ V$$

Example 1.6 For the circuit shown in Fig. 1.27, find I_C, V_{CE} and S.

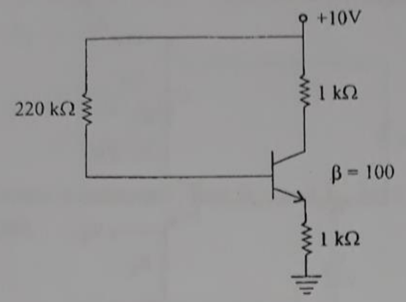


Fig. 1.27

Solution :

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$= \frac{10 - 0.7}{220 \times 10^3 + 101 \times 1 \times 10^3}$$

$$= 28.9\ \mu A$$

$$I_C = \beta I_B = 100 \times 28.9 \times 10^{-6}$$

$$= 2.89\ mA$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C)\ R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

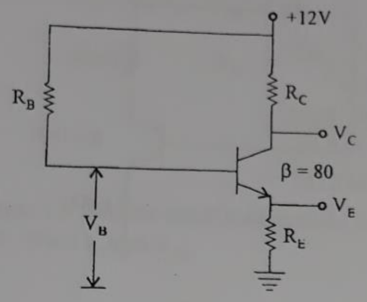
$$= 10 - 2.89 \times 10^{-3} \times 1 \times 10^3 - (28.9 \times 10^{-6} + 2.89 \times 10^{-3}) \times 1 \times 10^3$$

$$= 4.19\ V$$

$$S = \frac{\beta + 1}{1 + \beta \dfrac{R_E}{R_B + R_E}} = \frac{100 + 1}{1 + \dfrac{100 \times 1 \times 10^3}{220 \times 10^3 + 1 \times 10^3}}$$

$$= 69.53$$

Example 1.7 In the circuit shown in Fig. 1.28, find R_C, R_E, R_B, V_{CE} and V_B,



$V_C = 7.6V$

$I_C = 2mA$

$V_E = 2.4V$

Fig. 1.28

Solution :

Applying KVL to the output,

$$VCC - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_C = V_{CE} + I_E R_E$$

$$V_{CC} - I_C R_C - V_C = 0$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12 - 7.6}{2 \times 10^{-3}}$$

$$= 2.2\ k\Omega$$

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

$$= 12 - 2\times 10^{-3} \times 2.2\times 10^3 - 2.4$$

$$= 5.2\ V$$

$$I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{80} = 25\ \mu A$$

Applying KVL to the input,

$$V_{CC} - I_B R_B - V_{BE} - V_E = 0$$

$$R_B = \frac{V_{CC} - V_{BE} - V_E}{I_B}$$

$$= \frac{12 - 0.7 - 2.4}{25 \times 10^{-6}} = 356\ k\Omega$$

$$I_E = I_B + I_C$$

$$= 25 \times 10^{-6} + 2 \times 10^{-3}$$

$$= 2.025\ mA$$

$$V_B = V_{BE} + V_E$$

$$= 0.7 + 2.4$$

$$= 3.1\ V$$

$$V_E = I_E R_E$$

$$R_E = \frac{V_E}{I_E}$$

$$= \frac{2.4}{2.025 \times 10^{-3}}$$

$$= 1.185\ k\Omega$$

Example 1.8 In a fixed emitter bias circuit, find R_C and R_B such that $V_{CE} = 5$ V, $I_C = 2$ mA, $V_{CC} = 10$ V, $\beta = 100$, $R_E = 1\ k\Omega$.

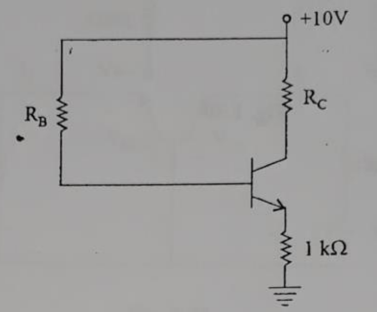


Fig. 1.29

Solution :

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{2 \times 10^{-3}}{100} = 20\ \mu A$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B) R_E = 0$$

$$R_C = \frac{V_{CC} - V_{CE} - (I_C + I_B) R_E}{I_C}$$

$$= \frac{10 - 5 - (2 \times 10^{-3} + 20 \times 10^{-6})\ 1 \times 10^3}{2 \times 10^{-3}}$$

$$= 1.49\ k\Omega$$

Applying KVL to the input,

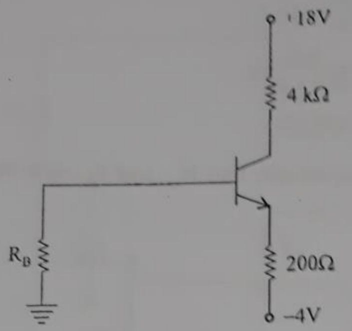
$$V_{CC} - I_B R_B - V_{BE} - (I_C + I_B) R_E = 0,$$

$$R_B = \frac{V_{CC} - V_{BE} - (I_C + I_B) R_E}{I_B}$$

$$= \frac{10 - 0.7 - (2 \times 10^{-3} + 20 \times 10^{-6})\ 1 \times 10^3}{20 \times 10^{-6}}$$

$$= 364\ k\Omega$$

Example 1.9 In the circuit of Fig. 1.30, find R_B and V_{CE}.



$\beta = 50$

$I_C = 2\text{ mA}$

Fig. 1.30

Solution :

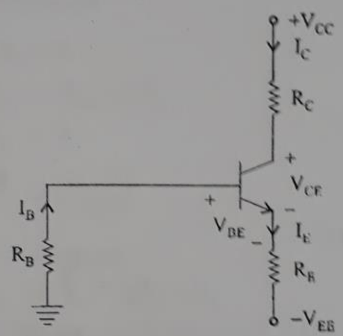


Fig. 1.31

$$I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{50} = 40\ \mu\text{A}$$

Applying KVL to input,

$$I_E = I_B + I_C = 40 \times 10^{-6} + 2 \times 10^{-3} = 2.04\text{ mA}$$

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$R_B = \frac{V_{EE} - V_{BE} - I_E R_E}{I_B}$$

$$= \frac{4 - 0.7 - 2.04 \times 10^{-3} \times 200}{40 \times 10^{-6}}$$

$$= 72.3\text{ k}\Omega$$

Applying KVL to the output,

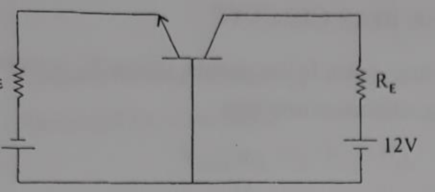
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{CC} + V_{EE} - I_C R_C - I_E R_E$$

$$= 18 + 4 - 2 \times 10^{-3} \times 4 \times 10^{3} - 2.04 \times 10^{-3} \times 200$$

$$= 13.59\text{ V}$$

Example 1.10 Find R_C and R_E in the circuit of Fig. 1.32.



$$\alpha = 0.99$$
$$V_{EE} = 4\text{ V}$$
$$V_{CC} = 12\text{ V}$$
$$I_E = 1.1\text{ mA}$$
$$V_{CE} = 7\text{ V}$$

Fig. 1.32

Solution :

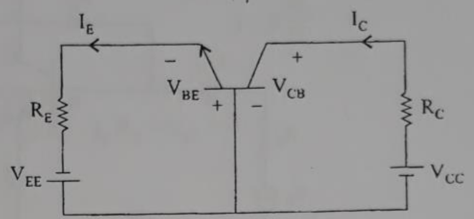


Fig. 1.33

Applying KVL to the input,

$$V_{EE} - I_E R_E - V_{BE} = 0$$

$$R_E = \frac{V_{EE} - V_{BE}}{I_E}$$

$$= \frac{4 - 0.7}{1.1 \times 10^{-3}}$$

$$= 3\ \Omega$$

Applying KVL around transistor terminal,

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE} = 7 - 0.7 = 6.3\text{ V}$$

$$I_C = \alpha I_E$$

$$= 0.99\,(1.1 \times 10^{-3}) = 1.089\text{ mA}$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CB} = 0$$

$$R_C = \frac{V_{CC} - V_{CB}}{I_C}$$

$$= \frac{12 - 6.3}{1.089 \times 10^{-3}}$$

$$= 5.234\text{ k}\Omega$$

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

1.13 COLLECTOR TO BASE BIAS CIRCUIT

Fig. 1.34 shows collector to base bias circuit. In this method, resistor R_B is connected between base and collector. Hence the circuit is called as collector-to-base bias.

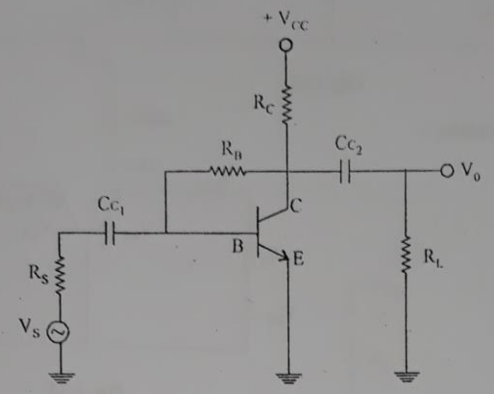


Fig. 1.34

DC analysis

For dc, $f = 0$, $X_C = \frac{1}{2\pi fC} = \infty$

Hence capacitors act as open circuits.

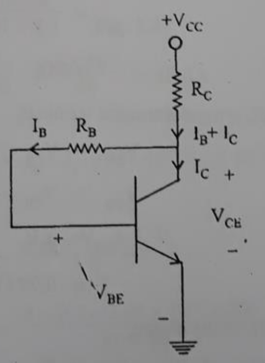


Fig. 1.35

Collector current I_C

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B [R_B + (1 + \beta) R_C]$$

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}$$

$$I_C = \beta I_B$$

Collector-emitter voltage V_{CE}

Applying KVL to the output,

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

Stability factor

$$S = \frac{\beta + 1}{1 - \beta \dfrac{\partial I_B}{\partial I_C}}$$

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

Differentiating w.r.t. I_C

$$0 - R_C \frac{\partial I_B}{\partial I_C} - R_C - R_B \frac{\partial I_B}{\partial I_C} - 0 = 0$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B}$$

Negative sign indicates that as I_C increases I_B decreases and vice versa.

$$S = \frac{\beta + 1}{1 - \beta \dfrac{\partial I_B}{\partial I_C}} = \frac{\beta + 1}{1 + \beta \dfrac{R_C}{R_B + R_C}}$$

Hence stability factor S is smaller than $(\beta + 1)$ which is obtained from fixed bias circuit. Thus stability is improved.

How stability is achieved?

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} - I_C R_C = (R_B + R_C)\ I_B$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$$

If temperature increases, collector current I_C tends to increase. As a result voltage drop across R_C increases which decreases base current I_B. As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. Hence variation in I_C with temperature is **minimized** and stability of Q-point is achieved.

Drawback

This circuit provides negative feedback which reduces the gain of the amplifier.

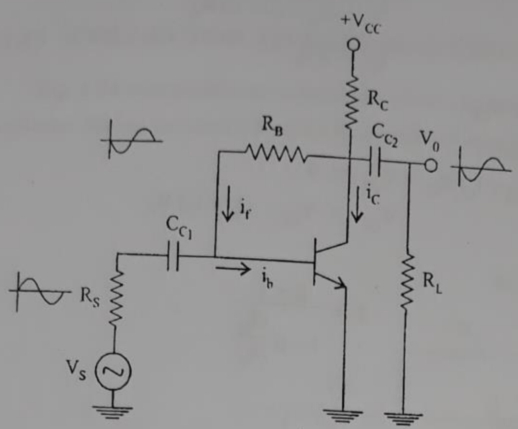


Fig. 1.36

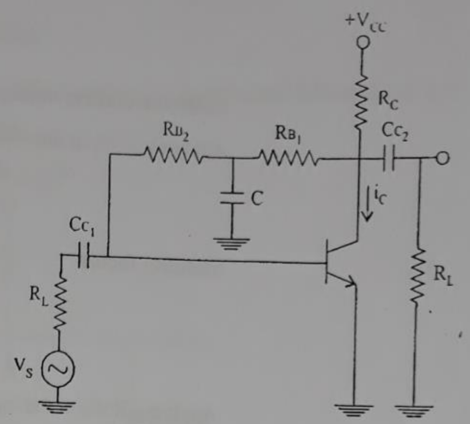


Fig. 1.37

In CE amplifier, output is 180° out of phase with input. If output is fedback to input, the net gain decreases. This process is known as ac degeneration.

If ac signal voltage increases, base current increases and collector current i_C increases. Hence the net base current through transistor decreases as i_f opposes i_b. Due to this gain of the amplifier decreases.

It can be avoided by splitting R_B into two parts and connecting a capacitor at the centre of both resistors. For dc operation, there is no effect of capacitor ($X_C = \infty$). For ac operation, as i_b increases, i_c increases. Hence component of base current through R_B is bypassed by C. Hence there is no change in i_b and there is no degeneration of input signal.

1.14 COLLECTOR TO BASE BIAS CIRCUIT WITH EMITTER RESISTOR

Fig. 1.38 shows collector to base bias circuit with emitter resistor. Emitter resistor R_E is connected in the emitter terminal.

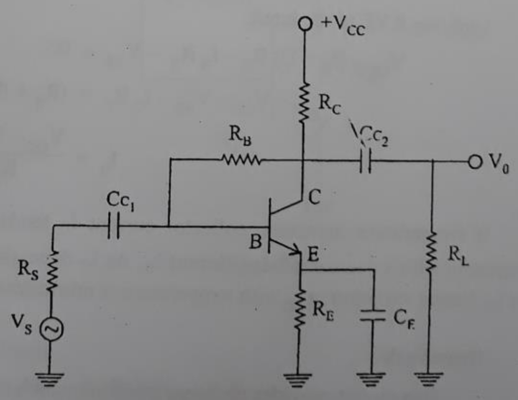


Fig. 1.38

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

DC analysis

For dc, $f = 0$, $X_C = \frac{1}{2\pi fC} = \infty$

Hence capacitors act as open circuits.

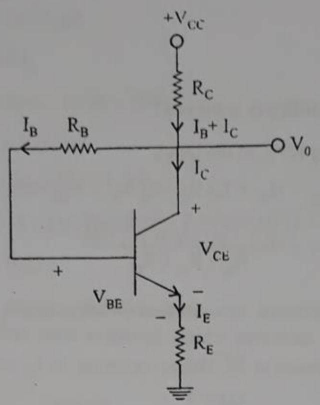


Fig. 1.39

Collector current I_C

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = I_B + I_C = I_B + \beta I_B = (\beta + 1) I_B$$

$$V_{CC} - V_{BE} = [R_B + (\beta + 1) R_C + (\beta + 1) R_E] I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$$

$$I_C = \beta I_B$$

Collector-emitter voltage V_{CE}

Applying KVL to the output,

$$V_{CC} - (I_B + I_C) R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C)(R_C + R_E)$$

Stability factor

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

Differentiating. w.r.t. I_C,

$$0 - \frac{\partial I_B}{\partial I_C} R_C - R_C - \frac{\partial I_B}{\partial I_C} R_B - 0 - \frac{\partial I_B}{\partial I_C} R_E - R_E = 0$$

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

$$\frac{\partial I_B}{\partial I_C} = -\frac{(R_C + R_E)}{R_B + R_C + R_E}$$

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}} = \frac{\beta + 1}{1 + \beta \frac{(R_C + R_E)}{R_B + R_C + R_E}}$$

How stability is achieved?

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C (R_C + R_E)}{R_B + R_C + R_E}$$

If temperature increases, collector current I_C tends to increase. As a result voltage drop across $(R_C + R_E)$ increases which decreases base current I_B. As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. Hence variation in I_C with temperature is **minimized** and stability of Q-point is achieved.

Example 1.11 For the circuit shown in Fig. 1.40 , find I_B, I_C and V_{CE}.

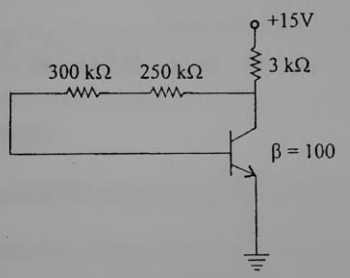


Fig. 1.40

Solution :

$$R_B = R_{B_1} + R_{B_2}$$

$$= 300 \times 10^3 + 250 \times 10^3$$

$$= 550\ k\Omega$$

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_C}$$

$$= \frac{15 - 0.7}{550 \times 10^3 + 101 \times 3 \times 10^3}$$

$$= 16.76\ \mu A$$

$$I_C = \beta I_B$$

$$= 100 \times 16.76 \times 10^{-6}$$

$$= 1.676\ mA$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

$$= 15 - (16.76 \times 10^{-6} + 1.676 \times 10^{-3}) \times 3 \times 10^3$$

$$= 9.92\ V$$

Example 1.12 Determine I_B, I_C, V_{CE} and stability factor.

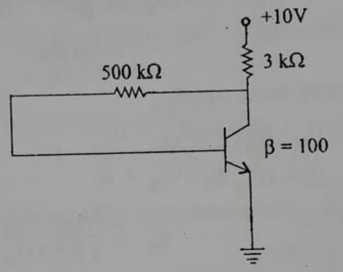


Fig. 1.41

Solution :

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_C}$$

$$= \frac{10 - 0.7}{500 \times 10^3 + 101 \times 3 \times 10^3}$$

$$= 11.58\ \mu A$$

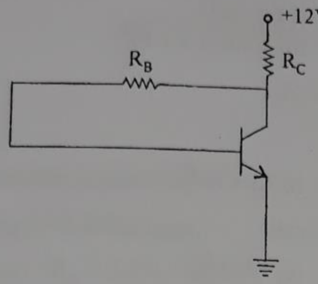
$$I_C = \beta I_B = 100 \times 11.58 \times 10^{-6}$$

$$= 1.158\ mA$$

$$S = \frac{\beta + 1}{1 + \beta \dfrac{R_C}{R_B + R_C}} = \frac{100 + 1}{1 + \dfrac{100 \times 3 \times 10^3}{500 \times 10^3 + 3 \times 10^3}}$$

$$= 63.26$$

Example 1.13 For the circuit shown in Fig. 1.42, find R_B and R_C,



$V_{CE} = 6$ V

$I_C = 2$ mA

$V_{CC} = 12$ V

$V_{BE} = 0.7$ V

$\beta = 100$

Fig. 1.42

Solution :

$$I_B = \frac{I_C}{\beta} = \frac{2 \times 10^{-3}}{100} = 20\ \mu A$$

Applying KVL to the output,

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - V_{CE} = 0$$

$$R_C = \frac{V_{CC} - V_{CE}}{(\beta + 1) I_B} = \frac{12 - 6}{101 \times 20 \times 10^{-6}} = 2.97\ k\Omega$$

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE} - (I_B + I_C) R_C}{I_B} = \frac{12 - 0.7 - 6}{20 \times 10^{-6}} = 265.4\ k\Omega$$

Example 1.14 For the circuit shown in Fig. 1.43, find I_C, V_{CE} and S.

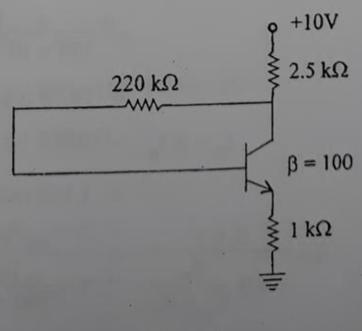


Fig. 1.43

Solution :

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$$

$$= \frac{10 - 0.7}{220 \times 10^3 + 101 \times (2.5 + 1) \times 10^3}$$

$$= 16.21\ \mu A$$

$$I_C = \beta I_B = 100 \times 16.21 \times 10^{-6}$$

$$= 1.621\ mA$$

Applying KVL to the output,

$$V_{CC} - (I_B + I_C) R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C)(R_C + R_E)$$

$$= 10 - (16.21 \times 10^{-6} + 1.621 \times 10^{-3})(2.5 + 1) \times 10^3$$

$$= 4.27\ V$$

$$S = \frac{\beta + 1}{1 + \beta \dfrac{(R_E + R_C)}{R_B + R_C + R_E}} = \frac{100 + 1}{1 + 100 \times \dfrac{1k + 2.5k}{(220k + 2.5k + 1k)}} = 39.36$$

Example 1.15 For the circuit shown in Fig. 1.44, determine I_C, V_C, V_E, V_{CE}.

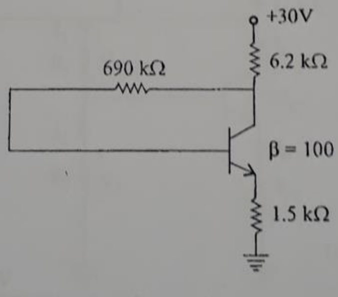


Fig. 1.44

Solution :

Applying KVL to the input,

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$$

$$= \frac{30 - 0.7}{690 \times 10^3 + 101 \times (6.2 + 1.5) \times 10^3}$$

$$= 19.9\ \mu A$$

$$I_C = \beta I_B = 100 \times 19.9 \times 10^{-6}$$
$$= 1.99 \text{ mA}$$
$$V_C = V_{CC} - (I_B + I_C) R_C$$
$$= 30 - (19.9 \times 10^{-6} + 1.99 \times 10^{-3})(6.2 \times 10^3)$$
$$= 17.5 \text{ V}$$
$$V_E = (I_B + I_C) R_E$$
$$= (19.9 \times 10^{-6} + 1.99 \times 10^{-3})(1.5 \times 10^3)$$
$$= 3.02 \text{ V}$$
$$V_{CE} = V_C - V_E$$
$$= 17.5 - 3.02$$
$$= 14.48 \text{ V}$$

Example 1.16 Calculate dc collector current I_C and voltage V_C for the bias circuit shown in Fig. 1.45.

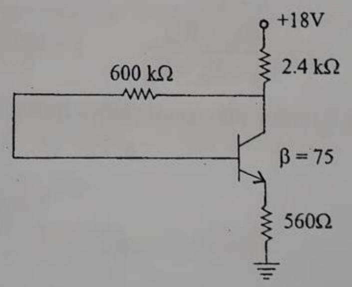


Fig. 1.45

Solution :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)(R_C + R_E)}$$
$$= \frac{18 - 0.7}{600 \times 10^3 + 76(2.4 + 0.56) \times 10^3}$$
$$= 20.9 \ \mu\text{A}$$
$$I_C = \beta I_B = 75 \times 20.9 \times 10^{-6}$$
$$= 1.57 \text{ mA}$$
$$V_{CE} = V_{CC} - (I_B + I_C)(R_C + R_E)$$
$$= 18 - (20.9 \times 10^{-6} + 1.57 \times 10^{-3})(2.4 + 0.56) \times 10^3$$
$$= 13.29 \text{ V}$$

1.15 VOLTAGE DIVIDER BIAS CIRCUIT

Fig. 1.52 shows voltage divider bias circuit. Resistors R_1 and R_2 form a voltage divider network.

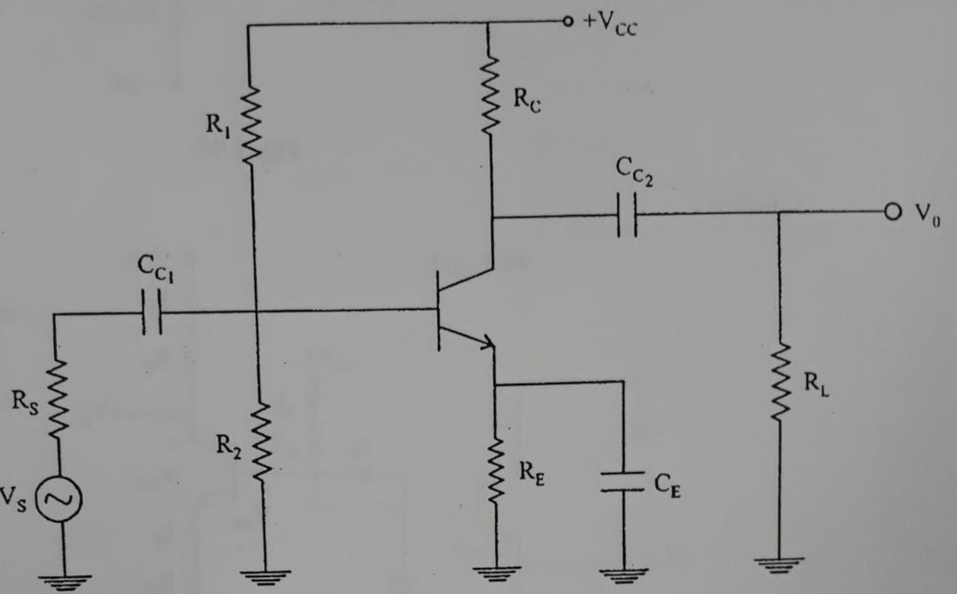


Fig. 1.52

DC analysis

For dc, $f = 0$, $X_C = \frac{1}{2\pi fC} = \infty$

Hence capacitors act as open circuits.

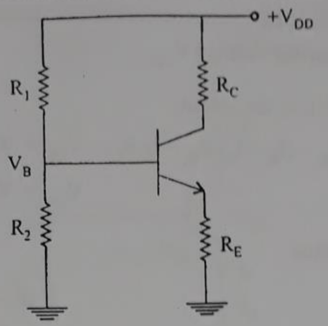


Fig. 1.53

The input circuit can be converted into Thevenin's equivalent as follows :

$$V_{Th} = V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_{Th} = R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

As R_1 and R_2 divides the voltage V_{CC} at the base, the circuit is called as voltage divider bias.

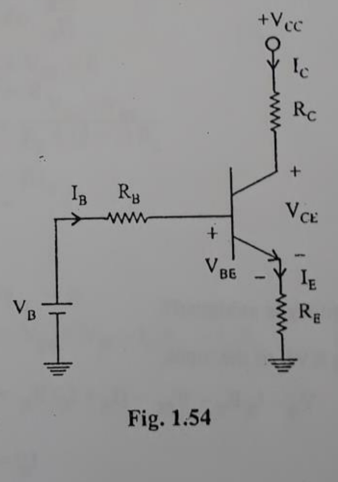


Fig. 1.54

Collector current I_C

Applying KVL to the input,

$$V_B - I_B R_B - V_{BE} - I_E R_E = 0$$

Now, $$I_E = I_B + \beta I_B = (\beta + 1) I_B$$

$$V_B - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$V_B - V_{BE} = [R_B + (\beta + 1) R_E] I_B$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_C = \beta I_B$$

Collector-emitter voltage V_{CE}

Applying KVL to the output,

$$V_{CC} - (I_B + I_C) R_E - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_E - I_C R_C$$

Stability factor

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Applying KVL to the input,

$$V_B - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

Differentiating. w.r.t. I_C,

$$0 - R_B \frac{\partial I_3}{\partial I_C} - 0 - R_E \frac{\partial I_B}{\partial I_C} - R_E = 0$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

$$= \frac{\beta + 1}{1 + \beta \frac{R_E}{R_B + R_E}}$$

Hcw stability is achieved?

Applying KVL to the input,

$$V_B - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$I_B = \frac{V_B - V_{BE} - I_C R_E}{R_B + R_E}$$

If temperature increases, collector current I_C tends to increase. As a result voltage drop across R_E increases which decreases base current I_B. As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. Hence variation in I_C with temperature is **minimized** and stability of Q-point is achieved.

1.16 EMITTER BIAS CIRCUIT

Fig. 1.55 shows an emitter bias circuit. It uses both positive and negative supply voltages. The voltage V_{EE} forward biases the emitter-base junction.

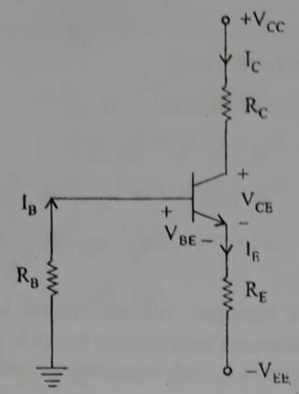


Fig. 1.55

For dc, $f = 0$, $X_C = \frac{1}{2\pi f C} = \infty$

Hence capacitors act as open circuits.

Collector current I_C

Applying KVL the input,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} + 0$$

$$-I_B R_B - V_{BE} - (\beta + 1) I_B R_E + V_{EE} = 0$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_C = \beta I_B$$

Collector-emitter voltage V_{CE}

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{CC} + V_{EE} - I_C R_C - I_E R_E$$

Stability factor

Applying KVL to the input,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$-I_B R_B - V_{BE} - I_B R_E + V_{EE} = 0$$

Differentiating w.r.t. I_C.

$$-R_B \frac{\partial I_B}{\partial I_C} - 0 - R_E \frac{\partial I_B}{\partial I_C} - R_E + 0 = 0$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{(R_B + R_E)}$$

$$S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}} = \frac{\beta + 1}{1 + \beta \frac{R_E}{(R_B + R_E)}}$$

How stability is achieved?

Applying KVL to the input,

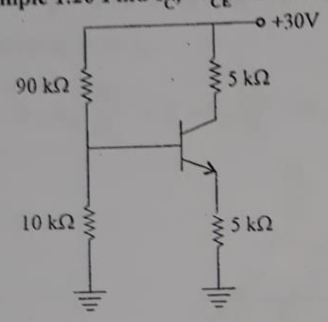
$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$-I_B R_B - V_{BE} - I_C R_E - I_B R_E + V_{EE} = 0$$

$$I_B = \frac{V_{EE} - V_{BE} - I_C R_E}{R_B + R_E}$$

If temperature increase, collector current I_C tends to increase. As a result voltage drop across R_E increases which decreases base current I_B. As I_C depends on I_B, decrease in I_B reduces the original increase in I_C. Hence variation in I_C with temperature is **minimized** and stability of Q-point is achieved.

Example 1.20 Find I_C, V_{CE} and stability factor S.



$$\beta = 100$$

$$I_{CBO} = 10\ \mu A$$

Fig. 1.56

Solution :

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10k}{10k + 90k} \times 30 = 3V$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{90k \times 10k}{90k + 10k} = 9\ k\Omega$$

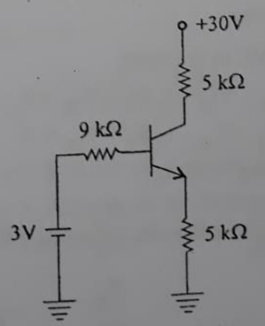


Fig. 1.57

Applying KVL to the input,

$$V_B - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_B - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

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$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$= \frac{3 - 0.7}{9\times 10^3 + (101)\, 5\times 10^3}$$

$$= 4.47\ \mu A$$

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$= 100\,(4.47\times 10^{-6}) + (101)\, 10\times 10^{-6}$$

$$= 1.457\ mA$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

$$= 30 - 1.457\times 10^{-3} \times 5\times 10^3 - (4.47\times 10^{-6} + 1.457\times 10^{-3})\, 5\times 10^3$$

$$= 15.4\ V$$

$$S = \frac{\beta + 1}{1 + \beta \frac{R_E}{R_B + R_E}}$$

$$= \frac{100 + 1}{1 + 100 \times \frac{5k}{9k + 5k}}$$

$$= 2.75$$

Example 1.21 Find R_1, R_2 and R_C of the circuit shown in Fig. 1.58 if $I_C = 1$ mA, $R_E = 1\ k\Omega$, $V_{CC} = 10$ V, $\beta = 100$, $S = 10$ and $V_{CE} = 5$ V.

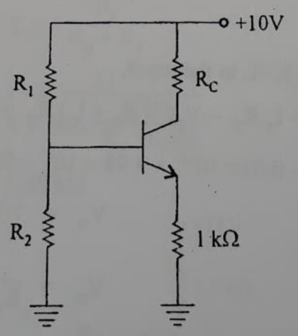


Fig. 1.58

Solution :

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{1\times 10^{-3}}{100} = 0.01\ mA$$

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$10 - 1 \times 10^{-3} \times R_C - 5 - (0.01 + 1) \times 10^{-3} \times 1 \times 10^3 = 0$$

$$R_C = 3.99\ k\Omega$$

$$S = \frac{\beta + 1}{1 + \beta \frac{R_E}{R_B + R_E}}$$

$$10 = \frac{100 + 1}{1 + 100 \times \frac{1k}{R_B + 1k}}$$

$$R_B = 9.98\ k\Omega$$

Replacing the base circuit by its Thevenin equivalent,

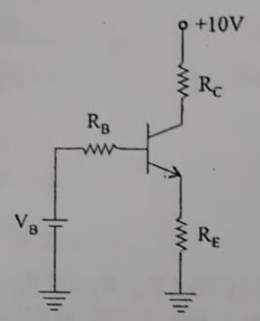


Fig. 1.59

Applying KVL to the input,

$$V_B - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$V_B - 0.01 \times 10^{-3} \times 9.98 \times 10^3 - 0.7 - (0.01 + 1) \times 10^{-3} \times 1 \times 10^3$$

$$V_B = 1.71\ V$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

Multiplying both the sides by R_1,

$$R_1 V_B = \frac{R_1 R_2}{R_1 + R_2} V_{CC} = R_B V_{CC}$$

$$R_1 = \frac{R_B V_{CC}}{R_1} = \frac{9.98 \times 10^3 \times 10}{1.71} = 58.36\ k\Omega$$

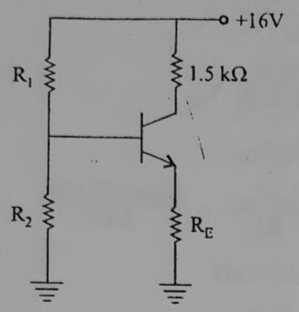
BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$9.98\times 10^3\ (58.36\times 10^3 + R_2) = 58.36\times 10^3 R_2$$

$$R_2 = 12.04\ k\Omega$$

Example 1.22 For the circuit shown in Fig. 1.60, find R_1, R_2 and R_E.



$V_{CE} = 8\ V$

$I_C = 4\ mA$

$\beta = 50$

$S = 10$

$V_{BE} = 0.3\ V$

Fig. 1.60

Solution :

$$I_B = \frac{I_C}{\beta} = \frac{4\times 10^{-3}}{50} = 0.08\ mA$$

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C)\ R_E = 0$$

$$16 - 4\times 10^{-3}\times 1.5\times 10^3 - 8 - (0.08 + 4)\times 10^{-3}\times R_E = 0$$

$$R_E = 0.49\ k\Omega$$

$$S = \frac{\beta + 1}{1 + \beta\dfrac{R_E}{R_B + R_E}}$$

$$10 = \frac{51}{1 + 50\times\dfrac{0.49k}{R_B + 0.49k}}$$

$$R_B = 5.49\ k\Omega$$

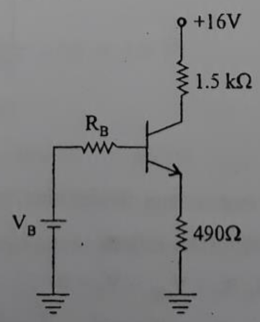


Fig. 1.61

Applying KVL to the input,

$$V_B = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= 0.08 \times 10^{-3} \times 5.49 \times 10^3 + 0.3 + (0.08 + 4) \times 10^{-3} \times 0.49 \times 10^{-3}$$

$$= 2.53 \text{ V}$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$R_1 V_B = \frac{R_1 R_2}{R_1 + R_2} V_{CC}$$

$$= R_B V_{CC}$$

$$R_1 = \frac{R_B V_{CC}}{R_1} = \frac{5.49 \times 10^3 \times 16}{2.53}$$

$$= 34.72 \text{ k}\Omega$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$5.49 \times 10^3 (R_1 + R_2) = R_1 R_2$$

$$5.49 \times 10^3 (34.72 \times 10^3 + R_2) = 34.72 \times 10^3 R_2$$

$$R_2 = 4.74 \text{ k}\Omega$$

Example 1.23 Transistor type BC 147A is used in CE configuration with collector load resistor R_C =1 kΩ and V_{CC} = 12 V. If V_{CE} = 6 V. Calculate the biasing components if biasing used is potential divider bias employing resistor R_1 and R_2 with emitter resistor R_E having 1 volt across R_E.

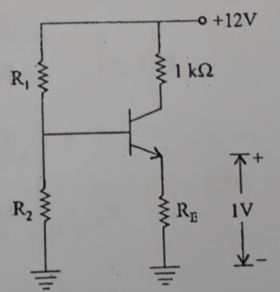


Fig. 1.62

Solution :

Assuming β free voltage divider bias, we have,

Applying KVL to the output,

$$V_{CC} - I_C R_C - V_{CE} - V_E = 0$$

$$I_C = \frac{V_{CC} - V_{CE} - V_E}{R_C} = \frac{12 - 6 - 1}{1 \times 10^3}$$

$$= 5 \text{ mA}$$

$$I_C \approx I_E = 5\text{ mA}$$

$$R_E = \frac{V_E}{I_E}$$

$$= \frac{1}{5 \times 10^{-3}} = 200\ \Omega$$

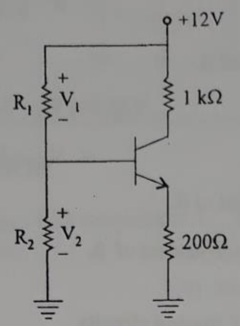


Fig. 1.63

If $\beta R_E >> 10 R_2$

$$I_B \approx 0$$

$$V_2 = V_{BE} + V_E$$

$$= 0.6 + 1 = 1.6\text{ V}$$

$$V_1 = V_{CC} - V_2$$

$$= 12 - 1.6$$

$$= 10.4\text{ V}$$

$$\frac{V_1}{V_2} = \frac{R_1}{R_2} = \frac{10.4}{1.6}$$

$$R_1 = 6.5 R_2$$

$$V_B = V_2 = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$= \frac{R_2}{7.5 R_2} \times 12 = 1.6\text{ V}$$

Assuming $R_2 = 10\text{ k}\Omega$

$$R_1 = 6.5 \times 10 \times 10^3 = 65\text{ k}\Omega$$

Example 1.24 Prove that Q point is independent of β in voltage divider bias circuit.

We know that,

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E}$$

Generally $(\beta + 1) R_E >> R_B$

$$\beta R_E >> R_B$$

$$I_C = \beta I_B$$

$$= \beta \frac{V_B - V_{BE}}{b R_E} = \frac{V_B - V_{BE}}{R_E}$$

I_C is independent of β.

Similarly,

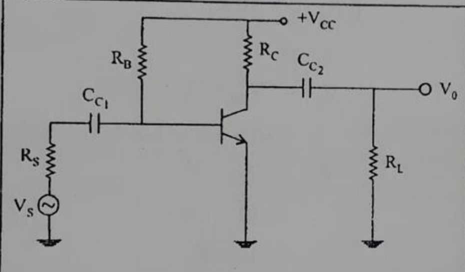
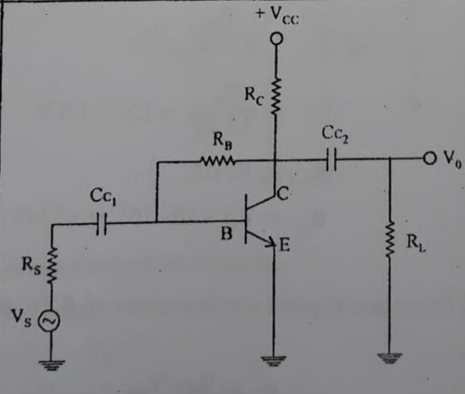
$$V_{CE} = V_{CC} - I_C R_C - I_E R_C$$

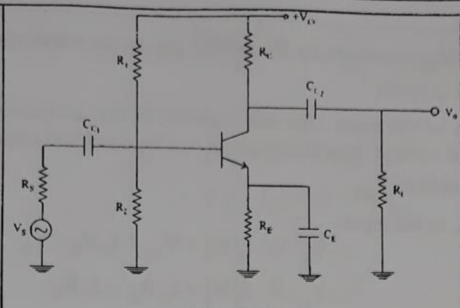
$$= V_{CC} - I_C (R_C + R_E) \qquad (\because I_B \approx 0)$$

V_{CE} is independent of β.

Thus Q point is independent of β.

Summary of BJT biasing circuits

Configuration	Circuit	Equation
Fixed Bias	 **Fig. 1.64**	$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B$ $S = \frac{\beta + 1}{1 - \beta \frac{\partial I_B}{\partial I_C}} = \beta + 1$
Collector to Base Bias	 **Fig. 1.65**	$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_C}$ $I_C = \beta I_B$ $S = \frac{\beta + 1}{1 + \beta \frac{R_C}{R_B + R_C}}$

Volage Divider Bias	 Fig. 1.66	$I_B = \dfrac{V_B - V_{BE}}{R_B + (\beta+1) R_E}$ $I_C = \beta I_B$ $S = \dfrac{\beta+1}{1+\beta \dfrac{R_E}{R_B+R_E}}$

1.17 BIAS COMPENSATION

The collector current I_C changes with temperature I_{CO}, β and V_{BE}. There are two methods to stabilize variation in I_C with above parameters.

(1) Thermal stabilization. (2) Bias compensation.

1.17.1 Thermal stabilization

In this method, resistive biasing circuit such as fixed bias circuit, collector to base bias circuit and voltage divider bias circuits are used to stabilize variation in I_C with I_{CO}.

1.17.2 Bias compensation

In this method, temperature sensitive devices such as diodes, transistors, thermistors etc. are used which provide compensating voltage and current to stabilize variations in I_C with V_{BE} and I_{CO}.

(1) Diode compensation for V_{BE}

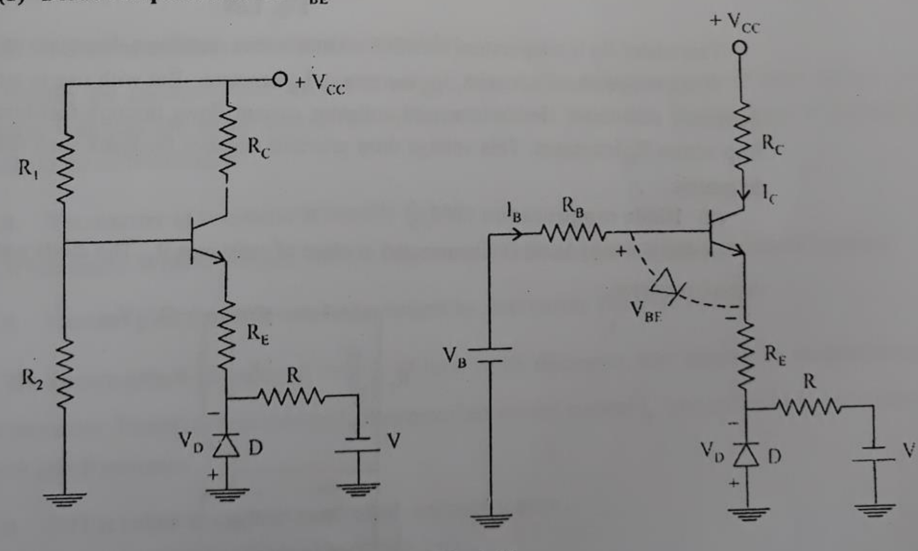


Fig. 1.67

As shown in Fig. 1.67 diode is forward biased by the voltage V and current limiting resistor R.

We know that V_{BE} decreases by 2.5 mV/°C i.e. device starts operating at lower voltage which changes I_B and I_C and hence Q point.

If the diode is of the same type and material as that of transistor (base emitter diode of BJT), then variation in V_{BE} and voltage drop across diode will be equal and opposite. Hence, they cancel out and I_B and I_C become independent of V_{BE}.

Applying KVL to the input,

$$V_B = I_B R_B + V_{BE} + I_C R_E - V_D$$

$$V_B = I_B R_B + I_C R_E \simeq I_C R_E \qquad (\because V_{BE} = V_D = 0.7 \text{ V})$$

$$I_C = \frac{V_B}{R_E} = \text{constant}$$

(2) Thermistor compensation for I_{CO}

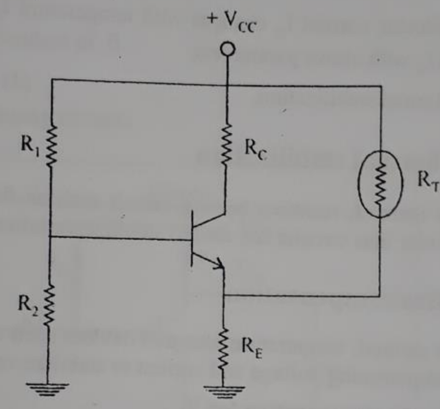


Fig. 1.68

Thermistor R_T is temperature sensitive resistor whose resistance decreases as temperature increases.

When temperature increases, I_{CO} increases, I_C increases. But with rise in temperature, resistance of the thermistor decreases. Hence increased collector current flows through thermistor into R_E. Hence voltage drop across R_E increases. This voltage drop provides negative feedback such that I_B decreases and hence I_C decreases.

(3) Diode compensation for I_{CO}

In this method, diode D is connected in place of resistance R_2. The diode used in of the same material as that of transistor.

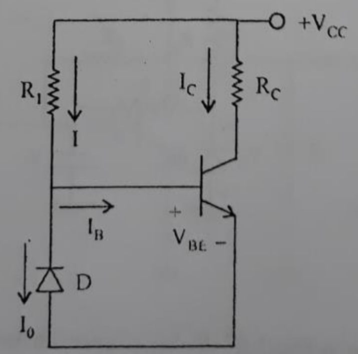


Fig. 1.69

$$I = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant}$$

$$I = I_O + I_B$$

We know that,

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$
$$= \beta (I - I_O) + (\beta + 1) I_{CO}$$
$$= \beta (I - I_O) + \beta I_{CO} \qquad (\because \ \beta + 1 \approx \beta)$$
$$= \beta [(I - (I_O - I_{CO})]$$

As temperature increases, I_O and I_{CO} will change by same amount. Hence, $I_O - I_{CO}$ will always be constant irrespective of change in I_{CO} due to change in temperature.

Give Reasons

1. The base of transistor is lightly doped.

In BJT, base current flows when electrons from the emitter recombine in the base. If the base is heavily doped, then the more electrons will recombine in the base and less electrons will travel to the collector. This increases the base current but decreases the collector current. In BJT, it is required that collector current I_C should be very high. Hence, base is lightly doped. If base is lightly doped, then the number of recombination in the base will less and more electrons will travel to collector thereby increasing the collector current.

2. Base width in a transistor is kept small.

If the width of base is increased, then electrons travelling from emitter to collector will remain in the base from more time thereby increasing number of recombination with the electrons which increases base current and reduces collector current. To get more collector current, width of base should be very small.

3. Collector width is maximum in transistor.

Usually the collector base junction is reverse biased. To withstand large reverse voltage such that collector base junction is not broken, the collector width is maximum. It also helps in dissipating heat quickly to the surrounding.

4. The emitter of transistor is heavily doped.

When emitter is heavily doped, there is large number of electrons available for recombination.

5. Current gain β of BJT can be increased by decreasing the base width.

The current gain is given by $\beta = \frac{I_C}{I_B}$. If base width decreases, then number of recombination in the base decreases. Therefore base current I_B decreases but emitter current I_E and collector I_C increases. Hence, current gain β increases.

6. BJT is called as current controlled current source .

In BJT, current equation is given by $I_E = I_B + I_C$.

I_B controls the flow of emitter collector current. In other words input current controls the output current. Hence, BJT is called as current controlled current source.

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

7. In CE configuration, transistor is not cut-off when $I_B = 0$.

In CE configuration, when $I_B = 0$ i.e. in the cut-off region, collector current is not zero. But a small leakage current flows from collector to emitter. Hence, transistor is not cut-off.

$$
\begin{aligned}
I_C &= \beta I_B + (\beta + 1) I_{CBO} \\
&= (\beta + 1) I_{CBO} \qquad \text{when } I_B = 0 \\
&= I_{CEO}
\end{aligned}
$$

8. Thermal runaway is of importance in BJT amplifiers than FET amplifiers.

In FET, drain current I_D decreases by 0.7%/°C.

In BJT, the collector current is $I_C = \beta I_B + (\beta + 1) I_{CO}$.

Due to increase in temperature, reverse saturation current I_{CO} increases, which increases collector current I_C. The increase in I_C, in turn increases junction temperature and hence I_{CBO}. This process continues, till I_C goes on increasing beyond limit and breakdown occurs, which is called as thermal runaway. Hence, it is important in BJT amplifiers.

9. Thermal stability of biasing is necessary in BJT amplifiers.

In order to use transistor as an amplifier, it is necessary to bias the transistor in active region of the characteristics. The biasing circuit should ensure that Q-point remains fixed with changes in temperature and transistor parameters.

If junction temperature increases, then I_{CBO} increases. Hence, I_C increases. If I_C continues to increase, Q-point moves to saturation region, which may distort the output signal. Hence thermal stability of Q-point is important.

10. Reverse saturation current in transistor increases with increase in temperature.

The reverse saturation current is due to thermally generated minority carriers. As temperature increases, more bonds are broken. Hence, more hole-electron pairs (thermally generated) are formed. Therefore, reverse saturation current also increases.

11. Fixed bias circuit cannot provide stable operating point.

In fixed bias circuit, $S = \beta + 1 = \frac{\partial I_C}{\partial I_{CO}}$ i.e. value of stability factor is very high. If $\beta = 50$ then $S = 57$. This indicates I_C will vary 51 times more than that of variations of I_{CO}. Hence, I_C goes on increasing with I_{CO} which leads to thermal runaway. Thus the circuit cannot provide stable operating point.

EXERCISE

1. (a) Draw and explain the biasing circuit in case of :
   (1) Fixed bias
   (2) Fixed bias with emitter resistor R_E in series with emitter reference ground,
   (3) Collector to base bias.

   (b) Derive expressions for stability factor S in terms of the device and circuit component specifications for the above circuits.

   (c) Compare the relative advantages and disadvantages of fixed biasing with potential divider biasing.

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

2. What is meant by bias stability? Which factors can make bias point unstable? Derive the necessary relation to show that in potential divider bias circuit Q-point can be made independent of β.
3. (a) For a CE transistor circuit, sketch the different biasing networks.
   (b) What are the criteria to select a suitable biasing network.
   (c) Compare and contrast the merits and demerits of different biasing schemes.
   (d) How do you avoid loss of signal gain in a self bias scheme.
   (e) Why is potential divider bias commonly used for BJT.
4. Draw and explain the working of following circuits :
   (i) Fixed bias (ii) Collector to base bias.
   Derive the expression for stability factor.
5. (a) Explain concept of operating point with the help of load line and BJT characteristics.
   (b) Draw fixed bias circuit with emitter resistance and derive expression for stability factor.
   (c) For the circuit shown in Fig. 1.70 find operating point, and stability factor.

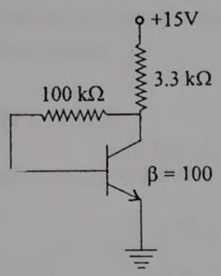


Fig. 1.70

6. Discuss various biasing circuits used for BJT, state their possible applications in actual circuits. Which biasing circuit will you use if BJT is to be used as constant current source.
7. In a circuit shown in Fig. 1.71, determine the co-ordinates of operating point of the transistor. Draw the dc load line on output characteristics and show the location of Q-point. Comment on region of operation. Determine S_{ICO}.

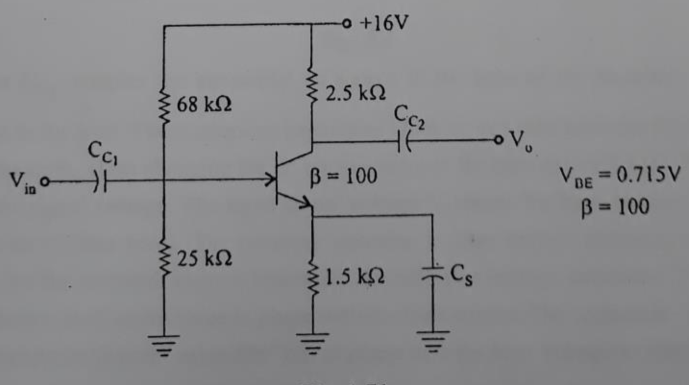


Fig. 1.71

BIPOLAR JUNCTION TRANSISTOR : BJT construction, working, bjt configurations, bjt characteristics, analysis of transistor amplifier, Necessity of DC biasing, Need for stabilization, Analyses and numerical on various BJT biasing circuits(Fixed bias, Fixed emitter bias, Collector to base bias, Collector to base bias with RE, voltage divider bias), derivation of stability factor all biasing circuits, Bias compensation techniques

8. What are the causes of instability of operating point of BJT? Derive expression for thermal stability factor "S_{ICO}" for potential divider bias circuit.

9. (a) State and explain various biasing techniques for BJT (Thermal biasing). Compare them using thermal stability factor.

   (b) Discuss the temperature compensation techniques used for BJT.

10. Determine V_{CE} and I_C for the following circuit.

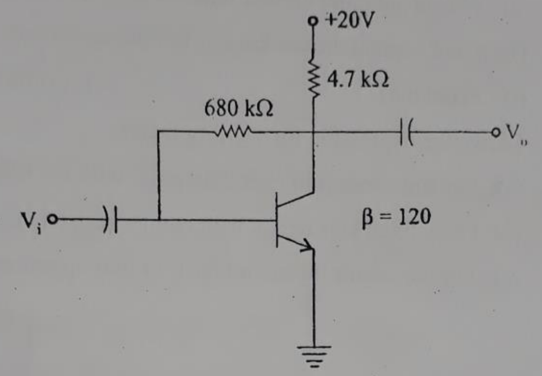


Fig. 1.72

11. Calculate I_B, I_C and V_{CE}.

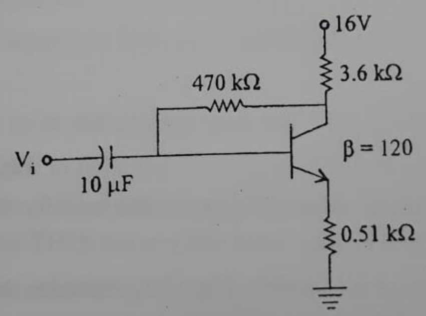


Fig. 1.73