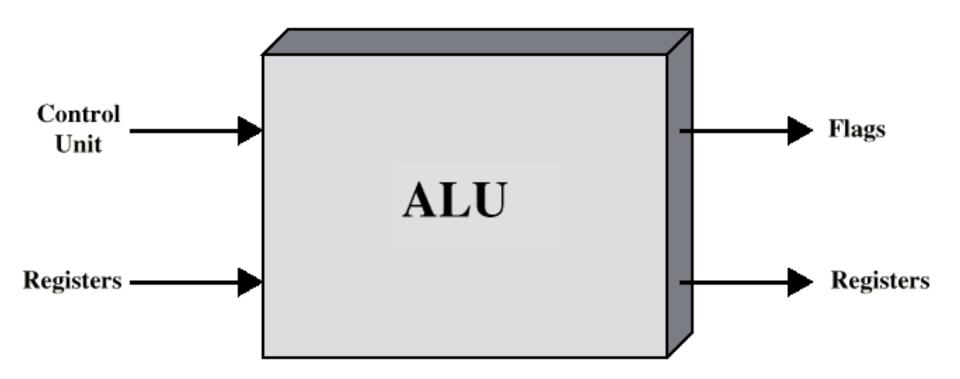
William Stallings Computer Organization and Architecture 6th Edition

Chapter 9 Computer Arithmetic

Arithmetic & Logic Unit

- Does the calculations
- Everything else in the computer is there to service this unit
- Handles integers
- May handle floating point (real) numbers
- May be separate FPU (maths co-processor)

ALU Inputs and Outputs



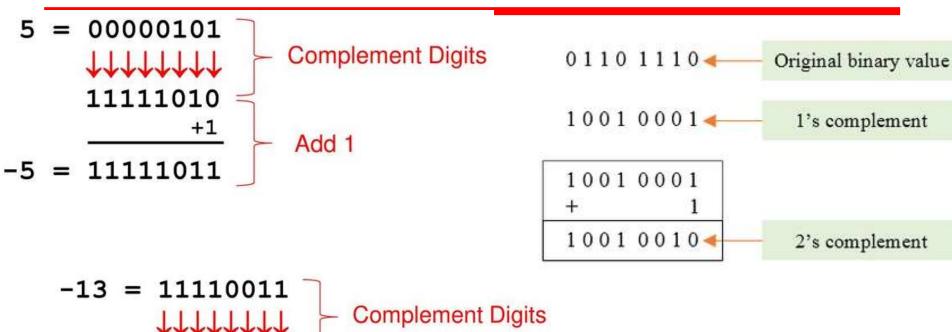
Addition and Subtraction

- Normal binary addition
- Monitor sign bit for overflow
- Take twos compliment of substahend and add to minuend

$$-i.e. a - b = a + (-b)$$

So we only need addition and complement circuits

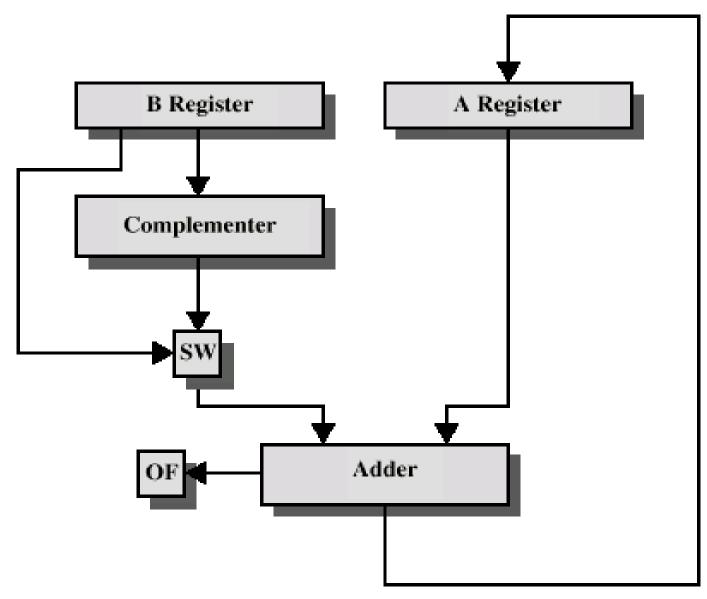
Example of 2's Compliment



$$\begin{array}{rcl}
-13 & = & 11110011 \\
& & \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \downarrow \\
& & 00001100 \\
& & & & +1 \\
13 & = & 00001101
\end{array}$$
Complement Digits

Add 1

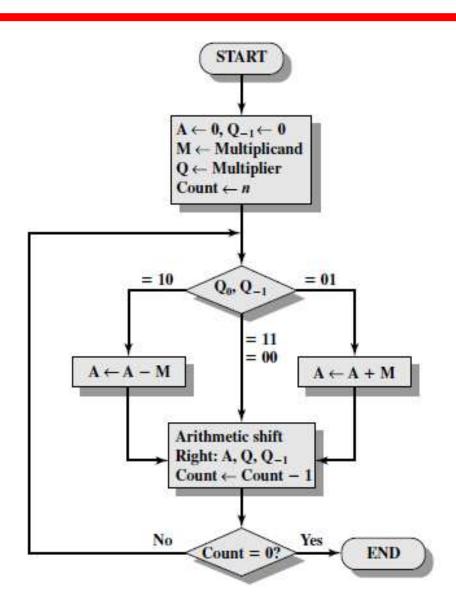
Hardware for Addition and Subtraction



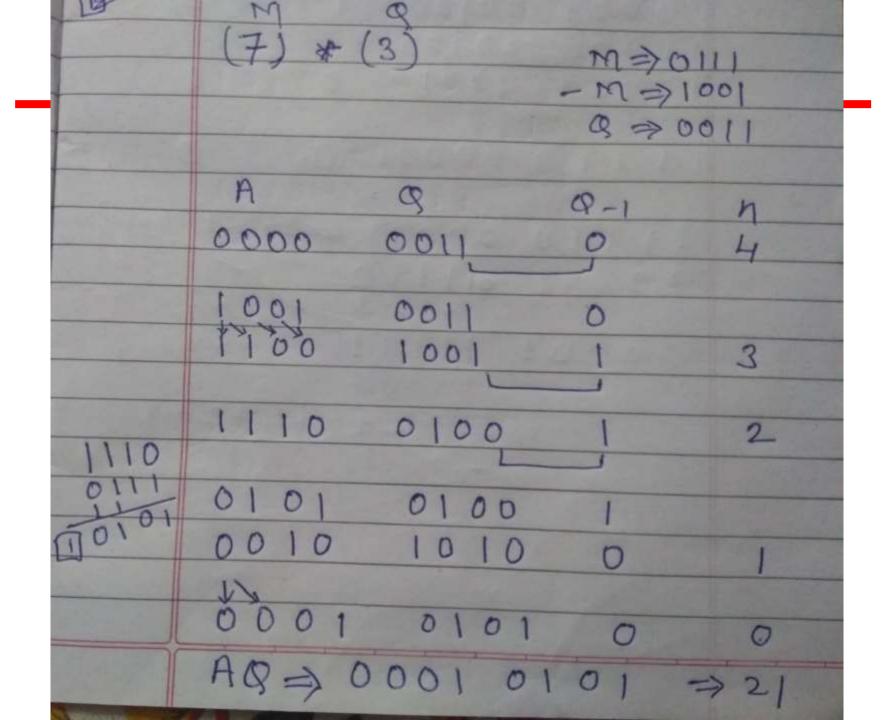
OF = overflow bit

SW = Switch (select addition or subtraction)

Booth's Algorithm



Q0	Q-1	Result
0	0	Only shift
1	1	
0	1	A=A+M ,then shift
1	0	A = A - M, then shift



Example of Booth's Algorithm:7(M)*3(Q)

5	Values	Initial	M 0111	Q_{-1}	Q 0011	A 0000
First	- M}	A = A	0111	0	0011	1001
Cycle	3	Shift	0111	1	1001	1100
nd e	} Second	Shift	0111	1	0100	1110
Third	+ M }	A = A	0111	1	0100	0101
Cycle	5	A = A Shift	0111	0	1010	0010
Fourth	}	Shift	0111	0	0101	0001

Answer is in A and $Q \rightarrow 0001 0101 = 21$

A 0000	Q 0011	Q_1 0	М 0111	Initial values
1001 1100	0011 1001	0	0111 0111	$A \leftarrow A - M$ First Shift Sycle
1110	0100	1	0111	Shift Second cycle
0101 0010	0100 1010	1 0	0111 0111	A ← A + M } Third Shift
0001	0101	0	0111	Shift } Fourth cycle

Figure 9.13 Example of Booth's Algorithm (7×3)

	A Q Q-1 n
	00000 00111 0 5
Mark Comment	
	01001 00111 0 4
	2001001011
	0001001001 1 3
00001	
10111	00001 00100 1 2
1100	11000 00100 1
	11100 00010 0
	11110000010
	10
	1111000001 = In 2's complime
	00001 811110
	0 6 0 0 1 1 1 1 1 1
	23 212 2 2 2
THEN	>32+16+8+4+2+1
	=>-63

Examples-size of n determines answer

Solve using Booths Algorithm

A.
$$M = 5$$
, $Q = 5$

B.
$$M = 12$$
, $Q = 11$

C.
$$M = 9$$
, $Q = -3$

D.
$$M = -13$$
 , $Q = 6$

E.
$$M = -15$$
 , $Q = 15$

F.
$$M = -19$$
 , $Q = -20$

G.
$$M = -7$$
, $Q = 3$

H.
$$M = 15$$
, $Q = -6$

I.
$$M = -12$$
, $Q = -18$

J.
$$M = -7$$
, $Q = 14$

Booths Recoding / Bit pair recording

Booths Recoding / Bit pair recording

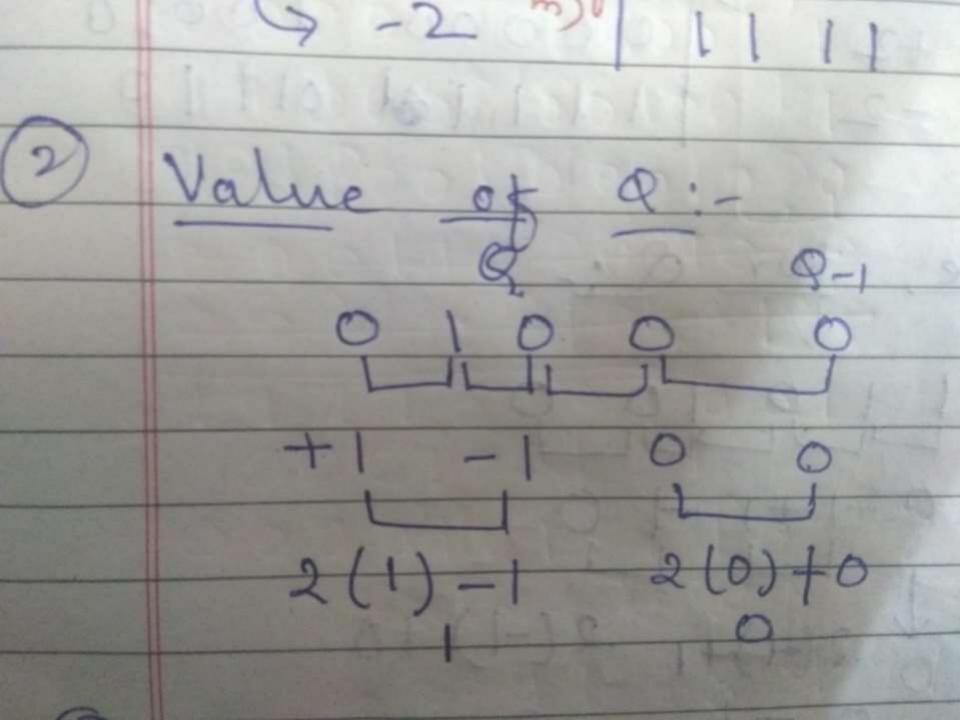
- Derived from the Booth's algorithm.
- Reduced number of steps
- 3 steps
- 1. Calculate the table of M
- 2. Solve for reduced value of Q for 01=+1

for
$$01=+1$$

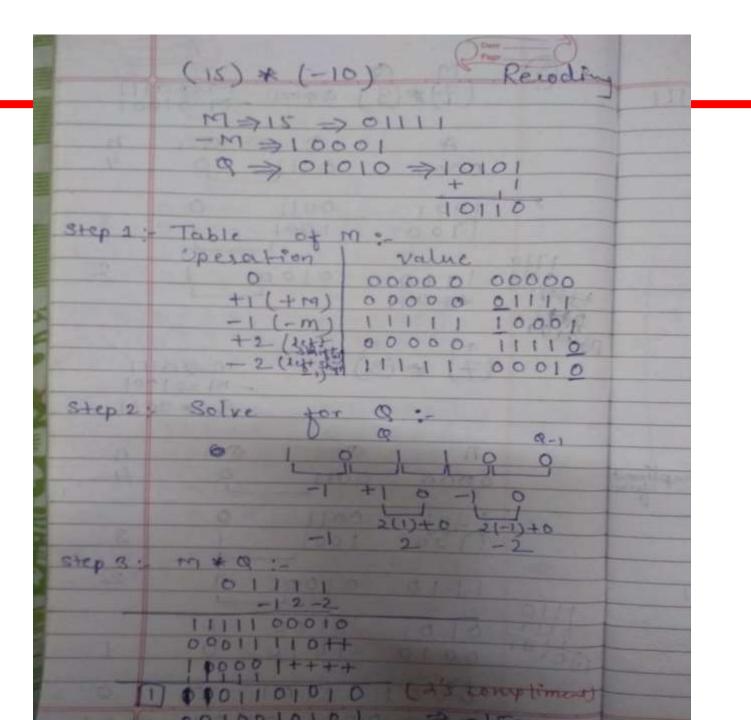
 $10=-1$
 $00/11=0$

3. Perform M*Q

pair recoding of multiplier fast multiplication metho



mra



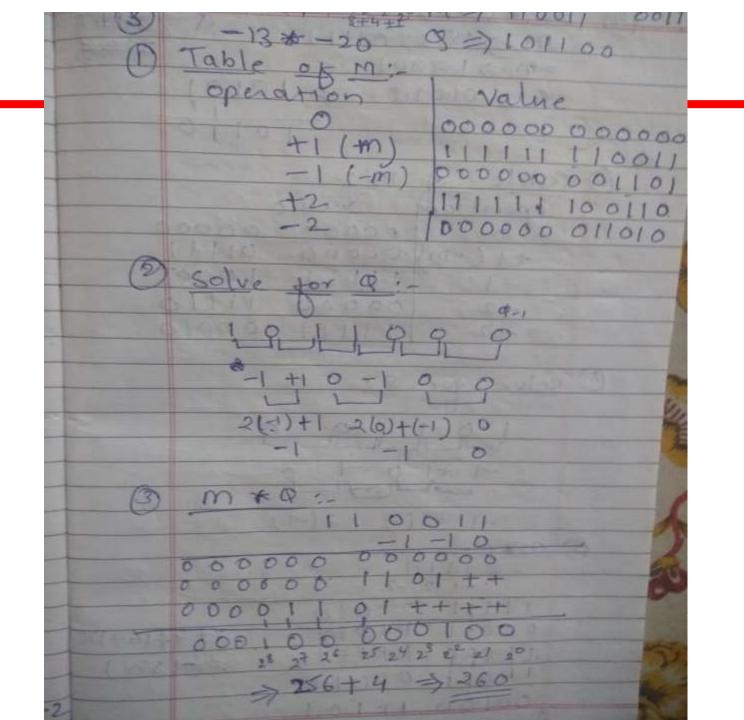
Booths Recoding / Bit pair recoding

Solve Booth's Recoding algorithm

1.
$$M = 9$$
, $Q = -6$ (take 5 bits)

2. Implement multiplication of the following pair of signed 2's complement numbers using bit-pair recoding.

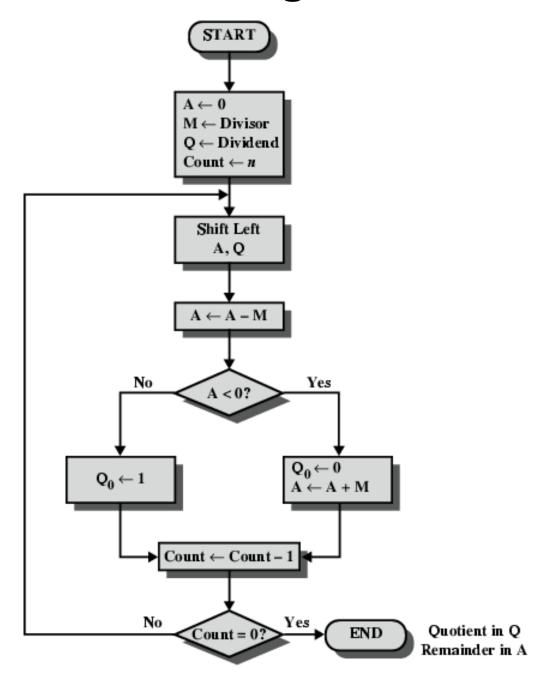
i.e. numbers are -13 * -20

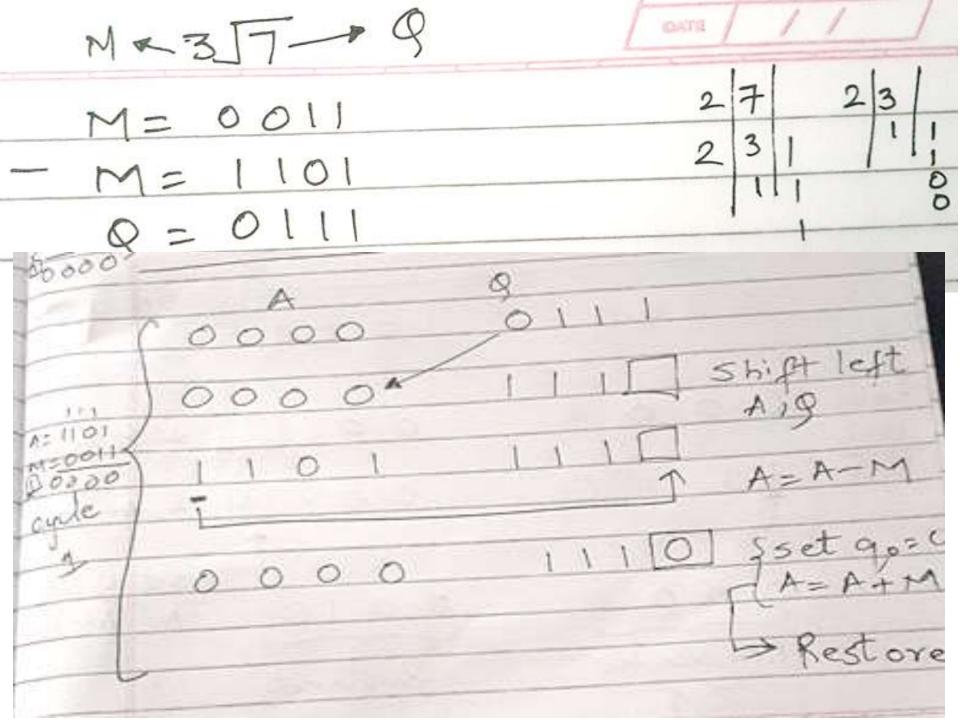


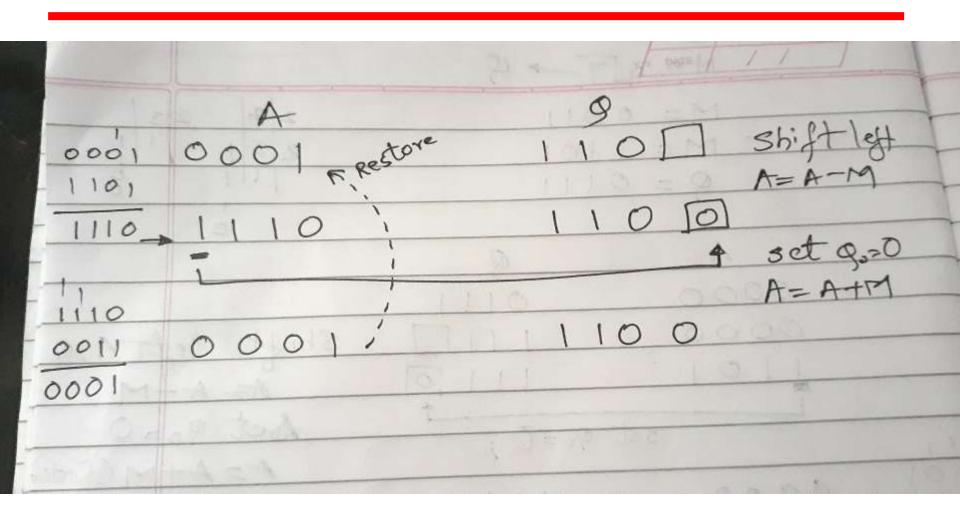
Division

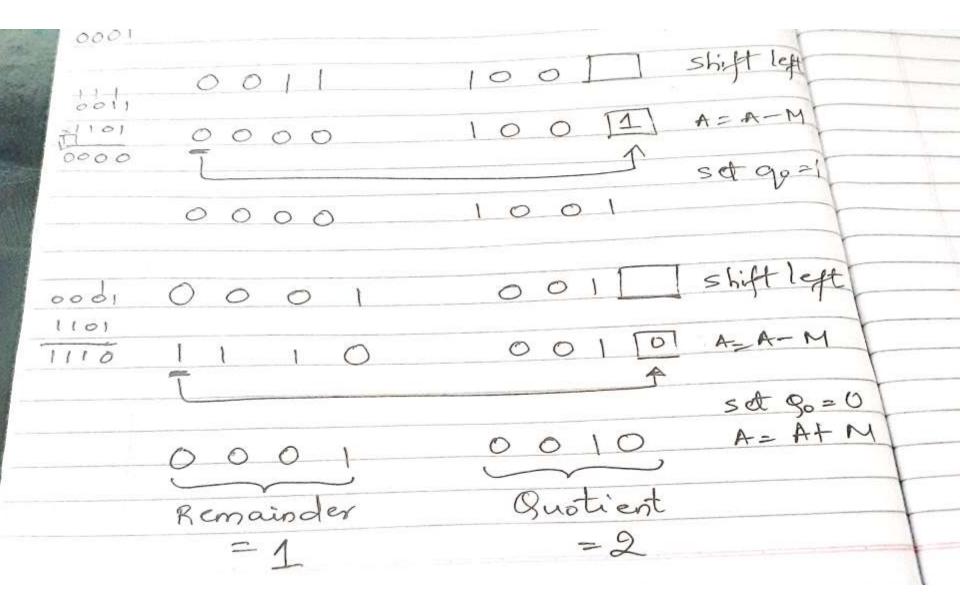
- More complex than multiplication
- Negative numbers are really bad!
- Based on long division

Flowchart for Restoring Division



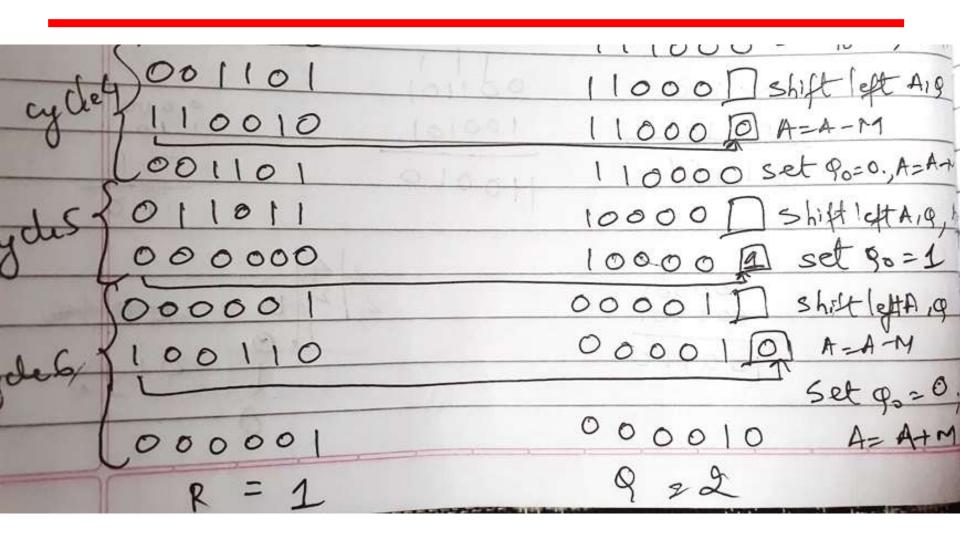


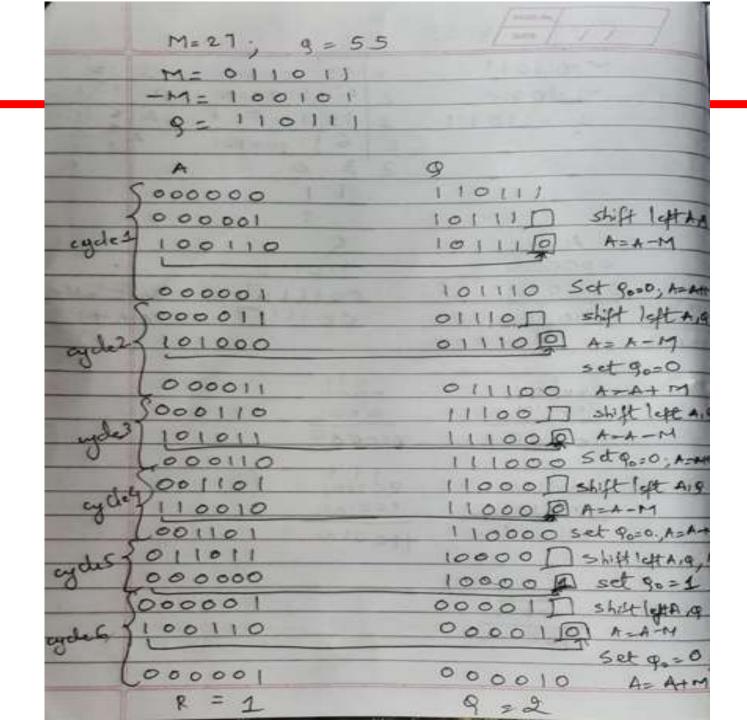




M=27 , 9=55 M= 011011 M= 100101 000000 110111 10111 Shift letter 000001 101110 A=4-M 100110 101110 Set 90=0, A=AH 000001

000011 101000 A= A-M set 90=0 000011 AZA+ M 000110 shift left All 100] 11100 D A=A-M 011 8 500 111000 Stp.=0; A=AA 000110 11000 Shift left A19 001101 11000 DA=A-M 10010 and coton A-At





Solve using Restoring Division

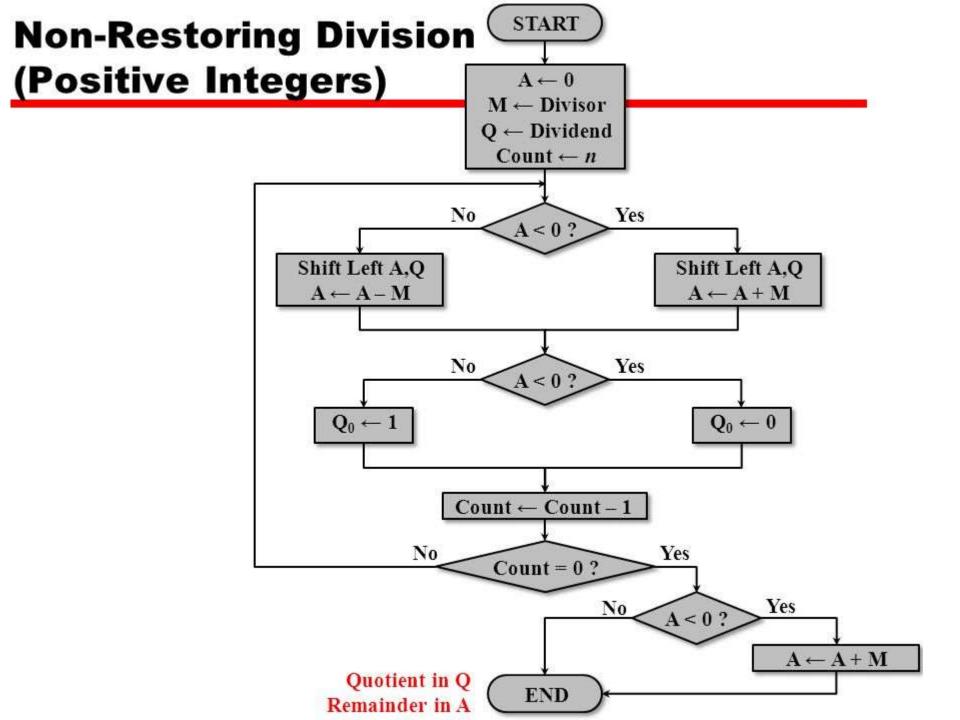
A.
$$M = 5$$
, $Q = 5$

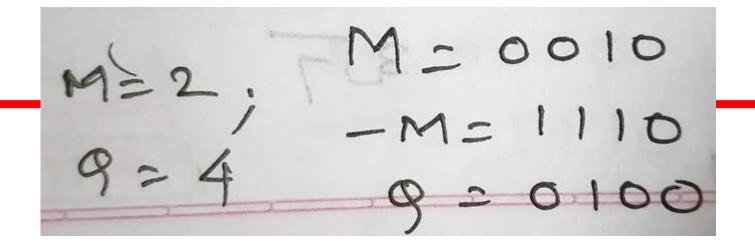
B.
$$M = 12$$
, $Q = 26$

C.
$$M = 9$$
, $Q = 19$

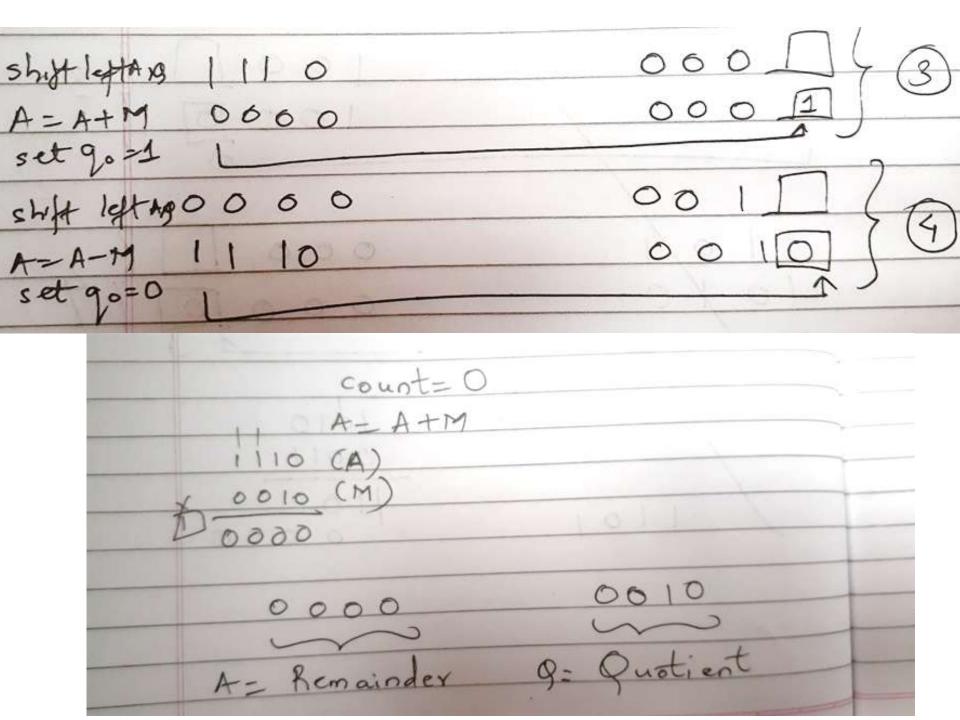
D.
$$M = 32$$
 , $Q = 59$

F.
$$M = 17$$
, $Q = 42$





4 113	9
0000	0100
Shiftlestaign 0000	100 17 (1)
A=A-M set 90=01110	1000)
	1
shift left A, 9 1 0 1	000 1 4 6
A=A+M	0000
set 90=0	1 1



Solve using Non Restoring

A.
$$M = 5$$
, $Q = 5$

B.
$$M = 12$$
, $Q = 26$

C.
$$M = 9$$
, $Q = 19$

D.
$$M = 32$$
 , $Q = 59$

E.
$$M = 17$$
, $Q = 42$

Division of signed numbers

- 1. Load the divisor into the M register and the dividend into the A, Q registers. The dividend must be expressed as a 2*n*-bit twos complement number. Thus, for example, the 4-bit 0111 becomes 00000111, and 1001 becomes 11111001.
- 2. Shift A, Q left 1 bit position.
 - 3. If M and A have the same signs, perform $A \leftarrow A M$; otherwise, $A \leftarrow A + M$.
 - 4. The preceding operation is successful if the sign of A is the same before and after the operation.
 - a. If the operation is successful or A = 0, then set $Q_0 \leftarrow 1$.
 - **b.** If the operation is unsuccessful and $A \neq 0$, then set $Q_0 \leftarrow 0$ and restore the previous value of A.
 - 5. Repeat steps 2 through 4 as many times as there are bit positions in Q.
 - 6. The remainder is in A. If the signs of the divisor and dividend were the same, then the quotient is in Q; otherwise, the correct quotient is the two complement of Q.

The reader will note from Figure 9.17 that $(-7) \div (3)$ and $(7) \div (-3)$ produce different remainders. This is because the remainder is defined by

$$D = Q \times V + R$$

vhere

D = dividend

Q = quotient

V = divisor

R = remainder

The results of Figure 9.17 are consistent with this formula.

A	0	M = 0011	A	Q	M = 1101
0000	0111	Initial value	0000	0111	Initial value
0000	1110	shift subtract	0000	1110	shift add
1101	1110	restore	0000	1110	restore
0001	1100	shift	0001	1100	shift
1110	1100	subtract restore	1110	1100	add restore
0011	1000	shift	0011	1000	shift
0000	1001	subtract set $Q_0 = 1$	0000	1001	$ add set Q_0 = 1 $
0001	0010	shift	0001	0010	shift
1110	0010	subtract restore	1110	0010	add restore

(a) (7)/(3) (b) (7)/(-3)

nea A than	Q Q	M = 0011	A	Q	M = 1101
1111	1001	Initial value	1111	1001	Initial value
1111	0010	shift	1111	0010	shift
0010	0010	restore	0010	0010	subtract restore
1111	0010	restore			
1110	0100	shift	1110	0100	shift subtract
0001	0100	add restore	0001	0100	restore
ft I bit M is s	ed to the le		d O registers to	p, the A and	each ste
1100	1000	shift add	1100	1000	shift subtract
1111	1001	$ set Q_0 = 1 $	1111	1001	$set Q_0 = 1$
es continues fo		ecremented an	count leinen d	S value. The	Dicklor
1111	0010	shift add	0010	0010	subtract
1111	0010	restore	1111	0010	restore
	() (7) (2)			(d) (-7)/(-3)	

(c) (-7)/(3)

(d) (-7)/(-3)

Floating Point

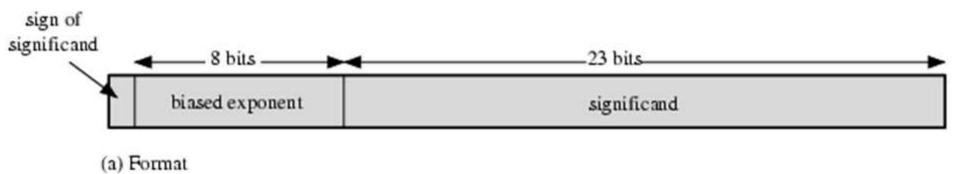
- IEEE Standard 754 floating point is the most common representation today for real numbers on computers, including Intel-based PC's, Macs, and most Unix platforms.
- IEEE, stands for the Institute of Electrical and Electronics Engineers.

Floating Point

Biased Exponent Significand or Mantissa

- +/- .significand x 2^{exponent}
- Point is actually fixed between sign bit and body of mantissa
- Exponent indicates place value (point position)
- E.g. 2.5*2^5

Floating Point Examples



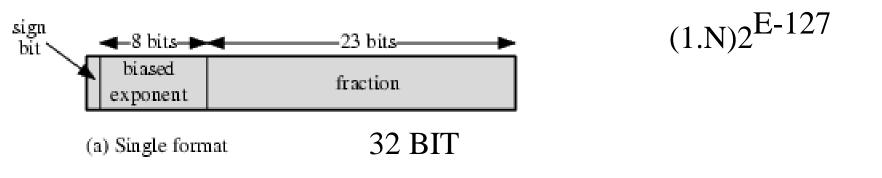
Signs for Floating Point

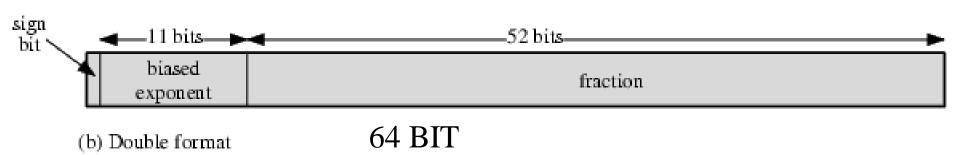
- Mantissa is stored in 2s compliment
- Exponent is in excess or biased notation
 - -e.g. Excess (bias) 128 means
 - —8 bit exponent field
 - —Pure value range 0-255
 - —Subtract 128 to get correct value
 - -Range -128 to +127

IEEE 754

- Standard for floating point storage
- 32 and 64 bit standards
- 8 and 11 bit exponent respectively
- Extended formats (both mantissa and exponent) for intermediate results

IEEE 754 Formats





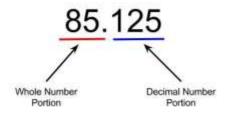
 $(1.N)2^{E-1023}$

Steps

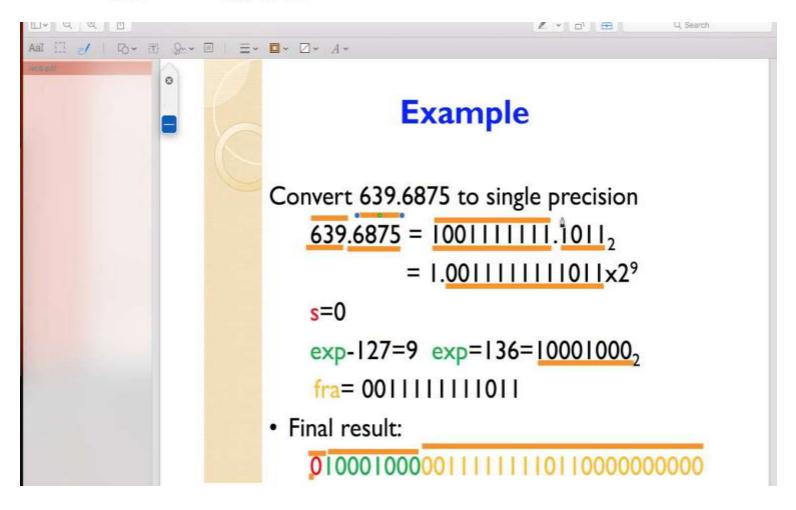
- 1. Convert Decimal to Binary
- 2. Normalization
 - Rewriting Step 1 into (1.N) form

- Ex:
$$1 1 1 . 0 1 1 = 1 . 1 1 0 1 1 x 2^{2}$$
- Ex: $0 . 0 0 0 1 0 = 0 0 0 0 1 . 0 x 2^{-4}$

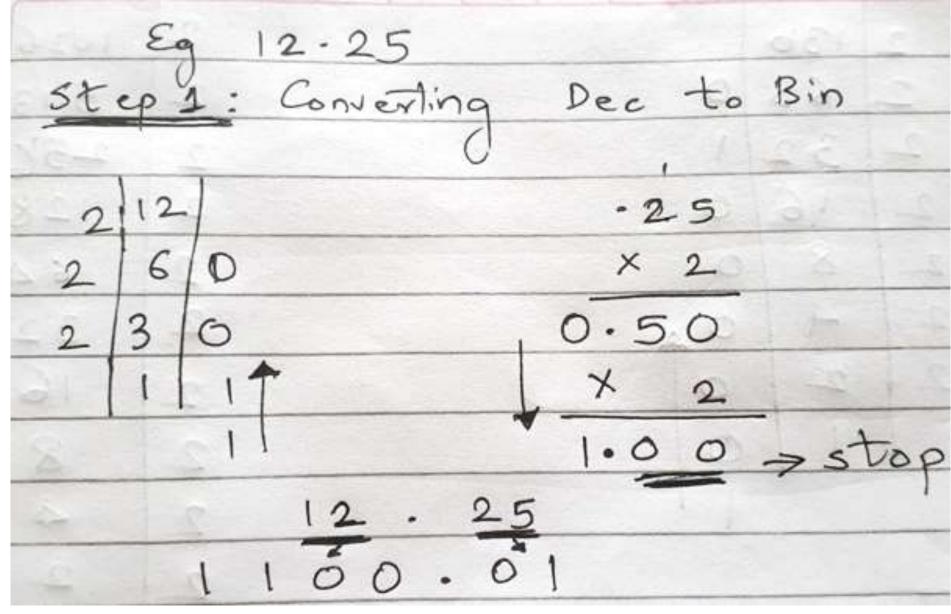
- 3.Biasing
 - Applying Single Precision (E 1 2 7) & Double Precision (E 1 0 2 3) on exponent from Step 2
- 4. Representation in Single (32 bit)and Double Precision (64 bit) Format



85 0.125



Solved Example



Normalization (1. N) Step 2: 1.10001 X 2 Exponent Step3: Biasing Single Precision Double precision E-127 E-1023 3= E-1023 3 = E-127 E=1023+3 E = 127 +3 = 1026

2 128 0 2 64 0 2 32 0 2 16 0 2 8 2 2 4 0
2 64 0 2 32 0 2 16 0
2 64 0 2 32 0 2 16 0
2 64 0
2 64 0
2 128 0
2 256 1
2 513 0

Single Precision (32 bits) Sign bit Biased Exponent Man Mantissa/Significana 10001 110000010 23 bits 1 bit 8 bits Precision (64 bits) Double 10001

#1 bits 52 bits

1 bit

Solve

25.44

178.1875 Single precision: 0 10000110 01100100011

Double precision: 0 1000000110 01100100011

-309.1875 Single precision: 1 10000111 00110101011

Double precision: 1 10000000111 00110101011

0.00635

-125.10

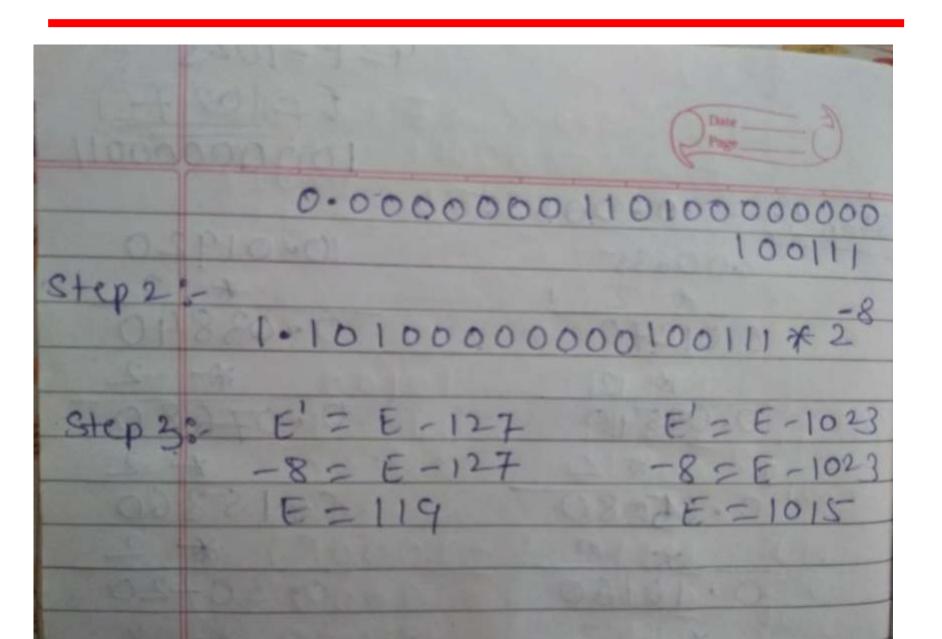
13.54 Single precision: 0 10000100 10110001010001111010111

Double precision: 0 10000000011 10110001010001111010111

Solve 0.00635

1=1-1023 E 51627 1000000011	0.01920	* 2	0-03840	* 2	0.07680	* 2	00 5360	* 2	0.30720	* 2	0.61440	* 2	1.22880	4	94	* 2	0.91520	*	1.83040	* 2	1.66080	70 块	1.32160			
0.00635	0.00635	121	0.01270	* 2	0.02540	* 2	0.04080	* 2	16	* 2	0 - 20320	* 2	190	* 2	128	* 2	1 . 62560	* 2	1.25120	* 2	5.50240	* 2	1.00480	* 2	09600.0	0.01920
Step 1:	1		4 1		Store.	1015	TORS																		1	

Solve 0.00635



FP Arithmetic +/-

- Check for zeros
- Align significands (adjusting exponents)
- Add or subtract significands
- Normalize result

Floating Point Addition

Add the following two decimal numbers in scientific notation:

$$8.70 \times 10^{-1}$$
 with 9.95×10^{1}

Rewrite the smaller number such that its exponent matches with the exponent of the larger number.

$$8.70 \times 10^{-1} = 0.087 \times 10^{1}$$

Add the mantissas

$$9.95 + 0.087 = 10.037$$
 and

write the sum 10.037×10^{1}

Put the result in Normalised Form

$$10.037 \times 10^1 = 1.0037 \times 10^2$$
 (shift mantissa, adjust exponent)

Check for overflow/underflow of the exponent after normalisation

Overflow

The exponent is too *large* to be represented in the Exponent field

Underflow

The number is too *small* to be represented in the Exponent field

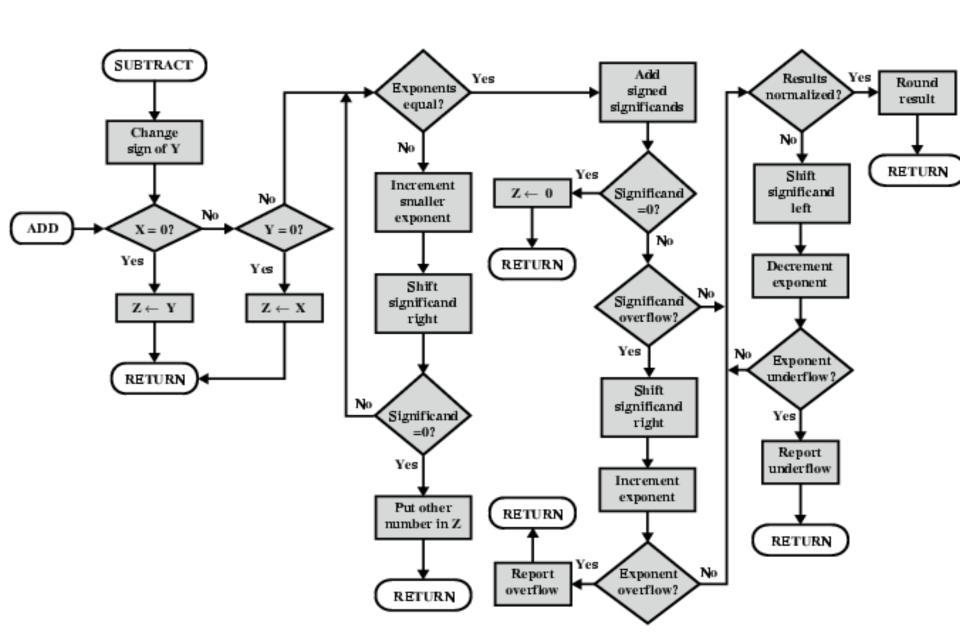
Round the result

If the mantissa does not fit in the space reserved for it, it has to be rounded off.

For Example: If only 4 digits are allowed for mantissa

$$1.0037 \times 10^2 ===> 1.004 \times 10^2$$

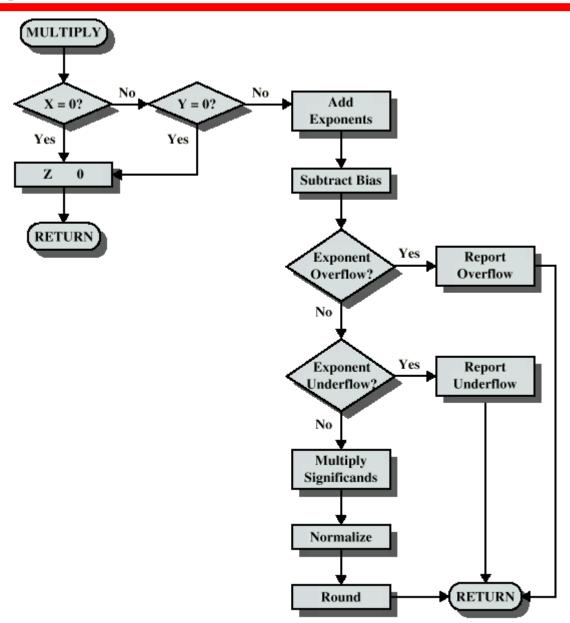
FP Addition & Subtraction Flowchart



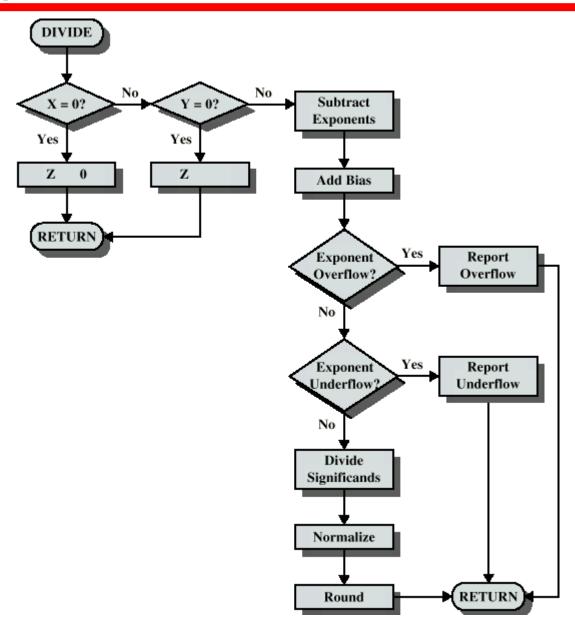
FP Arithmetic x/÷

- Check for zero
- Add/subtract exponents
- Multiply/divide significands (watch sign)
- Normalize
- Round
- All intermediate results should be in double length storage

Floating Point Multiplication



Floating Point Division



Example addition in binary Perform 0.5 + (-0.4375)

$$0.5 = 0.1 \times 2^0 = 1.000 \times 2^{-1}$$
 (normalised)

$$-0.4375 = -0.0111 \times 2^{0} = -1.110 \times 2^{-2}$$
 (normalised)

Rewrite the smaller number such that its exponent matches with the exponent of the larger number.

$$-1.110 \times 2^{-2} = -0.1110 \times 2^{-1}$$

Add the mantissas:

$$1.000 \times 2^{-1} + -0.1110 \times 2^{-1} = 0.001 \times 2^{-1}$$

Normalise the sum, checking for overflow/underflow:

$$0.001 \times 2^{-1} = 1.000 \times 2^{-4}$$

Round the sum:

The sum fits in 4 bits so rounding is not required

Check: $1.000 \times 2^{-4} = 0.0625$ which is equal to 0.5 - 0.4375