K. J. Somaiya College of Engineering, Mumbai-77
(A Constituent College of Somaiya Vidyavihar University)
Department of Computer Engineering

Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**_02_ / _08_ / __2024____**	**Batch No:**	**E-2**
Faculty Name:		**Roll No:**	**16010123325**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 1
Title: Study of Basic Gates and Universal Gates

Aim and Objective of the Experiment:

Understand Basic Logic Gates and Universal Gates

COs to be achieved:

CO1: Recall basic gates & logic families and binary, octal & hexadecimal calculations and conversions.

Tools used:

Trainer kits

Theory:

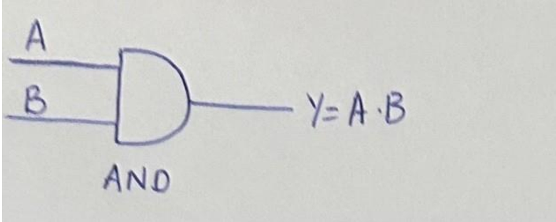
Logic gates are electronic circuits that perform logical operations on one or more input signals to produce an output signal based on a set of logical rules. Logic gates can be classified into the following categories:

1. Basic Gates:
    a. AND Gate: The AND gate produces a high output (1) only when all of its inputs are high (1).
    b. OR Gate: The OR gate produces a high output (1) if any of its inputs is high (1).
    c. NOT Gate (Inverter): The NOT gate produces the logical complement of its input. It takes a single input and produces the opposite value as the output.
2. Derived Gates:
    a. NAND Gate: The NAND gate is a combination of an AND gate followed by a NOT gate. It produces the inverse of the AND gate's output. It outputs a low (0) only when all of its inputs are high (1).
    b. NOR Gate: The NOR gate is a combination of an OR gate followed by a NOT gate. It produces the inverse of the OR gate's output. It outputs a high (1) only when all of its inputs are low (0).
    c. XOR Gate (Exclusive OR): The XOR gate produces a high output (1) when the number of high inputs is odd. It outputs a low (0) when the number of high inputs is even.
    d. XNOR Gate (Exclusive NOR): The XNOR gate produces a high output (1) when the number of high inputs is even. It outputs a low (0) when the number of high inputs is odd.
3. Universal Gates:
    NAND and NOR gates are considered universal gates because any logic function can be implemented using only NAND gates or only NOR gates. This means that with a sufficient number of NAND or NOR gates, you can create circuits that can perform any logical operation.

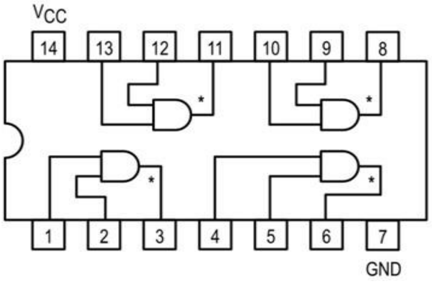
Implementation Details

1. AND Gate: Y = A.B

Symbol



Pin Diagram

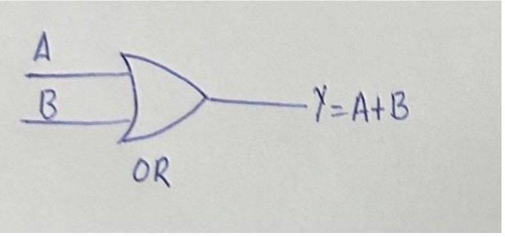


Truth Table:

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

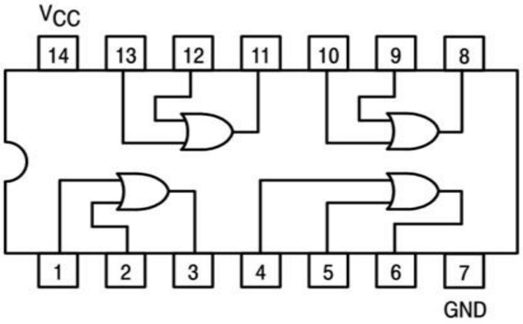
2. OR Gate: Y = A+B

Symbol



Pin Diagram

IC 7432

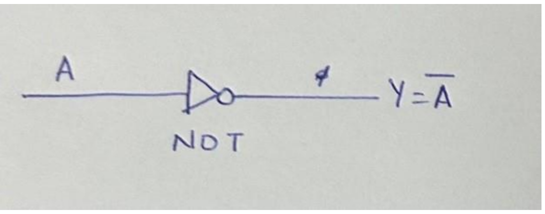


Truth Table:

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

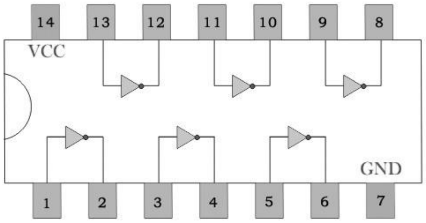
3. NOT Gate: Y = Ā

Symbol



Pin Diagram

IC 7404

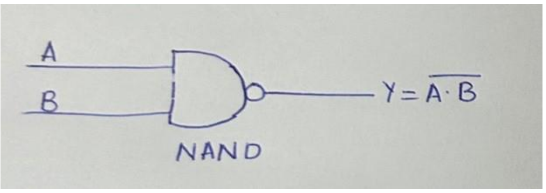


Truth Table:

A	Ā
0	0
0	1
1	0
1	1

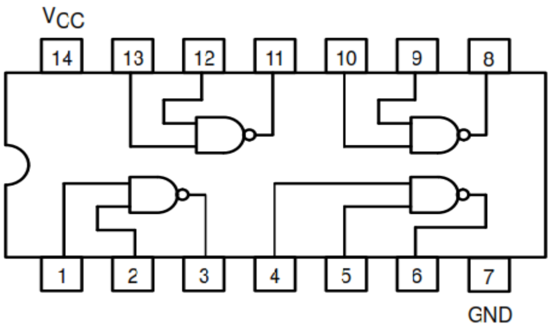
4. NAND Gate: $Y = (A.B)^c$

Symbol



Pin Diagram

IC 7400

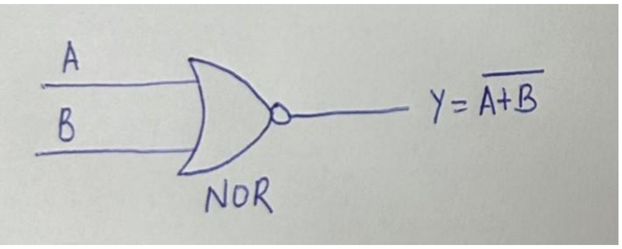


Truth Table:

A	B	$(A.B)^c$
0	0	1
0	1	1
1	0	1
1	1	0

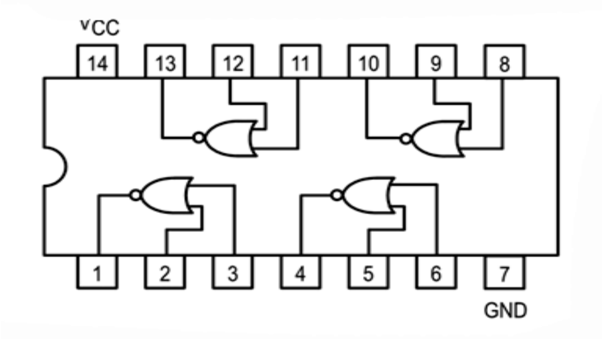
5. NOR Gate: Y = $(A+B)^c$

Symbol



Pin Diagram

IC 7402

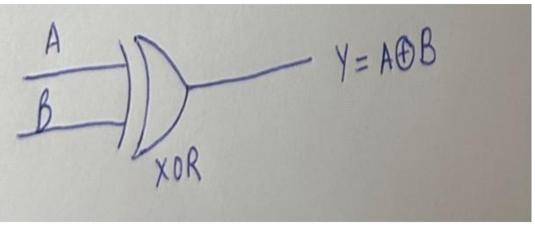


Truth Table:

A	B	$(A+B)^c$
0	0	1
0	1	0
1	0	0
1	1	0

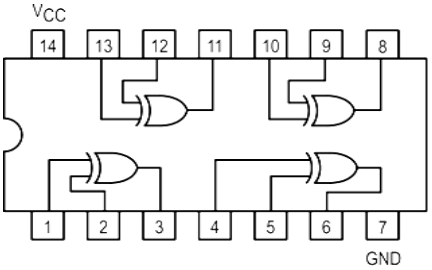
6. XOR Gate: $Y = A \oplus B$

Symbol



Pin Diagram

IC 7486

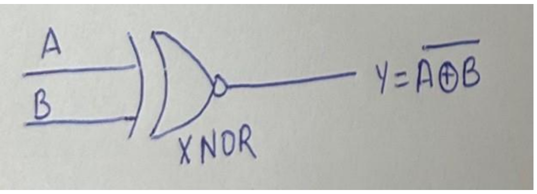


Truth Table:

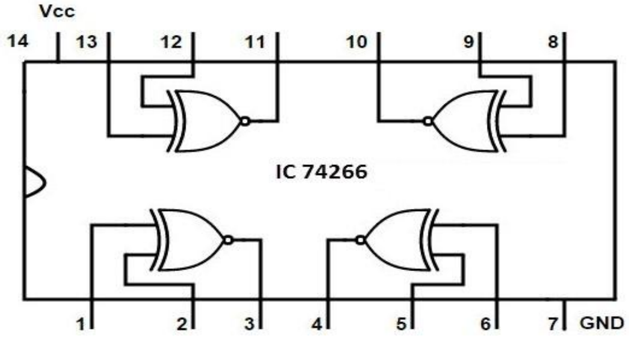
A	B	$(A \oplus B)^c$
0	0	0
0	1	1
1	0	1
1	1	0

7. XNOR Gate: Y =

Symbol



Pin Diagram

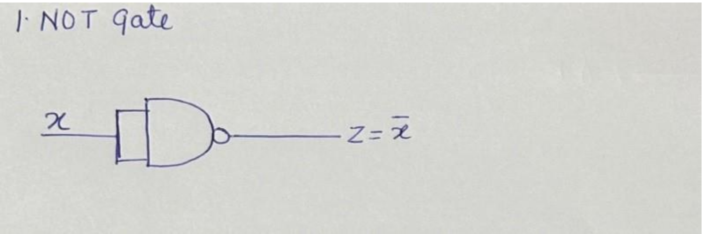


Truth Table:

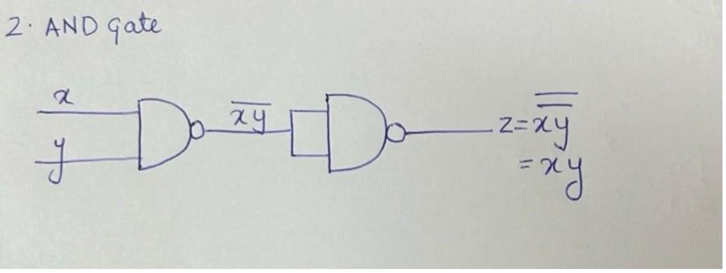
A	B	A ⊕ B
0	0	1
0	1	0
1	0	0
1	1	1

Implementation Using NAND Gate

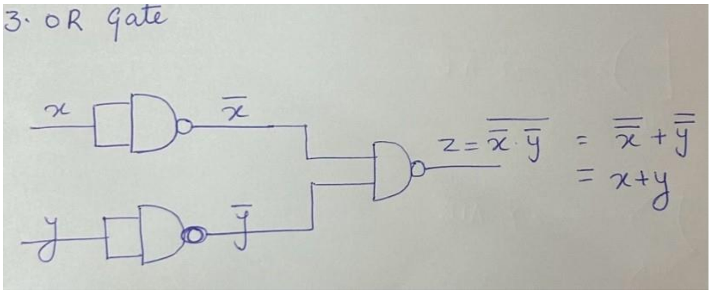
NOT GATE



AND GATE

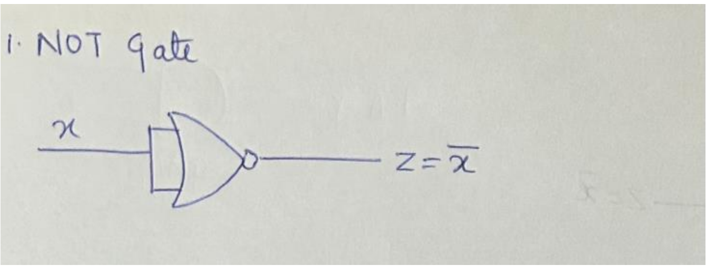


OR GATE

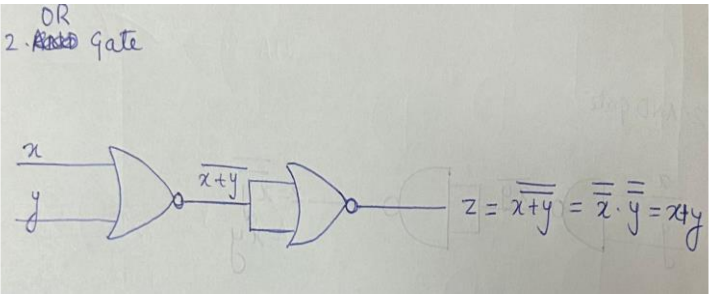

3. OR gate
x
$\bar{x}$
y
$\bar{y}$
$z = \overline{\bar{x} \cdot \bar{y}}$
$= \bar{\bar{x}} + \bar{\bar{y}}$
$= x+y$

Implementation Using NOR Gate

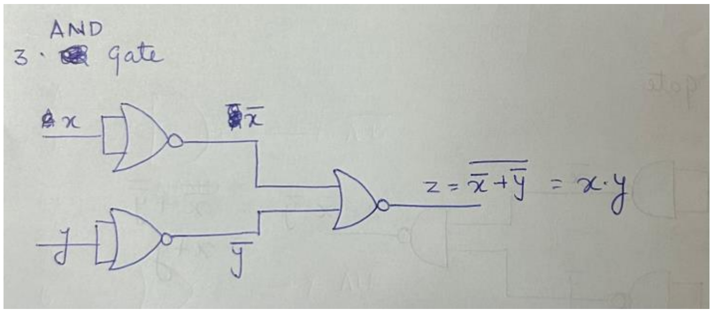
NOT GATE



OR GATE

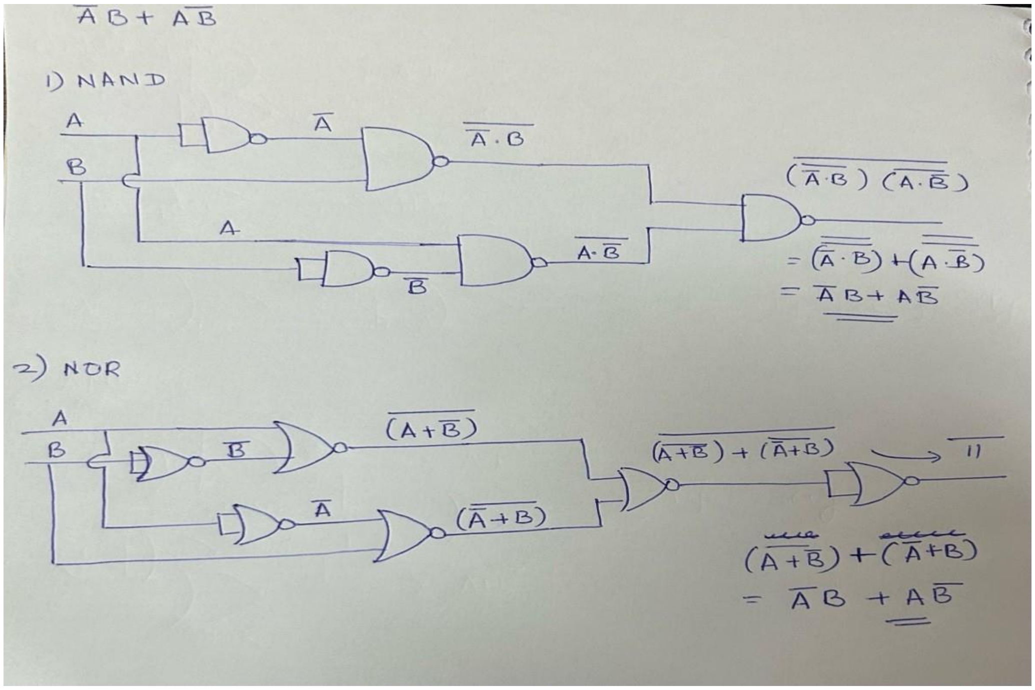

2. OR Gate
x
y
$\overline{x+y}$
$z = \overline{\overline{x+y}} = \overline{\overline{x}} \cdot \overline{\overline{y}} = x+y$

AND GATE

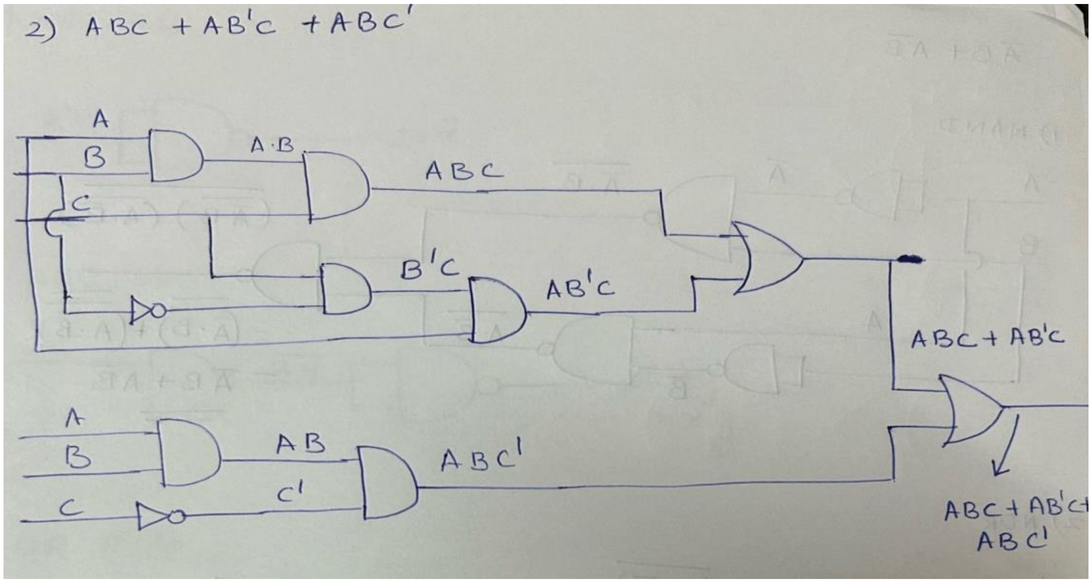


Post Lab Subjective/Objective type Questions:

1. Implement the Boolean function using NAND gates and NOR gates F=A’B + AB’


$\bar{A}B + A\bar{B}$
1) NAND
A
B
$\bar{A}$
$\overline{\bar{A} \cdot B}$
A
$\bar{B}$
$\overline{A \cdot \bar{B}}$
$\overline{(\overline{\bar{A} \cdot B})(\overline{A \cdot \bar{B}})}$
$= (\overline{\overline{\bar{A} \cdot B}}) + (\overline{\overline{A \cdot \bar{B}}})$
$= \bar{A}B + A\bar{B}$
2) NOR
A
B
$\bar{B}$
$\overline{(A+\bar{B})}$
$\bar{A}$
$\overline{(\bar{A}+B)}$
$\overline{\overline{(A+\bar{B})} + \overline{(\bar{A}+B)}}$
$\overline{\overline{\quad}}$
$\overline{\overline{(A+\bar{B})}} + \overline{\overline{(\bar{A}+B)}}$
$= \bar{A}B + A\bar{B}$

2. Implement using combination of gates F = ABC + AB’C + ABC’



Conclusion:
Through this experiment we learned about using Logic gates IC on the kit and also how to do implementations of equations using logic gates.

Signature of faculty in-charge with Date: