Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:		**Batch No:**	**E2**
Faculty Name:		**Roll No:**	**16010123325**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 7
Title: Asynchronous Counter

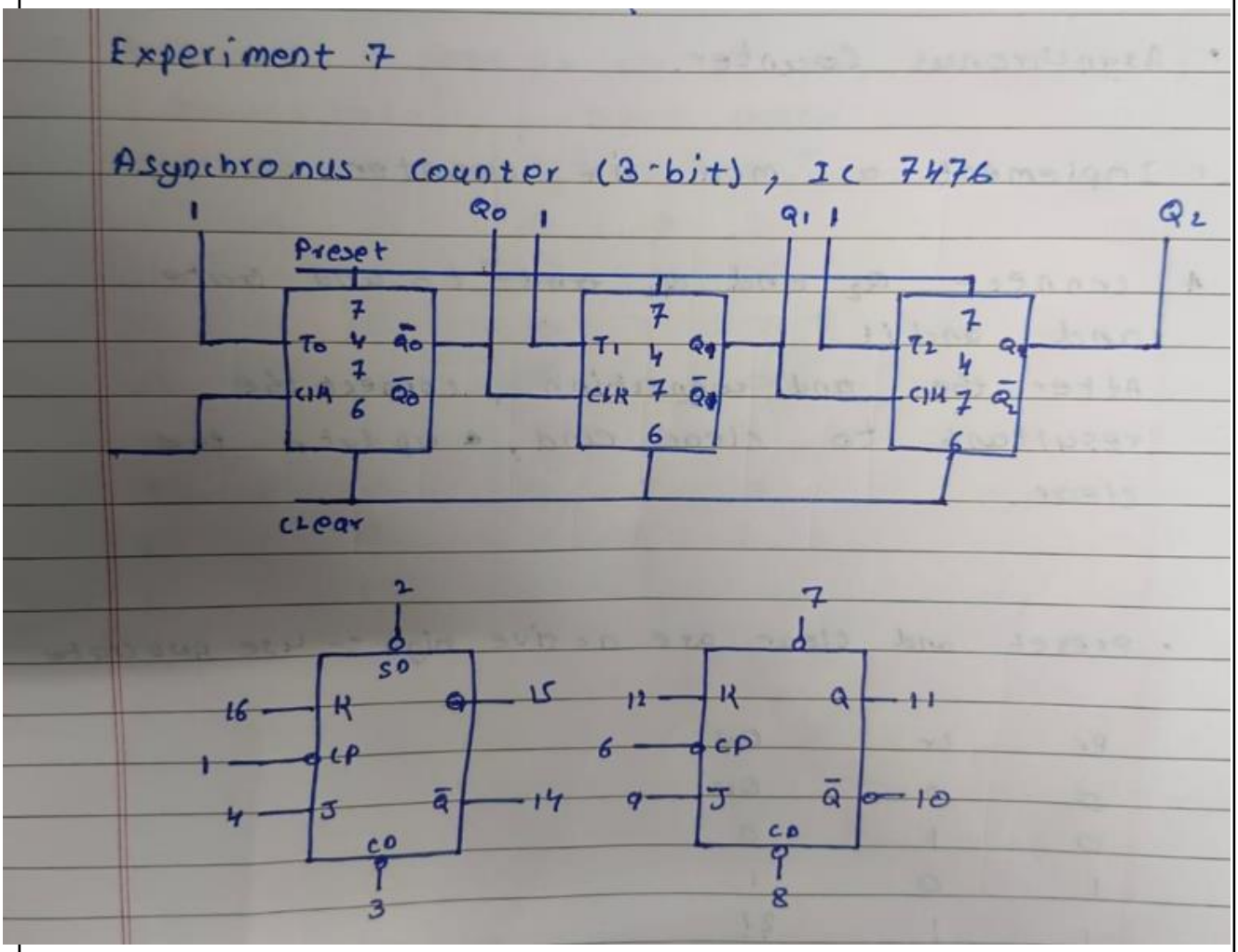
Aim and Objective of the Experiment:
To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:
CO3: Design synchronous and asynchronous sequential circuits.

Tools used:
Trainer kits

Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)



Implementation Details

Procedure

1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

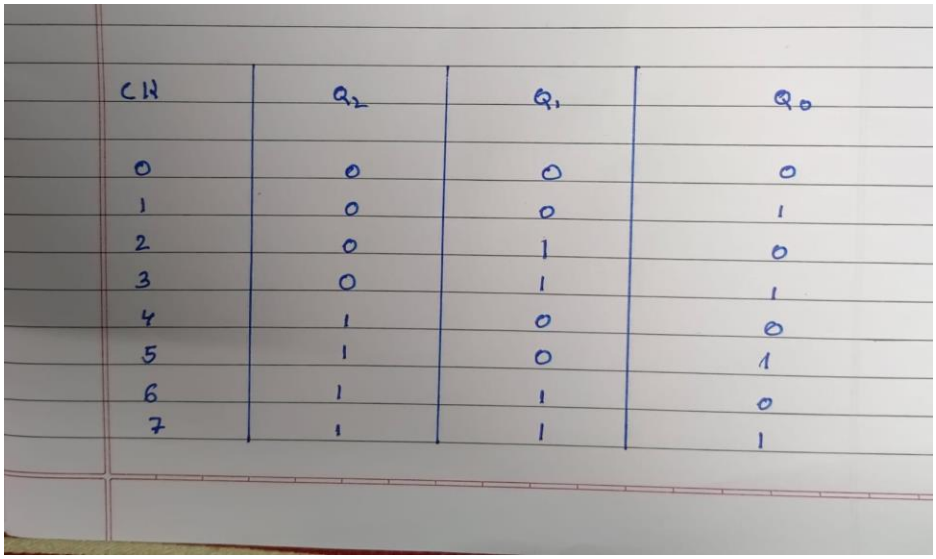
1. How JK FF need to be configured to use for counter operation?

- **Answer :** JK flip-flops are configured to toggle their state when both J and K inputs are set to 1. For counter operations, each flip-flop in the series is typically connected so that the output of one serves as the clock input of the next. The first flip-flop (LSB) toggles on every clock pulse, and subsequent flip-flops toggle based on the output of the preceding one.

2. What changes are required to use the same counter as 3 bit asynchronous down counter?

- **Answer:** In a synchronous down counter, all flip-flops are clocked simultaneously (synchronously), but the toggling logic must be modified. The flip-flops toggle when the previous stage's output is 0 instead of 1, as in the up counter. The logic that controls each flip-flop's J and K inputs is inverted from that of an up counter.

3. Draw the timing diagram of 3 bit Asynchronous up counter.



CN	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

4. What is mod n concept used in counters?

- **Answer:** A mod-n counter is a counter that goes through n unique states before resetting to zero. The number of states corresponds to the modulus of the counter. For example, a mod-8 counter counts from 0 to 7 (8 states) before starting over. The modulus determines the maximum count the counter can hold**.**

5. For Mod-5 counter how many JK FFs are required?

- **Answer:** The number of flip-flops required for a counter is determined by the smallest number n such that $2n \geq$ mod number. For a Mod-5 counter: 23=8 (since 22=4 is not enough to represent 5 states, we need 3 flip-flops). Therefore, 3 JK Flip-Flops are required for a Mod-5 counter.

Conclusion:

We learnt to design and implement 3 bit Synchronous up counter using JK Flip Flop.

Signature of faculty in-charge with Date: