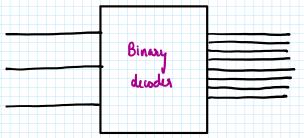
26 August 2024 08:54

## DECODERS

n inputs -> 2<sup>n</sup> outputs: no select signal and no demarcation of control & data signal



Pata signal itself is the control signal

## ENCODERS

Opposite of decoders

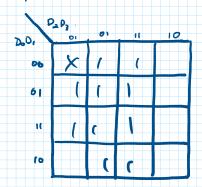
2" input --> n outputs

8:3 -> odal to

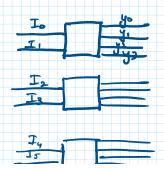
· At any given time, only one input line is at 1

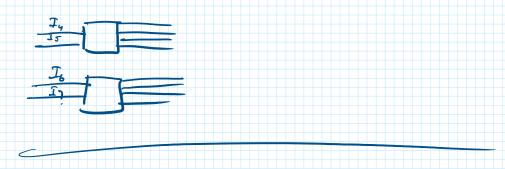
Priority encoder

If more than one input line is high, the higher input is given priority to get
output.

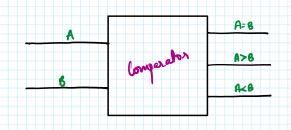


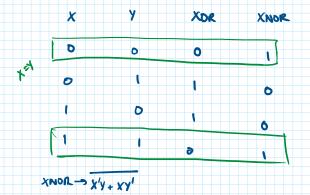
Construct 4:16 line decoder with 5 2:4 line decoder with enable.





# 4-BIT MAGNITUDE COMPARATOR Say A - A3A, A, A6 A bit binary numbers B = B3 B, B6





$$A = B \implies A_{3} = B_{3}, A_{3} = B_{3}, A_{1} = B_{1}, A_{0} = B_{0}$$

$$\implies (A_{3}B_{3}' + A_{3}'B_{3})(---)(---)(---)(---)$$

$$A > B \implies A_{3} > B_{3}$$

$$A_{2} = B_{3}, A_{2} > B_{2}$$

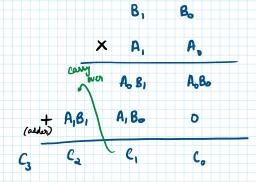
$$A_{3} = B_{3}, A_{2} > B_{3}$$

$$A_{3} = B_{3}, A_{2} > B_{3}$$

$$A_{1} = B_{1}, A_{0} > B_{0}$$

$$A > B \implies A_{3}B_{3}' + X_{3} \cdot A_{2}B_{2}' + X_{3}X_{2}A_{1}B_{1}' + X_{3}X_{2}X_{1}A_{0}B_{0}'$$

# 2 BIT BY & BIT BINARY MULTIPLIER



# 4 Bit by 3 BIT BINARY MULTIPLIER

Let 
$$A = A_2 A_1 A_6$$
  
 $B = B_3 B_2 B_1 B_6$ 

TWOS COMPLEMENT NONSENSE

BCD ADDER (DECIMAL ADDER)