Verilog -> HDL (Hardware Description Language)

Module Declaration

```
module module_name circuit_name (port_list);
//port list contains all the input and output ports
        port declarations;    // declaring which are input and which are output
        ...
        variable declaration
        ...
        description of behaviour
endmodule
```

- Nesting of modules possible

Basic Structure

- For whatever digital circuit, you **have** to create two files: main file and validation file

Main file

```
/* Simple AND gate: and2.v */
module andgate2 (y,a,b);
        input a,b;
        output y;
        assign y = a&b;  /* assign -> keyword that assigns value to op var */
endmodule
```

Validation file

```
/* testbench for AND gate: and2_tb.v */
module and_test;
        reg a, b;   // register a and b
        wire y;    // named container for values that are "stateless" (no memory)
        andgate2 and_test(y,a,b);
        // calling the function defined earlier and assigning it to and_test

        initial   // initialises a block
        begin    // begins block statements
                #0 a=0; b=0;
                #100 a=0; b=1;
                #100 a=1; b=0;
                #100 a=1; b=1;
                #100 a=1; b=1;
        end    // ends block
        initial
        begin
                $monitor($time, "a=%b, b=%b, y=%b", a, b, y);   // display function
        end

        initial
        begin
                $dumpfile("and2_test.vcd");
                $dumpvars(0, and_test);
        end
endmodule
```

NOTE - Dumpfiles:
VCD is an ASCII format of dumping defined originally by Verilog IEEE standard (1364–1995) . It contains information about value changes in variables across time. There are system functions supported to control dump scope and duration.
It was originally intended to be used with waveform viewers for debug. Given that it is part of the IEEE Verilog standard, all waveform viewers across vendors support it. However since it is ASCII, the dump file sizes can be really large and generally it is not commonly used these days. The other usage of VCD dump is for estimating power consumption (RTL/gate power analysis) based on signals toggling across various time boundaries.

Execution

```
>> iverilog -o output_file_name and2.v and2_tb.v
>> vvp output_file_name
>> gtkwave and2_test.vcd
```

- `-o` = output
- Line 1 creates a compiled simulation file with the name `output_file_name`. Line 2 runs that simulation using the `vvp` command.
- Line 3 opens GTKWave where you can view the input and output waveforms.