

PES University, Bangalore (Established under Karnataka Act No. 16 of 2013)

UE20EC101

August 2021: END SEMESTER ASSESSMENT- B.TECH. II SEMESTER **UE20EC101** – Electronic Principles and Devices

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Mov Morlo	Max Marks. 100	n current is 15nA at n current is 12nA at	wn values for the	4.7 KD	A 9- 9	00K. Find diode is 0.27 volts.	tifier with Centre	00μF Capacitor is ge at the output if Iso find the ripple	e in the "on" state
Answer All Oriections		V and its reverse saturation V and its reverse saturation It at 43°C and 48°C.	diode to determine the unknown values for the circuit (ii) Determine I _D and V ₀ for the circuit	+8 V 0 1.2 kg		it of 15μA at temperature 30. If the forward bias voltage	principle of Full wave Recsion for V _{dc} and V _{ms}	oltage for the FWR if a 10 rrent. What is the dc voltagend frequency is 50Hz? Al	ill maintain the Zener diode
		Solve the following (i) The knee voltage of a Si diode is 0.68V and its reverse saturation current is 15nA at 25°C. Determine knee Voltage at 40°C. (ii) The knee voltage of a Si diode is 0.69V and its reverse saturation current is 12nA at 28°C. Determine reverse saturation current at 43°C and 48°C.	nd approximation for a mine I and V _o for the the Figure below	\$i ₹ 11 Si ₹ € 11	1.7kΩ \$ -4V	A Ge diode has a reverse saturation current of $15\mu\text{A}$ at temperature 300K. Find diode current at 40°C using Shockley's equation, If the forward bias voltage is 0.27 volts.	With a neat diagram, explain the working principle of Full wave Rectifier with Centre tapped Transformer and derive the expression for V _{dc} and V _{ms}	Calculate the RMS value of the ripple voltage for the FWR if a $100\mu F$ Capacitor is connected to a load drawing 50mA of current. What is the dc voltage at the output if the peak rectified output voltage is 30V and frequency is 50Hz? Also find the ripple factor.	Determine the range of values of Vi that will maintain the Zener diode in the "on" state for the following Circuit.
Time: 180 mins			-			A Ge d current	With a tapped	Calcula connect the pea factor.	Determ for the
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$\begin{pmatrix} R & I_R \\ + & 200\Omega \\ V_Z = 18V & V_Z \\ V_{ZM} = 60 \text{ mA} & R_L \\ \end{pmatrix} I_L$	Realize The following Logical gates using NAND Gates only (i) NOR (ii) XOR (iii) AND (iv) NOT	With Characteristic Table and a neat circuit Diagram using ONLY NAND Gates, explain JK Flip flop.	Define shift register. Draw the circuit diagram for 4-bit shift register. If the initial values of all the flip-flops are at logic zero and the data input given serially is 0001011 (LSB first), Find the states of the register for seven clock pulses.	With a neat diagram, explain the Input and output V-I characteristics of PNP Common Base BJT. Find the value of α and I_B , if $I_E=1.32 mA$ and $I_C=1.11 mA$.	With a neat block diagram, explain Communication System.	With respect to Cellular Communication, define Cell. What are the Principles of Cellular Communication? Explain	Give the Differences between: (i) Second Generation Embedded System and Third Generation Embedded System (ii) General Purpose Computing system and Embedded Systems (iii) RAM and ROM (iv) Microprocessor and Microcontroller	Explain the Data Flow Model of ARM Processor with a neat diagram.		4. Automotive industry
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