Chapter 1

Introduction

Verilog is a hardware description language (HDL). It can be roughly divided into synthesizable Verilog and non-synthesizable Verilog or Verilog for verification. Verilog written at register-transfer level is always synthesizable.

1.1 Register-Transfer Level

According to Wikipedia, register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals between hardware registers, and the logical operations performed on those signals. The term Verilog RTL refers to Verilog written at the register-transfer level abstraction.

Chapter 2

Synthesizable Verilog

Synthesizable Verilog is (colloquially) referred to as Verilog for synthesis.

Chapter 3

Verilog for Verification

Verilog for verification refers to Verilog used to check behavior, and is different from Verilog for synthesis. This may refer to System Verilog which contains Verilog.