



Automatic Place & Route

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Derived from slides by Chung-Hao Wu

NTU MicroSystem Research Lab.



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Outline

- Introduction
- Prepare Data
- Automatic Place & Route - Innovus
- Stream Out Data



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• Introduction

- Design Flow Overview



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IC design flow(1/2)

Electronic System
Level (ESL) Design

Functional /
Logic Design

Logic Synthesis
(Design Compiler)

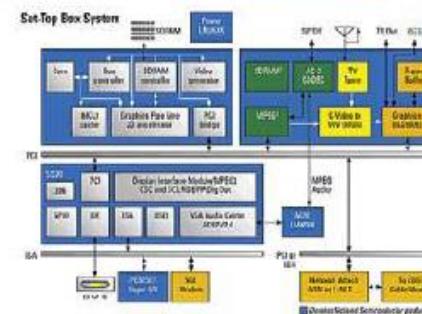


System
Specification

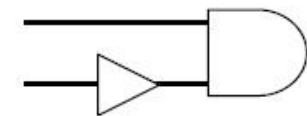
Block
Diagram

RTL
Code

Gate-level
Netlist



```
model MUX(o,a,b,s);
output o;
input a,b,s;
assign o=s?a:b;
endmodule
```



SystemC / System Verilog

VHDL / Verilog

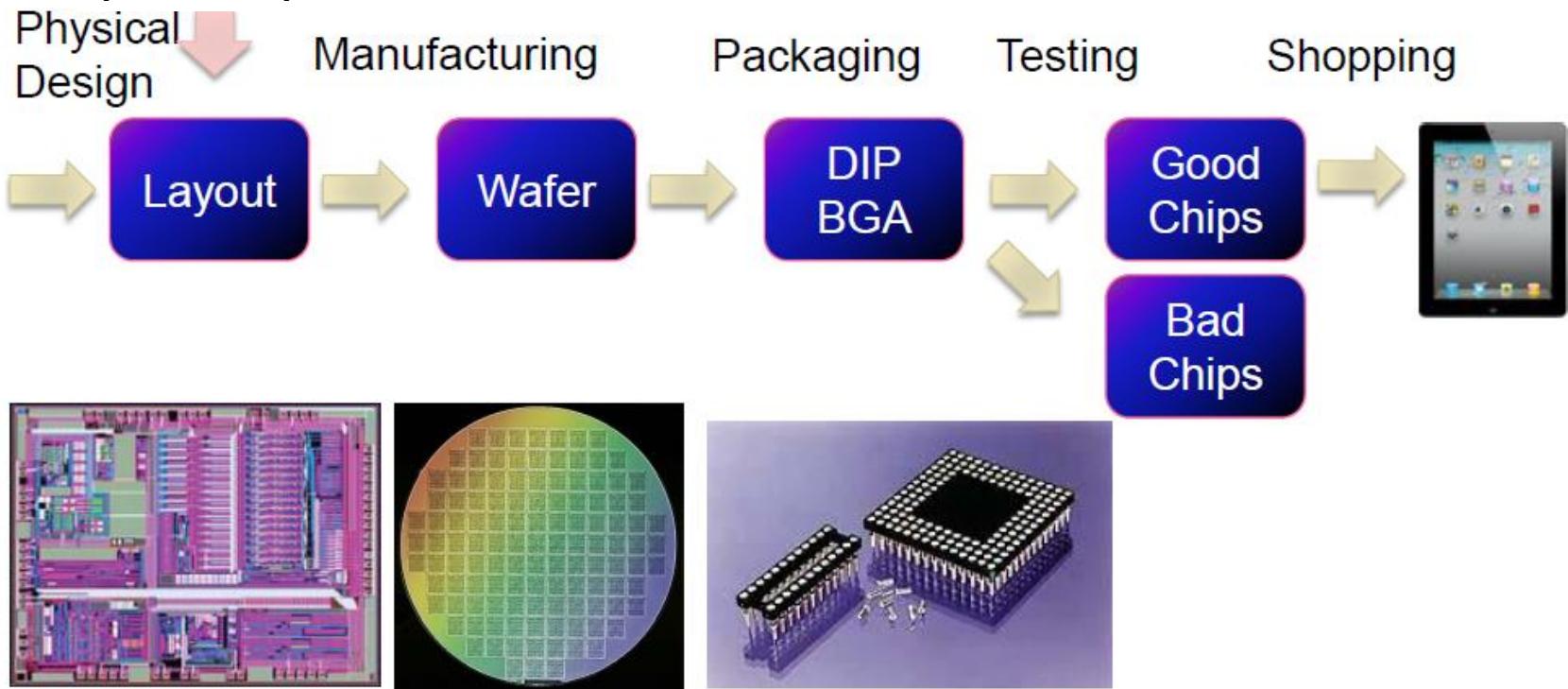
VHDL / Verilog



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IC design flow(2/2)

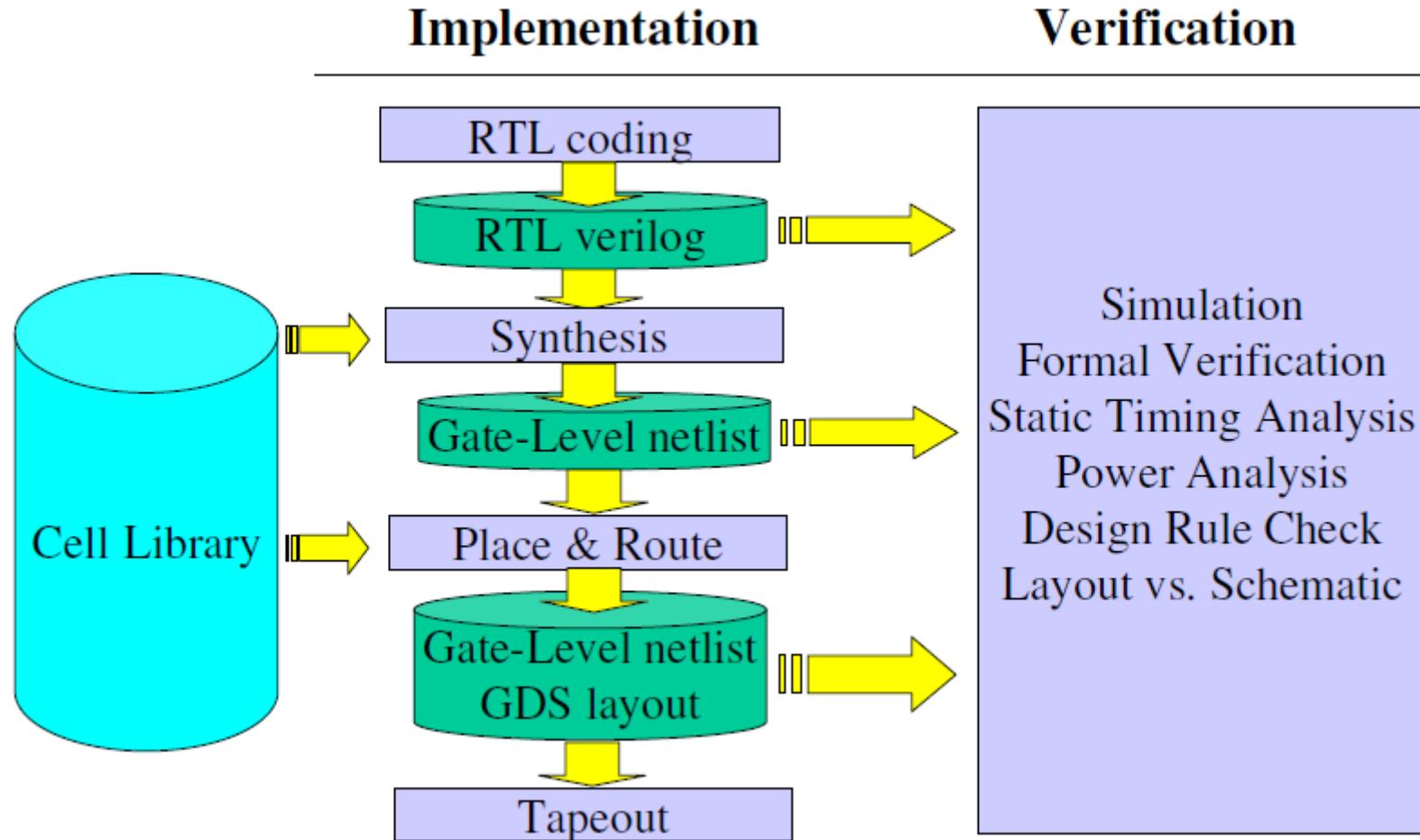
Place & Route (Innovus)





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Cell-Based Design Flow





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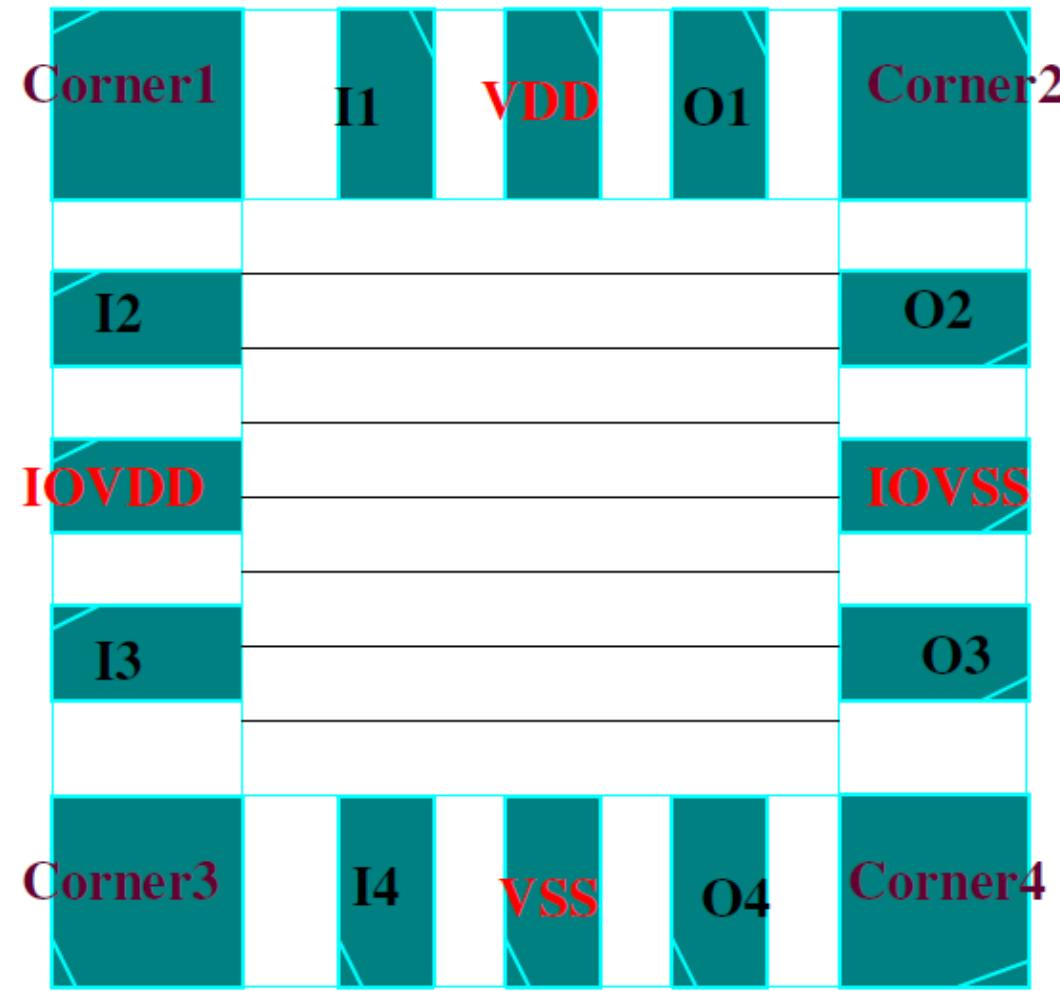
Cell Library

function	NAND	NOR	XOR	INV	ADD	FF
schematic						
layout						
Symbol		
timing	A1→O 0.1ns A2→O 0.2ns	A1→O 0.1ns A2→O 0.2ns
abstract		
	diffusion和poly不管他						



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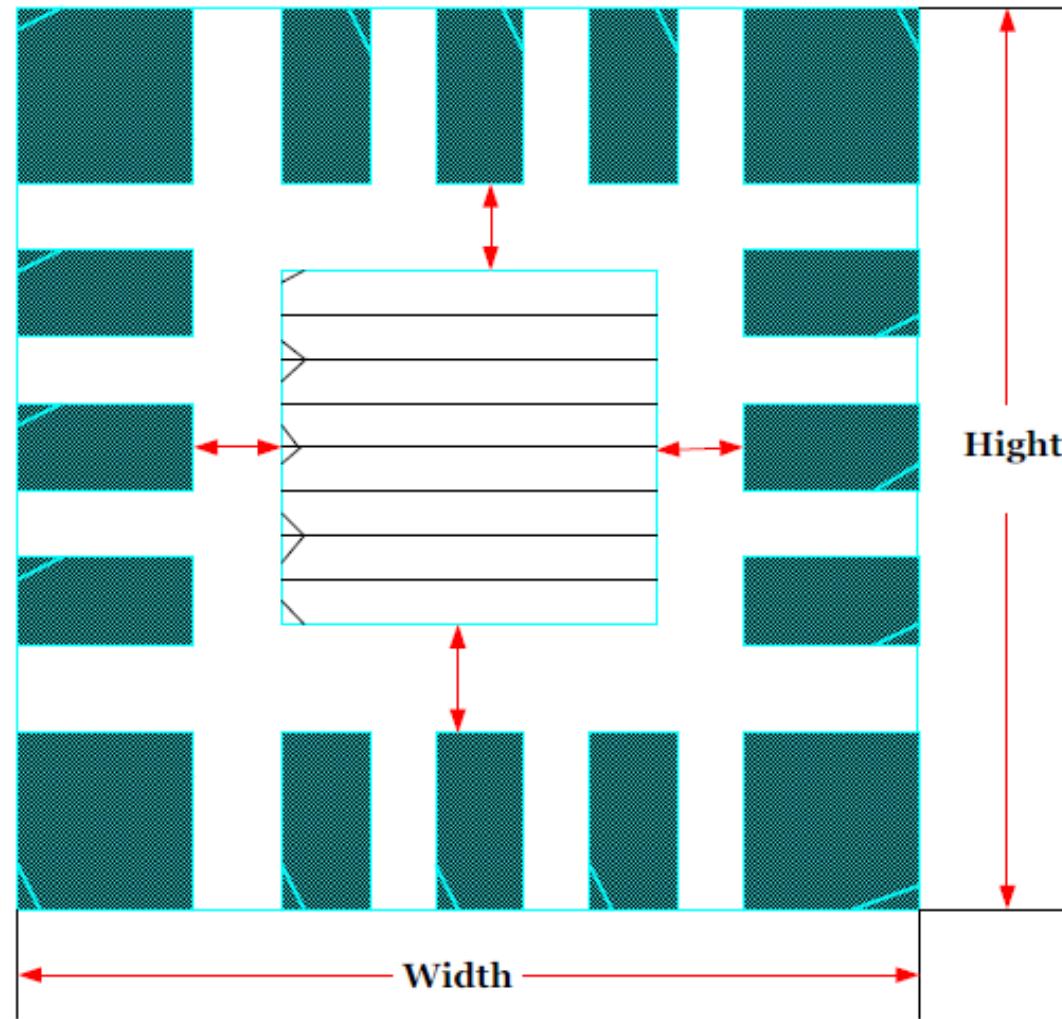
IO,P/G Placement





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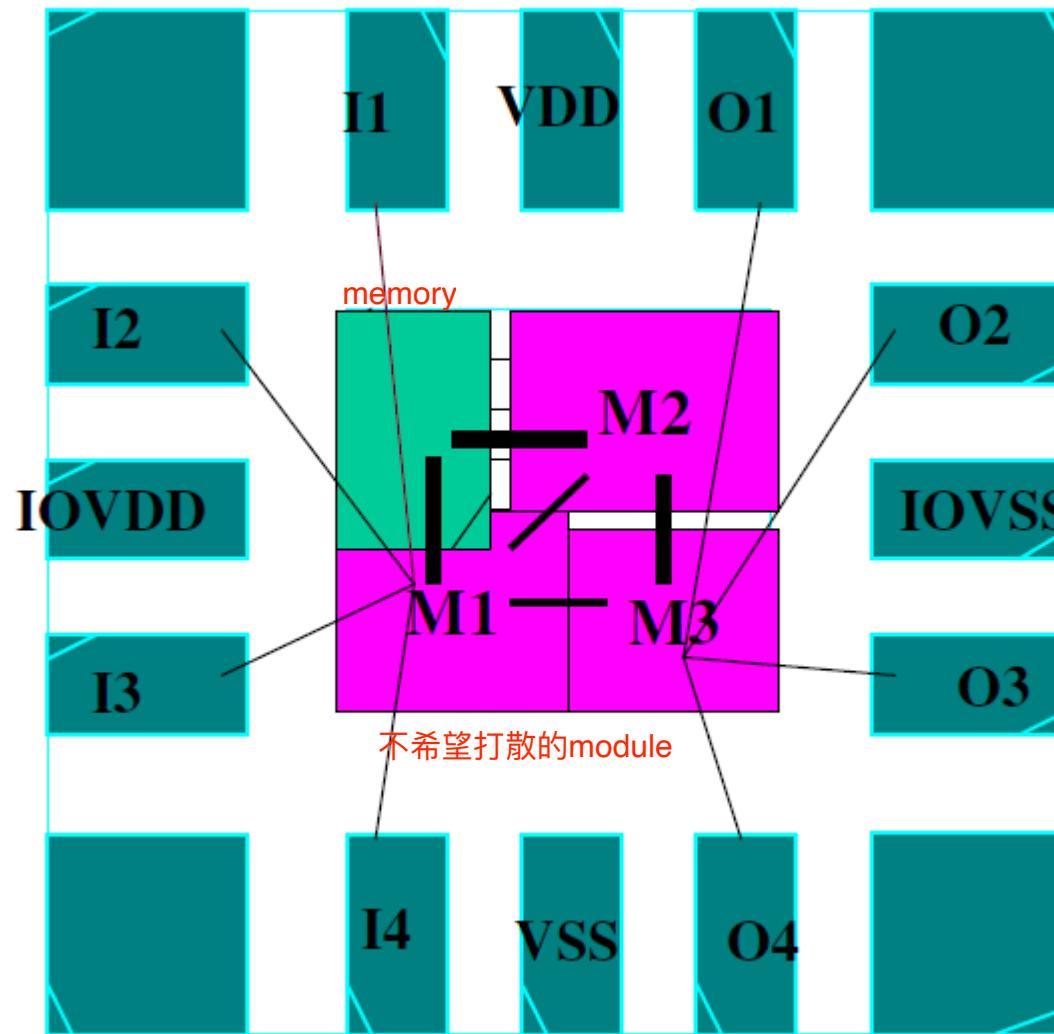
Specify Floorplan





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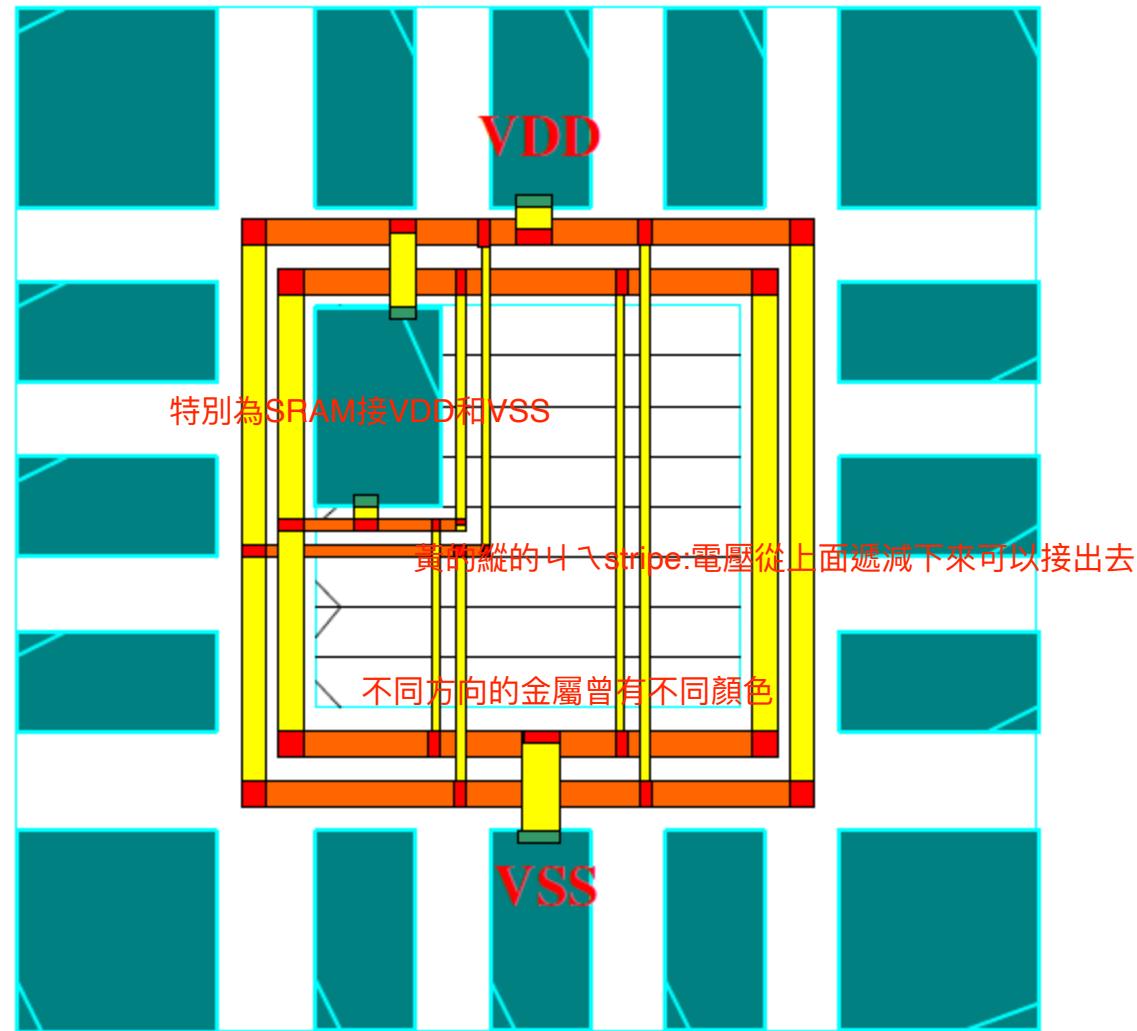
Floorplan





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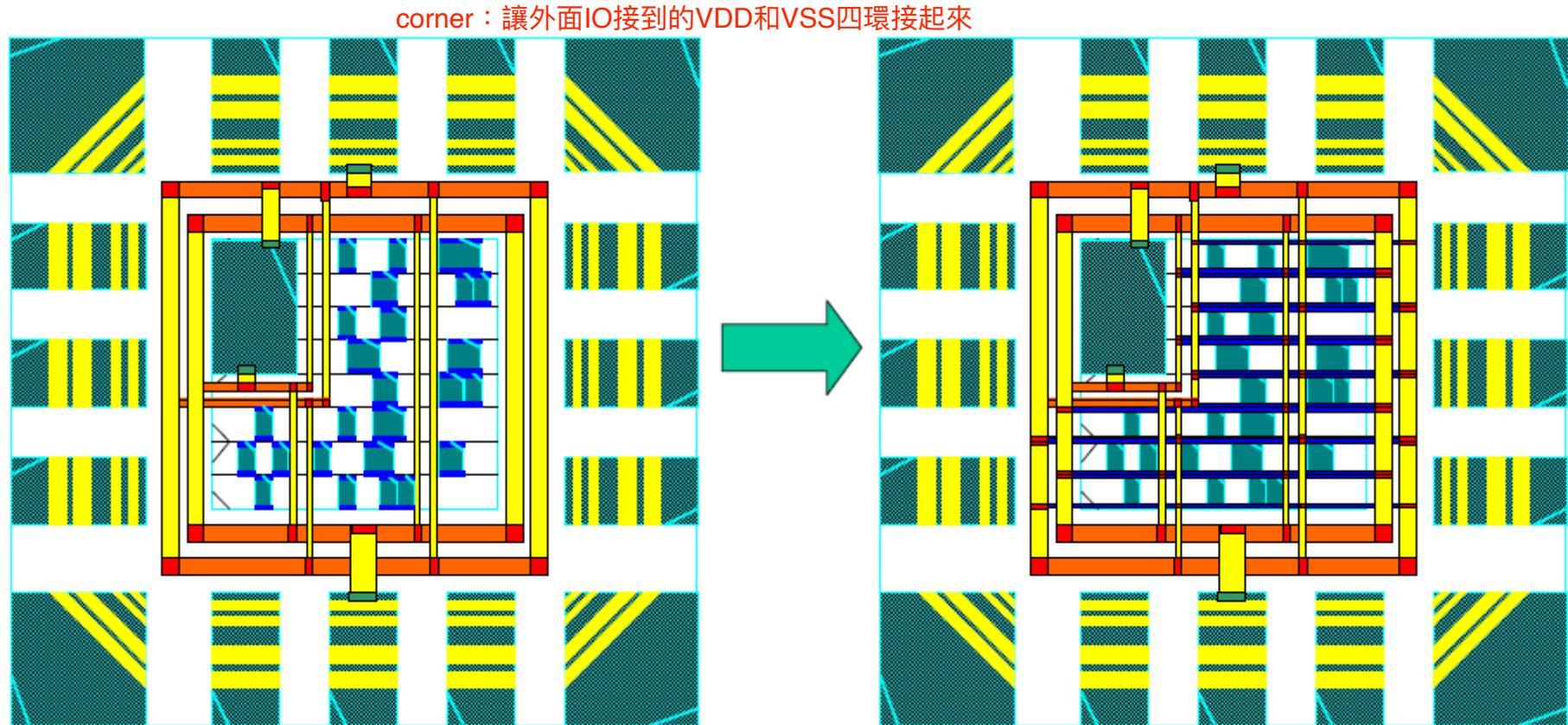
Power Planning





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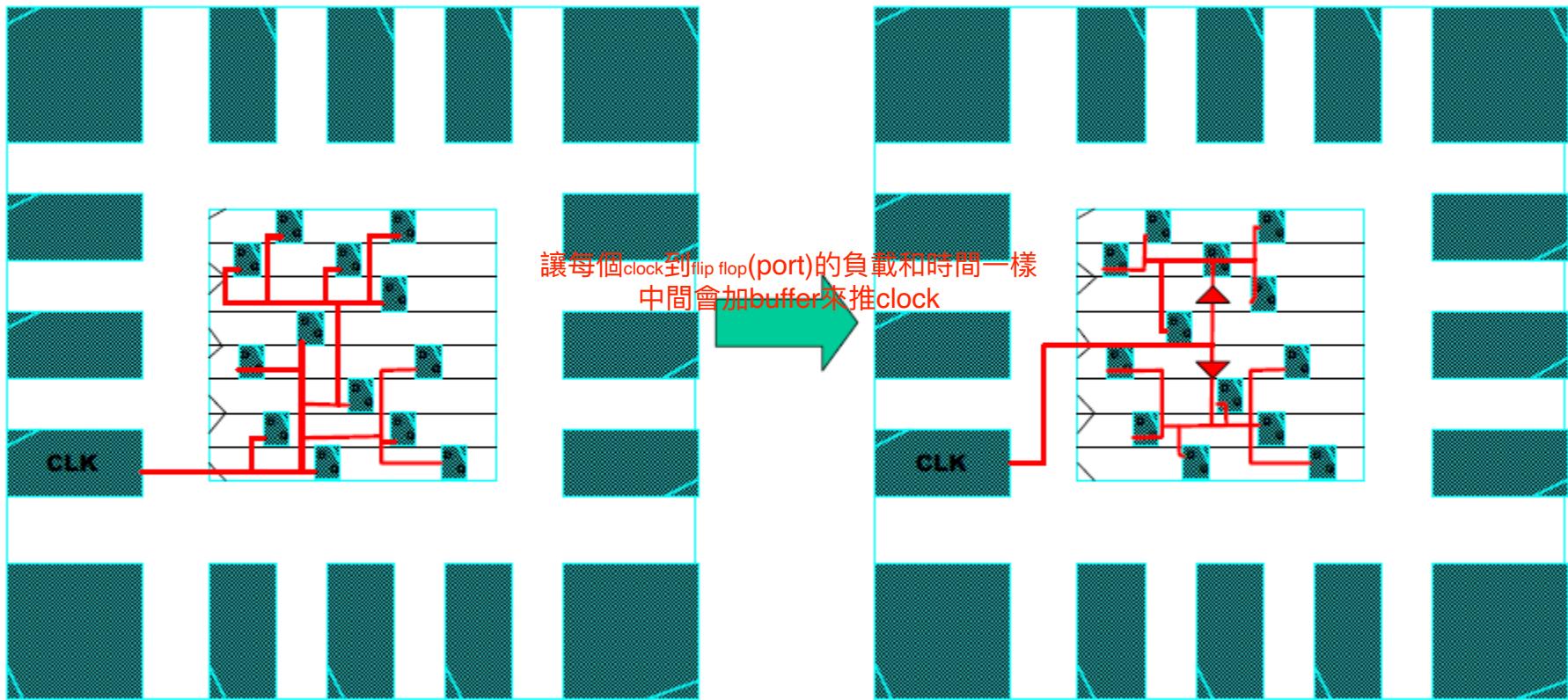
Power Routing





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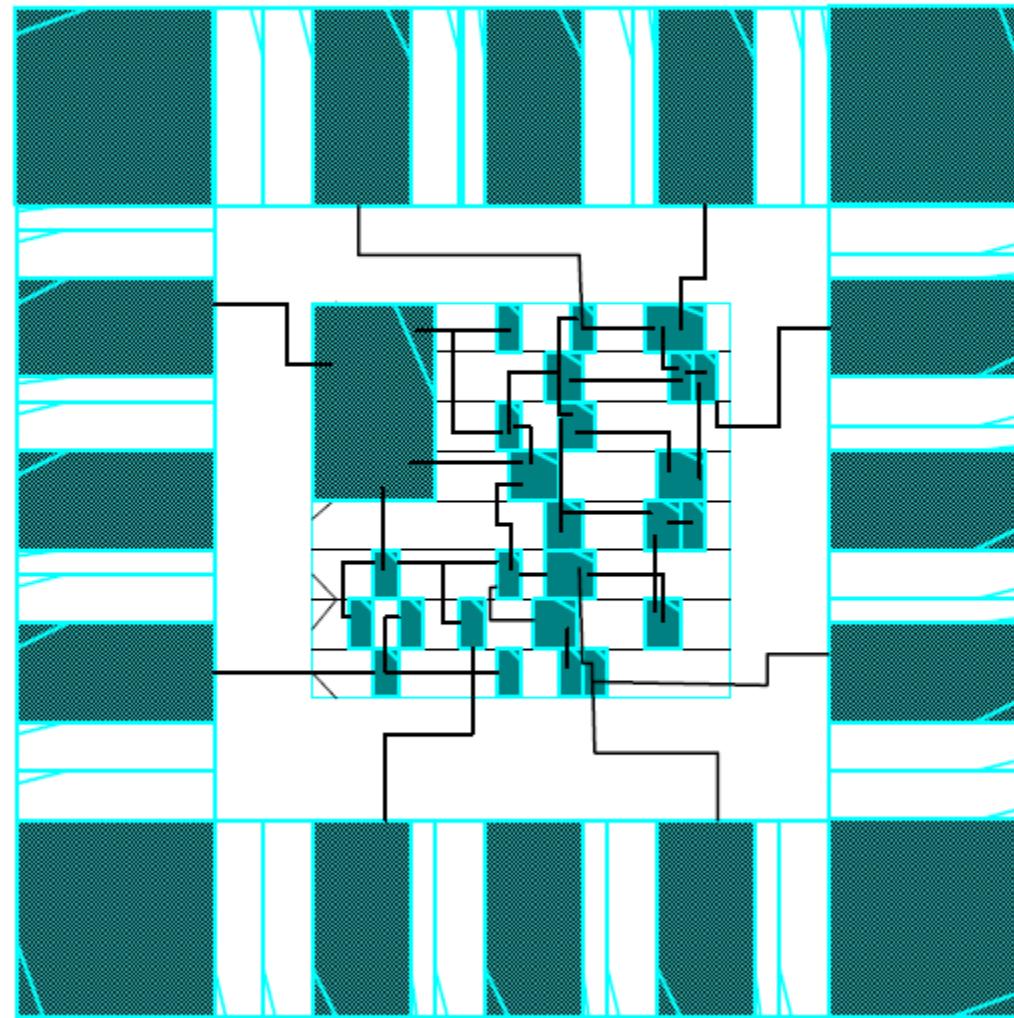
Clock Tree Synthesis





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Routing

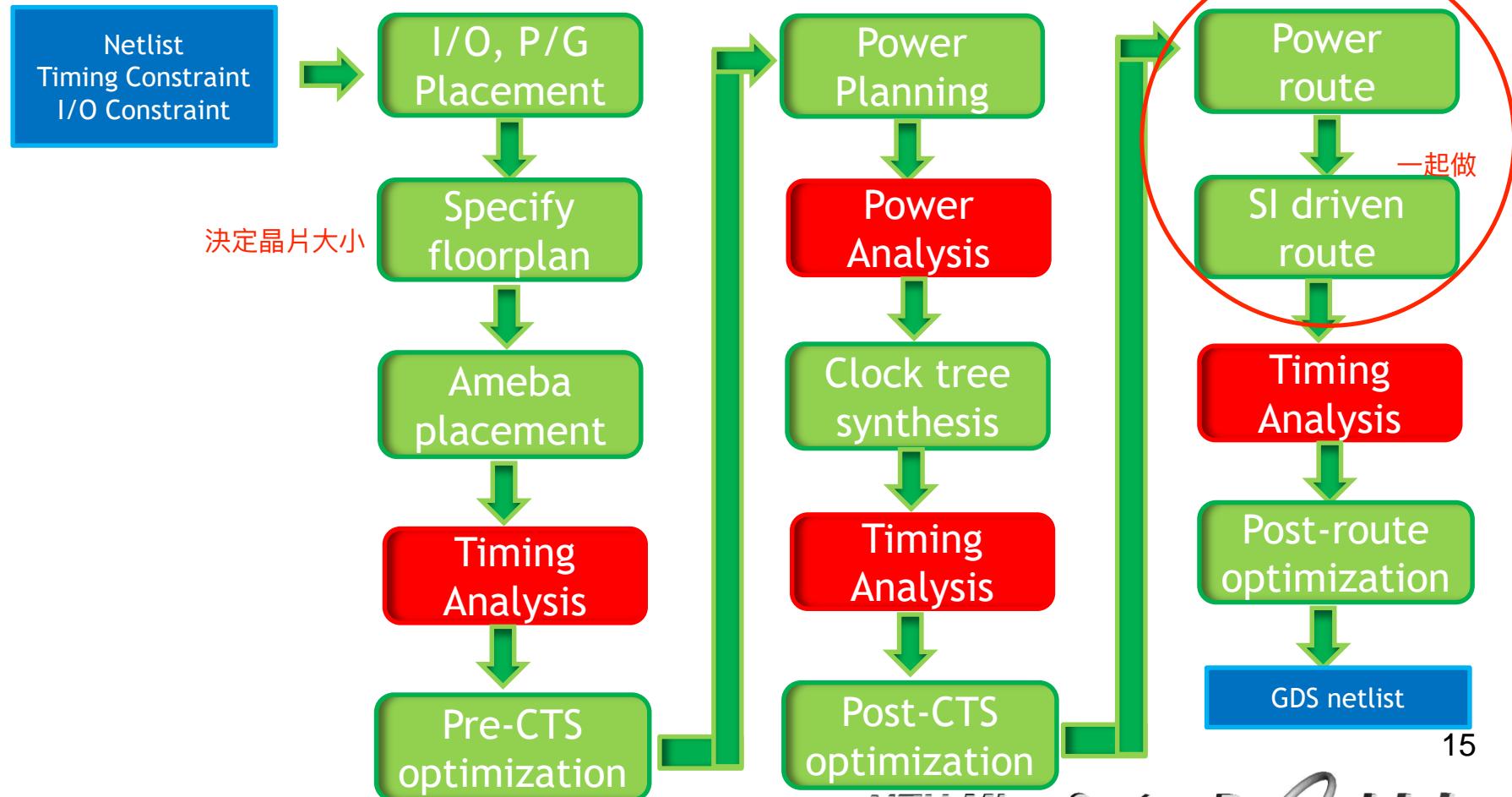




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P&R Flow

- Main steps: Floorplan, place and route.





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• Prepare Data

- Technology File
- Gate-Level Netlist
- Timing Constraints
- IO Constraints



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Design Setup

- Library Data
 - Technology File
 - Reference Libraries
- Design Data
 - Gate-level Netlist
 - Timing Constraints
 - IO constraints



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Technology File - Process Tech.

有幾層：普通事9層

Layers



不能改變厚度
厚度會影響電組



Design Rule

線和線的最短距離

- Net width
- Net spacing
- Area
- Enclosure
- Wide metal slot
- Antenna
- Current density

Parasitic

- Resistance
- Capacitance

一條線的每單位面積電容量



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Gate-Level Netlist

- Use same process technology during synthesis and P&R.
- Make sure that there is no “assign” statement in the netlist.

To remove “assign” statement in synthesis tool

- set_fix_multiple_port_nets -all -buffer_constraints

To remove “assign” statement in ~~SOC Encounter~~

Innovous

- setDoAssign -buffer buf_name on



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SDC Constraint

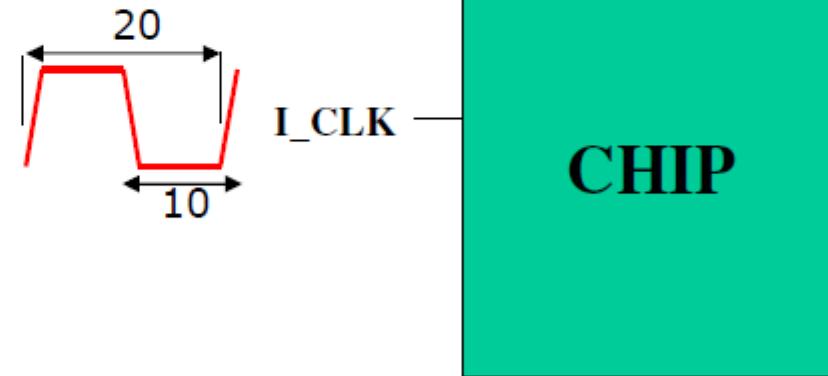
- Clock constraints
- Input delay / Input drive
- Output delay / Output load
- All in a .sdc file



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SDC - Create Clock

```
create_clock [-name clock_name]  
[-period period_value]  
[-waveform edge_list]  
[sources]
```



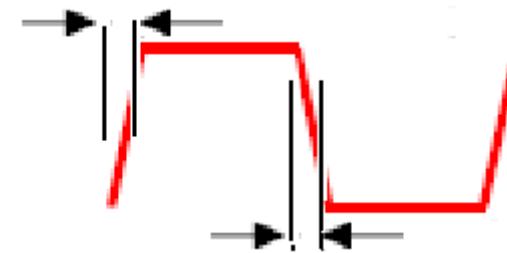
```
create_clock -name CLK1 -period 20 -waveform {0 10} [get_ports I_CLK]
```



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SDC - Clock Transition

```
set_clock_transition [-rise | -fall]
    transition
    clock_list
```



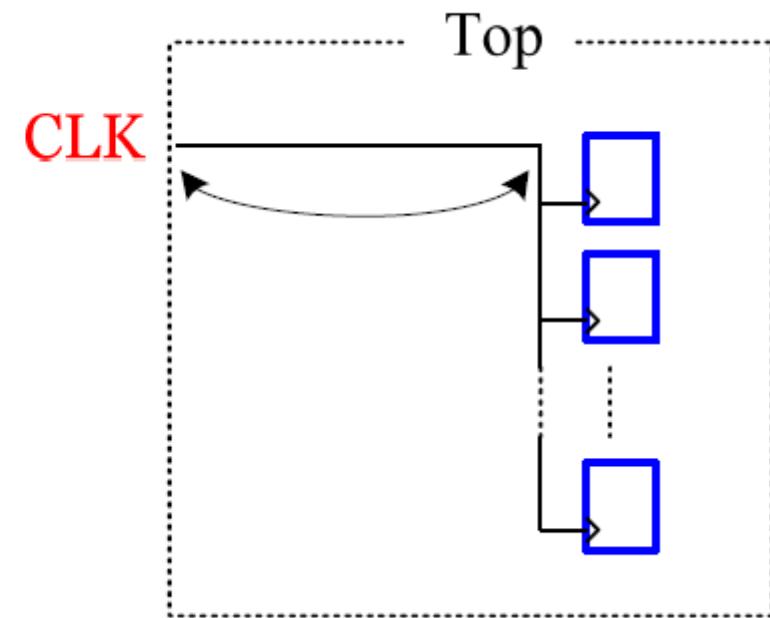
```
set_clock_transition -rise 0.2 [get_clocks {clk}]
```



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SDC - Clock Latency (1)

```
set_clock_latency [-source]  
    latency  
    pin_or_clock_list
```



```
set_clock_latency 2 [get_clocks {CLK1}]
```



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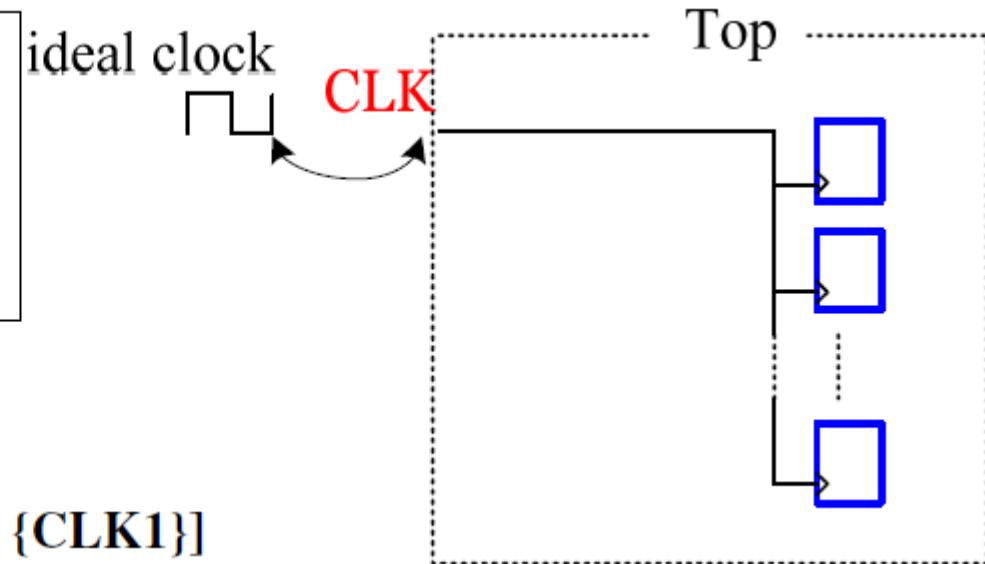
SDC - Clock Latency (2)

```
set_clock_latency [-source]
```

```
latency
```

```
pin_or_clock_list
```

```
set_clock_latency -source 6 [get_clocks {CLK1}]
```



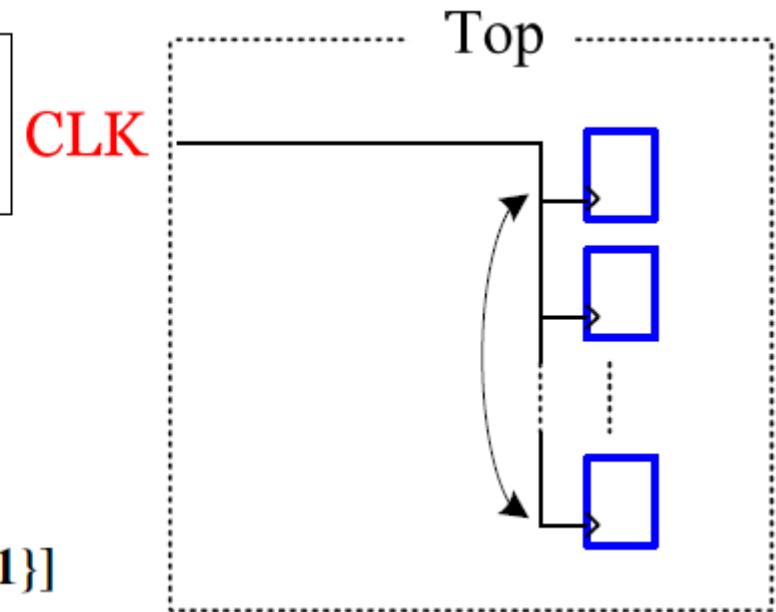


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SDC - Clock Uncertainty

```
set_clock_uncertainty float  
pin_or_clock_list
```

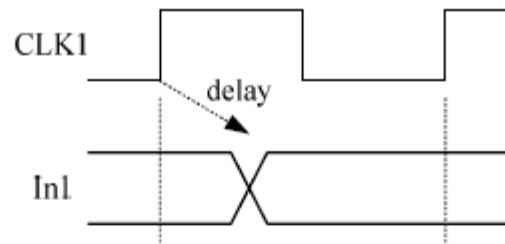
```
set_clock_uncertainty 0.5 [get_clocks {CLK1}]
```



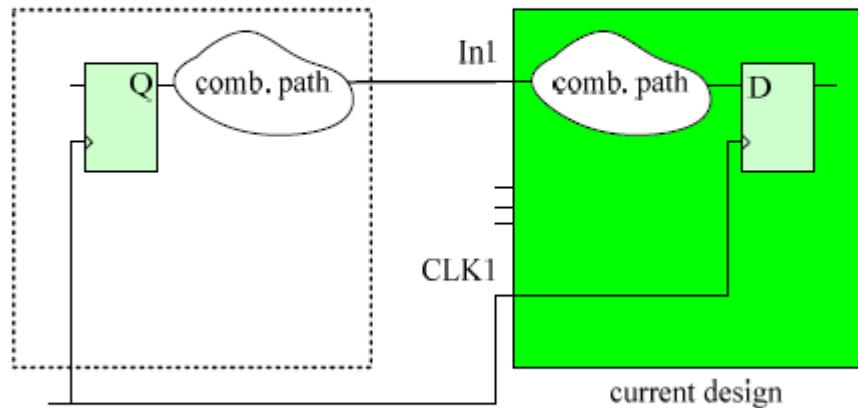


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SDC - Input Delay



```
set_input_delay delay_value
[-clock clock_name]
port_pin_list
```



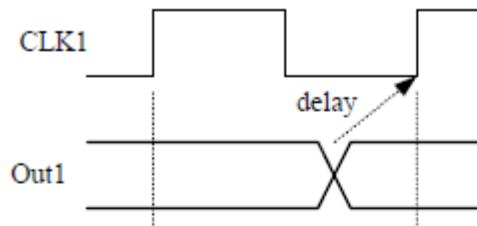
sdc會有每個port的delay，可以個別改變

```
set_input_delay 1 -clock [get_clocks {CLK1}] [get_ports {In*}]
```

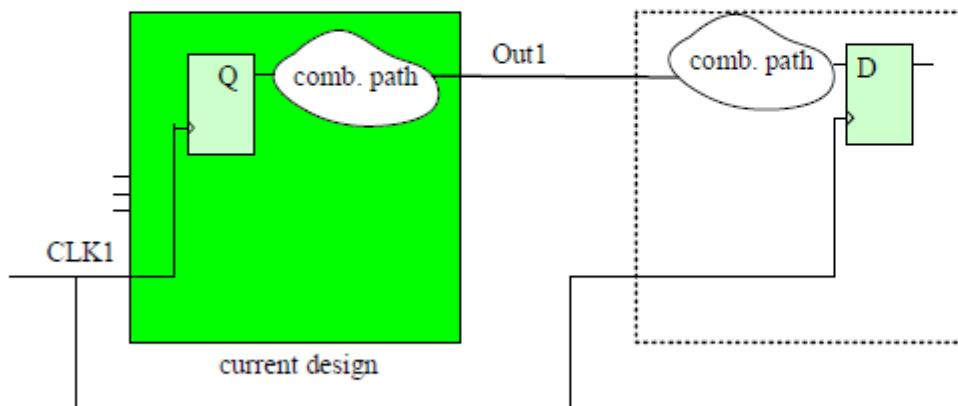


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SDC - Output Delay



```
set_output_delay delay_value
[-clock clock_name]
port_pin_list
```

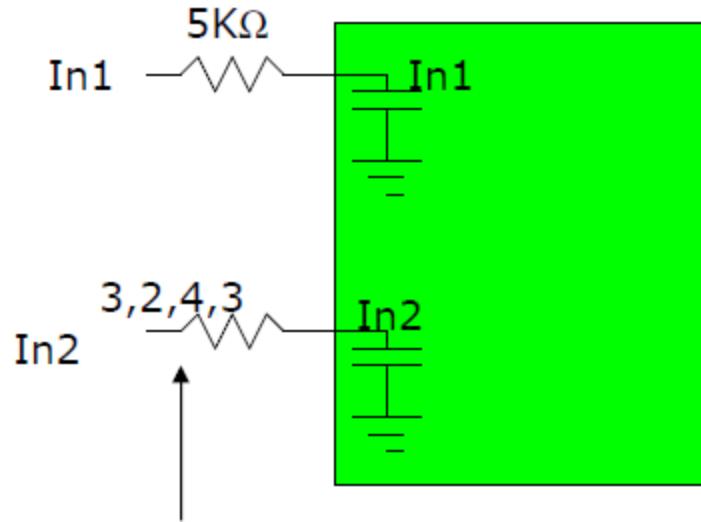


```
set_output_delay 1 -clock [get_clocks {CLK1}] [get_ports {Out*}]
```



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SDC - Input Drive



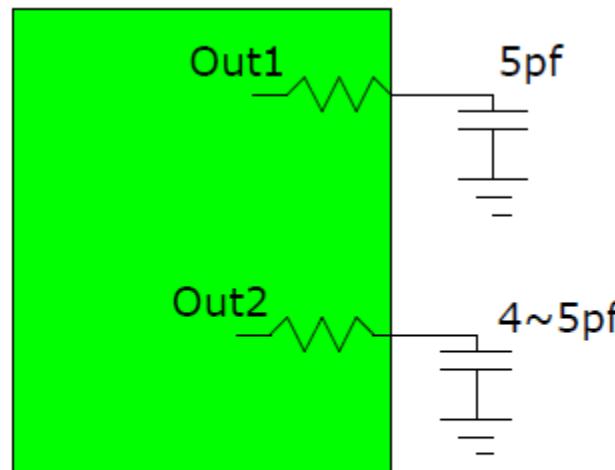
```
set_drive [-min] [-max]
[-rise] [-fall]
drive_strength
port_list
```

```
set_drive 5 [get_ports {In1}]
```



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SDC - Output Load



```
set_load [-min] [-max]  
load_value  
port_list
```

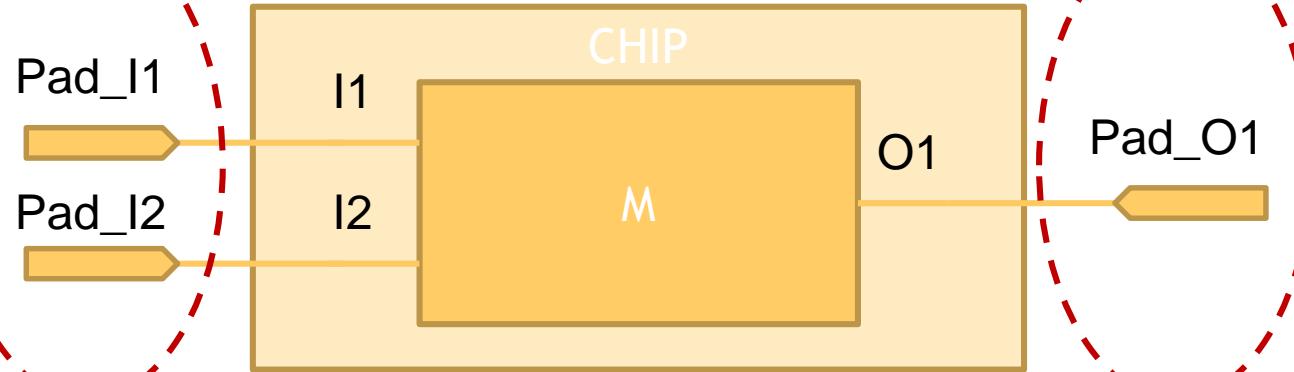
```
set_load 5 [get_ports {Out1}]
```



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IO Constraints

For a chip design, the I/O pads should be added on the top module.





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```
module M (O1, I1, I2);
  output O1;
  input I1;
  input I2;
endmodule;
```

Original design (M.v)



IO Constraints

```
module M (O1, I1, I2);
  output O1;
  input I1;
  input I2;
endmodule;
```

```
module CHIP (O1, I1, I2); // top module with I/O pads
  output O1;
  input I1, I2;
  wire i_I1, i_I2, i_O1;
  M M (.O1(i_O1), .I1(i_I1), .I2(i_I2));
  PDIDGZ Pad_I1 (.PAD(I1), .C(i_I1));
  PDIDGZ Pad_i2 (.PAD(I2), .C(i_I2));
  PDO12CDG Pad_O1(.PAD(O1), .I(i_O1));
endmodule;
```

Modified design (CHIP_syn.v)



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• Automatic Place & Route - Innovus

- Setup Environment
- Floorplan
- Placement
- CTS
- Routing
- Design for Manufacturing

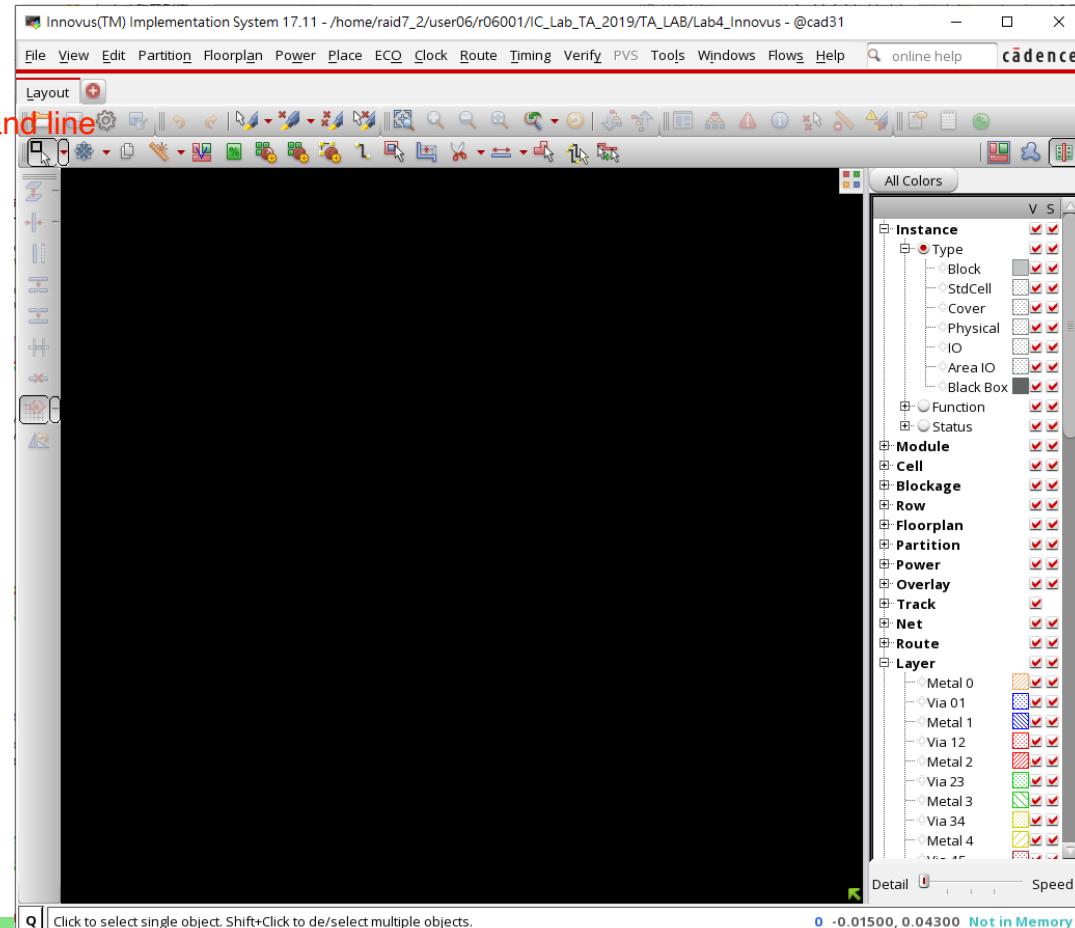


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Setup Environment

- source /usr/cad/innovus/CIC/license.cshrc
- source /usr/cad/innovus/CIC/innovus.cshrc
- innovus

不能加&，背景執行會沒法打command line





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Import Design

File → Design Import ...

- Import LEF in the order:
 - Technology **first**
 - Geometry lef for cell/block
 - Antenna lef for cell/block
- IO Assignment File

IO pad的順序



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Import Design -Power

- Specify the names of Power Nets and Ground Nets

Netlist:

Verilog
 OA

Files: design/CHIP_syn.v *io pad放進去後的合成檔* ...
Top Cell: Auto Assign By User: CHIP

Library:
Cell:
View:

Technology/Physical Libraries:

OA
 LEF Files ef/FSA0M_A_T33_GENERIC_IO_ANT_V55.lef lef/BONDPAD.lef ...

Floorplan

IO Assignment File: design/CHIP.ioc

Power

Power Nets: VCC
Ground Nets: GND
CPF File: *分析的時候要用快or慢的library或是電容*

Analysis Configuration

MMMC View Definition File: mmmc.view *分析的時候要用快or慢的library或是電容*
Create Analysis Configuration ...

OK Save... Load... Cancel Help



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Global Net Connection

Power → Connect Global Nets

Connection List

- VCC:PIN:*,VCC:All
- GND:PIN:*,GND:All

Power Ground Connection

Connect

- Pin
- Tie High
- Tie Low

Instance Basename: *

Pin Name(s): GND ✓

- Net Basename:

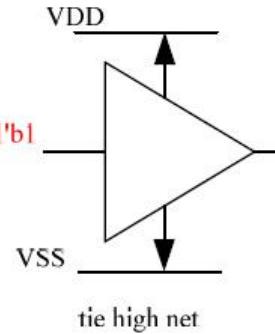
Scope

- Single Instance:
- Under Module:
- Under Power Domain:
- Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0
- Apply All ✓

To Global Net: GND ✓

Override prior connection

Verbose Output



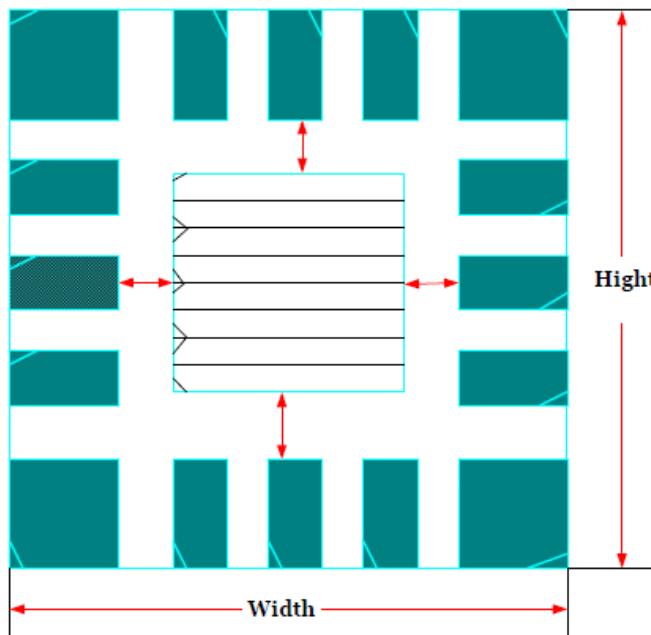
INV inv1(.I(1'b1), .O(o));



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Specify Floorplan

Floorplan → Specify Floorplan

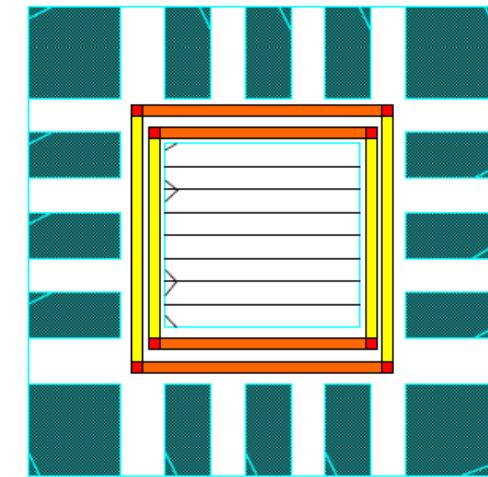
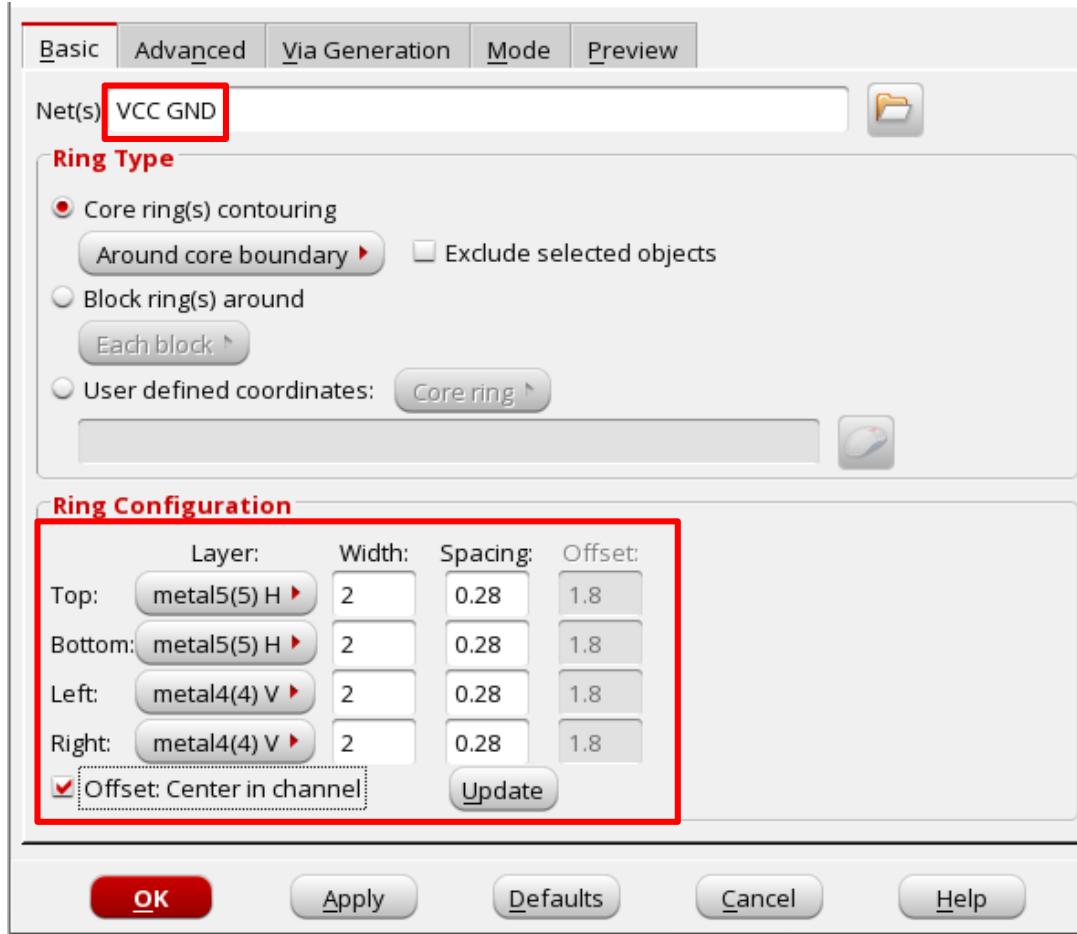




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Power Planning-Add Rings

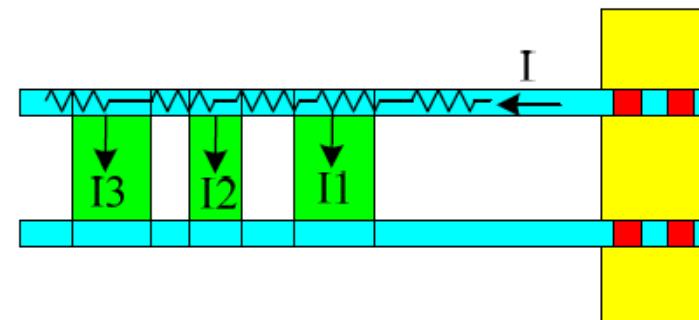
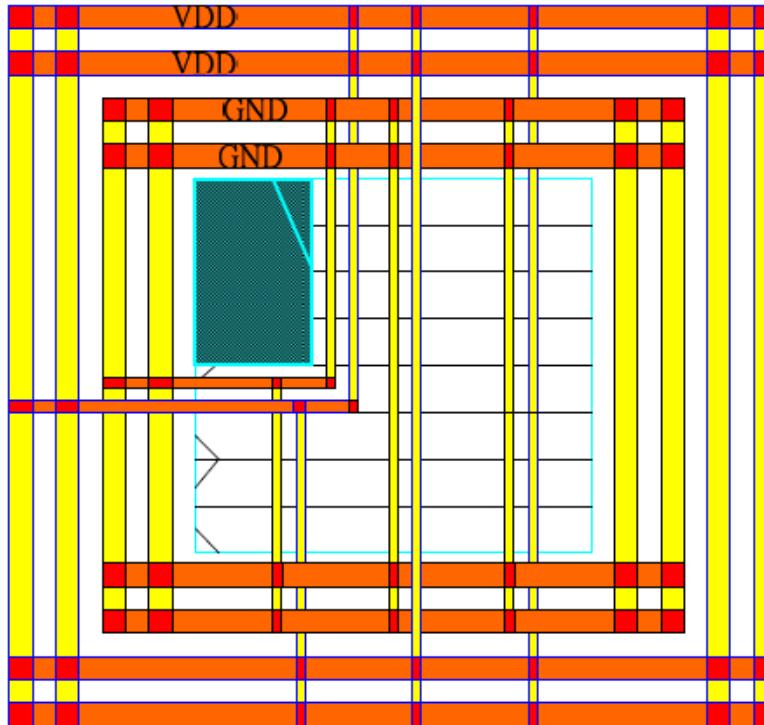
Power → Power Planning → Add Rings ...





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Power Planning-Add stripes



IR drop



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Early Power Analysis

- View IR drop. 主要分析memory
- Can be skip if no macros(memory) are used.



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Early Power Analysis

- Execute `irun -f vlog.f`
- Inside `vlog.f`
 - Your testbench
 - Your Verilog file after synthesis
 - Librarys
 - Tcl
 - Run time
 - Output file
 - Module

```
vlog.f
CHIP_sim.v \
CHIP_syn.v \
-v CIC018.v \
+access+r \
-input irun.tcl \
-clean \
+ncmaxdelays+full64
```

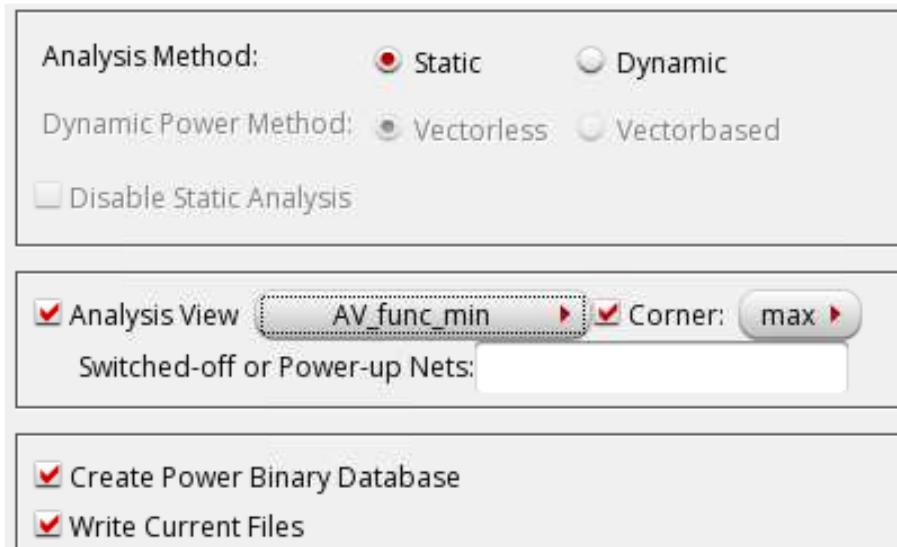
```
irun.tcl
run 500ns
dumptcf -scope test.CHIP -output CHIP.tcf \
-inctoggle -overwrite
run 1000ns
dumptcf -end
run
exit
```



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Early Power Analysis

- Power -> Power Analysis -> Setup
 - Analysis Method : Static
 - Analysis View : your function view





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Early Power Analysis

- Execute power analysis.

```
set_default_switching_activity -reset  
set_default_switching_activity -input_activity 0.2 -period 10.0  
read_activity_file -reset  
read_activity_file -format TCF pre_sim/CHIP.tcf -scope CHIP  
set_power -reset  
set_powerup_analysis -reset  
set_dynamic_power_simulation -reset  
report_power -rail_analysis_format VS -outfile ./CHIP.rpt
```

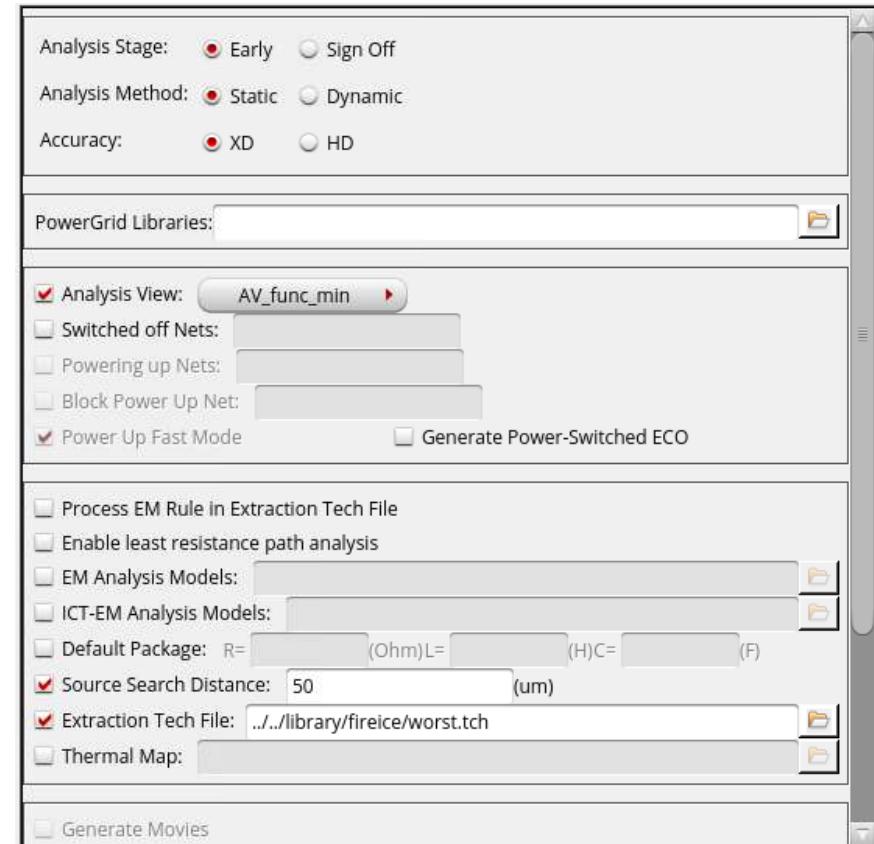
- If don't want to generate tcf file, skip read activity_file.



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Early Rail Analysis

- Power -> Rail Analysis
-> Setup Rail Analysis
 - Analysis Stage : Early
 - Analysis View : your function view
 - Check Extraction Tech File, choose tch file

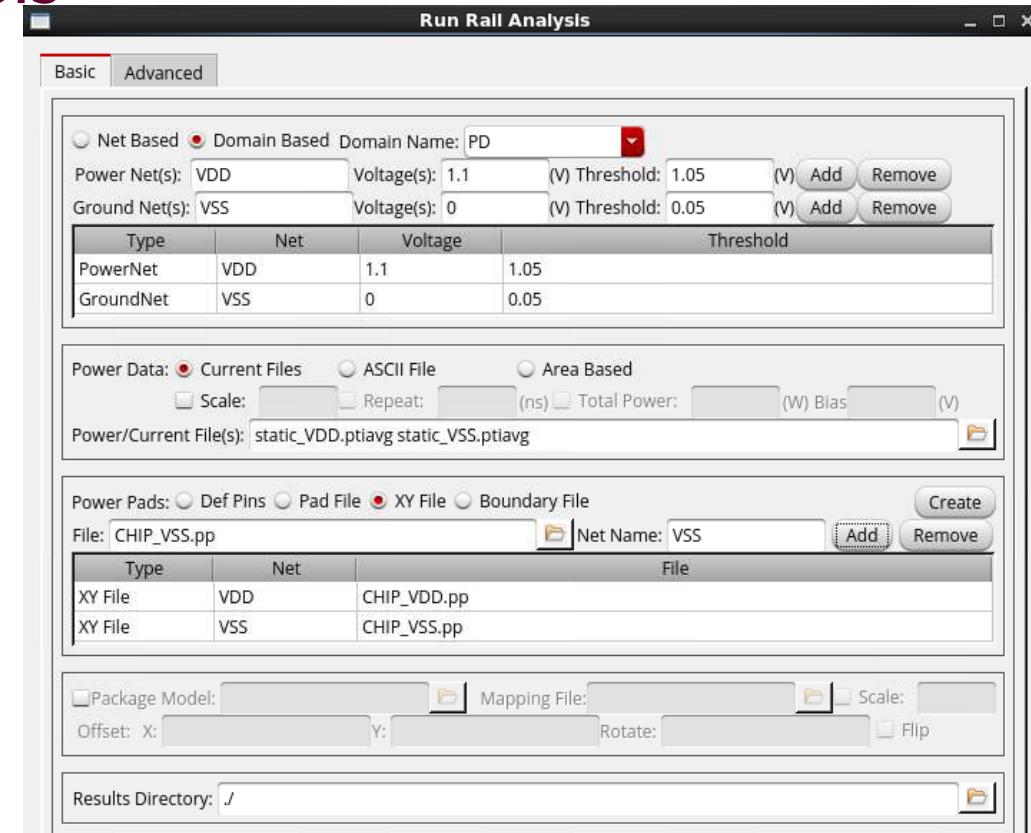




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Early Rail Analysis

- Power -> Rail Analysis
-> Run Rail Analysis
 - Domain Based, name:PD
 - Power Nets VDD
 - Ground Nets VSS
 - Power/Current File: static_VDD.ptiavg
static_VSS.ptiavg

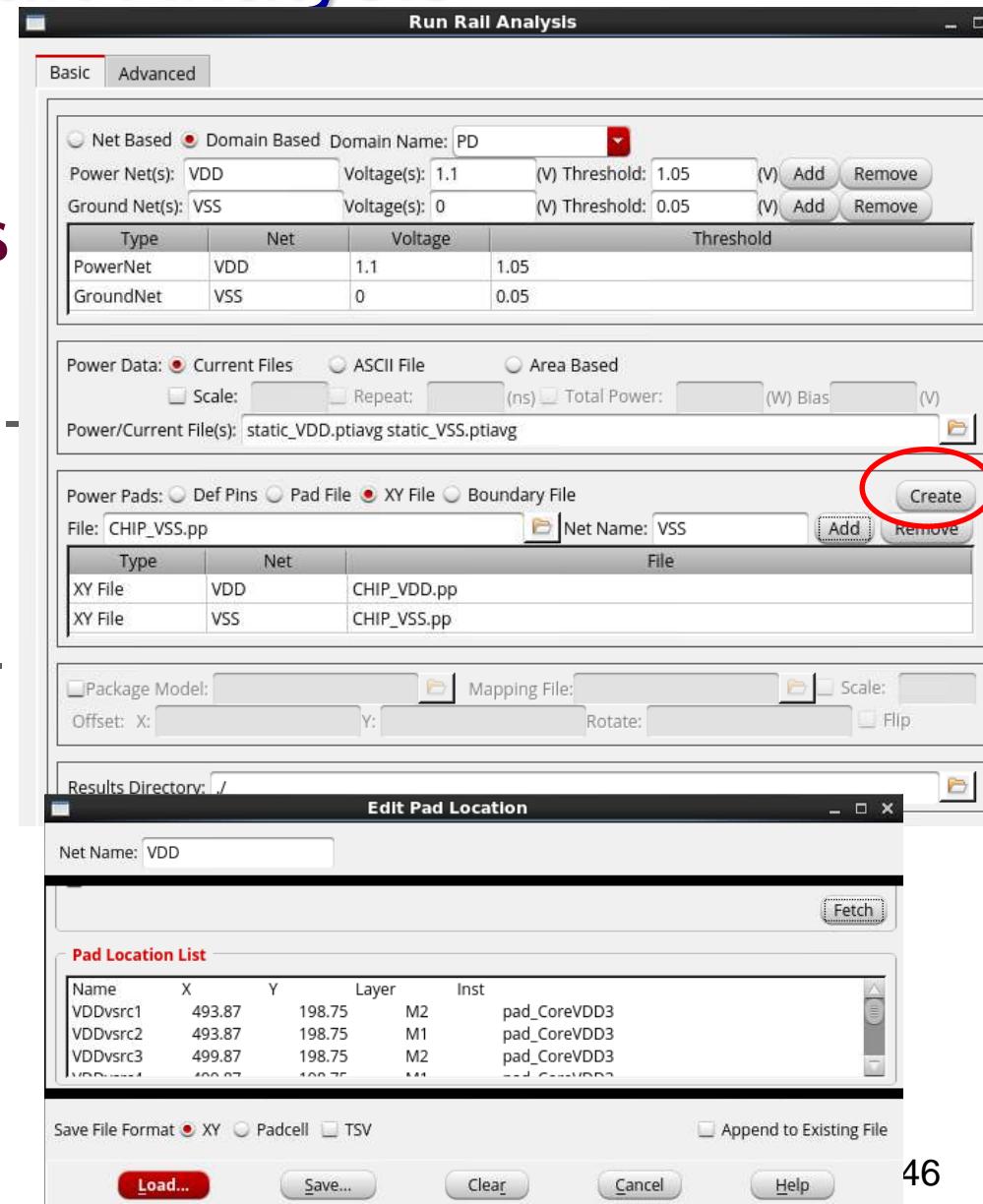




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Early Rail Analysis

- Power -> Rail Analysis
-> Run Rail Analysis
 - Create : VDD -> fetch ->Format XY ->save CHIP_VDD.pp
 - Create : VSS -> fetch ->Format XY ->save CHIP_VSS.pp
- Run, IR drop information is in command log





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Early Rail Analysis

- IR drop for VCC

```
=====
IR DROP ANALYSIS
=====
Layer based IR Drop Report: See Report
Minimum, Average, Maximum IR drop: 1.800V 1.800V 1.800V
Please refer to ../VCC/ir_linear.gif for more details
Total Static Current Loaded: 0.133uA
Number of Violations: 0
```

- IR drop for GND

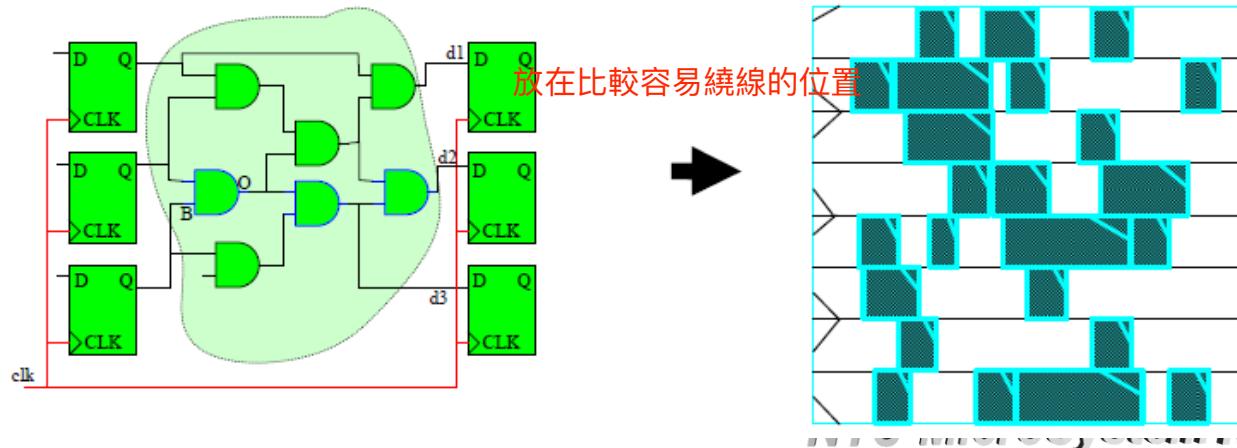
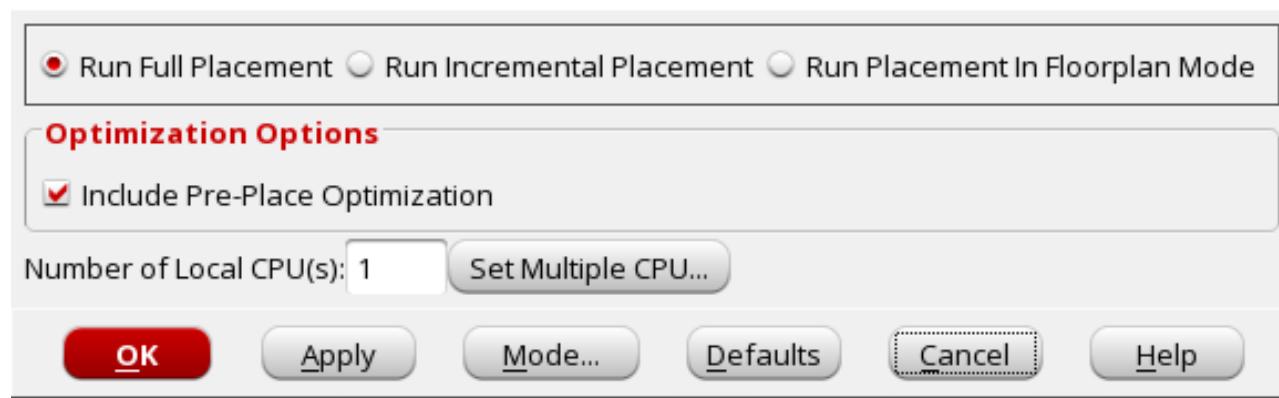
```
=====
IR DROP ANALYSIS
=====
Layer based IR Drop Report: See Report
Minimum, Average, Maximum IR drop: 0.000V 0.000V 0.000aV
Please refer to ../GND/ir_linear.gif for more details
Total Static Current Loaded: 0.000A
Number of Violations: 0
```



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Placement

Place → Place Standard Cells ...





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Clock Tree Synthesis (CTS)

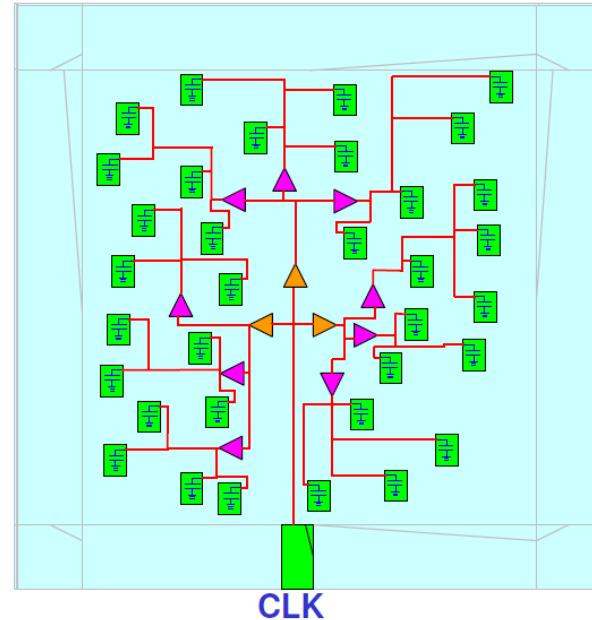
- Add Multi-level **buffer** trees according to your clock specification.
- A good clock tree should have the same feature as described in the clock estimation.
- CTS result will be always bad if the clock estimation is not realistic.



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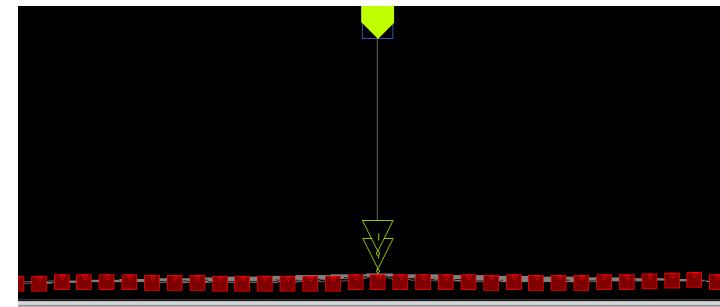
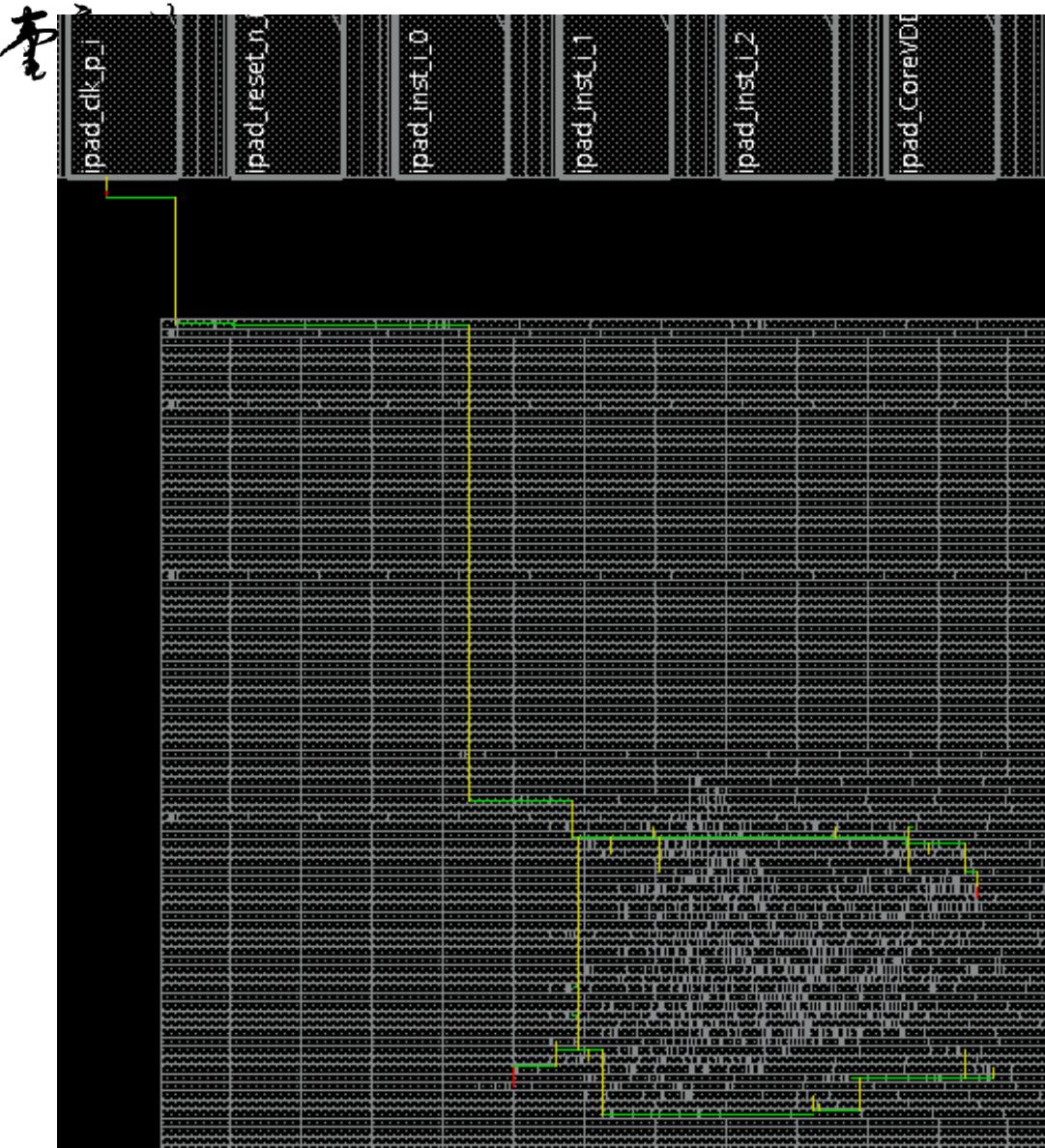
Effects of CTS

- More buffers added
- Other cells may move
- Congestion may increase
- Might introduce new timing violations





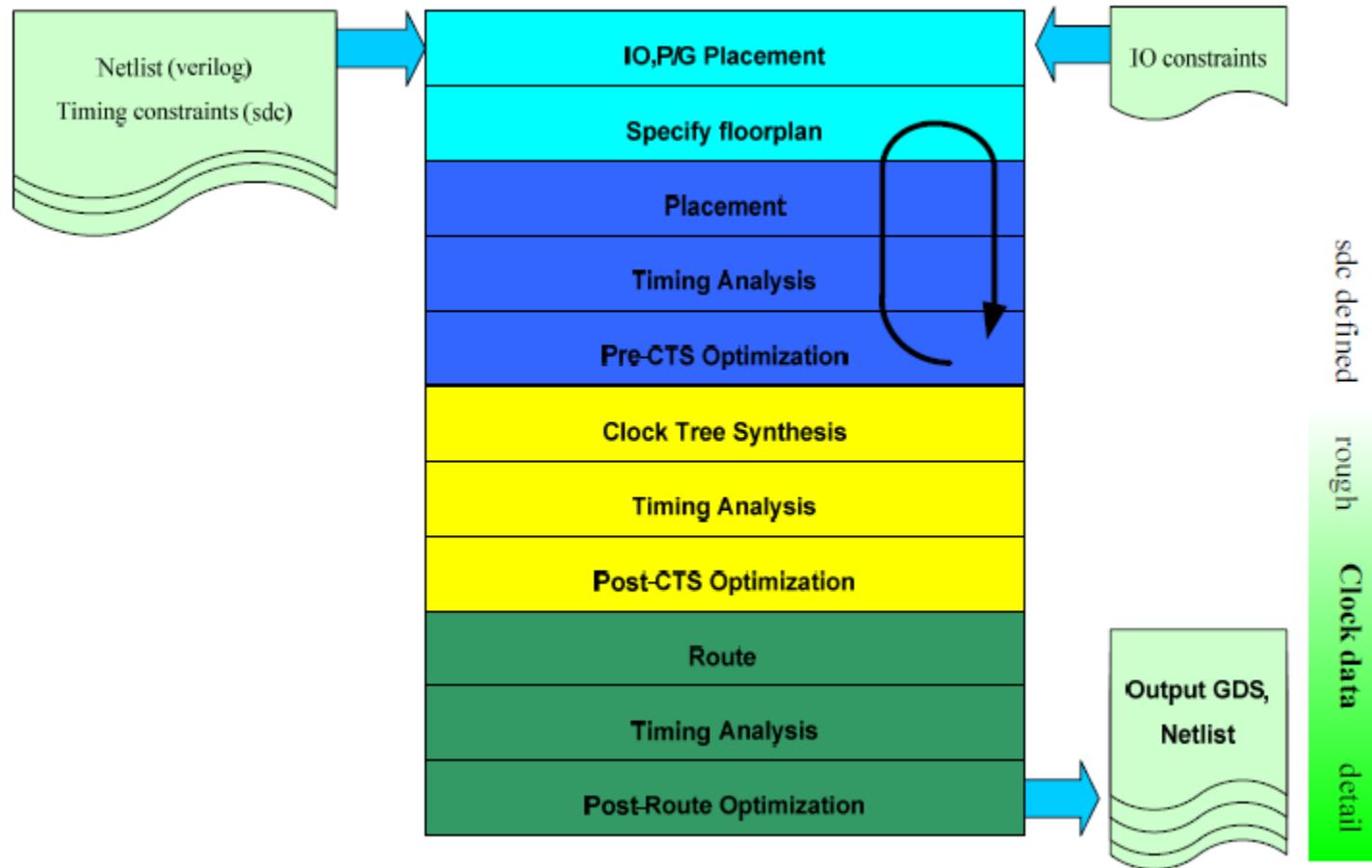
Display Clock Tree





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Relationship of Flow and Clock





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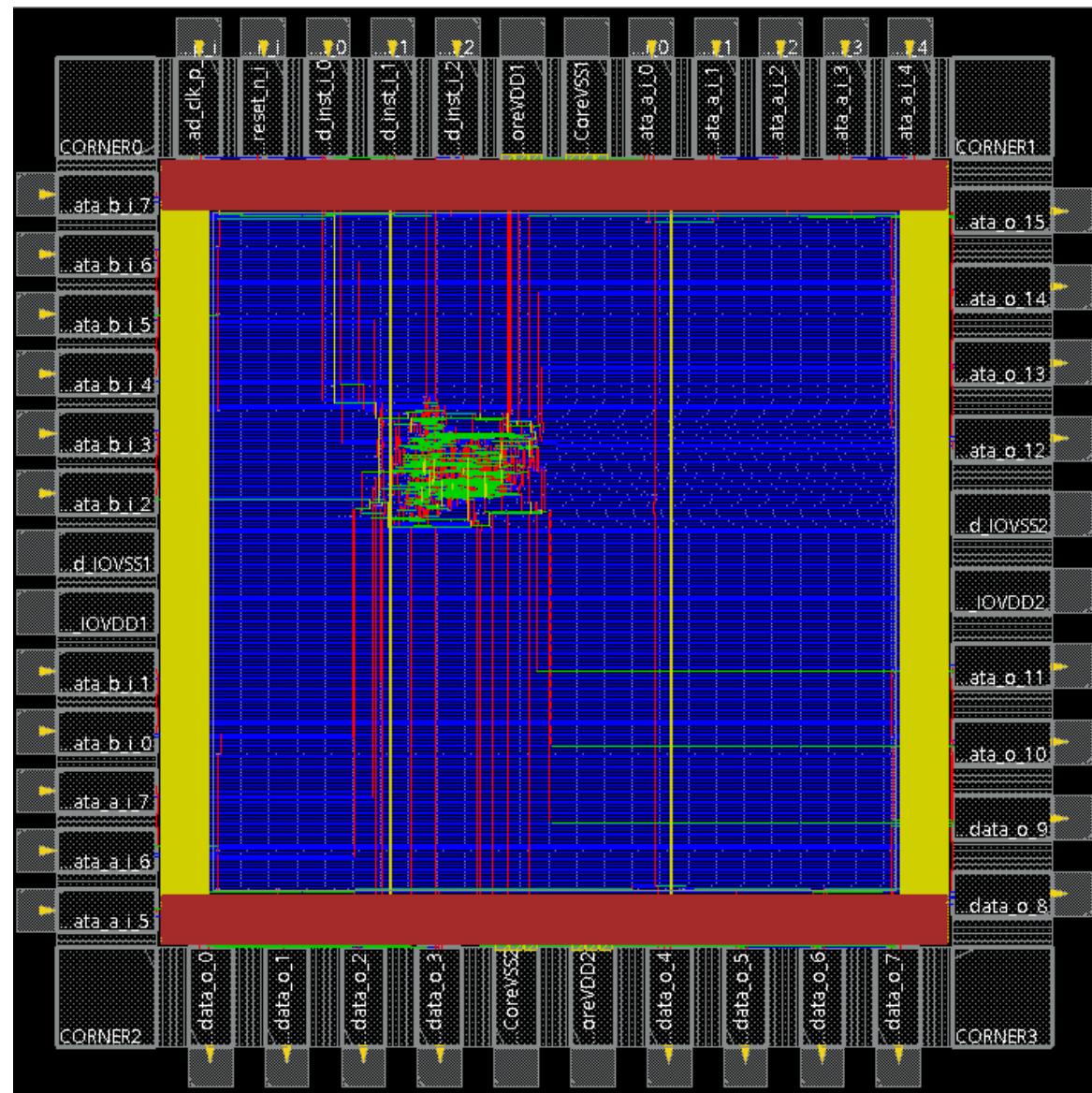
Routing

- Still may have DRC violations since it uses tricks to prevent checking rules and fasten the process.
 - “Search and Repair” after routing.
 - Use other tools to do DRC check.
- If DRC violations cannot be cleared in ~50 search & repair loops
→ Change your **floorplan** or **redesign** your system.



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Routing





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Design for Manufacturing

- Add core fillers
- Add dummy metals
- Add bonding pad
- Verify DRC & LVS

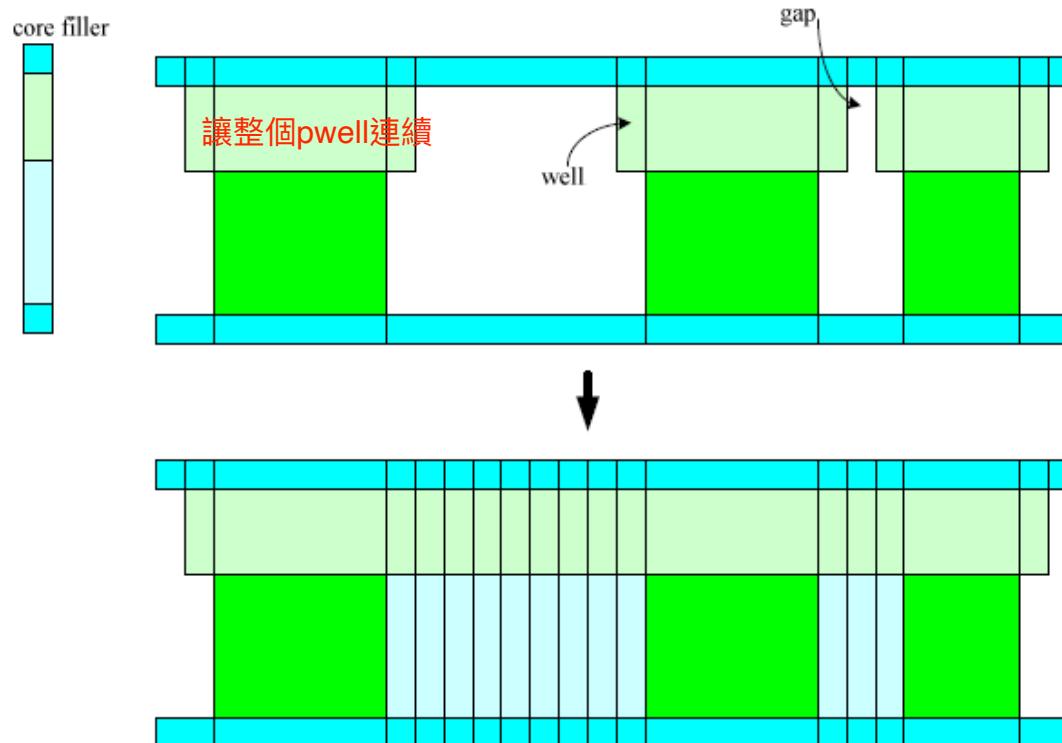


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Add core fillers

Place → Filler → Add Filler...

- Connect the NWELL/PWELL layer in core rows
- Insert Well contact
- Add from wider filler to narrow filler





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Add dummy metals

Why add dummy metal...

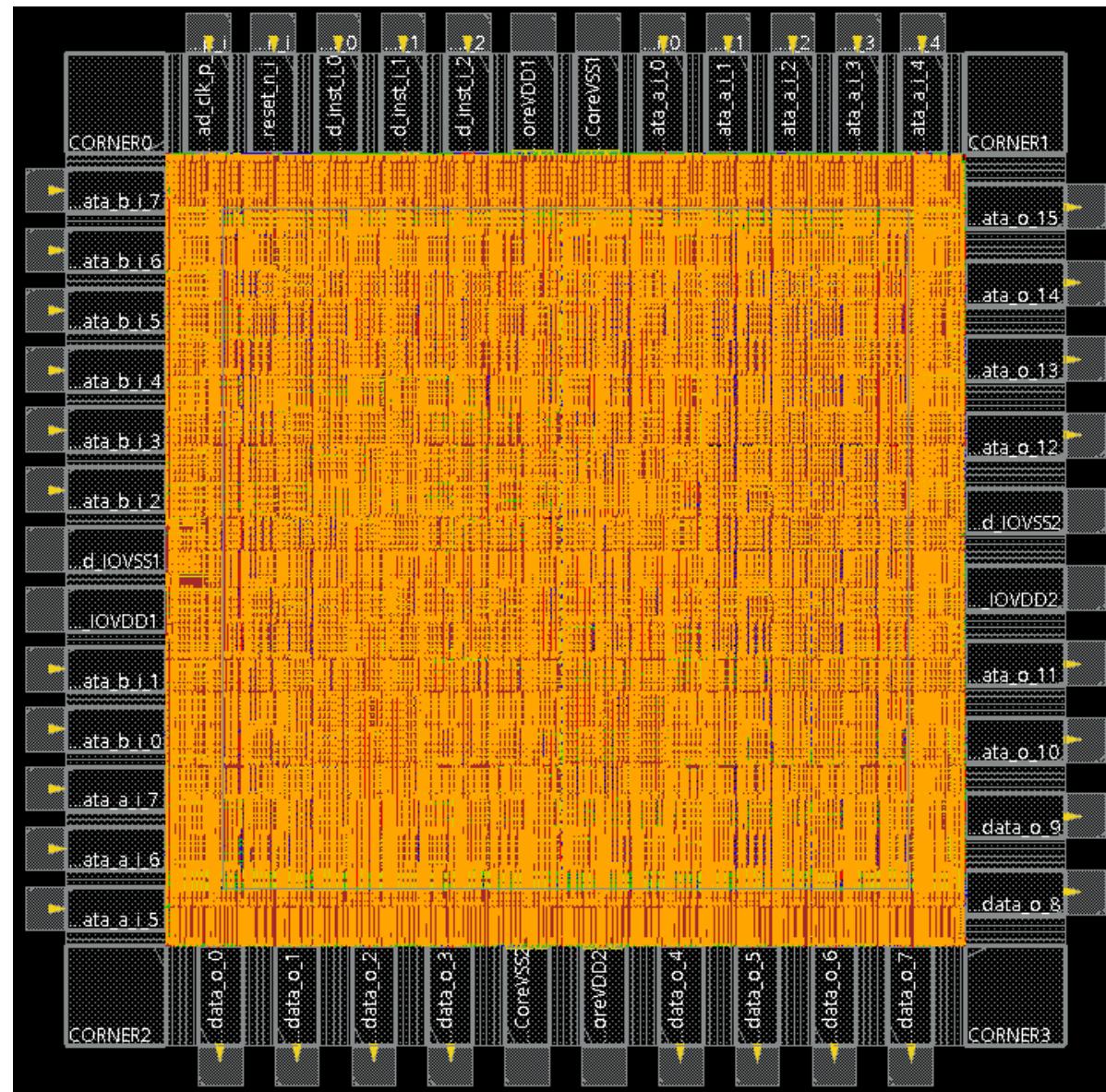
- Meet minimize metal density rule
- Prevent over etching
- Prevent sagging in local area
- Improve yield
- Reduce on chip variation

Better connect dummy metal to VSS



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Add Dummy Metals





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• Stream Out Data

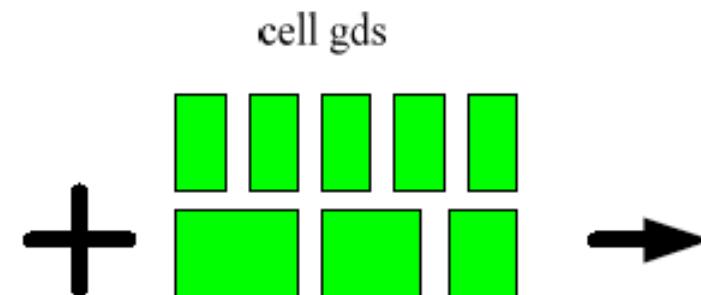
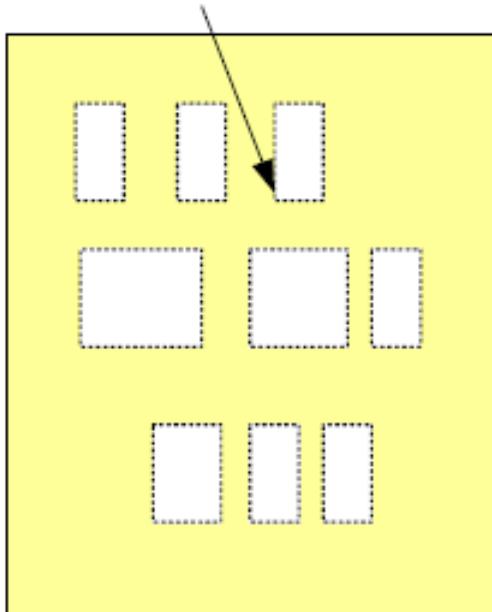
- GDS file
- Verilog file and SDF file



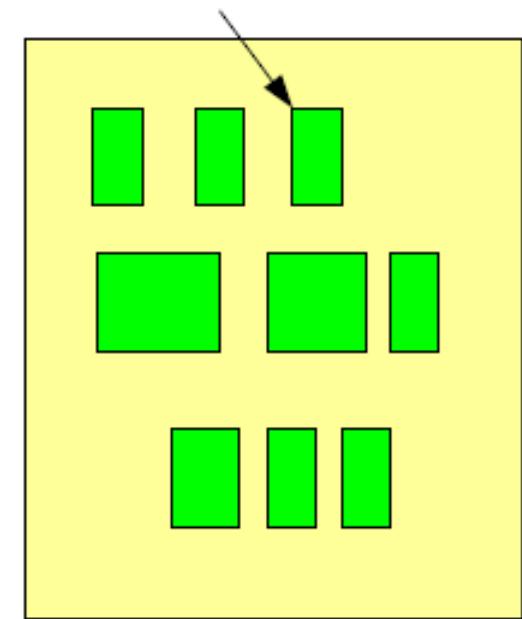
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Stream Out GDS

only cell name and location



full cell layout information





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Stream Out .v and .sdf

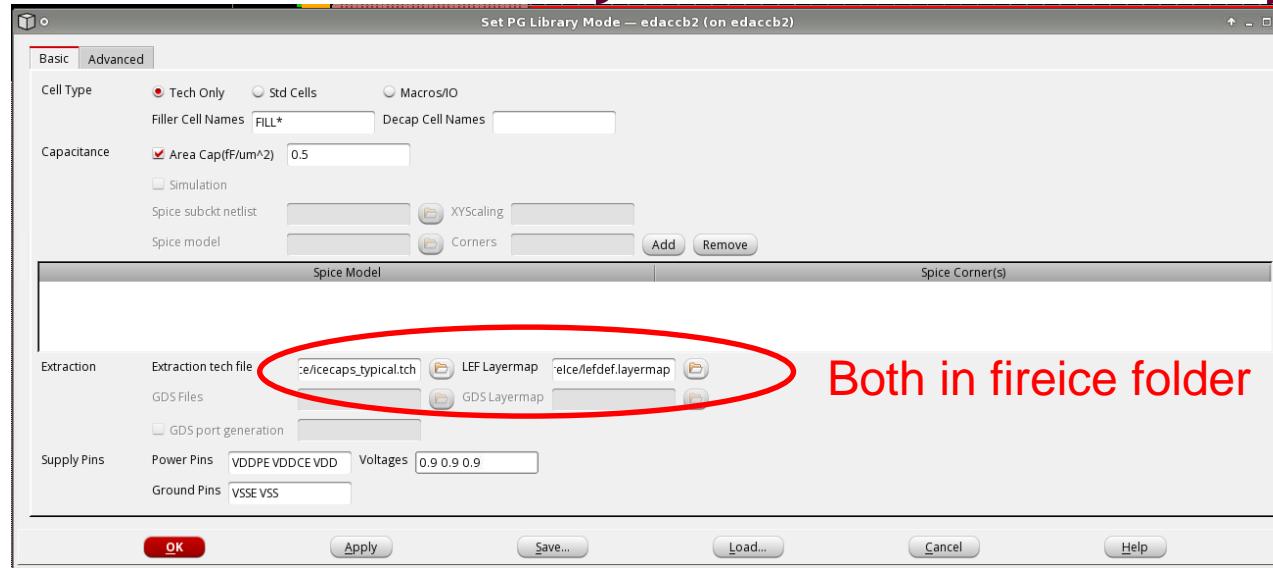
- .v for simulation: no pad/corefiller, 1'b1 for VDD, 1'b0 for GND.
- .sdf is the timing information to run simulation.



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Power Analysis

- Run your postroute Verilog file and generate vcd file
- Power -> Rail Analysis -> Set PG Library Mode



- Power -> Rail Analysis -> Generate PG library -> generate techonly.cl

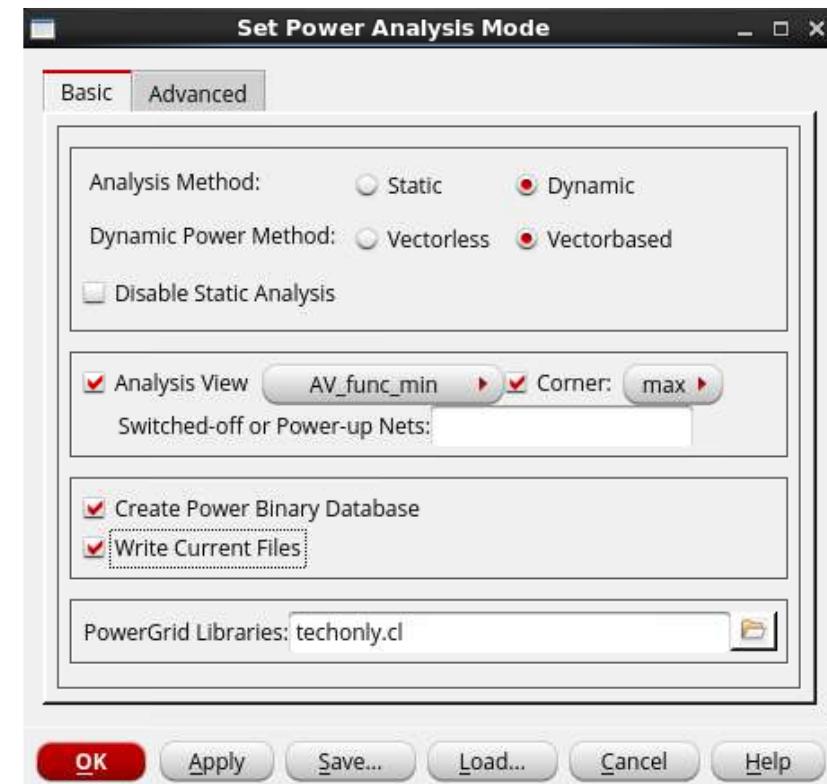


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Power Analysis

- Power -> Power Analysis -> Setup

- Analysis Method : Dynamic
- Dynamic Power Method : Vectorbased
- Analysis View : your function view
- Create Power Binary Database
- Write Current Files
- PowerGrid Libraries -> techonly.cl

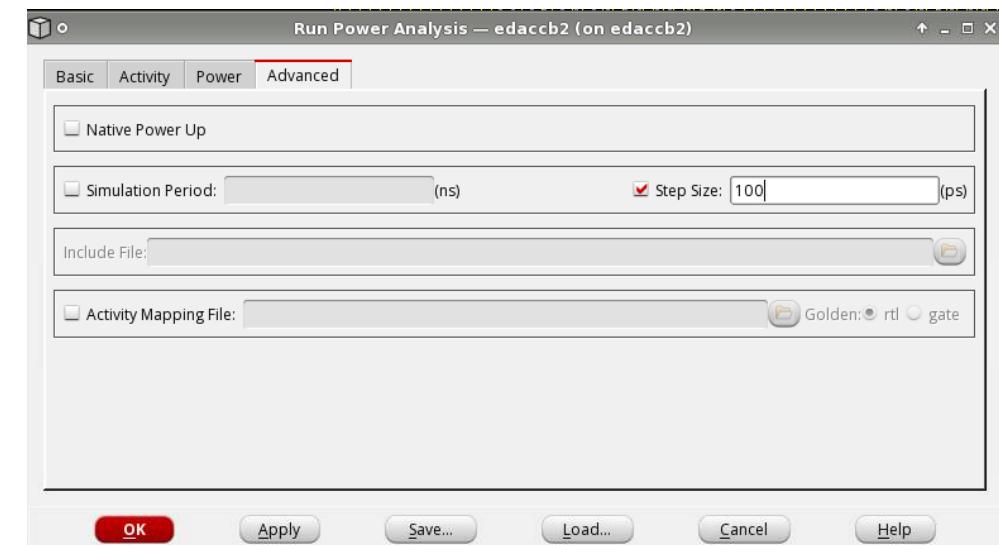
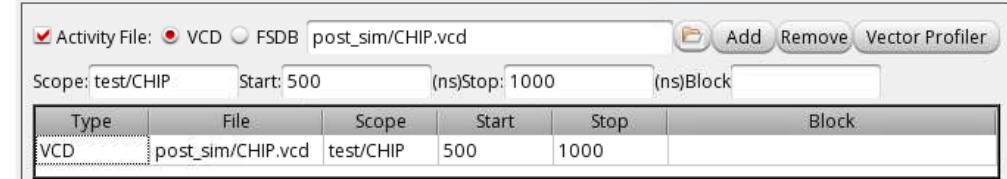




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Power Analysis

- Power -> Power Analysis -> Run
 - Activity File : vcd
 - Change to Advanced Page: check Step Size:100
- Output in power.rpt





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Rail Analysis

- Power -> Rail Analysis
-> Setup Rail Analysis
 - PowerGrid Libraries :
techonly.cl

Analysis Stage: Early Sign Off

Analysis Method: Static Dynamic

Accuracy: XD HD

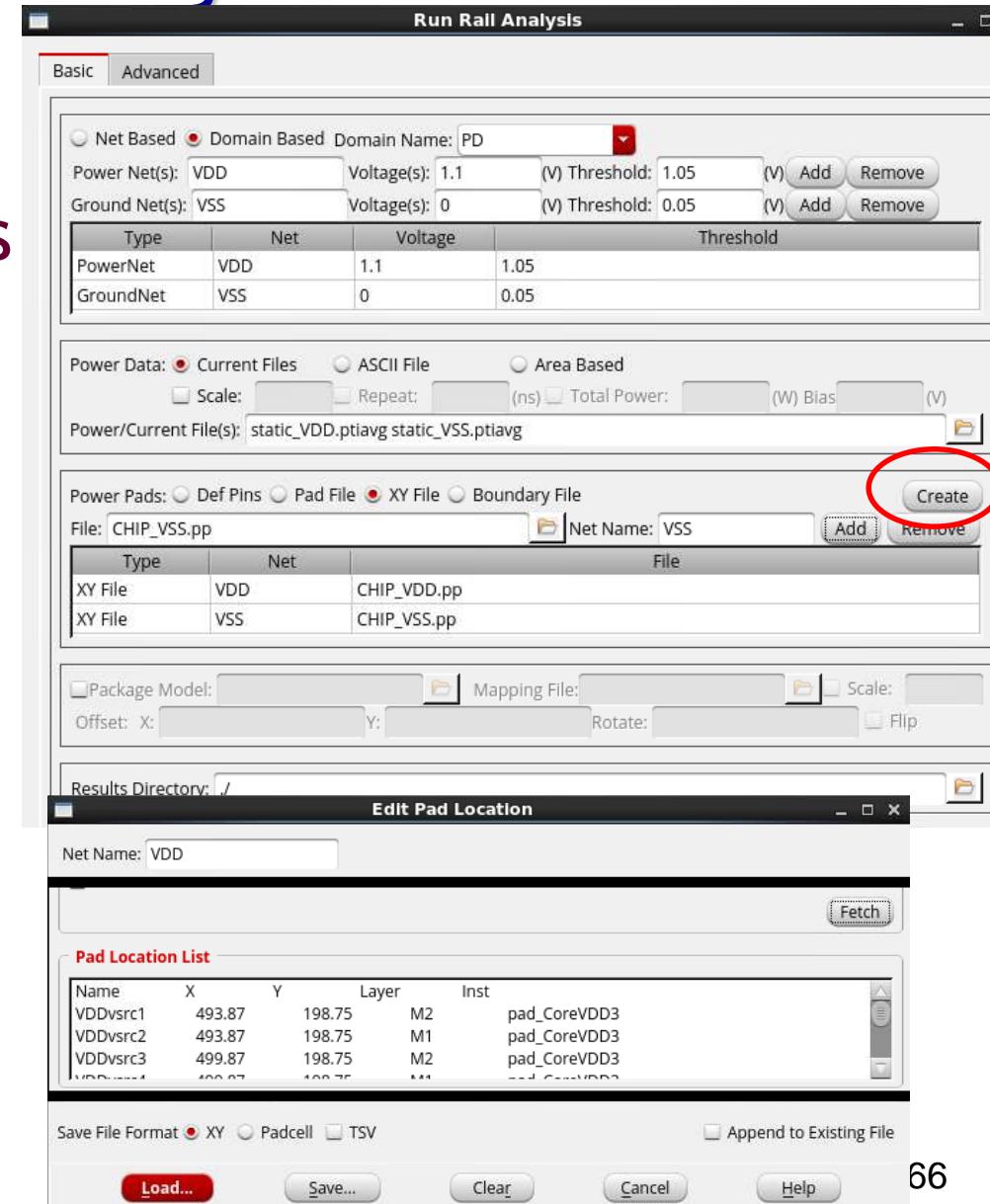
PowerGrid Libraries: techonly.cl



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Rail Analysis

- Power -> Rail Analysis
-> Run Rail Analysis
 - Same as Early Rail Analysis
- Run, IR drop information is in command log

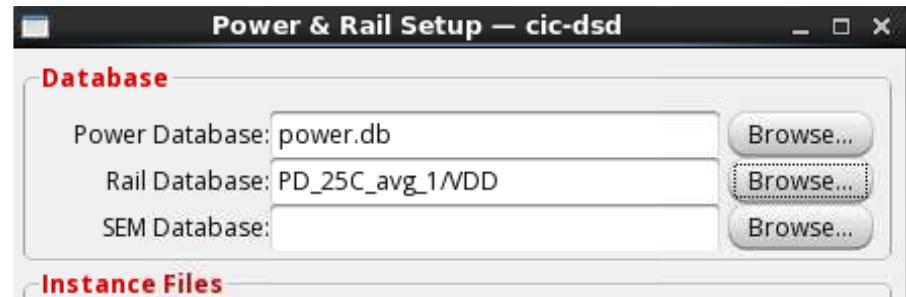
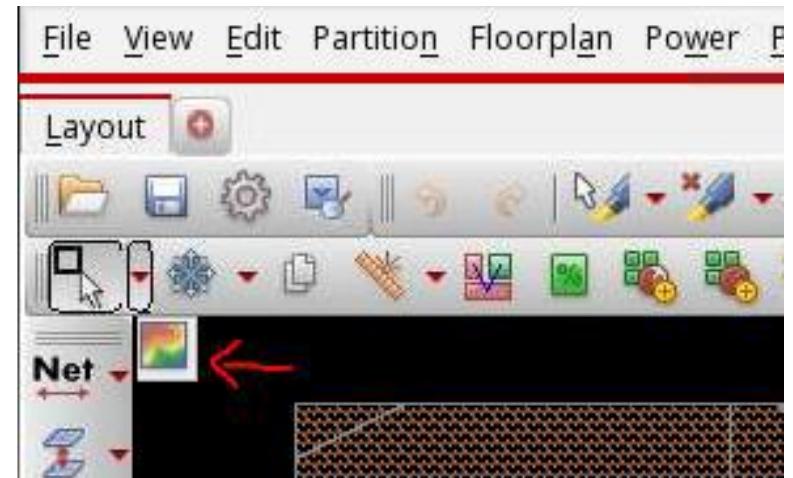




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View Result in Innovus

- Power -> Report -> Power Rail Result
- DB setup -> Power Database: power.db
- Rail Database : PD_25C_avg_#/VDD (# is the number you execute rail analysis)





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Dynamic Analysis

- Power -> Rail Analysis -> Setup Rail Analysis
 - Choose Dynamic
 - Generate Movies
- Power -> Report -> Dynamic Movie
 - Choose PD_25C_dynamic_#/VDD/movie_analysis
- You can view current and IR drop



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Reference

- [1] CVSD " I/O Pad Insertion for SOC Encounter" Yi-Fang Chen, Meng-Kai Hsu, EDA Lab
- [2] CVSD " SOC EncounterTM 10.10(1/2)" Yi-Fang Chen, Meng-Kai Hsu, EDA Lab ,Tung-Hsing Wu, Media IC & System Lab
- [3] CVSD " SOC EncounterTM 10.10(2/2)" Hung-Chih Ou,Xin-Wei Shih, EDA Lab, 曾鈺翔, Media IC & System Lab
- [4] CIC"Cell-Based IC Physical Design and Verification-Encounter Digital Implementation"
- [5] ICD_Lab" Automatic Place & Route" Chung-Hao Wu,MRSLab