



Automatic Place & Route

Derived from slides by Chung-Hao Wu

NTU MicroSystem Research Lab.



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Outline

- Prepare Data
- Automatic Place & Route - Innovus
- Stream Out Data



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Design Setup

- Library Data
 - Technology File
 - Reference Libraries
- Design Data
 - Gate-level Netlist (.v) with pad definitions
 - Timing Constraints (.sdc)
 - IO constraints (.ioc)



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Design Setup (cont.)

- Put .v, .sdc, and .ioc into folder “design”
- Simulation lib in folder “Verilog”
 - Core and io pad lib

名稱	修改日期	類型	大小
celtic	2017/3/21 下午 1...	檔案資料夾	
design	2017/3/21 下午 1...	檔案資料夾	
Firelce	2017/3/21 下午 1...	檔案資料夾	
lef	2017/3/21 下午 1...	檔案資料夾	
lef2gds	2017/3/21 下午 1...	檔案資料夾	
lib	2017/3/21 下午 1...	檔案資料夾	
Phantom	2017/3/21 下午 1...	檔案資料夾	
Verilog	2018/3/27 下午 0...	檔案資料夾	
00_readme.txt	2015/8/2 下午 03...	TXT 檔案	1 KB
addbonding_v3.8C.pl	2015/8/2 下午 03...	PL 檔案	40 KB
addbonding_v3.8D.pl	2015/8/2 下午 03...	PL 檔案	40 KB
addIoFiller.cmd	2015/8/2 下午 03...	Windows 命令指...	1 KB
bondingdraw_v2b4.pl	2015/8/2 下午 03...	PL 檔案	19 KB
CHIP.ioc.example	2015/8/2 下午 03...	EXAMPLE 檔案	3 KB
io_C.list	2015/8/2 下午 03...	LIST 檔案	7 KB
io_D.list	2015/8/2 下午 03...	LIST 檔案	6 KB
Lab4.doc	2018/3/27 下午 0...	Microsoft Word ...	182 KB
mmmc.view	2015/8/2 下午 03...	VIEW 檔案	3 KB
savegds.cmd.example	2015/8/2 下午 03...	EXAMPLE 檔案	1 KB
savesdf.cmd.example	2015/8/2 下午 03...	EXAMPLE 檔案	1 KB
streamOut.map	2015/8/2 下午 03...	MAP 檔案	2 KB
u18_Faraday.CapTbl	2015/8/2 下午 03...	CAPTBL 檔案	348 KB



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Pad definitions

- Instantiate your design in module “CHIP”
- XMD is input pad and YA2GSD is output pad
- Using “TIE” module to assign 0/1

```
module CHIP ( clk_p_i, reset_n_i, data_a_i, data_b_i, inst_i, data_o );
  input [7:0] data_a_i;
  input [7:0] data_b_i;
  input [2:0] inst_i;
  output [15:0] data_o;
  input clk_p_i, reset_n_i;

  wire [7:0] i_data_a_i;
  wire [7:0] i_data_b_i;
  wire [2:0] i_inst_i;
  wire [15:0] i_data_o;
  wire i_clk_p_i, i_reset_n_i;
  wire n_logic0,n_logic1;
  alu alu_in( .clk_p_i(i_clk_p_i), .reset_n_i(i_reset_n_i), .data_a_i(i_data_a_i), .data_b_i(i_data_b_i), .inst_i(i_inst_i), .data_o(i_data_o) );

  TIE0 ipad_n_logic0(.O(n_logic0));
  TIE1 ipad_n_logic1(.O(n_logic1));
  XMD ipad_clk_p_i (.O(i_clk_p_i), .I(clk_p_i), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_reset_n_i (.O(i_reset_n_i), .I(reset_n_i), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_inst_i_0 (.O(i_inst_i[0]), .I(inst_i[0]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_inst_i_1 (.O(i_inst_i[1]), .I(inst_i[1]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_inst_i_2 (.O(i_inst_i[2]), .I(inst_i[2]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_data_a_i_0 (.O(i_data_a_i[0]), .I(data_a_i[0]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_data_a_i_1 (.O(i_data_a_i[1]), .I(data_a_i[1]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
  XMD ipad_data_a_i_2 (.O(i_data_a_i[2]), .I(data_a_i[2]), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));

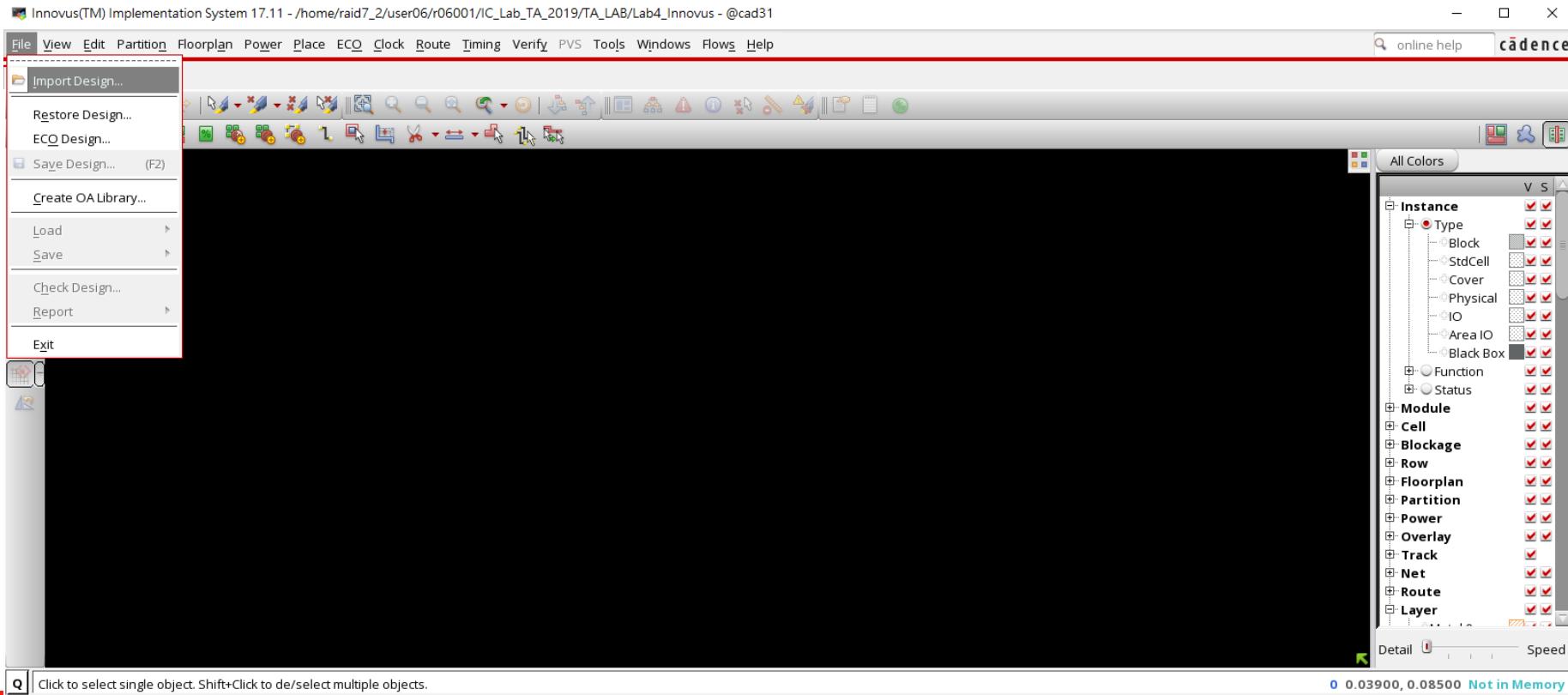
  YA2GSD ipad_data_o_0 (.O(data_o[0]), .I(i_data_o[0]), .E(n_logic1), .E2(n_logic0), .E4(n_logic0), .E8(n_logic0), .SR(n_logic0));
  YA2GSD ipad_data_o_1 (.O(data_o[1]), .I(i_data_o[1]), .E(n_logic1), .E2(n_logic0), .E4(n_logic0), .E8(n_logic0), .SR(n_logic0));
  YA2GSD ipad_data_o_2 (.O(data_o[2]), .I(i_data_o[2]), .E(n_logic1), .E2(n_logic0), .E4(n_logic0), .E8(n_logic0), .SR(n_logic0));
```



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Start Innovus

- > source /usr/cad/innovus/CIC/license.cshrc
- > source /usr/cad/innovus/CIC/innovus.cshrc
- > innovus
- File → Import Design...





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Import Design

Netlist:

Verilog

Files: `design/CHIP_syn.v`

Top Cell: Auto Assign By User: CHIP

Library:

Cell:

View:

Technology/Physical Libraries:

OA

Reference Libraries:

Abstract View Names:

Layout View Names:

LEF Files

`ef/FSA0M_A_T33_GENERIC_IO_ANT_V55.lef` `lef/BONDPAD.lef`

Floorplan

IO Assignment File: `design/CHIP.ioc`

Power

Power Nets: VCC

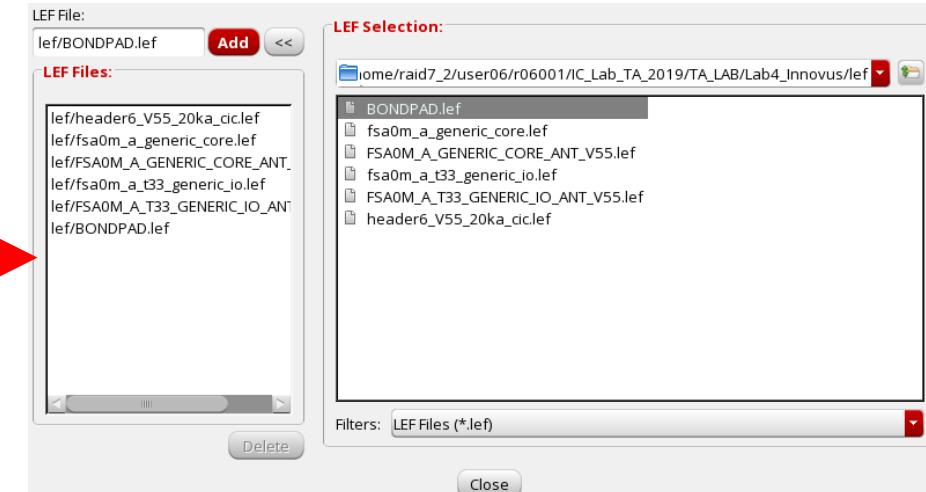
Ground Nets: GND

CPF File:

Analysis Configuration

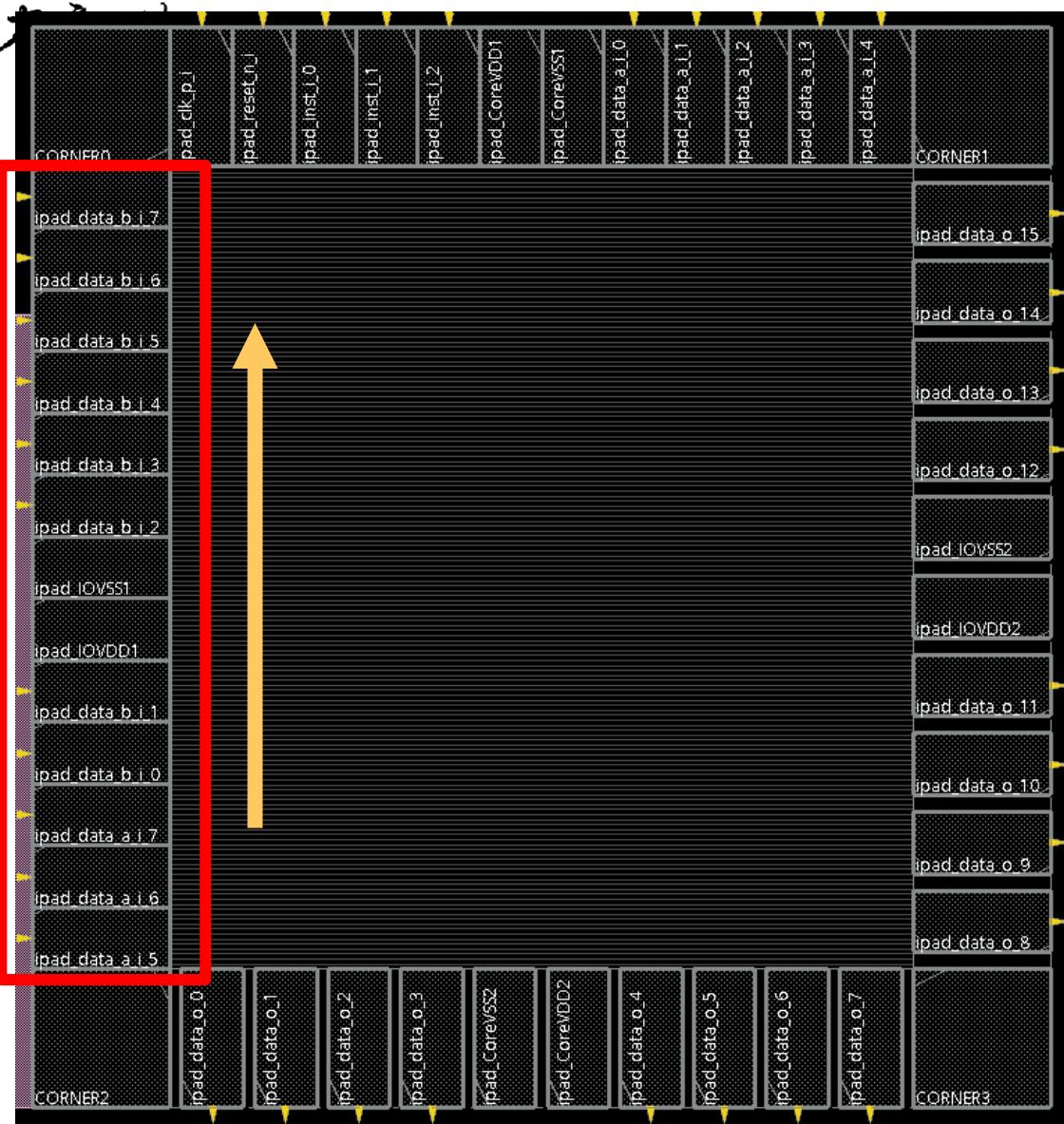
MMMC View Definition File: `mmmc.view`

- Be careful with order of LEF files





IOC file and chip view



Pad: CORNER1	NE	CORNERD
Pad: ipad_data_a_i_5	W	
Pad: ipad_data_a_i_6	W	
Pad: ipad_data_a_i_7	W	
Pad: ipad_data_b_i_0	W	
Pad: ipad_data_b_i_1	W	
Pad: ipad_IOVDD1	W	VCC3IOD
Pad: ipad_IOVSS1	W	GNDIOD
Pad: ipad_data_b_i_2	W	
Pad: ipad_data_b_i_3	W	
Pad: ipad_data_b_i_4	W	
Pad: ipad_data_b_i_5	W	
Pad: ipad_data_b_i_6	W	
Pad: ipad_data_b_i_7	W	

Pad: CORNER3	SE	CORNERD
Pad: ipad_data_o_8	E	
Pad: ipad_data_o_9	E	
Pad: ipad_data_o_10	E	
Pad: ipad_data_o_11	E	
Pad: ipad_IOVDD2	E	VCC3IOD
Pad: ipad_IOVSS2	E	GNDIOD
Pad: ipad_data_o_12	E	
Pad: ipad_data_o_13	E	
Pad: ipad_data_o_14	E	
Pad: ipad_data_o_15	E	

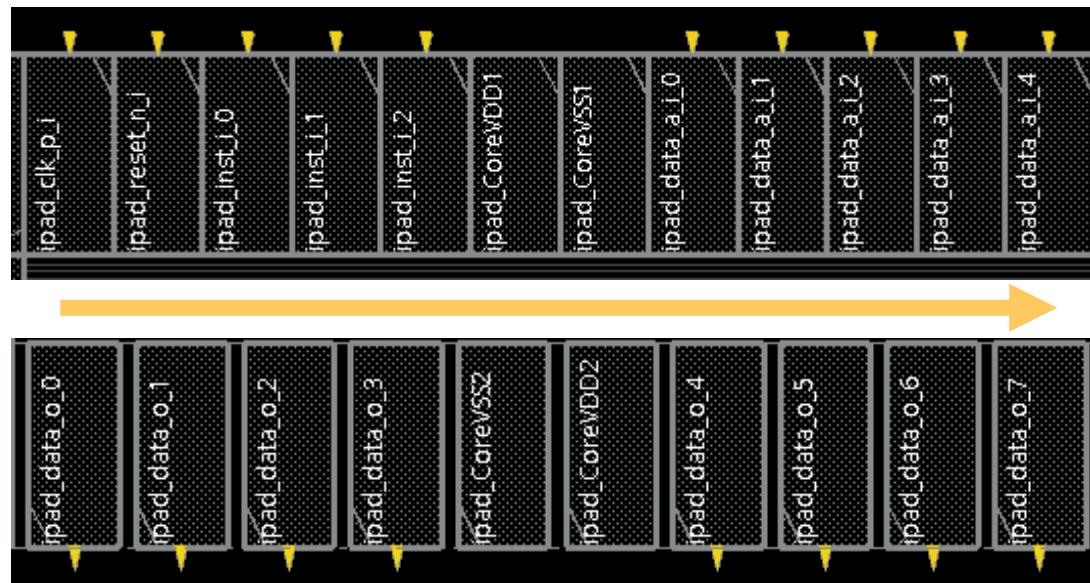


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IOC file and chip view (cont.)

Pad: CORNER0	NW	CORNERD
Pad: ipad_clk_p_i	N	
Pad: ipad_reset_n_i	N	
Pad: ipad_inst_i_0	N	
Pad: ipad_inst_i_1	N	
Pad: ipad_inst_i_2	N	
Pad: ipad_CoreVDD1	N	VCCKD
Pad: ipad_CoreVSS1	N	GNDKD
Pad: ipad_data_a_i_0	N	
Pad: ipad_data_a_i_1	N	
Pad: ipad_data_a_i_2	N	
Pad: ipad_data_a_i_3	N	
Pad: ipad_data_a_i_4	N	

Pad: CORNER2	SW	CORNERD
Pad: ipad_data_o_0	S	
Pad: ipad_data_o_1	S	
Pad: ipad_data_o_2	S	
Pad: ipad_data_o_3	S	
Pad: ipad_CoreVSS2	S	GNDKD
Pad: ipad_CoreVDD2	S	VCCKD
Pad: ipad_data_o_4	S	
Pad: ipad_data_o_5	S	
Pad: ipad_data_o_6	S	
Pad: ipad_data_o_7	S	





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IOC file and chip view (cont.)

- Pad name = module name

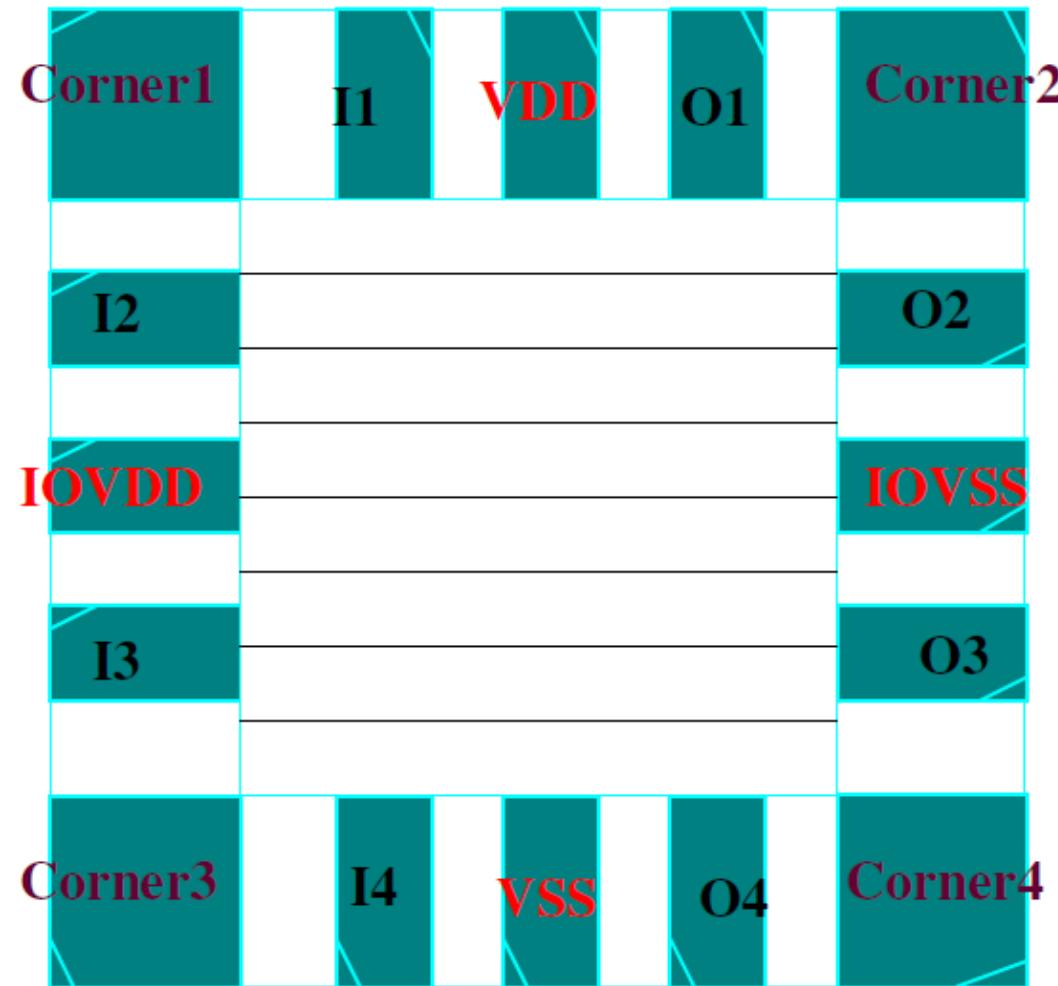
Pad: ipad_clk_p_i N

```
XMD ipad_clk_p_i (.O(i_clk_p_i), .I(clk_p_i), .PU(n_logic0), .PD(n_logic0), .SMT(n_logic0));
```



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IOC file and chip view (cont.)

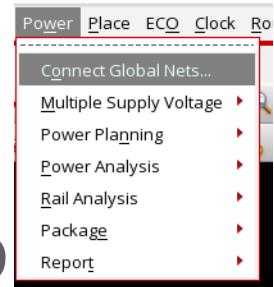




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Global Net Connect

- Power → Connect Global Nets
 - Connect cells' power/ground pin to VCC/GND



Connection List

VCC:PIN:* VCC:All

Power Ground Connection

Connect

Pin
 Tie High
 Tie Low

Instance Basename: *

Pin Name(s): VCC

Net Basename:

Scope

Single Instance:
 Under Module:
 Under Power Domain:
 Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0

Apply All

To Global Net: VCC

Override prior connection
 Verbose Output

Connection List

GND:PIN:*.GND:All

Power Ground Connection

Connect

Pin
 Tie High
 Tie Low

Instance Basename: *

Pin Name(s): GND

Net Basename:

Scope

Single Instance:
 Under Module:
 Under Power Domain:
 Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0

Apply All

To Global Net: GND

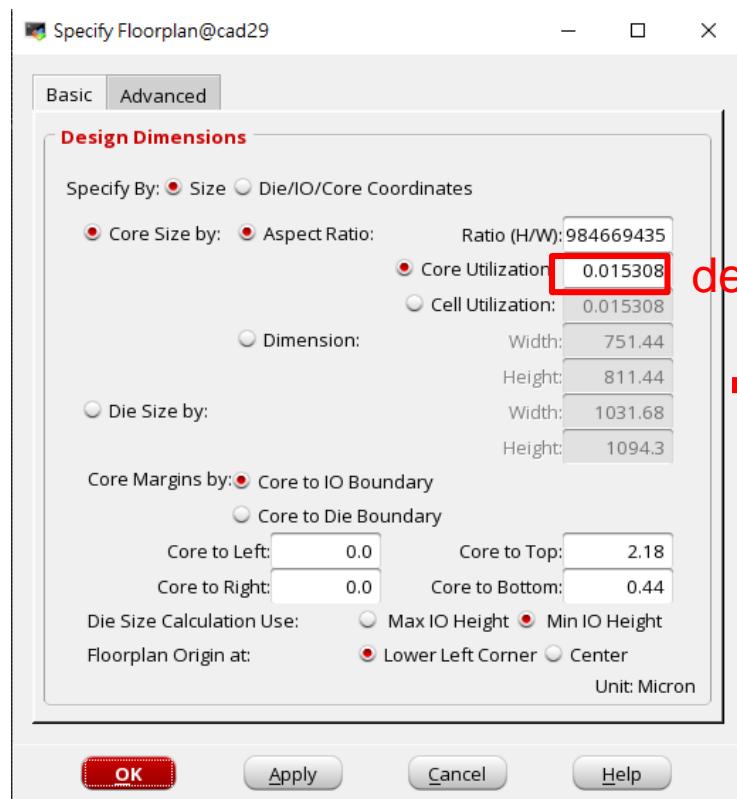
Override prior connection
 Verbose Output



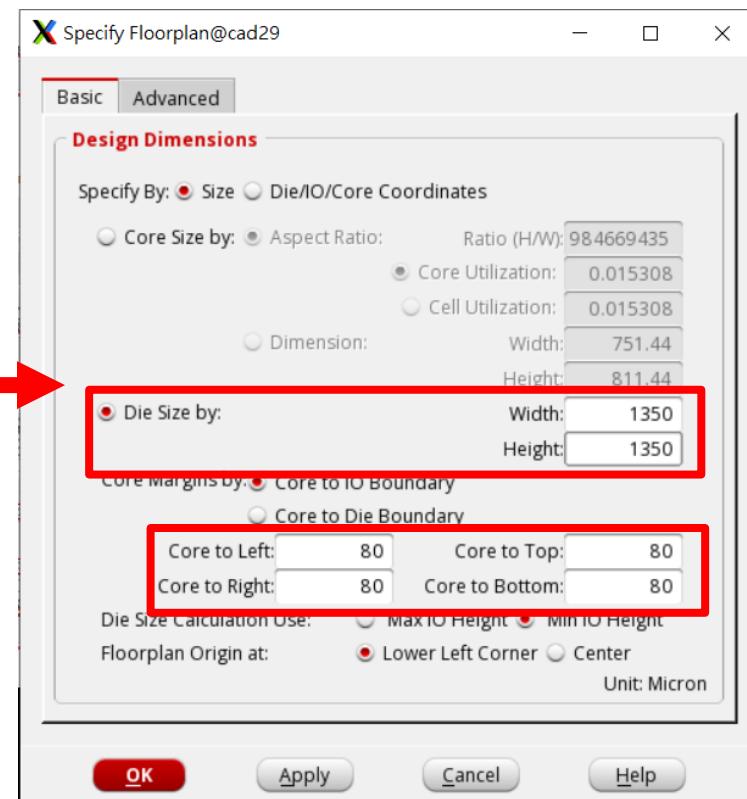
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Specify Floorplan

- Floorplan → Specify Floorplan
 - Be careful with space between pads



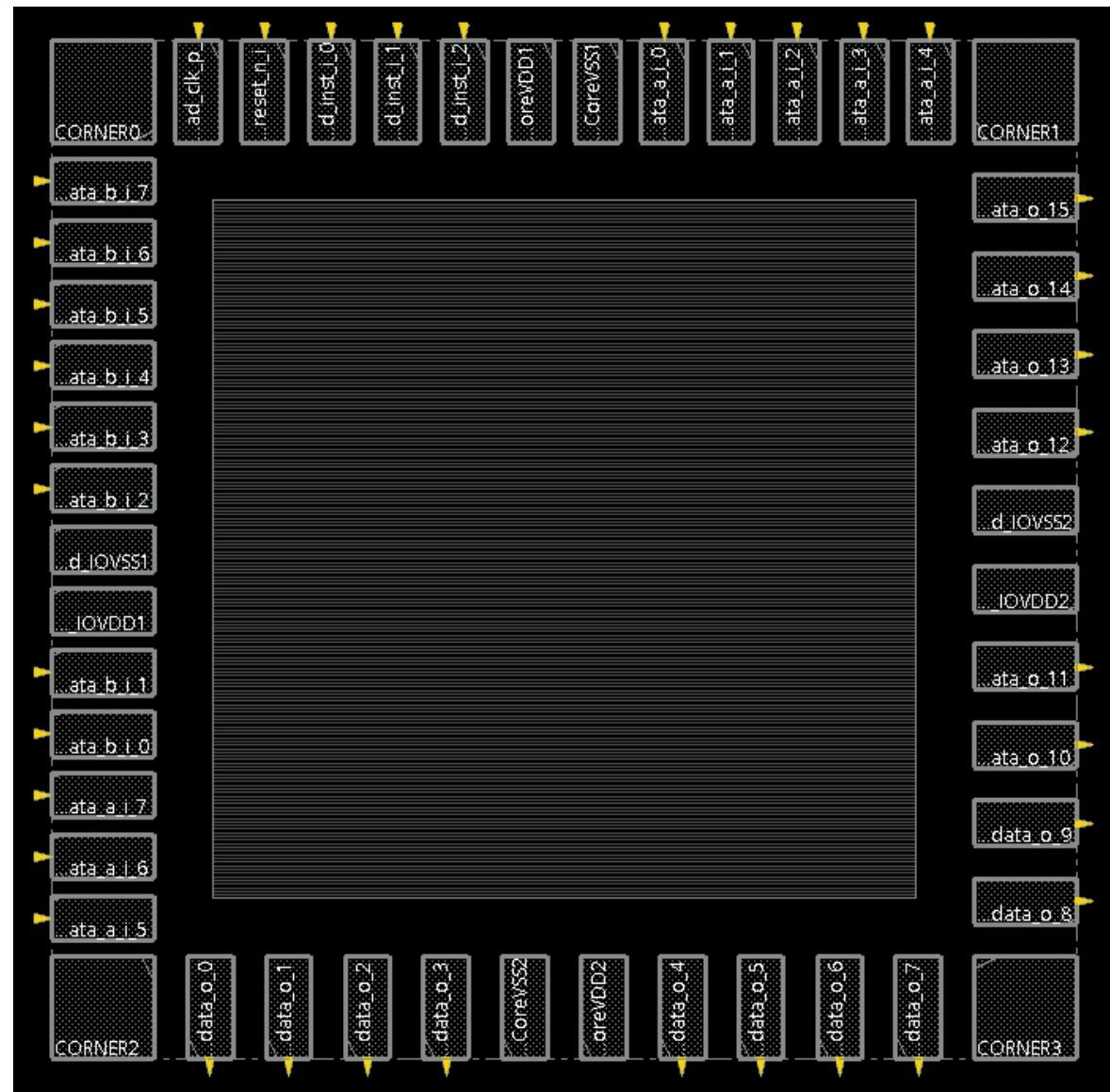
default





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Specify Floorplan (cont.)

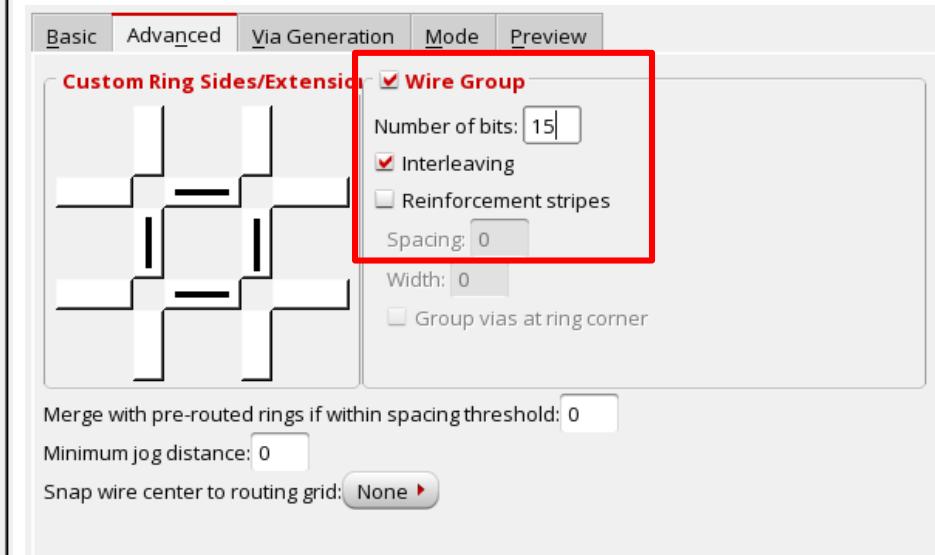
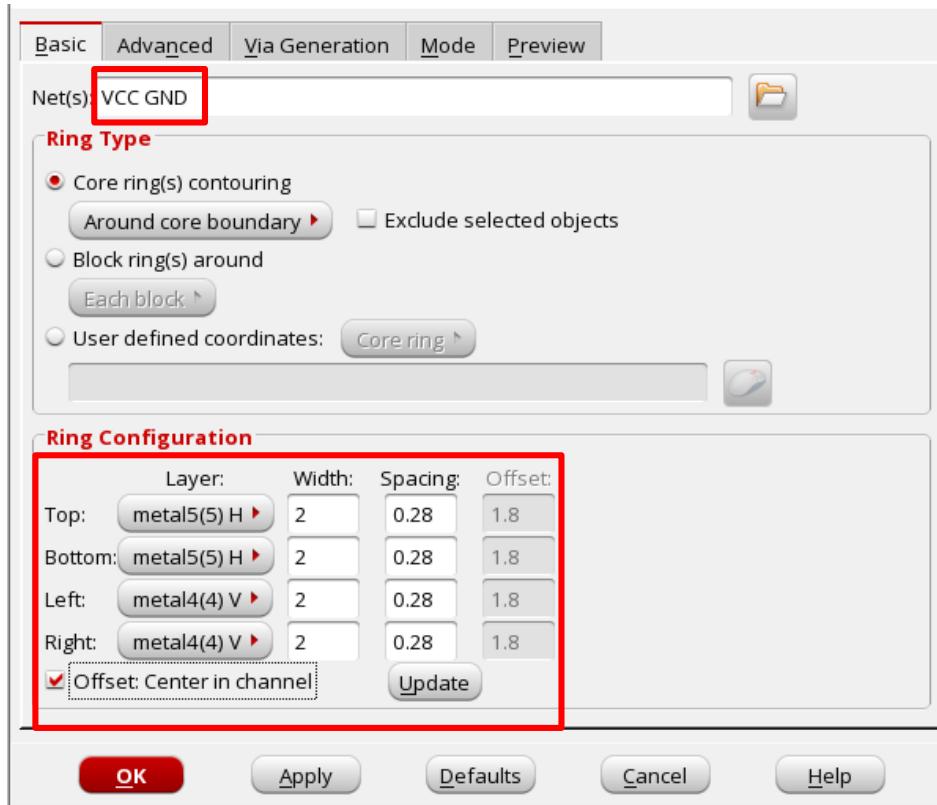
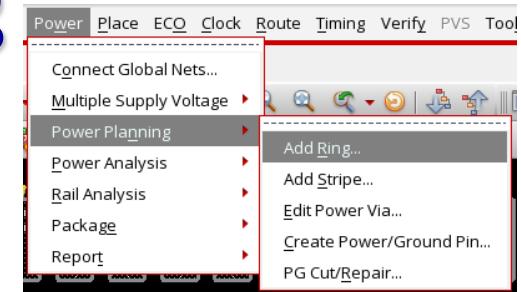




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Create Power-ring

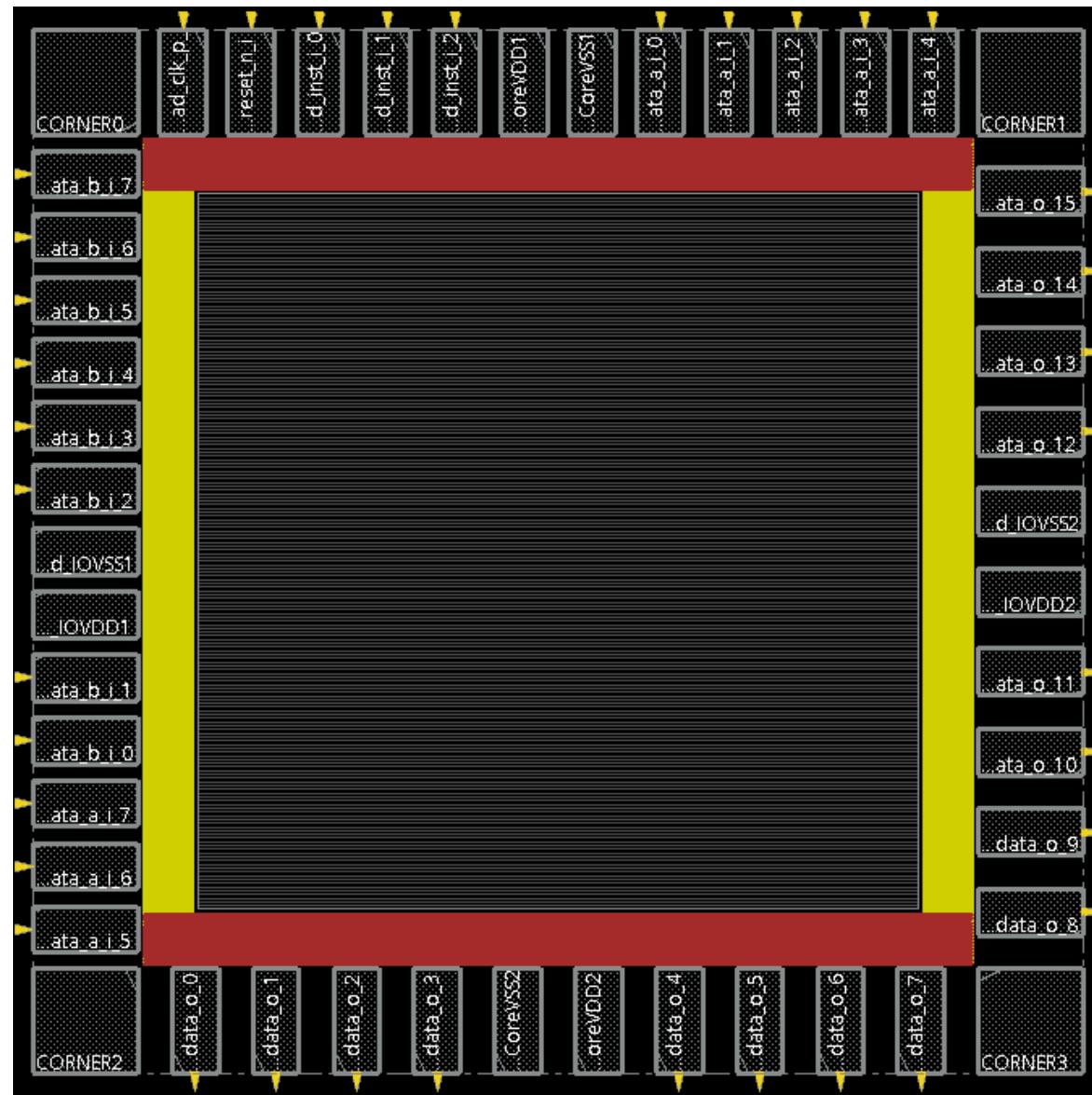
- Power → Power Planning → Add Rings





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Create Power-ring (cont.)

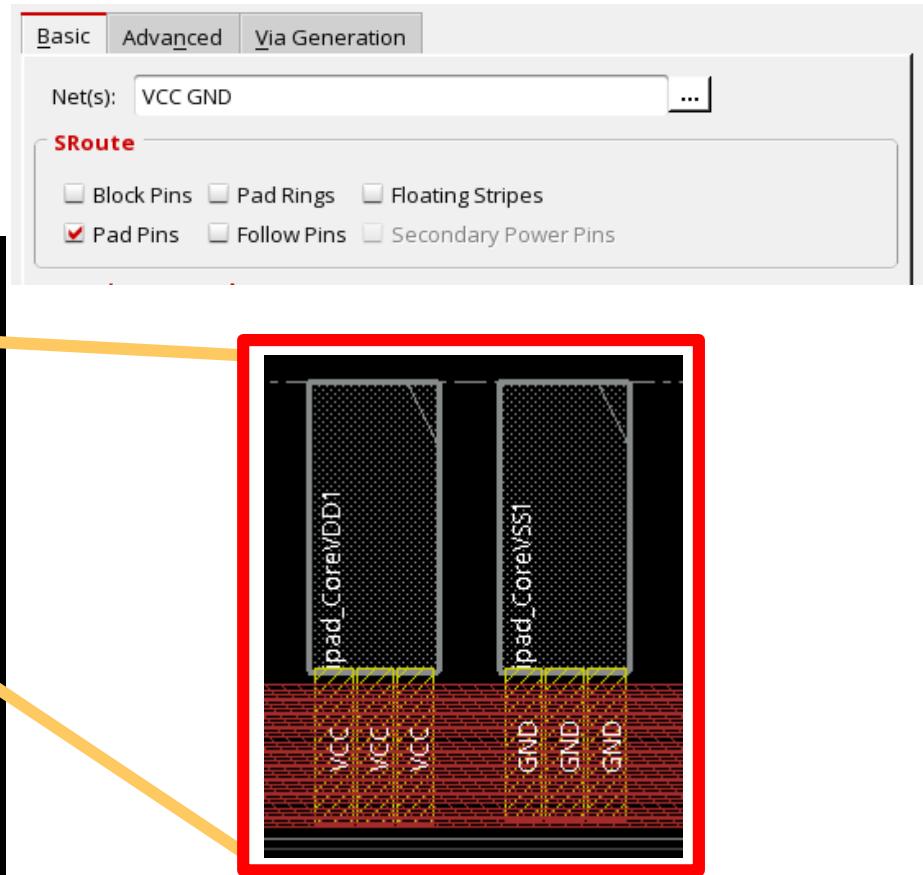
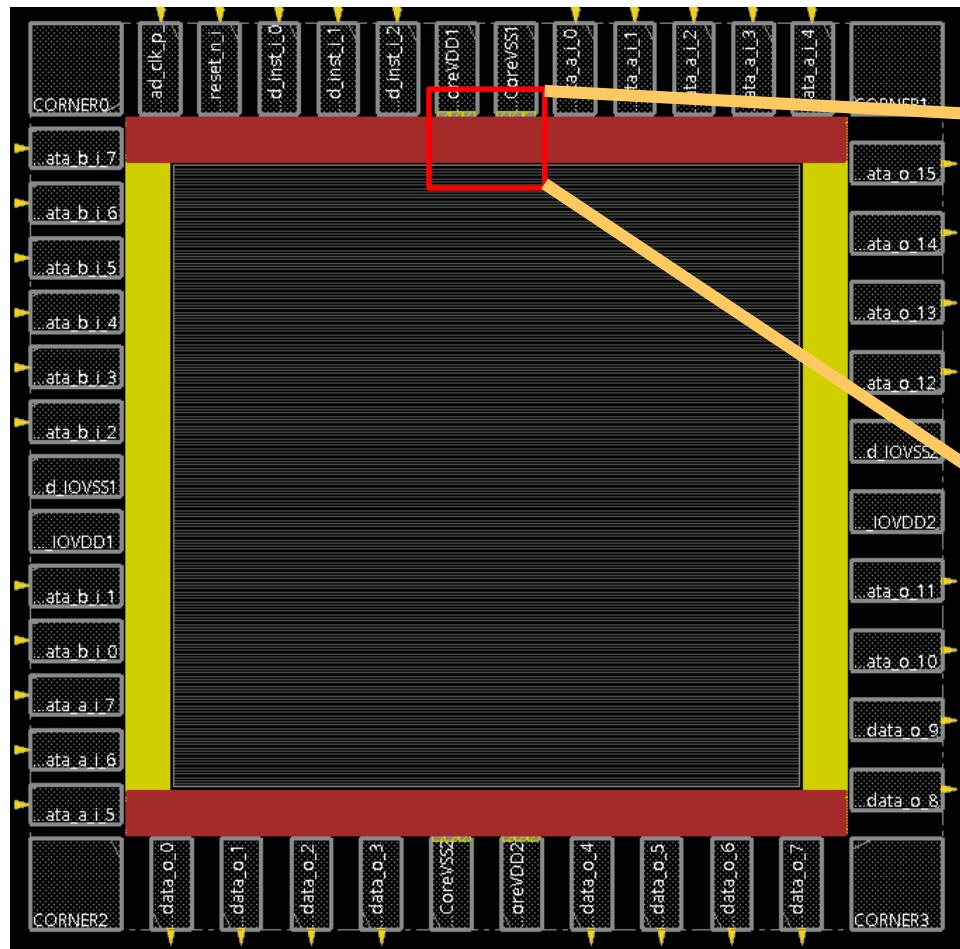




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Connect power pad

- Route → Special Route



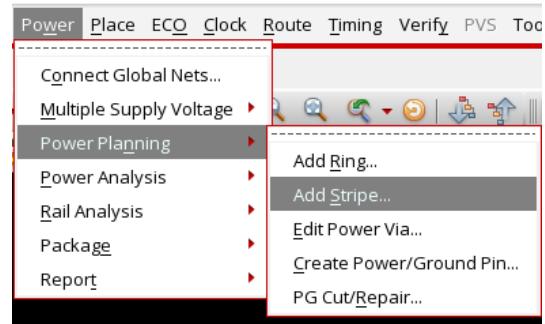


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Create Power-stripe

- Power → Power Planning → Add Stripes

- You could edit Set-to-set distance or start position of the first stripe if needed.



Basic Advanced Via Generation Mode Preview

Set Configuration

Net(s): VCC GND

Layer: metal4(4) Directions: Vertical Horizontal

Width: 1 Spacing: 0.28

Set Pattern

Set-to-set distance: 400 Number of sets: 1 Bumps

Over P/G pins Pin layer: Top pin layer Pin Width:

Master name: Selected blocks All blocks

Over Physical Pins Pin layer: Top pin layer Pin Width:

Stripe Boundary

Core ring Pad ring: All domains

Design boundary Create pins Each selected block/domain/fence

Specify rectangular area X1: Y1: X2: Y2:

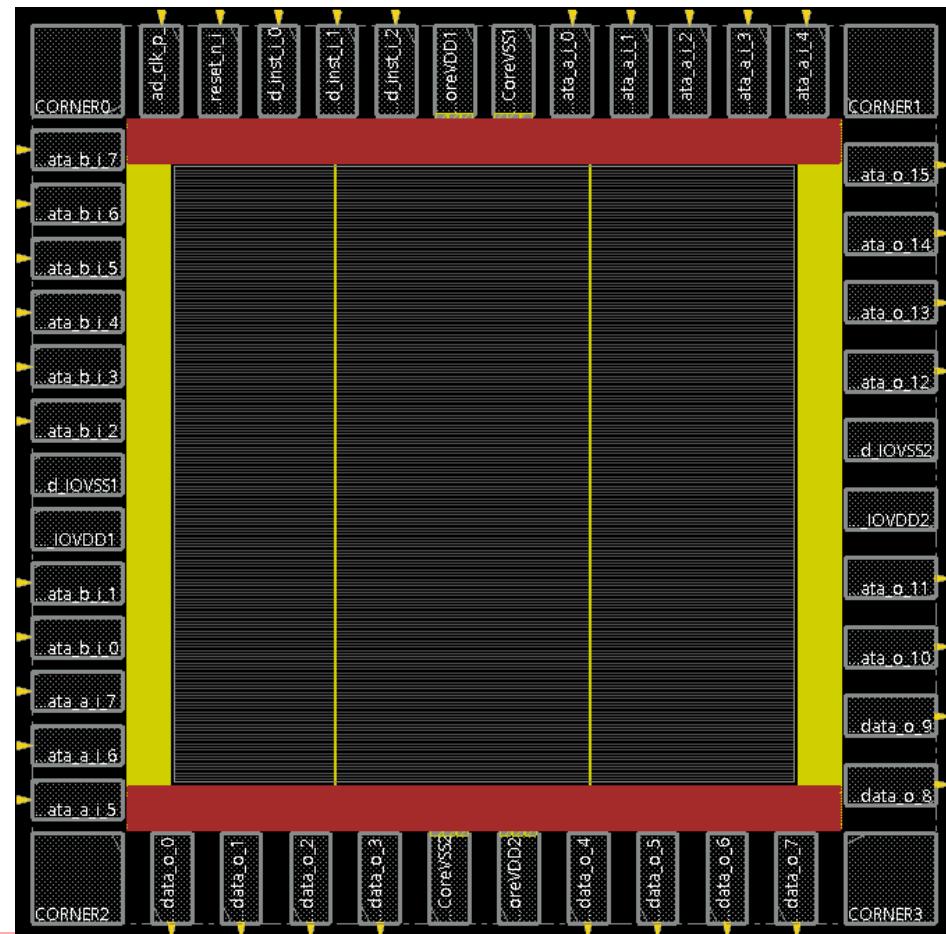
Specify rectilinear area

First/Last Stripe

Start from: Left Right Top Bottom

Relative from core or selected area Start: Stop:

Absolute Start: Stop:





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Connect Powerpin

- Route → Special Route

SRoute

Net(s): GND VCC

Block Pins Pad Rings Floating Stripes
 Pad Pins Follow Pins Secondary Power Pins

System Research Lab. 19

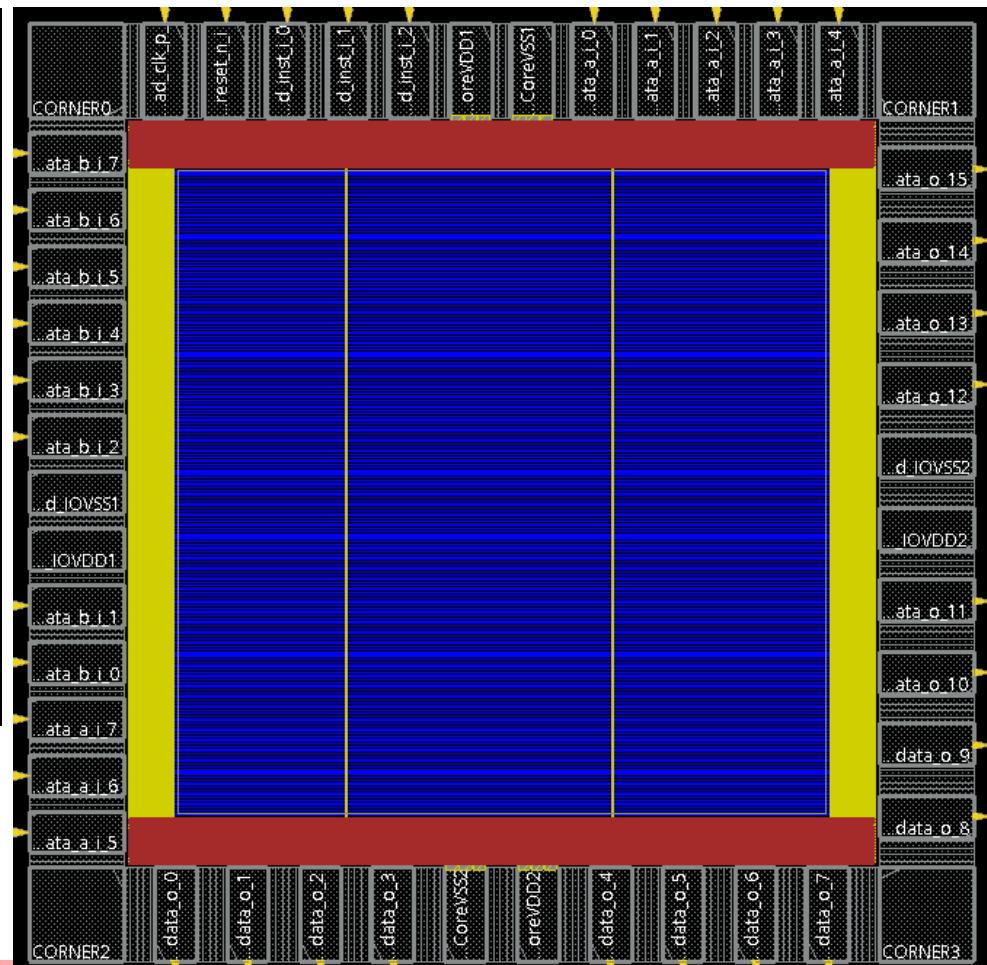


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Add IO Filler

- innovus> source addIoFiller.cmd

```
innovus 1> source addIoFiller.cmd
Added 26 of filler cell 'EMPTY16D' on top side.
Added 28 of filler cell 'EMPTY16D' on left side.
Added 44 of filler cell 'EMPTY16D' on bottom side.
Added 44 of filler cell 'EMPTY16D' on right side.
Added 13 of filler cell 'EMPTY8D' on top side.
Added 0 of filler cell 'EMPTY8D' on left side.
Added 11 of filler cell 'EMPTY8D' on bottom side.
Added 11 of filler cell 'EMPTY8D' on right side.
Added 13 of filler cell 'EMPTY4D' on top side.
Added 0 of filler cell 'EMPTY4D' on left side.
Added 0 of filler cell 'EMPTY4D' on bottom side.
Added 0 of filler cell 'EMPTY4D' on right side.
Added 13 of filler cell 'EMPTY2D' on top side.
Added 14 of filler cell 'EMPTY2D' on left side.
Added 11 of filler cell 'EMPTY2D' on bottom side.
Added 0 of filler cell 'EMPTY2D' on right side.
Added 26 of filler cell 'EMPTY1D' on top side.
Added 28 of filler cell 'EMPTY1D' on left side.
Added 0 of filler cell 'EMPTY1D' on bottom side.
Added 11 of filler cell 'EMPTY1D' on right side.
innovus 2>
```

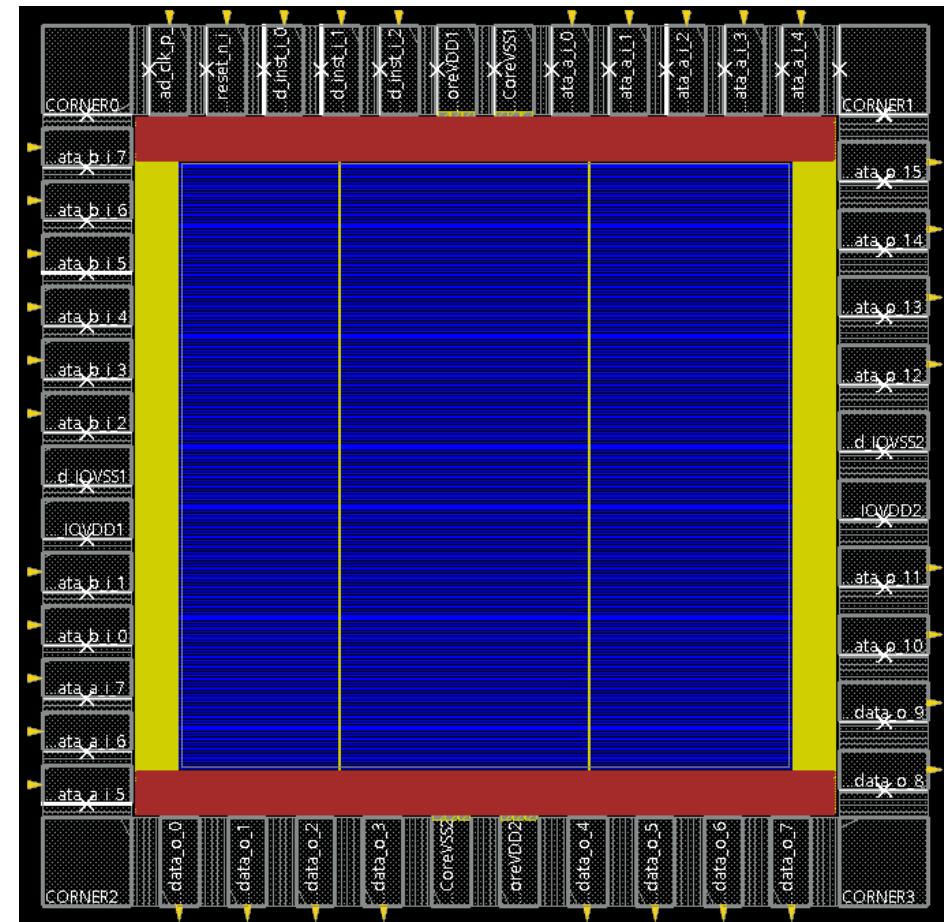
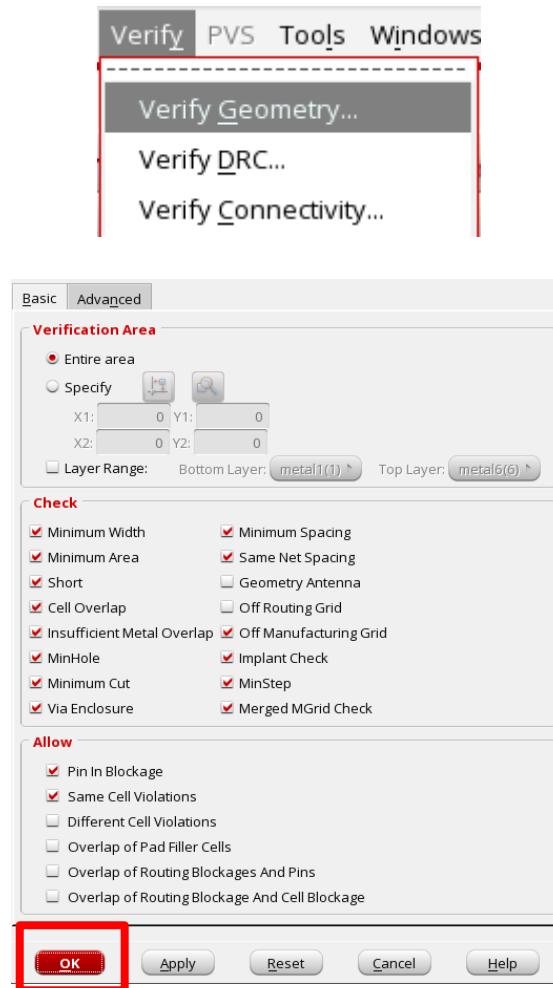




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Check Violation by far

- Verify Geometry (ignore xx between pad)

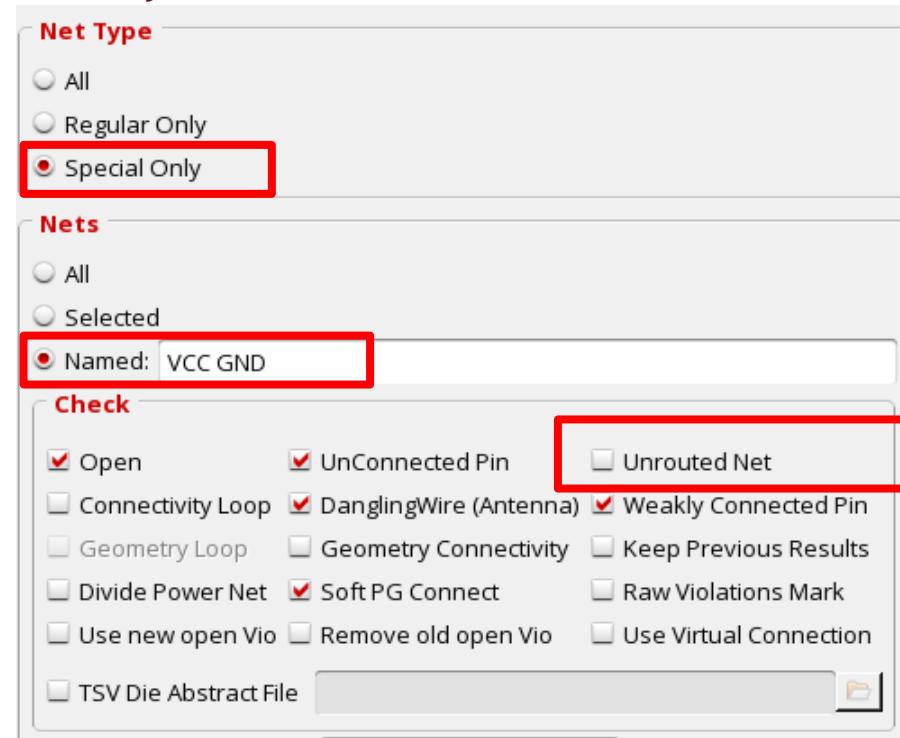
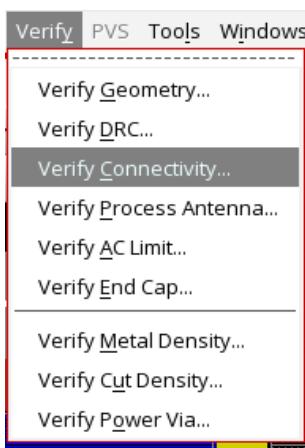




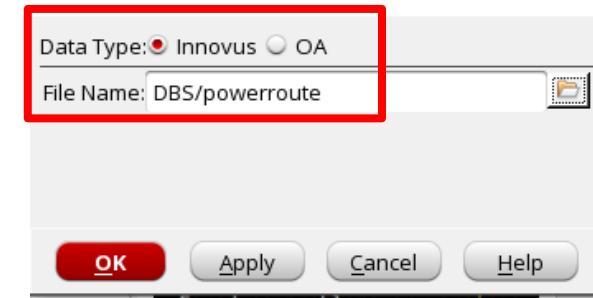
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Check Violation by far (cont.)

- Verify Connectivity

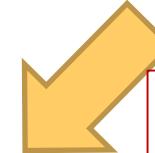


- Save your design by now.



```
Check specified nets
*** Checking Net VCC
*** Checking Net GND

Begin Summary
  Found no problems or warnings.
End Summary
```



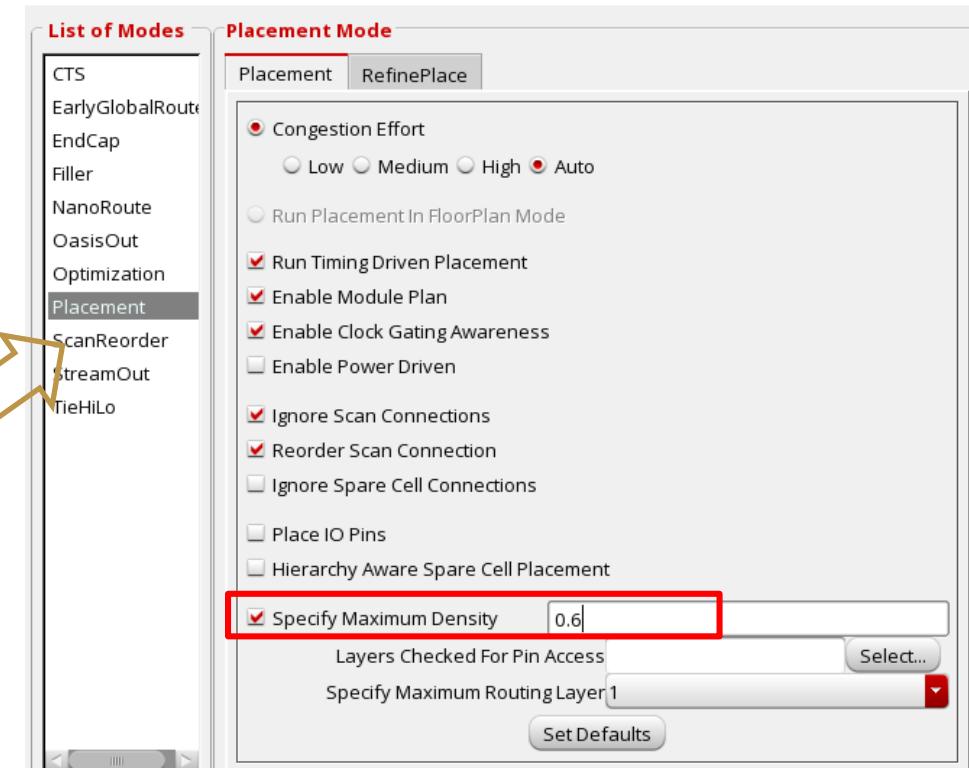
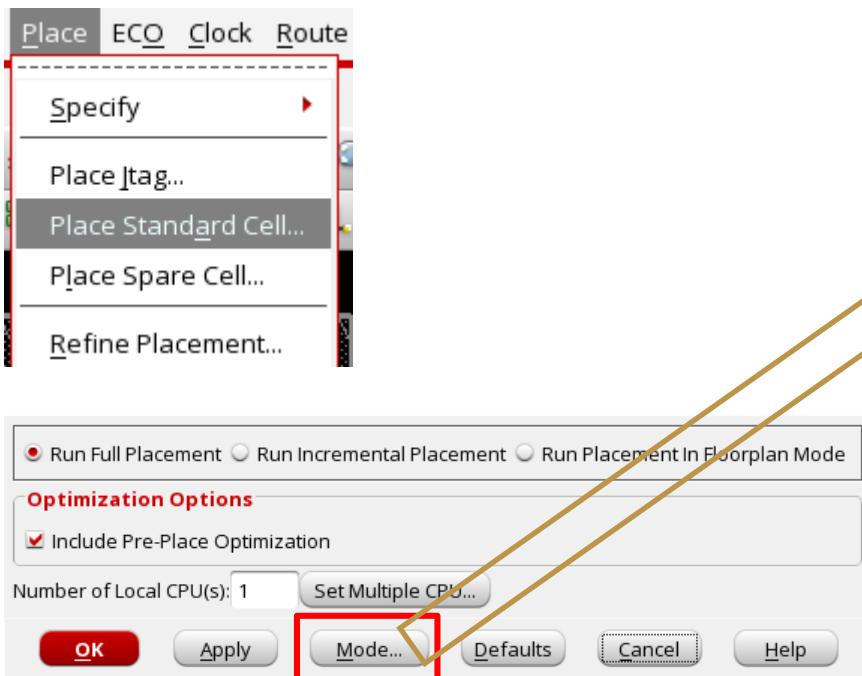
Message shows in terminal.



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Pre-CTS placement

- Place → Place Standard Cells





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Check Timing

- Timing → Report Timing
- ECO → Optimize Design
 - If WNS is negative or design has violation, try this step

Basic	Advanced
<input type="checkbox"/> Use Existing Extraction and Timing Data	
Design Stage	
<input checked="" type="radio"/> Pre-Place <input checked="" type="radio"/> Pre-CTS <input type="radio"/> Post-CTS <input type="radio"/> Post-Route <input type="radio"/> Sign-Off	
Analysis Type	
<input checked="" type="radio"/> Setup <input type="radio"/> Hold	
<input type="checkbox"/> Include SI	
Reporting Options	
Number of Paths: <input type="text" value="50"/>	
Report file(s) Prefix: <input type="text" value="CHIP_preCTS"/>	
Output Directory: <input type="text" value="timingReports"/>	
<input type="button" value="OK"/>	<input type="button" value="Apply"/>
<input type="button" value="Cancel"/>	<input type="button" value="Help"/>

Setup views included:
 av_func_mode_max av_scan_mode_max

Setup mode	all	reg2reg	default
WNS (ns):	1.241	1.241	6.091
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	70	19	54

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	1 (1)	-0.840	1 (1)
max_tran	0 (0)	0.000	0 (0)
max_fanout	27 (27)	-121	28 (28)
max_length	0 (0)	0	0 (0)



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Check Timing (cont.)

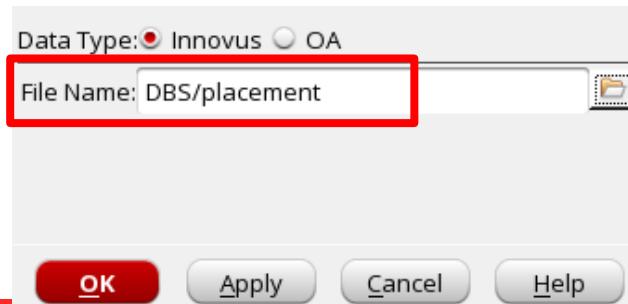
- ECO → Optimize Design

- If WNS is negative or design has violation, try this step



optDesign Final Summary			
Setup views included: av_func_mode_max			
Setup mode	all	reg2reg	default
WNS (ns):	1.069	1.069	6.015
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	70	19	54
<hr/>			
Real			
DRVs	Nr nets(terms)	Worst Vio	Total
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	1 (1)
max_length	0 (0)	0	0 (0)

- Save your design by now.





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Clock tree synthesis

- innovus> create_ccopt_clock_tree_spec -file ccopt.spec

```
innovus 1> create_ccopt_clock_tree_spec -file ccopt.spec
Creating clock tree spec for modes (timing configs): tunc_mode scan_mode
extract_clock_generator_skew_groups=true: create_ccopt_clock_tree_spec will generate skew groups with a name prefix of "_clock_gen" to balance clock generator connected flops with the clock generator they drive.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Ignoring AAE DB Resetting ...
Analyzing clock structure...
Analyzing clock structure done.
Reset timing graph...
Ignoring AAE DB Resetting ...
Reset timing graph done.
Wrote: ccopt.spec
```

- innovus> source ./ccopt.spec

```
innovus 2> source ./ccopt.spec
Extracting original clock gating for clk_p_i...
  clock_tree clk_p_i contains 35 sinks and 0 clock gates.
  Extraction for clk_p_i complete.
Extracting original clock gating for clk_p_i done.
Checking clock tree convergence...
Checking clock tree convergence done.
innovus 2>
```

- innovus> ccopt_design -cts

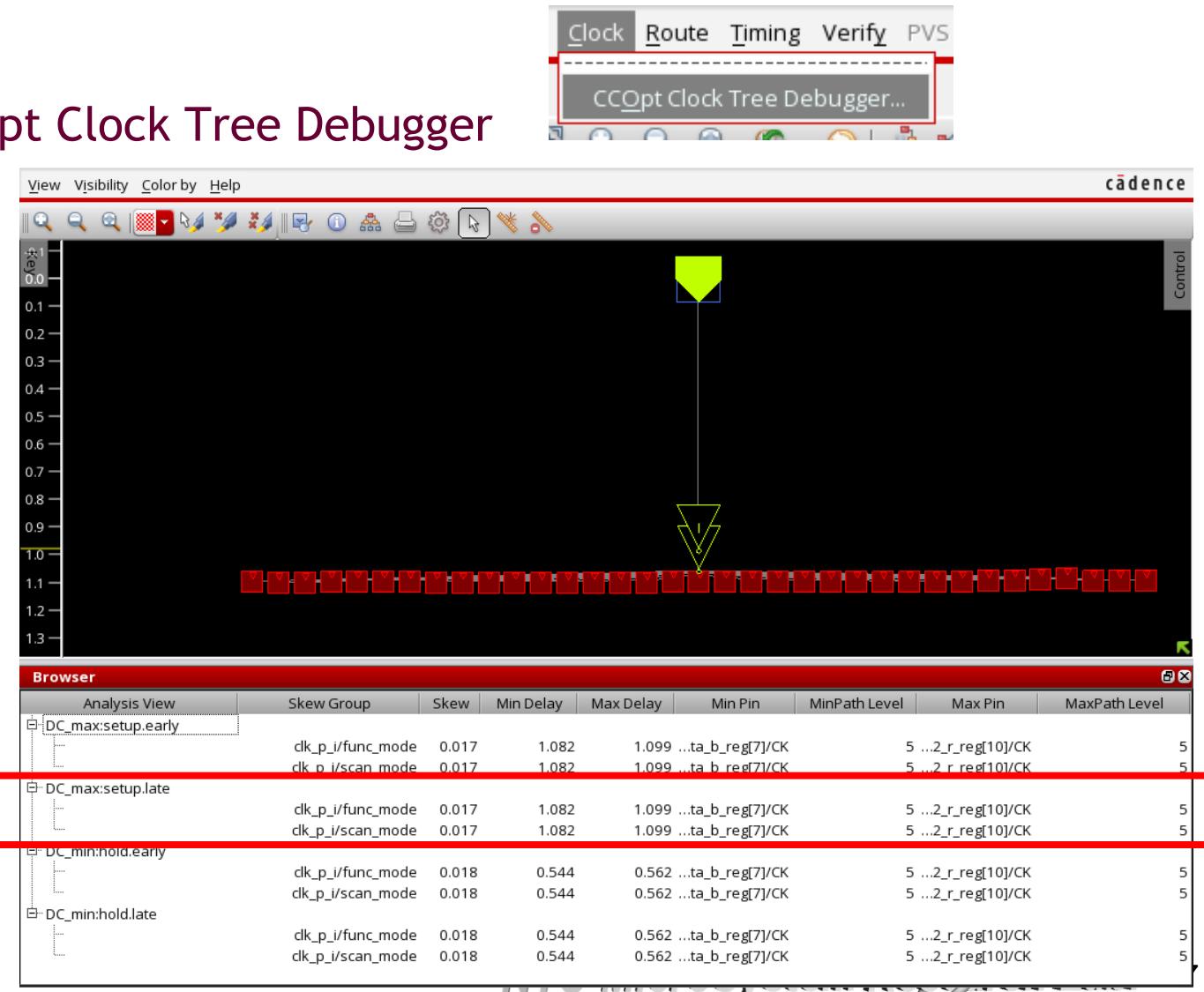


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Clock tree synthesis (cont.)

- Clock → CCOpt Clock Tree Debugger

- Skew
- Min delay
- Max delay

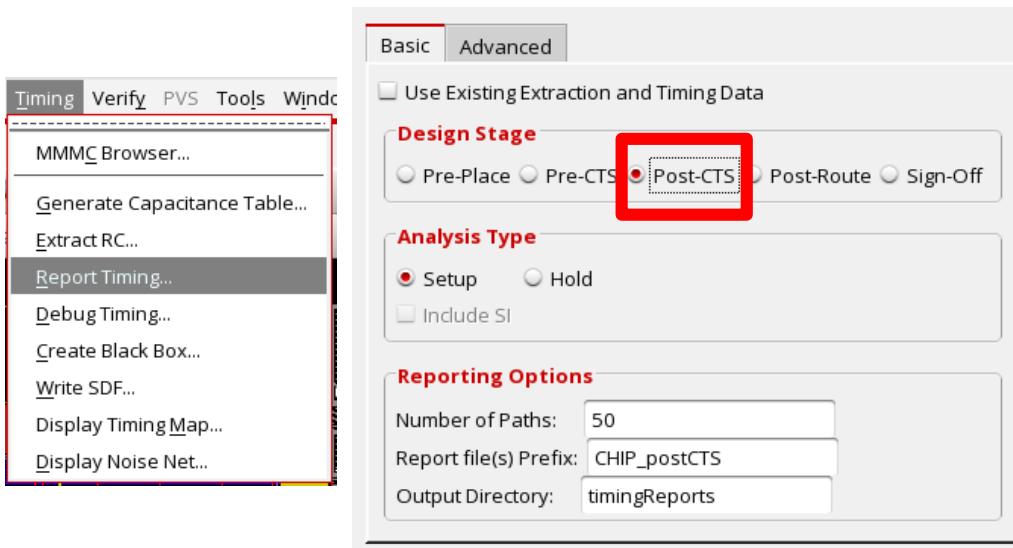




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Clock tree synthesis (cont.)

- Do the timing analysis again.
- Timing → Report Timing
 - Design stage is Post-CTS



timeDesign Summary			
Setup views included: av_func_mode_max			
Setup mode	all	reg2reg	default
WNS (ns):	1.037	1.037	6.012
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	70	19	54

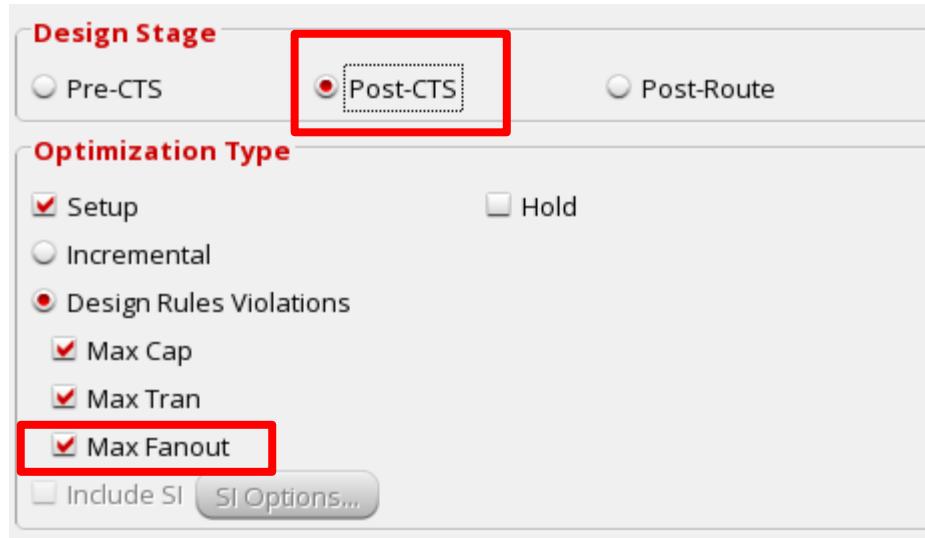
DRVs	Real		Total
	Nr nets(terms)	Worst Vio	
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	1 (1)
max_length	0 (0)	0	0 (0)



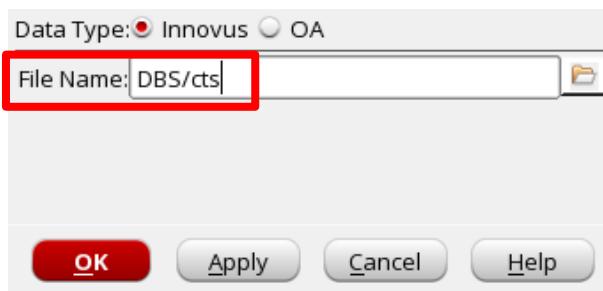
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Clock tree synthesis (cont.)

- ECO → Optimize Design
 - If WNS is negative or design has violation, try this step



- Save your design by now.





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Route

- Route → NanoRoute → Route

Routing Phase

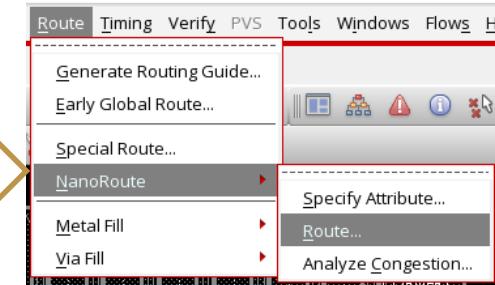
- Global Route
- Detail Route Start Iteration default End Iteration default
- Post Route Optimization Optimize Via Optimize Wire

Concurrent Routing Features

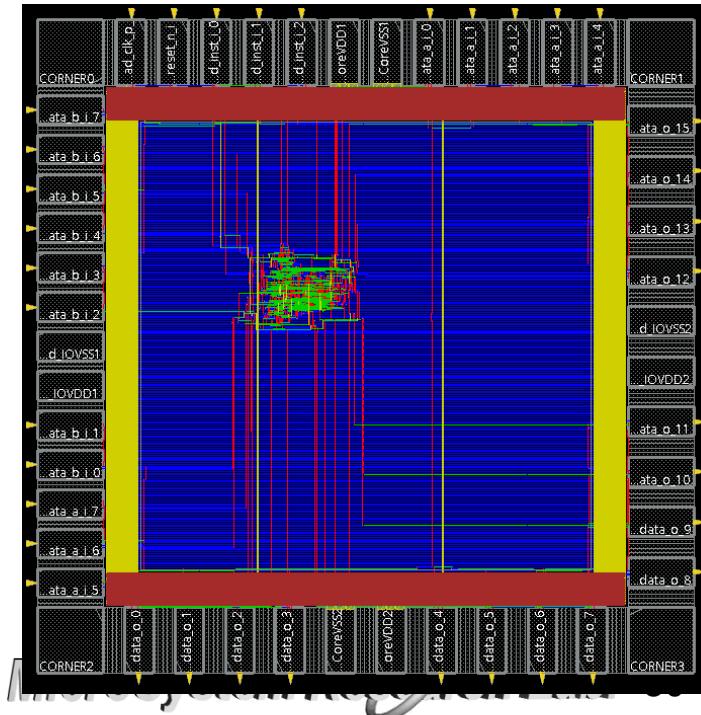
- Fix Antenna
- Insert Diodes Diode Cell Name ANTENNA
- Timing Driven
- SI Driven
- Post Route SI SI Victim File

Effort 5 Congestion Timing S.M.A.R.T.

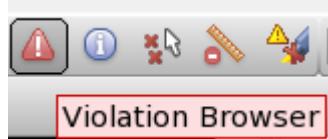
If innovus crashed, then cancel out Timing Driven.



Physical mode



Clear IO filler's
overlap violation.





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Route (cont.)

- Since the restriction of Innovus, we need to set Mode before we do the timing analysis.
 - Innovus > setAnalysisMode -analysisType onChipVariation

```
innovus 4> setAnalysisMode -analysisType onChipVariation
```

- Timing → Report Timing (Check setup and hold)

Basic Advanced

Use Existing Extraction and Timing Data

Design Stage

Pre-Place Pre-CTS Post-CTS Post-Route Sign-Off

Analysis Type

Setup Hold

Include SI

Reporting Options

Number of Paths: 50

Report file(s) Prefix: CHIP_postRoute

Output Directory: timingReports

Setup views included:
av_func_mode_max

Setup mode	all	req2reg	default
WNS (ns):	1.689	1.689	6.591
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	70	19	54

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	1 (1)
max_length	0 (0)	0	0 (0)

timeDesign Summary

Hold views included:
av_func_mode_min av_scan_mode_min

Hold mode	all	reg2reg	default
WNS (ns):	0.211	0.211	1.715
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	35	19	16

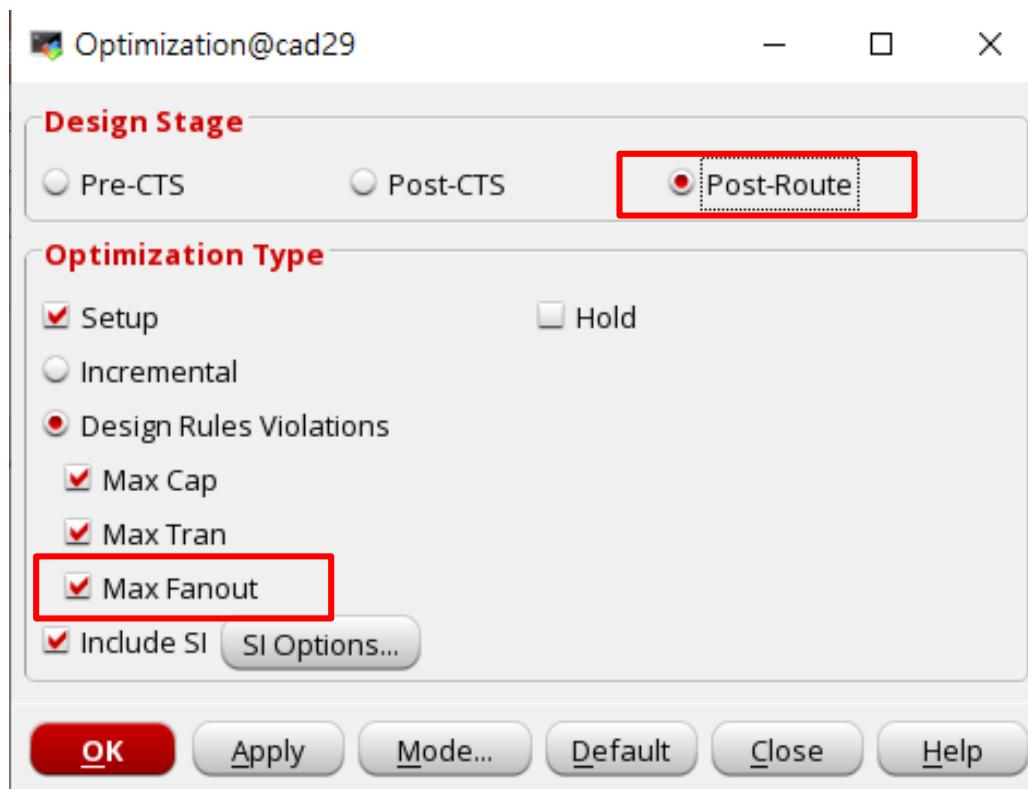


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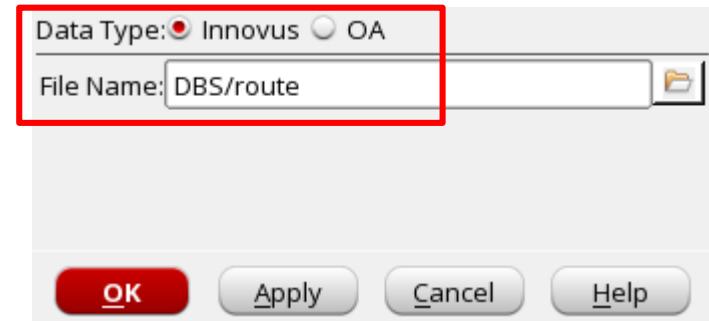
Route (cont.)

- ECO → Optimize Design

- If WNS or max_fanout is negative, try this step



- Save your design by now.

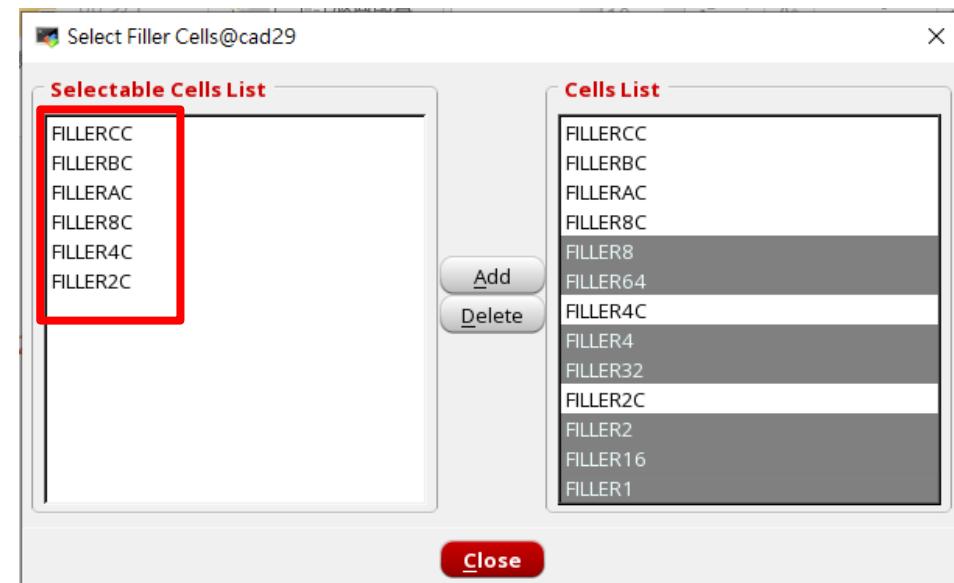
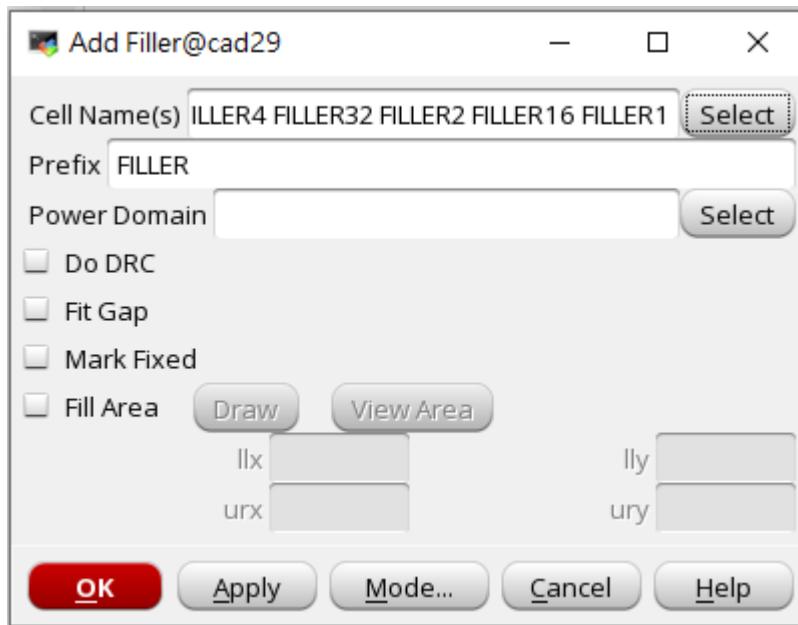
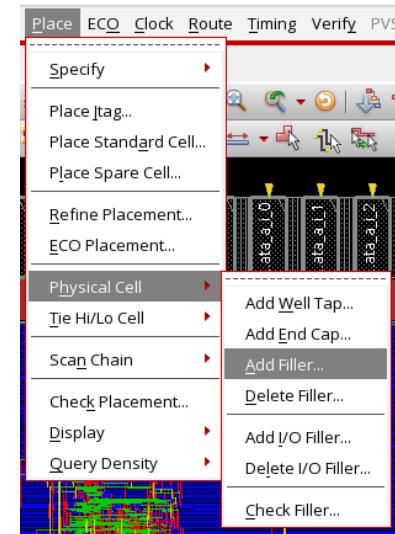




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Add Core Filler

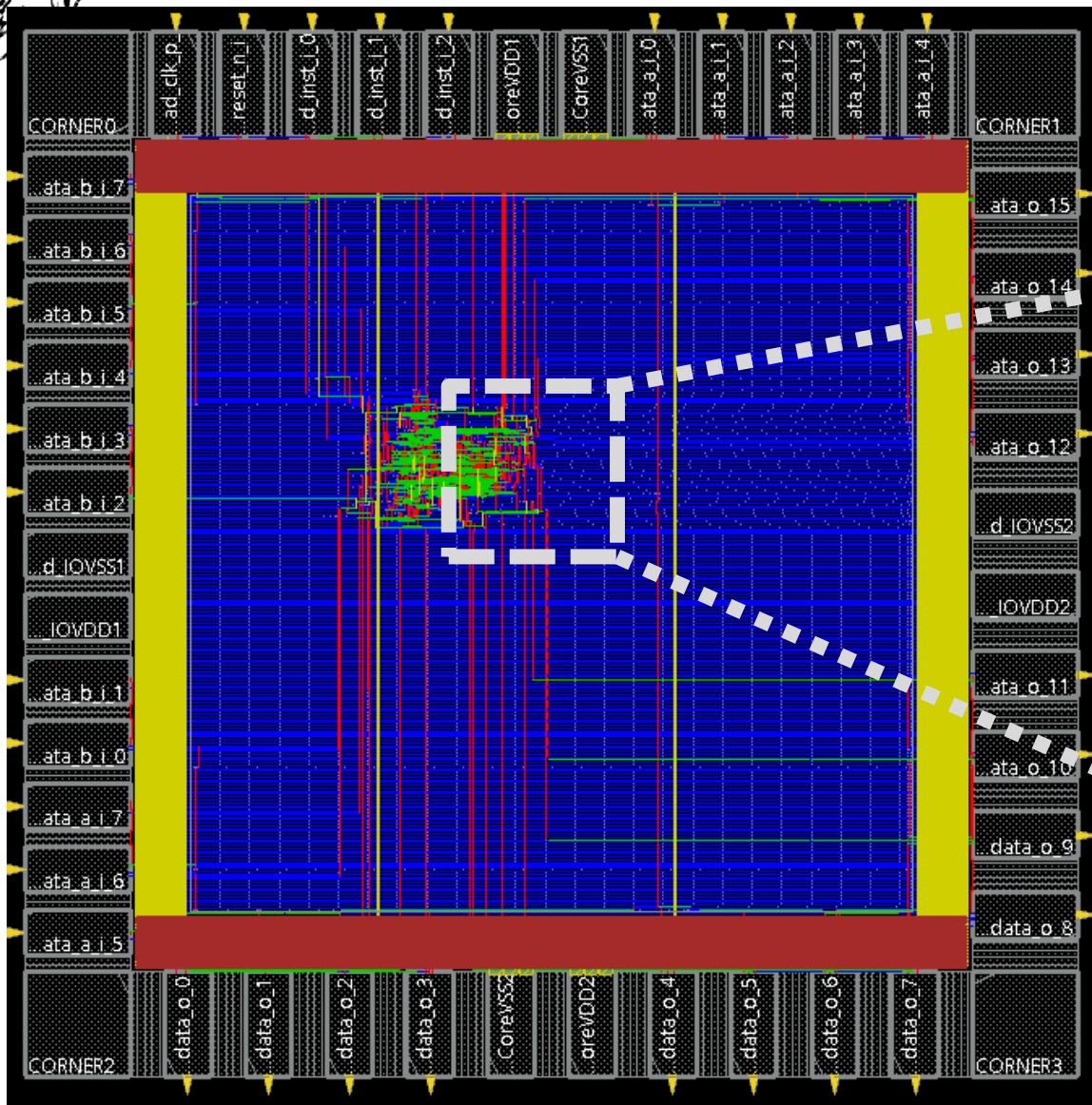
- Place → Physical Cells → Add Filler
- 有C的先載入
 - 載入後如果出現Violation就Edit → Undo，改載入沒有C的





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Add Core Filler (cont.)



FILLER 4336	FILLER 4337	FILLER 4338	FILLER 4339
FILLER 4302	FILLER 4303	FILLER 4305	FILLER 4306
FILLER 4255	FILLER 4260	FILLER 4261	FILLER 4262
FILLER 4223	FILLER 4223	FILLER 4229	FILLER 4230
FILLER 4181	FILLER 4181	FILLER 4191	FILLER 4192
FILLER 4138	FILLER 4138	FILLER 4140	FILLER 4141
FILLER 4101	FILLER 4101	FILLER 4104	FILLER 4105
FILLER 4068	FILLER 4069	FILLER 4070	FILLER 4071
FILLER 3956	FILLER 3957	FILLER 3958	FILLER 3961
FILLER 3936	FILLER 3937	FILLER 3938	FILLER 3924
FILLER 3881	FILLER 3881	FILLER 3884	FILLER 3885
FILLER 3865	FILLER 3865	FILLER 3867	FILLER 3868
FILLER 3822	FILLER 3822	FILLER 3779	FILLER 3776
FILLER 3776	FILLER 3776	FILLER 3726	FILLER 3727
FILLER 3751	FILLER 3751	FILLER 3751	FILLER 3752
FILLER 3711	FILLER 3711	FILLER 3619	FILLER 3620
FILLER 3623	FILLER 3623	FILLER 3622	FILLER 3623
FILLER 3596	FILLER 3596	FILLER 3571	FILLER 3572
FILLER 3559	FILLER 3559	FILLER 3507	FILLER 3508
FILLER 3525	FILLER 3525	FILLER 3504	FILLER 3505
FILLER 3504	FILLER 3504	FILLER 3457	FILLER 3453
FILLER 3482	FILLER 3482	FILLER 3402	FILLER 3403
FILLER 3457	FILLER 3457	FILLER 3402	FILLER 3403
FILLER 3432	FILLER 3432	FILLER 3356	FILLER 3358
FILLER 3407	FILLER 3407	FILLER 3357	FILLER 3358
FILLER 3382	FILLER 3382	FILLER 3296	FILLER 3297
FILLER 3357	FILLER 3357	FILLER 3245	FILLER 3246
FILLER 3332	FILLER 3332	FILLER 3194	FILLER 3195
FILLER 3315	FILLER 3315	FILLER 3136	FILLER 3138
FILLER 3303	FILLER 3303	FILLER 3137	FILLER 3138
FILLER 3043	FILLER 3043	FILLER 3045	FILLER 3046
FILLER 2995	FILLER 2995	FILLER 3001	FILLER 3001
FILLER 2958	FILLER 2958	FILLER 2957	FILLER 2958
FILLER 2911	FILLER 2911	FILLER 2912	FILLER 2913
FILLER 2870	FILLER 2870	FILLER 2871	FILLER 2872
FILLER 2834	FILLER 2834	FILLER 2835	FILLER 2837
FILLER 2800	FILLER 2800	FILLER 2801	FILLER 2801



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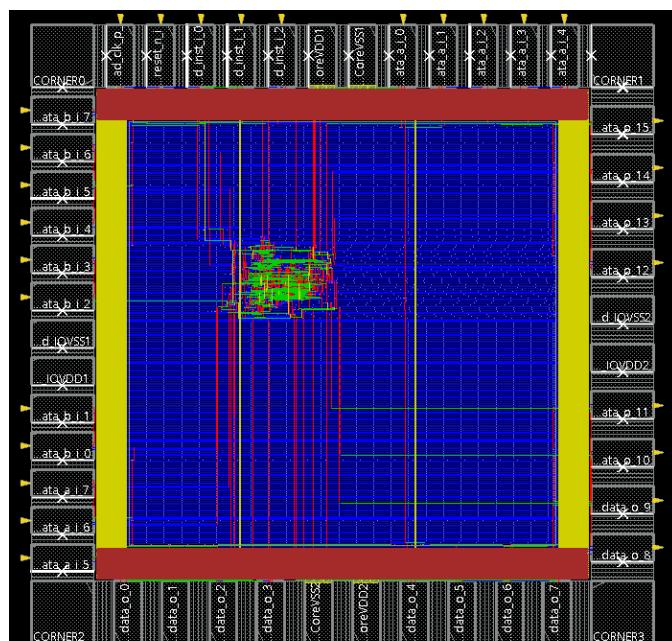
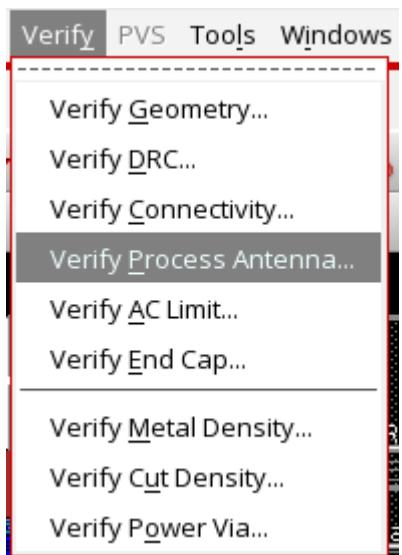
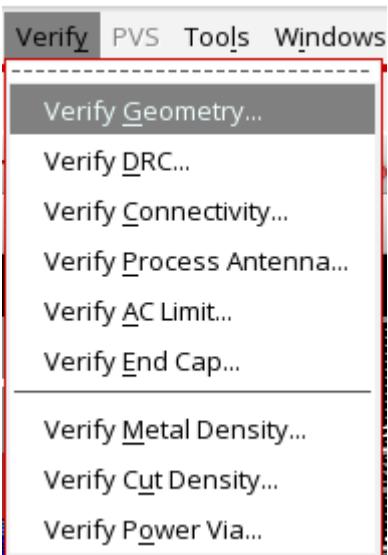
Verify

- Verify → Verify Geometry
- Verify → Verify Process Antenna
- Verify → Verify Connectivity

```
***** START VERIFY ANTENNA *****
Report File: CHIP.antenna.rpt
LEF Macro File: CHIP.antenna.lef
Verification Complete: 0 Violations
***** DONE VERIFY ANTENNA *****
(CPU Time: 0:00:00.0  MEM: 0.000M)

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1411.1200, 1403.4800)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary
```



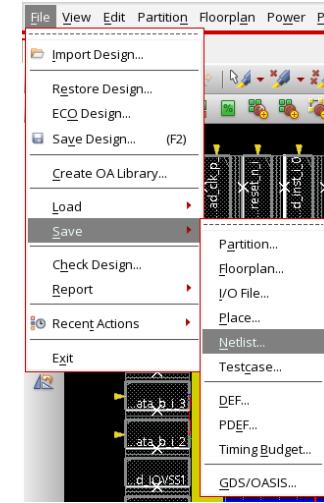
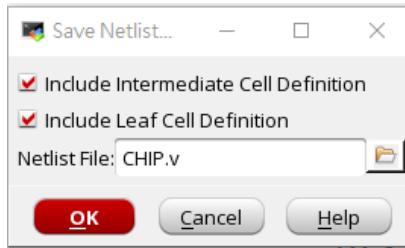
- Save your design by now.
 - DBS/corefiller



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Write .v and .sdf

- File → Save → Netlist..., Netlist File 填 CHIP.v



- innovus > setAnalysisMode -analysisType bcwc
- innovus > write_sdf -max_view av_func_mode_max -min_view av_func_mode_min -edges noedge -splitsetuphold -remashold -splitrecrm -min_period_edges none CHIP.sdf

Posim

- > ncverilog HW3_alu_tb.v CHIP.v -v
fsa0m_a_generic_core_21.lib.src fsa0m_a_t33_generic_io_21.lib.src
+define+SDF



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Add bonding pad

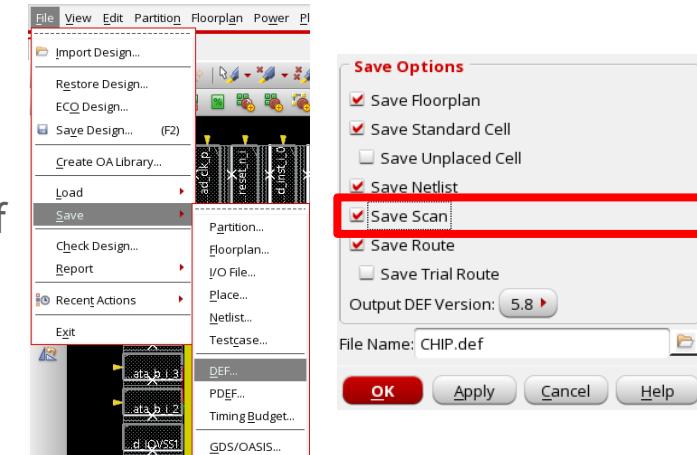
- File → Save → DEF ...
 - Select Save Scan, File Name should be CHIP.def
- In Unix terminal
 - > perl addbonding_v3.8D.pl CHIP.def

```
[r06001@cad29 Lab4_Innovus]$ perl addbonding_v3.8D.pl CHIP.def
===== create SOCE cmd for add bonding pad =====
-- complete, To add bonding cell, execute command below in SOC Encounter terminal
    Encounter> source addbond.cmd

===== create Bonding XY file: CHIP.bondinfo =====
-- complete
===== create SOCE cmd for add routing blockage on IO Pad =====
-- complete, to add blockage, execute command below in SOC Encounter terminal:
    Encounter> source addbond.cmd
```

- In innovus terminal
 - Innovus > source addbond.cmd

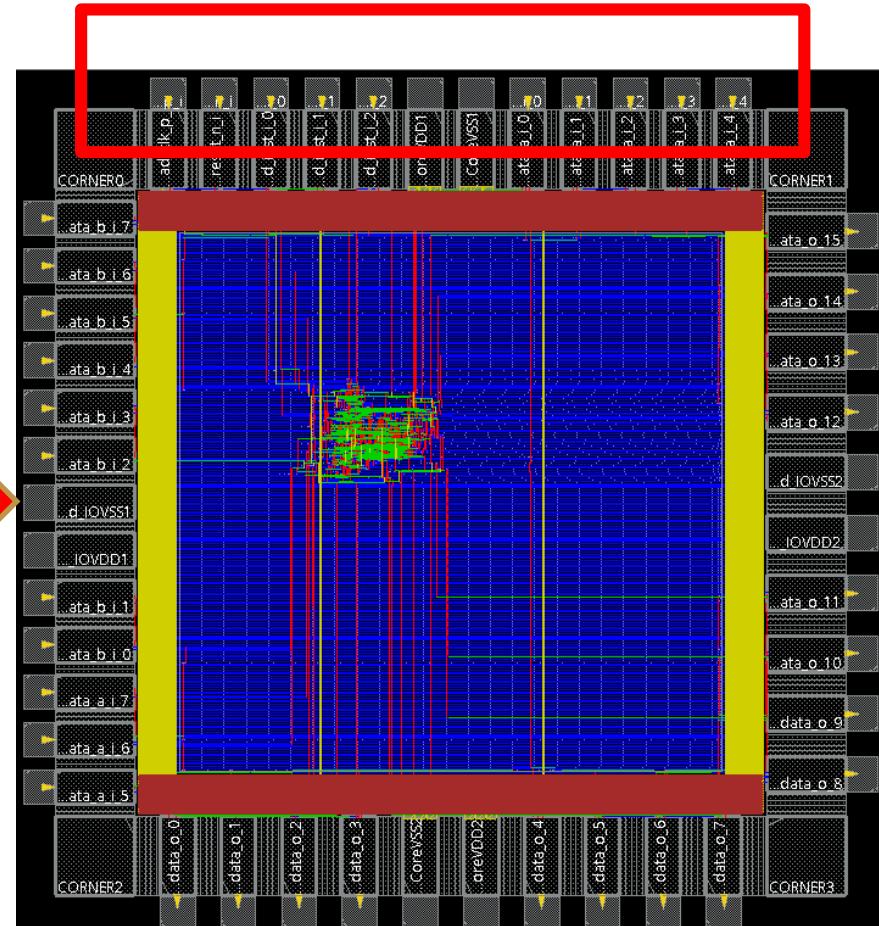
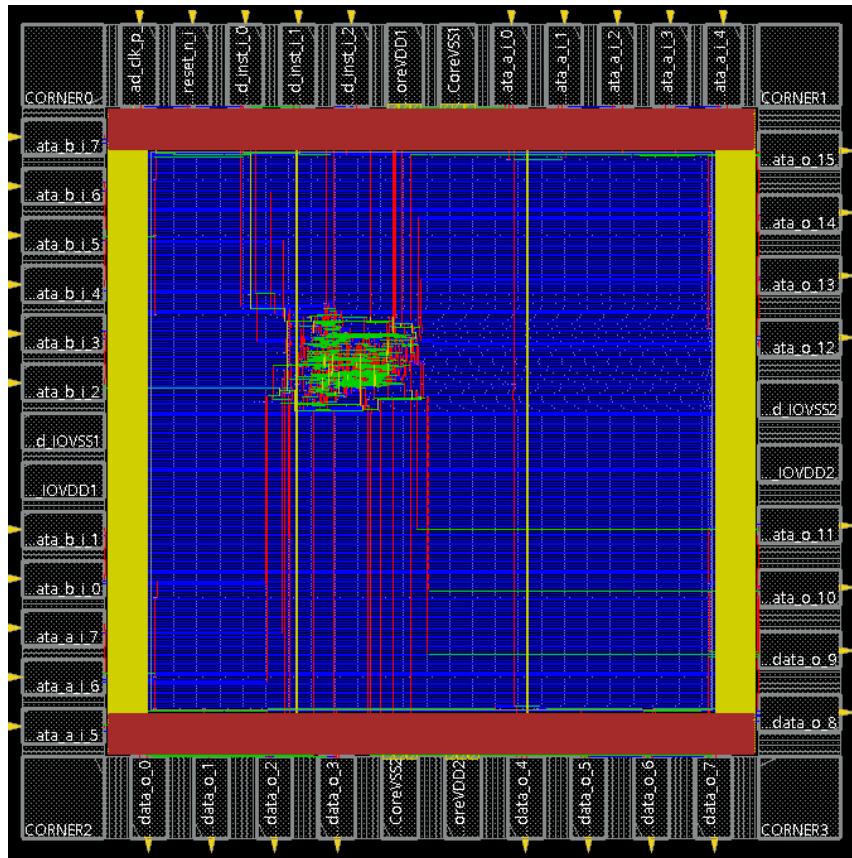
```
innovus 7> source addbond.cmd
```





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Add bonding pad (cont.)





Power label

為了在LVS驗證與posim extraction時可以找到IO power的位置，要在export GDS之間在IO power pad外加上power label，預計輸入的位置在右下角的IO power pad及IO ground pad外的bounding pad上(注意：label一定要打在pad上面才有效)

- Type below commands in innovus

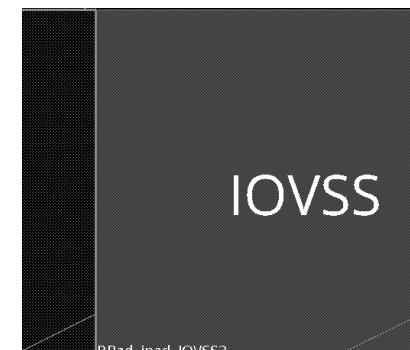
- innovus > add_text -layer metal5 -pt 1435 640 -label IOVDD -height 10

```
innovus 3> add_text -layer metal5 -pt 1435 640 -label IOVDD -height 10
0x7fae0787d7f8
```

- innovus > add_text -layer metal5 -pt 1435 750 -label IOVSS -height 10

```
innovus 4> add_text -layer metal5 -pt 1435 750 -label IOVSS -height 10
0x7fae0787d830
```

- -pt 之後的數值是IO power pad的位置，pad的位置不同會有不一樣的值，同時Layout要放大到很大才看的到，請自行在Layout上確認位置。



- Save your design by now.

- DBS/finish



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Stream out GDS

- innovus > setStreamOutMode -specifyViaName default -SEvianames false -virtualConnection false -uniquifyCellNamesPrefix false -snapToMGrid false -textSize 1 -version 3

```
innovus 5> setStreamOutMode -specifyViaName default -SEvianames false -virtualConnection false -uniquifyCellNamesPrefix false -snapToMGrid false -textSize 1 -version 3
```

- innovus > streamOut CHIP.gds -mapFile streamOut.map -merge {
 ./Phantom/fsa0m_a_generic_core_cic.gds
 ./Phantom/fsa0m_a_t33_generic_io_cic.gds
 ./Phantom/BONDPAD.gds} -stripes 1 -units 1000 -mode ALL

```
innovus 5> streamOut CHIP.gds -mapFile streamOut.map -merge { ./Phantom/fsa0m_a_generic_core_cic.gds ./Phantom/fsa0m_a_t33_generic_io_cic.gds  

.../Phantom/BONDPAD.gds} -stripes 1 -units 1000 -mode ALL  

Finding the highest version number among the merge files  

Merge file: ./Phantom/fsa0m_a_generic_core_cic.gds has version number: 5  

Merge file: ./Phantom/fsa0m_a_t33_generic_io_cic.gds has version number: 5  

Merge file: ./Phantom/BONDPAD.gds has version number: 5
```