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New PICs, New Errata [Update 2]

Posted on **October 31, 2014**

It's been a while since the topic of chip errata has come up. This is due to the fact that things have pretty much settled down for existing PIC32MX parts (See the last update). Now by that I mean that everyone now pretty much codes around these errata on a permanent basis.

Sometime ago, a new series of PIC32MZ parts was announced and these are now starting to become available. What new and exciting features will be available here to power new products and projects? Here's a really brief summary:

- Operation up to 200 MHz with Instruction and Data Caching for up to 330 DMIPS of performance. [No too shabby at all but no speed demon either!]
- Internal memory of up to 2048 KB of flash memory and 512 KB of ram. [YAY!]
- An external 50 MHz memory interface for further external memory.
- A Serial Quad Interface allows this PIC to take advantage of serial flash devices that move four bits at a time rather than the pokey one bit at a time [finally!] An added bonus is that the PIC can actually execute from serial memory using XIP mode! [Don't cheer just yet…]
- An Analog to Digital converter that can operate as high as 500 K Samples per Second. [Ditto.]

That is a lot of text, so here's a cool picture:
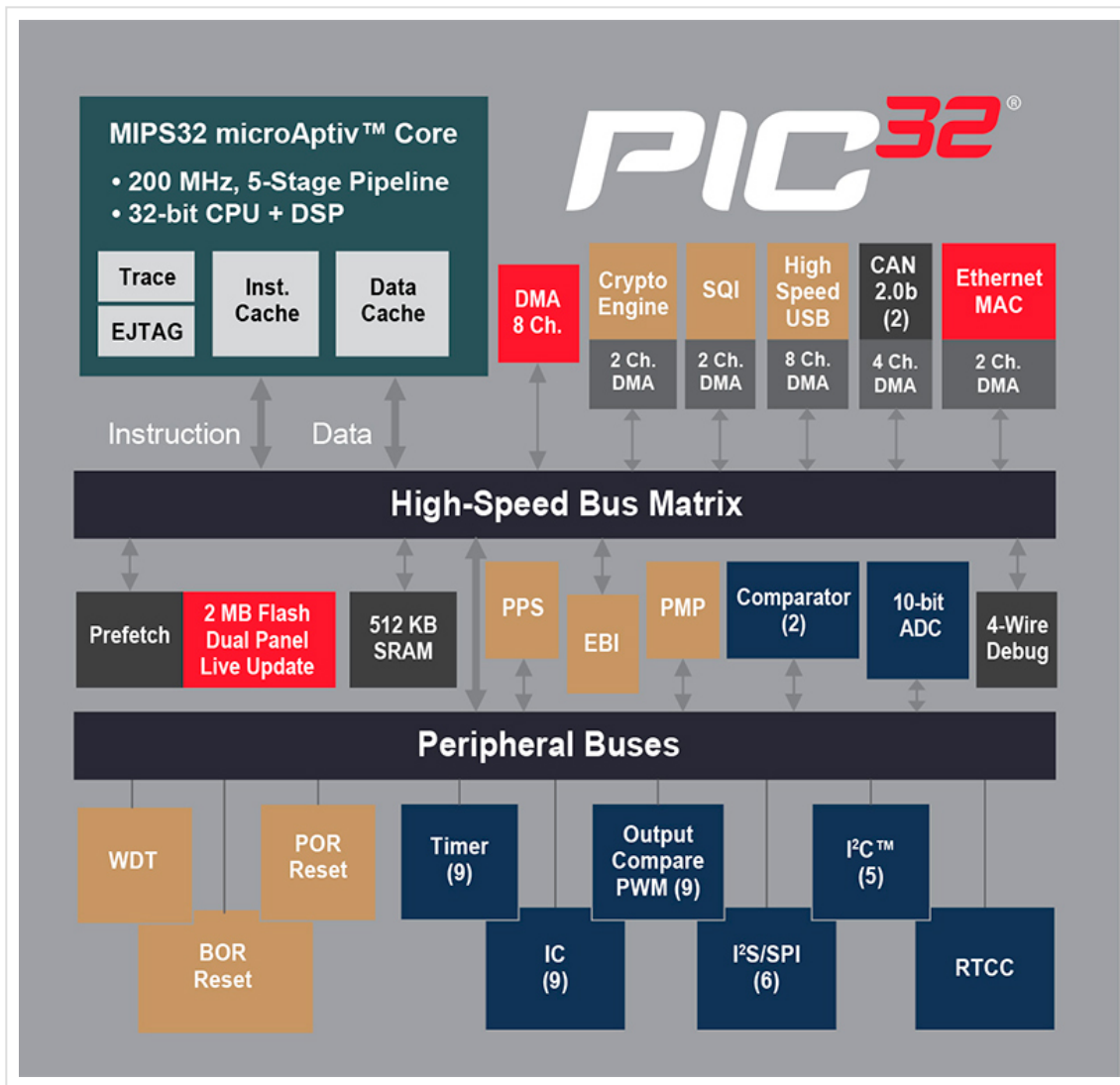
There is a lot of new stuff going on here, so the skeptics and other normal people may be wondering about errata. Well here are the PIC32MZ Family Datasheet 60001191C and the latest PIC32MZ Errata 80000588F.

They ARE pretty dense reading so I'll give a very brief summary of the issues. First some good news. While earlier PICs suffered from serious flaws in the CPU and Flash memory, these new PICs are not repeating those mistakes. This is a HUGE relief. The peripherals however have a few notable gosh-darns. Here are some selected notes:

11. Module: Secondary Oscillator
A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSCI/SOSCO pins).
Work around
Instead, use the external clock. [This is all well and good except that this clock input is usually used for a 32.768 KHz RTC clock and getting battery operation may be more difficult to achieve with an external oscillator]

13. Module: Power-Saving Modes
Dream mode is intended as a feature allowing DMA operation while the CPU is in Idle

mode; however, Dream mode does not function.

Work around

None. [Too bad, this sounds like a great idea.]

15. Module: SPI

The SPI clock speed does not meet the published specification. The maximum supported SPI clock speed is 27 MHz.

Work around

None.. [Bye bye 50 Mhz… On the bright side, 27 MHz should be useful for jamming annoying people who still use CB radio!]

27. Module: Random Number Generator

True RNG mode does not function.

Work around

Instead, use Pseudo-Random Number Generator (PRNG) mode. [I guess the NSA was not happy with the idea of people having *effective* security. PRNGs are easily cracked.]

31. Module: SQI

XIP mode is not operational (MODE<2:0> bits = 011 in the SQI1CFG register).

Work around

Use PIO mode (MODE<2:0> bits = 001) or DMA mode (MODE<2:0> bits = 010). [Sigh… This feature had such promise for code executing out of a pluggable memory device without a lot of extra expenses.]

34. Module: SQI

Clock speed for read operations does not meet the maximum specification (SQ10) of 50 MHz. For read operations the maximum clock is 25 MHz.

Work around

None. [Drat! Now we can't even jam CB radios!]

44. Module: ADC

For Revision A3 and A4 silicon: The ADC module does not meet the published Throughput Rate (AD51) and Full-Scale Input Range (AD12) specifications. The updated Maximum Throughput Rate (AD51) specification is 125 ksps, assuming 16x Oversampling mode. The updated Maximum Full-Scale Input Range is 2.5V for both Differential and Singled-Ended modes. The updated Minimum Full-Scale Input Range is -2.5V for Differential mode.

For Revision A5 and newer silicon: The ADC module does not meet [the] published throughput rate (AD51) and accuracy specifications. More information will be provided in a subsequent October 2014 update of this document.

Work around

None. [So the ADC runs at 1/4 speed but that may change. I'll post an update when I get one.]

OK, so how do these errata compare? Overall, they are pretty light. While it is true that some nifty features are making an exit, on the whole the core is solid and the peripherals are a significant

improvement over any available before. I look forward to working with this new PIC and will write about any interesting things that may come up.

As always, comments and suggestions are most welcome.

Best regards;

Peter Camilleri (aka Squidly Jones)

[**Update Nov 27, 2014**]

It has come to my attention that I've left out at least one important errata. Here it is:

41. Module: Oscillator
A crystal oscillator cannot be used as the input to the Primary Oscillator (OSC1/OSC2 pins).
Work around
Use an external clock or an internal FRC. [I did not see this as a killer bug as I routinely design in both a crystal and an oscillator module (and populate only one part). The modules often perform better and it makes for more options in the final BOM while consuming very little space.]

As usual, check the docs for yourself and you be the judge!

Peter Camilleri (aka Squidly Jones)

[**Update Jan 3, 2015**]
The most recent errata (80000588G) for the PIC32MZ family reveals that the latest revision of silicon can finally use a crystal for its main oscillator. Yay! Mind you there are still some spec issues here, and those errata remain. IMHO those issues are minor compared to not being able to run with a crystal at all. For the most demanding applications though, an external oscillator module may still be the best bet.

Again, check the docs for yourself and you be the judge!

Peter Camilleri (aka Squidly Jones)

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Fabian Romo
on **November 27, 2014 at 12:37 pm** said:

There is an interesting discussion in an unofficial forum MCHP:

http://picforum.ric323.com/viewtopic.php?f=69&t=81

Comments are closed.

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