CONFIDENTIAL

November 21, 2017

240 Student
ECE Consultants, Inc
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Pittsburgh, PA 15213

Esteemed Pong Expert,

I seek knowledge about the behavior of the Pong240. Would you please answer the following questions about the **`sadd2017.asm`** benchmark and your new SADD instruction:

1) Where is the table of numbers stored? Which one is loaded first?

2) Wait, isn't this backwards? When the result is negative, the program loads a positive number. Please explain.

3) Is the timing data dependent? i.e., does it depend on the values being added?

4) How many clock ticks does it take to execute the whole benchmark? You could have the SystemVerilog simulator print this information.

5) Have the simulator print out the information for the following table. How many clock ticks does it take to execute from "ADD R3,R2" to "BRA CKEND" (inclusive) assuming that the BRV is taken? You'll need to add some rows here -- or attach a listing.

CLOCK TICK	R0	R1	R2	R3	IR	PC	MAR	MDR	INSTRUCTION
i									
i+1									
i+2									
i+3									
i+4									
:									
:									

6.) How many Logic Elements does the original processor and memory occupy?

Second week questions:

1.) Now using your new design (week 2) and new benchmark program with the new instruction in it, trace through the execution of the SADD instruction (only). Yes, a bunch of assembly code went away when compared to the original benchmark. Simulate your new SystemVerilog and have it print out the information for this table.

CLOCK TICK	R0	R1	R2	R3	IR	PC	MAR	MDR	INSTRUCTION
i									
i+1									
i+2									
i+3									
i+4									
:									
:									

2) How many clock ticks does it take to run the whole new SADD benchmark?

3) How many Logic Elements does the new processor design and memory occupy?

4) How long (approximately) did it take to synthesize the original design, including place and route?

Sincerely yours,

Mr. Ping

PingsPong, Inc.