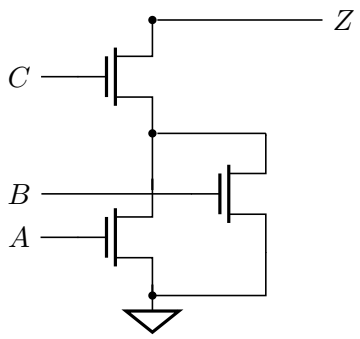
ECEN 2350: Digital Logic

Assignment #3

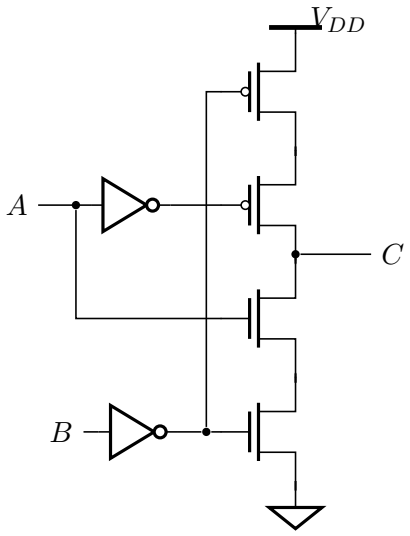
1. [10 points.] Shown below is the pull-down network of a fully complementary CMOS gate.



   (a) Draw the corresponding pull-up network. In other words, you are given the "bottom half" of a CMOS circuit, and you are to draw the "top half".

   (b) What is the function performed by the resulting circuit?

2. [8 points.] Draw the truth table for the following circuit. If the output is High-Z, write **Z**.



A	B	C
0	0	
0	1	
1	0	
1	1	

3. [10 points.] The power dissipated when a capacitance C is charged to V_{DD} and discharged at frequency f is $f \cdot C \cdot V_{DD}^2$. Suppose an inverter drives a load of $50\,\text{fF}$ and its input goes up and down at a frequency of $100\,\text{MHz}$. Suppose also that $V_{DD} = 2\,\text{V}$. What is the power dissipated by this inverter?

4. [10 points.] Given the circuit described by: $d = a \cdot b + b \cdot \bar{c}$, and the logical order of operations (not, and, or):

   (a) Draw the given circuit using AND, OR, and NOT gates

   (b) Draw the given circuit using only NAND and and NOT gates

5. [10 points.] Using De Morgan's Law, translate the following into an equation that only uses AND and NOT: $\overline{x + y \cdot z}$.

   Show these are equivalent using a truth table.