ECEN 2350: Digital Logic

Assignment #7

1. [5 points.] Compute the two's complement of the following binary numbers:

   (a) 0010

   (b) 1101

   (c) 0000

   (d) 0001

   (e) 1111

2. [5 points.] Interpret the following numbers as a signed (two's complement) and unsigned binary number:

	signed	unsigned
0010		
1101		
1111		
0111		
111101		

3. [5 points.] Carry out the following two's complement additions and subtractions. Do not show the carry out of the MSB (i.e. your answer should be 4 bits). For the subractions, add the two's complement of the number to be subtracted (the subtrahend) to the other one (the minuend).

$$\begin{array}{r} 1101\\ +0011\\ \hline \end{array} \qquad \begin{array}{r} 01101\\ +01101\\ \hline \end{array} \qquad \begin{array}{r} 10110\\ +00001\\ \hline \end{array} \qquad \begin{array}{r} 1111\\ +0001\\ \hline \end{array}$$

$$\begin{array}{r} 0101\\ -0101\\ \hline \end{array} \qquad \begin{array}{r} 1011\\ -0010\\ \hline \end{array} \qquad \begin{array}{r} 00101010\\ -00111000\\ \hline \end{array} \qquad \begin{array}{r} 1011\\ -0111\\ \hline \end{array}$$

Check your results by converting the operations to (signed-magnitude) base-10. Note if overflow occurs.

4. [5 points.] Write a verilog module that performs the two's complement on a 4-bit input. You should use the following prototype:

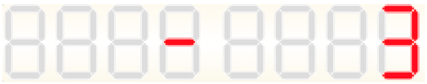
   ```
   module negate(input [3:0] in, output [3:0] out);
   ```

   Turn in your verilog module as `negate.txt`.

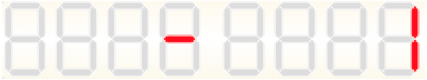
5. [5 points.] Using the Boolean Board, display the 4 right-most switches on the 7-segment hex display as a **signed** number. If the number is a negative number, you should display a negative sign (dash) on the left 7-segment display.

   You may modify your solution from Lab 6, or use the solutions posted to Canvas.

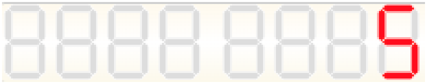
   For instance, if the switches were set to 1101, you should display this as -3:

   A simple check to see if all is working is that all 1s (1111) should be -1:

   Meanwhile, positive (signed) numbers should show their positive representation. E.g. 0101 should display 5:

   Turn in your top-level Verilog file as `lab7-q5.txt`.