2023 DCS Lab 3

Frequency Divider

- Some systems have stable clock sources
  - FPGA
- Need different frequency
  - Use counters

Counter.sv

Input Signal	Bit Width	Definition
clk	1	10 ns Clock
rst_n	1	Asynchronous reset and active-low Clk2 should be 0 after the reset signal is asserted.

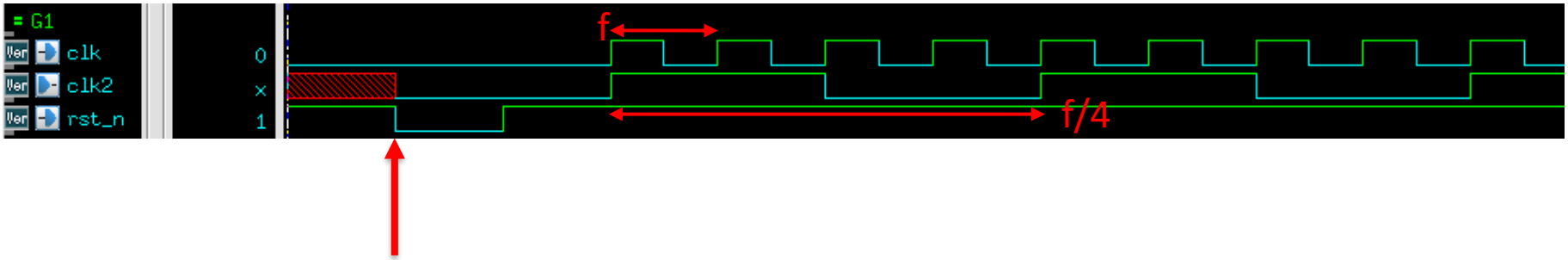
Output Signal	Bit Width	Definition
clk2	1	The frequency of clk2 is clk/4

Specifications

- Top module name：Counter.sv
- Asynchronous and active-low reset.
- All output signals should be reset when reset is asserted.
- Output should be correct within 10 cycles after reset.
- The clock period is 10 ns, and cannot be modified.
- The synthesis result cannot include errors and latches.
- After synthesis, the slack in the timing report should be met.
- Gate-level simulation cannot include any timing violations.
- Separate sequential and combinational blocks.
- For loops are forbidden.

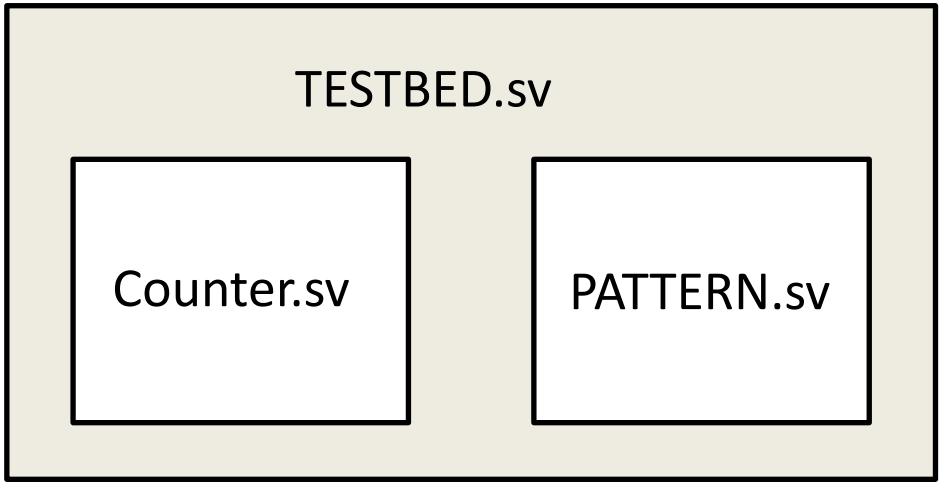
Output & Waveform

- Waveform



Clk2 should be set to 0 at the negative edge of rst_n

Block Diagram



Command

- tar xvf ~dcsta01/Lab03.tar
- Template folders and reference commands:
  - 01_RTL/ (RTL simulation) → **./01_run**
  - 02_SYN/ (RTL synthesis) → **./01_run_dc**
  - 03_GATE/ (GATE simulation) → **./01_run**
  - 09_UPLOAD/ (upload) → **./01_upload**

Grading Policy

- In this lab, pattern is already given.
- Please finish Counter.sv and make sure you pass all 01/02/03 simulations.
- Pass RTL & Synthesis & Gate sim：100%
  - 1 failure will lead to all credit lost.

- DEMO1：3/16 16:20:00 (100%)
- DEMO2：3/16 23:59:59 (70%)