Lab01 Binary-Coded Decimal(BCD)

Inputs

- There is only 1 input, and the value is from 0 to 511.

Outputs

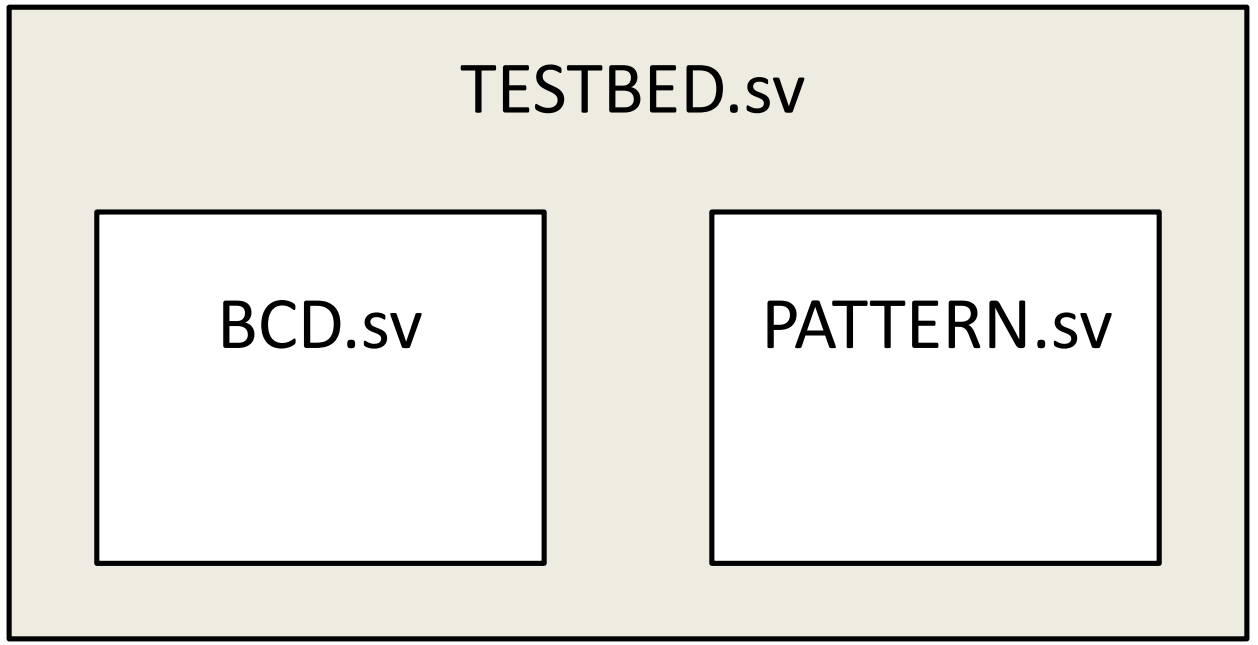
- Three outputs out_hundred [2:0], out_ten[3:0], out_unit[3:0] represent hundreds, tens, and units digit of input signal

- When input signal is given, outputs should change at the same cycle

Specifications

Top module name	BCD (File name : BCD.sv)
Input pins	in_bin [8:0]
Output pins	out_hundred [2:0]
	out_ten [3:0]
	out_unit [3:0]

Block Diagram

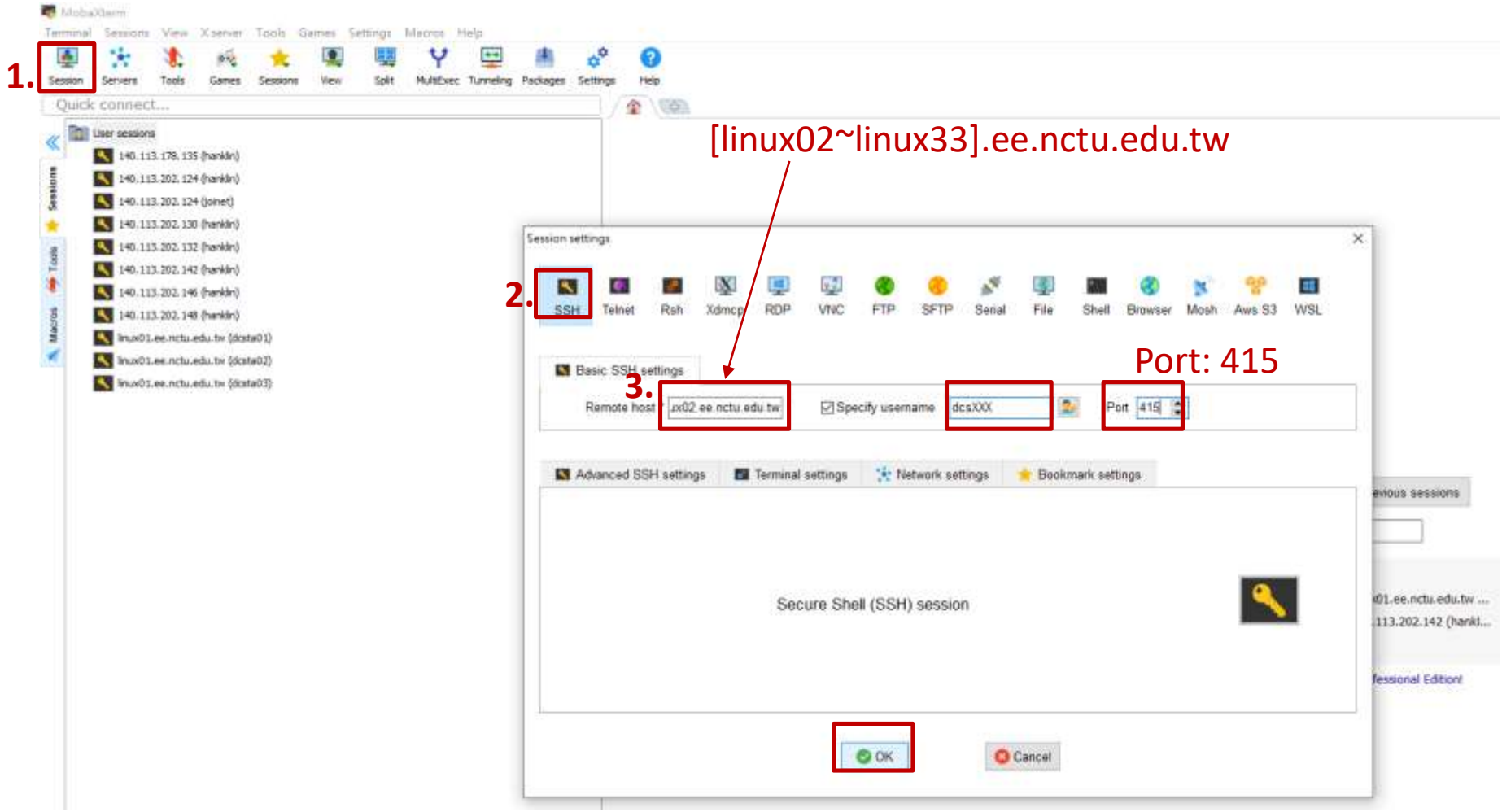


Directory

- 00_TESTBED
  - TESTBED.sv
  - PATTERN.sv
- 01_RTL
  - 01_run
  - 09_clean_up
  - BCD.sv
- 02_SYN
  - 01_run_dc
  - 09_clean_up
- 03_GATE
  - 01_run
  - 09_clean_up
- 09_UPLOAD
  - 01_upload
  - 02_download

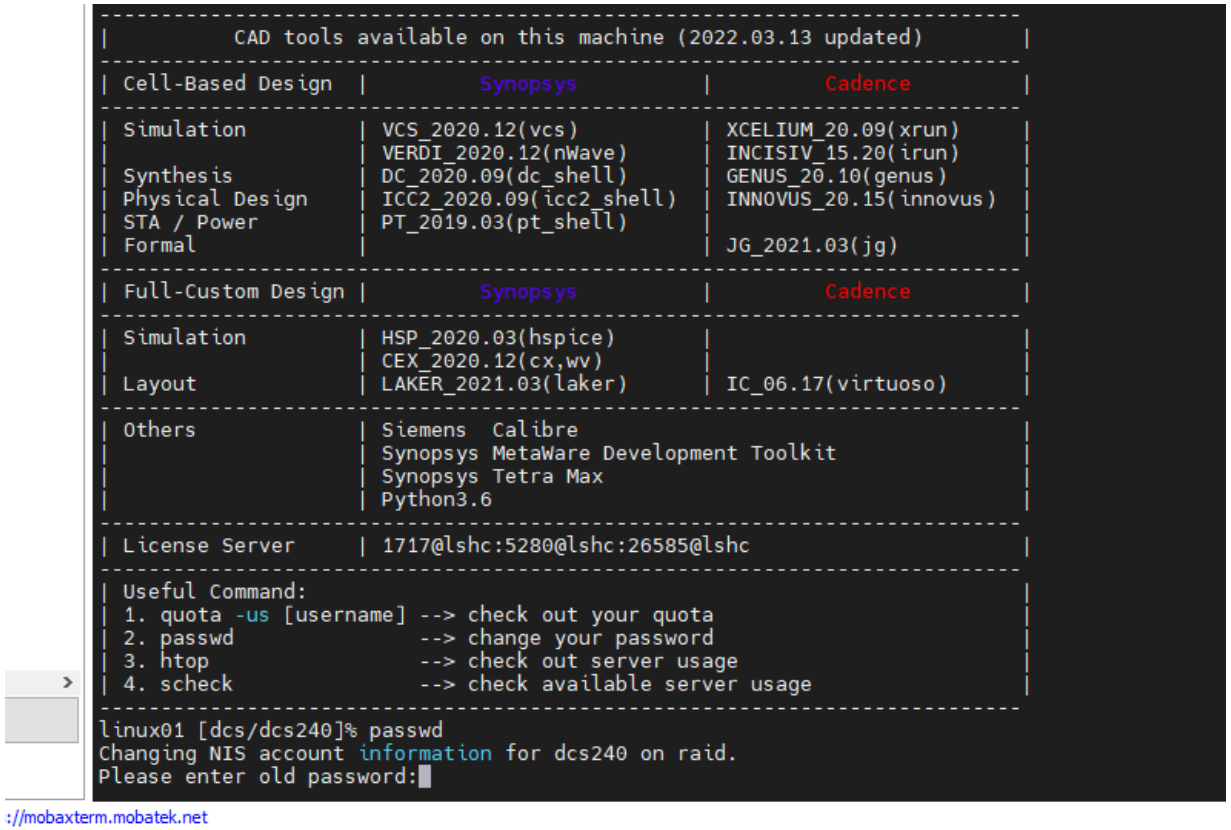
MobaXterm

- Create New Session



Change Password

- Default password: dcs
- Change password: passwd

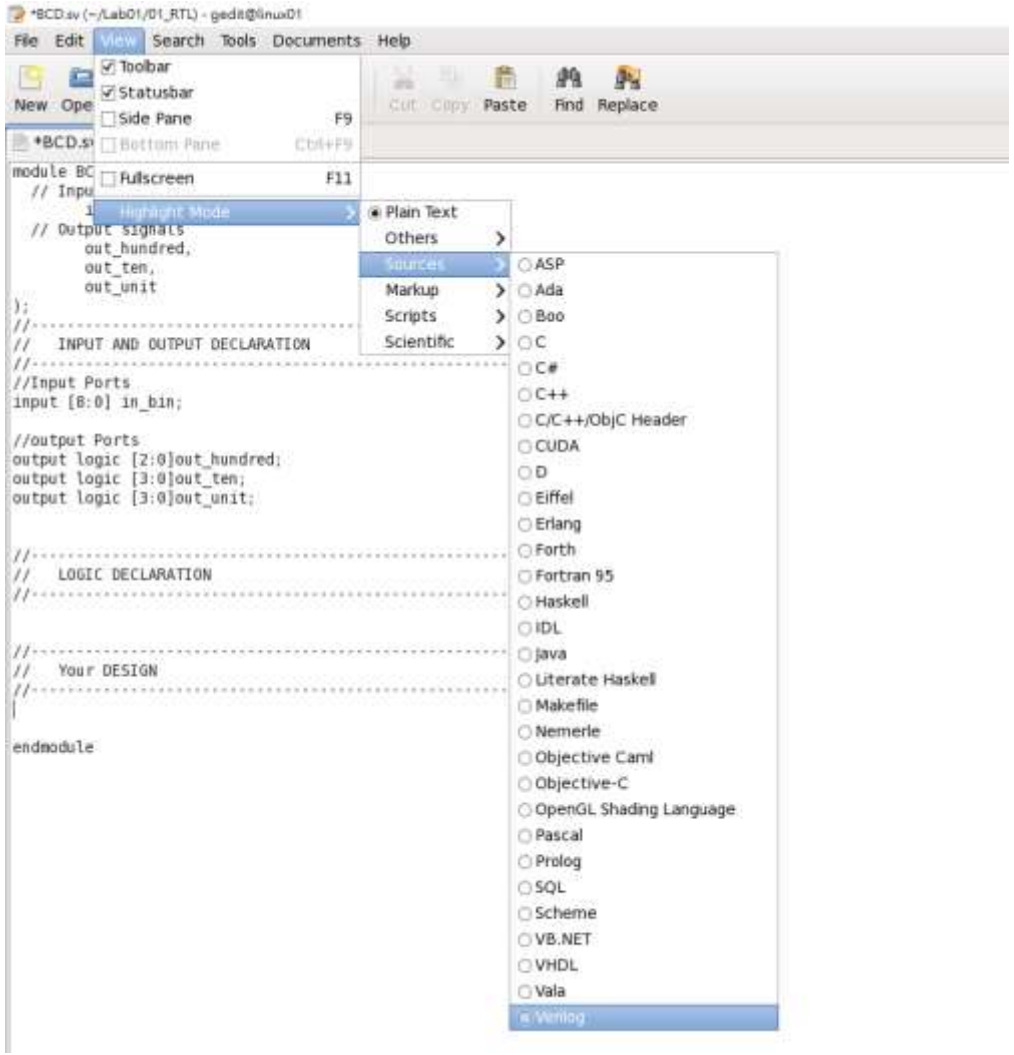


Command

- tar -xvf ~dcsta01/Lab01.tar
- cd Lab01/01_RTL/

- vim BCD.sv (text editor)
  - i (輸入模式)
  - [Esc] (退回普通模式)
  - :w (儲存)
  - :q (結束)
- gedit BCD.sv (text editor)
  - view →Highlight Mode →Sources→Verilog
  - If you use Windows/MacOS, you can use Notepad++, or any editors you are used to using.

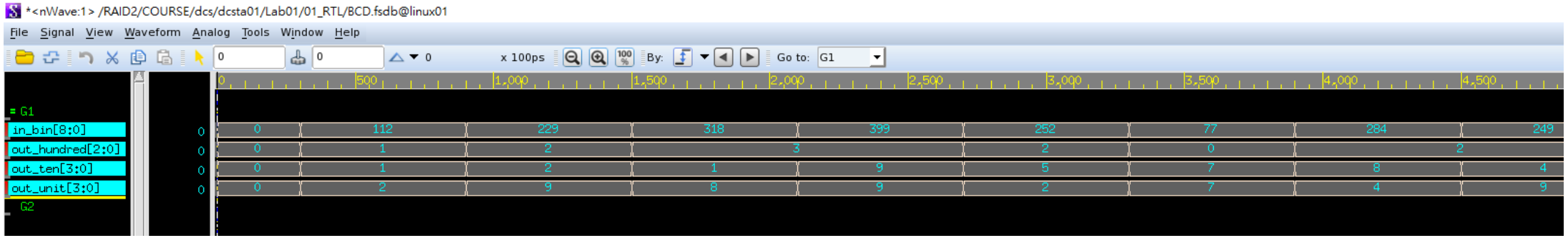
gedit


*BCD.sv (~/Lab01/01_RTL) - gedit@linux01
File Edit View Search Tools Documents Help
Toolbar
Statusbar
Side Pane F9
Bottom Pane Ctrl+F9
Fullscreen F11
Highlight Mode
New Ope
Cut Copy Paste Find Replace
*BCD.sv
module BC
// Inpu
// Output signals
out_hundred,
out_ten,
out_unit
);
//----------
// INPUT AND OUTPUT DECLARATION
//----------
//Input Ports
input [8:0] in_bin;
//output Ports
output logic [2:0]out_hundred;
output logic [3:0]out_ten;
output logic [3:0]out_unit;
//----------
// LOGIC DECLARATION
//----------
//----------
// Your DESIGN
//----------
endmodule
Plain Text
Others
Sources
Markup
Scripts
Scientific
ASP
Ada
Boo
C
C#
C++
C/C++/ObjC Header
CUDA
D
Eiffel
Erlang
Forth
Fortran 95
Haskell
IDL
Java
Literate Haskell
Makefile
Nemerle
Objective Caml
Objective-C
OpenGL Shading Language
Pascal
Prolog
SQL
Scheme
VB.NET
VHDL
Vala
Verilog

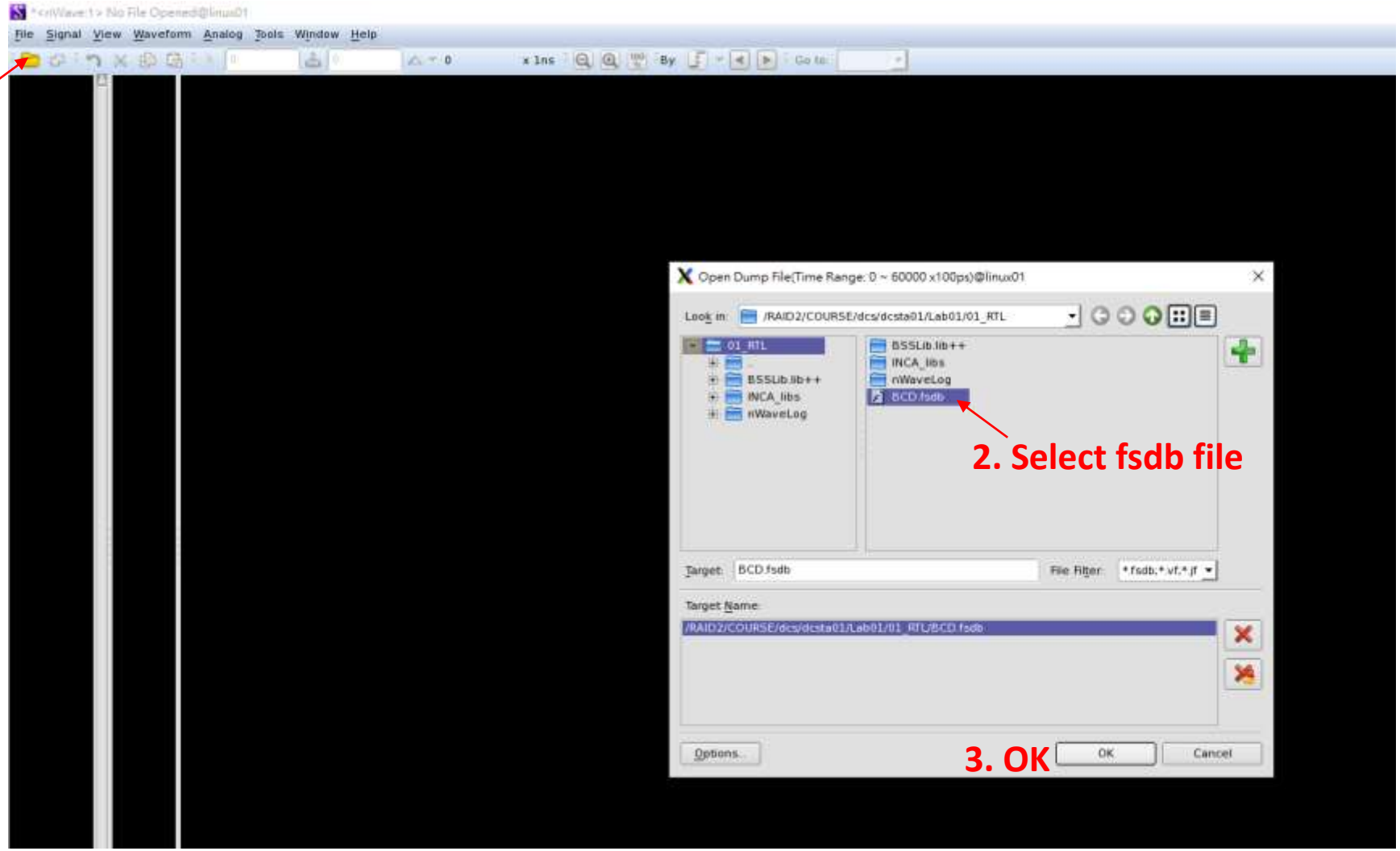
RTL simulation

- cd Lab01/01_RTL/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波型

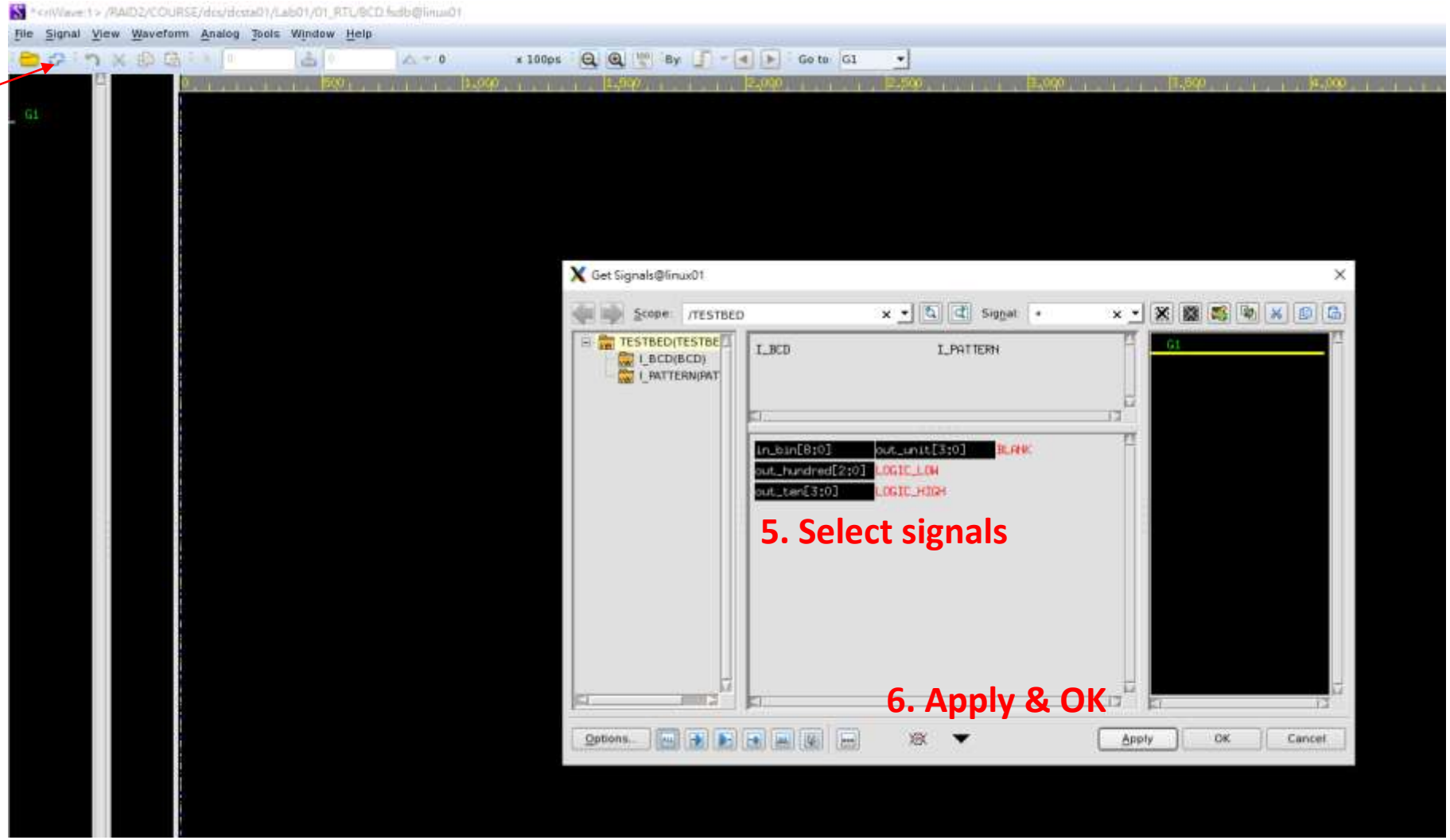
```
-------------------------------------------------------------------------------
| License Server     | 1717@lshc:5280@lshc:26585@lshc                         |
-------------------------------------------------------------------------------
| Useful Command:                                                             |
| 1. quota -us [username] --> check out your quota                            |
| 2. passwd               --> change your password                            |
| 3. htop                 --> check out server usage                          |
| 4. scheck               --> check available server usage                    |
-------------------------------------------------------------------------------
linux02 [dcs/dcs240]% cd Lab01/01_RTL/
linux02 [Lab01/01_RTL]% ./01_run
```



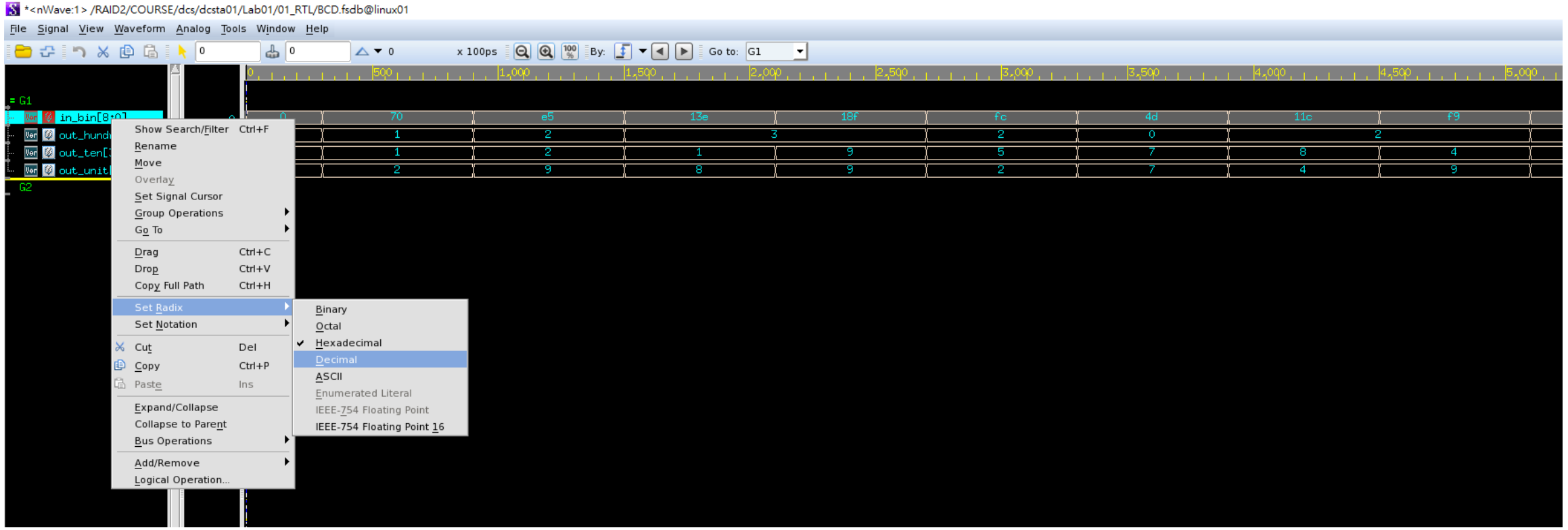
nWave


File Signal View Waveform Analog Tools Window Help
1. file
Open Dump File(Time Range: 0 ~ 60000 x100ps)@linux01
Look in: /RAID2/COURSE/dcs/dcsta01/Lab01/01_RTL
01_RTL
BSSLib.lib++
INCA_libs
nWaveLog
BCD.fsdb
2. Select fsdb file
Target: BCD.fsdb
File Filter: *.fsdb,*.vf,*.jf
Target Name:
/RAID2/COURSE/dcs/dcsta01/Lab01/01_RTL/BCD.fsdb
Options...
3. OK
OK
Cancel

nWave


4. signal
File Signal View Waveform Analog Tools Window Help
Get Signals@linux01
Scope: /TESTBED
Signal:
TESTBED(TESTBE
I_BCD(BCD)
I_PATTERN(PAT
I_BCD
I_PATTERN
in_bin[8:0]
out_unit[3:0]
BLANK
out_hundred[2:0]
LOGIC_LOW
out_ten[3:0]
LOGIC_HIGH
5. Select signals
6. Apply & OK
Options...
Apply
OK
Cancel

nWave (change radix)



Synthesis

- cd ../02_SYN/
- ./01_run_dc (**合成電路**)
- ./09_clean_up (**清除合成結果**)
  - **合成結果**: (**不能有**Error、 **要有**Area report、Timing report slack met、**不能有**Latch)

```
Number of ports:                           20
Number of nets:                           103
Number of cells:                           94
Number of combinational cells:             94
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         22
Number of references:                      22

Combinational area:               1333.886419
Buf/Inv area:                      222.868808
Noncombinational area:               0.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  1333.886419
Total area:                 undefined
```

Synthesis

- 合成的timing report中的 slack必須≧0 (MET)
- 如果出現timing violation → Demo Fail ! (slack < 0)

Point	Incr	Path
input external delay	0.00	0.00 f
in_bin[6] (in)	0.00	0.00 f
U36/Y (AOI2BB1XL)	0.29	0.29 f
U53/Y (INVXL)	0.21	0.50 r
U37/Y (AOI22XL)	0.23	0.73 f
U76/Y (AOI221XL)	0.51	1.24 r
U73/Y (INVXL)	0.15	1.39 f
U28/Y (NAND2XL)	0.14	1.53 r
U27/Y (OAI2BB1XL)	0.10	1.63 f
U8/Y (NOR2XL)	0.17	1.80 r
U18/Y (NOR2X1)	0.07	1.87 f
U17/Y (NOR2X1)	0.21	2.08 r
U40/Y (INVXL)	0.12	2.20 f
U26/Y (MXI2XL)	0.25	2.45 r
U39/Y (NAND2XL)	0.10	2.55 f
U38/Y (AOI21XL)	0.52	3.07 r
U51/Y (MXI2XL)	0.39	3.45 f
U11/Y (NOR2XL)	0.24	3.69 r
U15/Y (NOR2X1)	0.11	3.80 f
U52/Y (OR2XL)	0.32	4.12 f
U49/Y (NAND2XL)	0.14	4.27 r
U67/Y (OAI2BB1XL)	0.20	4.47 r
U66/Y (OAI2BB2XL)	0.20	4.68 r
U48/Y (INVXL)	0.13	4.81 f
U46/Y (OR2XL)	0.28	5.09 f
U96/Y (OAI2BB2XL)	0.19	5.28 f
out_unit[2] (out)	0.00	5.28 f
data arrival time		5.28
max_delay	12.00	12.00
output external delay	0.00	12.00
data required time		12.00
data required time		12.00
data arrival time		-5.28
slack (MET)		6.72

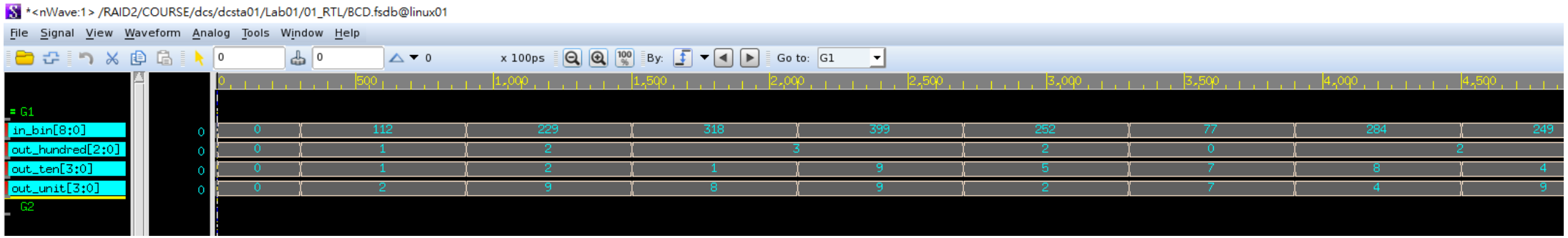
Synthesis

- 記得檢查是否合成出Latch和error
  - 可以在syn.log用ctrl+F尋找關鍵字Latch、error
- 如果出現Latch 、error → Demo Fail

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
out_num2_reg	Latch	6	Y	N	N	N	-	-	-

Gate-level simulation

- cd Lab01/03_GATE/
- ./01_run (電路模擬)
- ./09_clean_up (清除波型檔)
- nWave & (看波型)
  - 範例波型



Grading policy

- Pass the RTL & Synthesis & Gate-level simulation: 100%
  - 合成結果: (不能有Error、 Timing report slack met、不能有Latch)

- Demo2 打7折

Upload

- cd ../09_UPLOAD/
- ./01_upload (**上傳**code)
- ./02_download [argument] (**下載上傳結果**)
  - [argument] = demo1 or demo2
  - **檢查是否上傳成功&正確**
- Demo1: 3/3, 23:59:59，Demo2: 3/10, 23:59:59

Facebook社團

- We establish a discussion club for all students
- You can join this club to ask questions and discuss with classmates

- The following is the link of FB club:
  www.facebook.com/groups/641166254678986/