

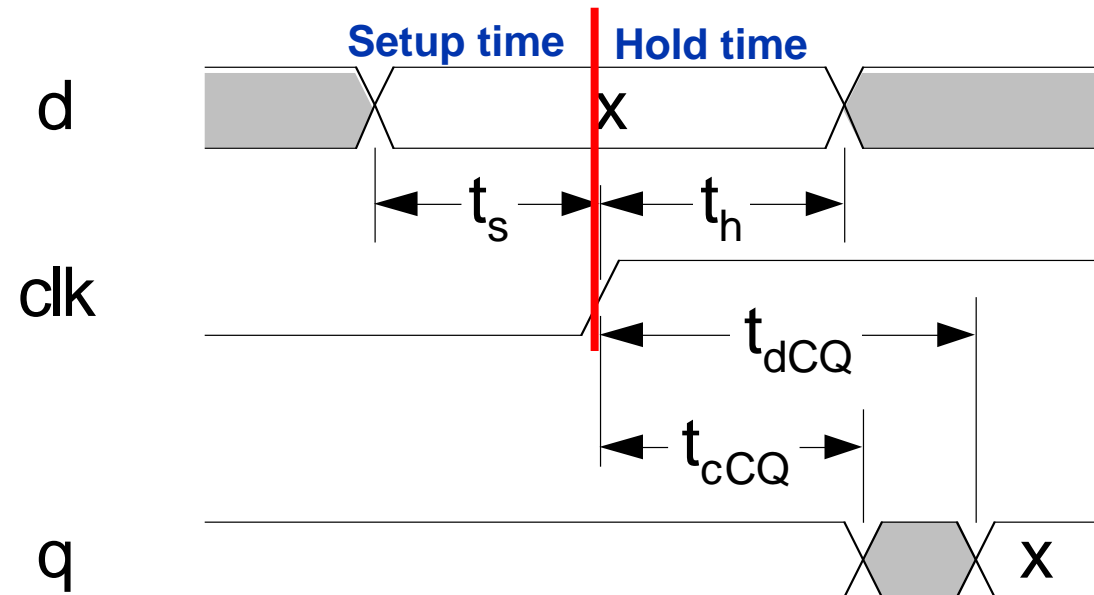
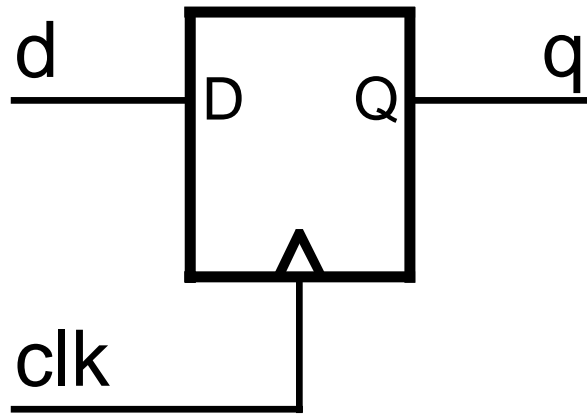
Lecture 3-2 Timing

Outlines

- Timing definition
- How to read a timing report

SOME DEFINITIONS

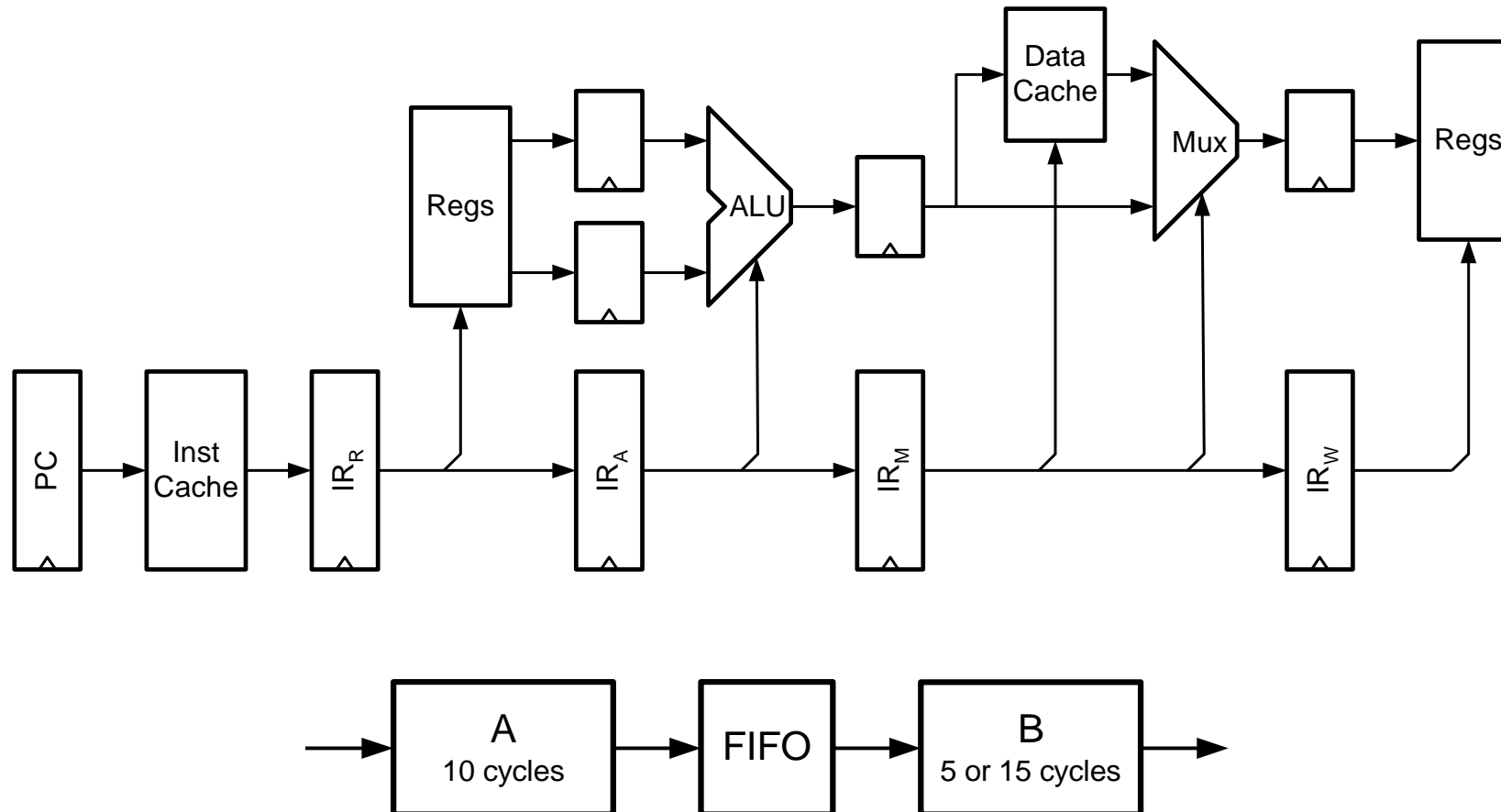
Edge-Triggered D Flip Flop



Setup time: inputs become stable before rising clock;
Hold time: inputs remain stable after rising clock;

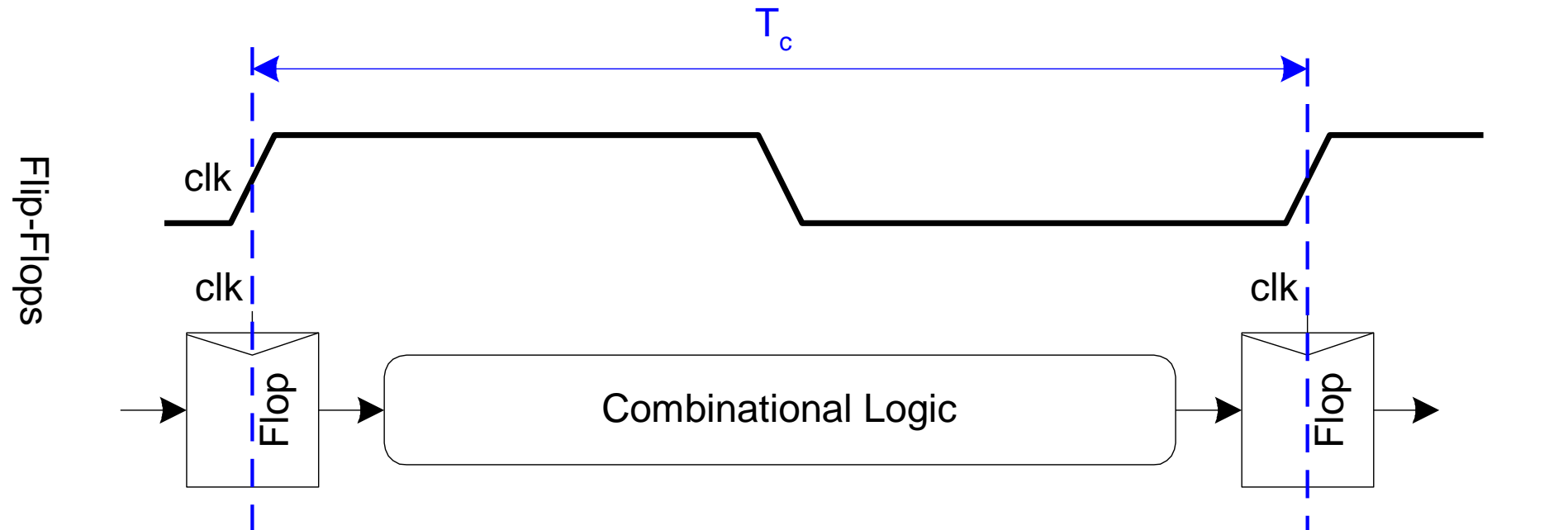
How Fast My Design Can Run?

- Up to 100MHz? 200MHz?
- Slower at 10KHz, 20KHz? Any speed?

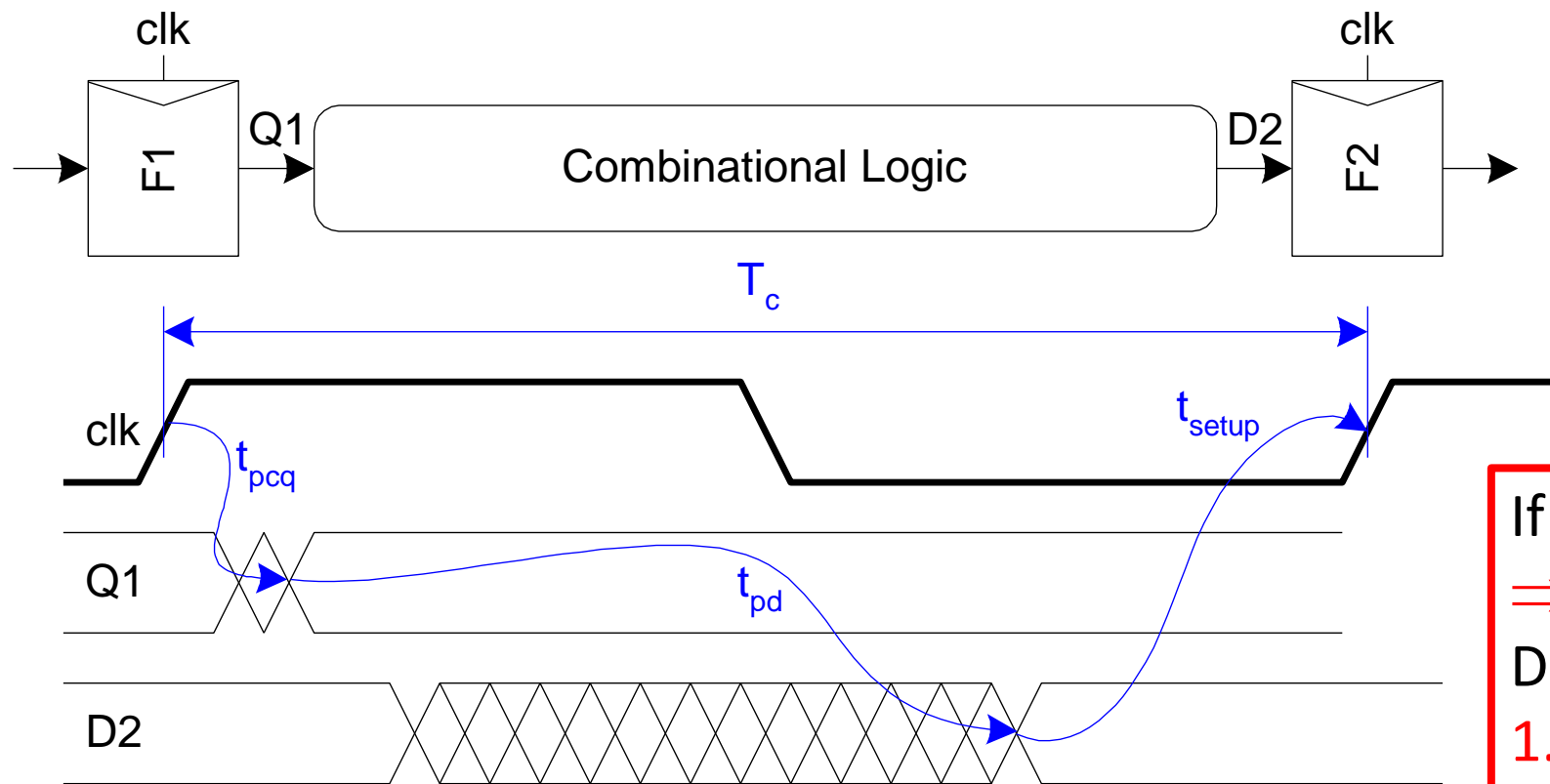


How Fast My Design Can Run?

- Fastest clock cycle time: T_c



Max Delay



$$T_c \geq t_{pcq} + t_{pd} + t_{setup}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup})$$

Register overhead

If delay of comb. Logic is too long)

⇒ Setup time violation

DFF will catch the wrong value

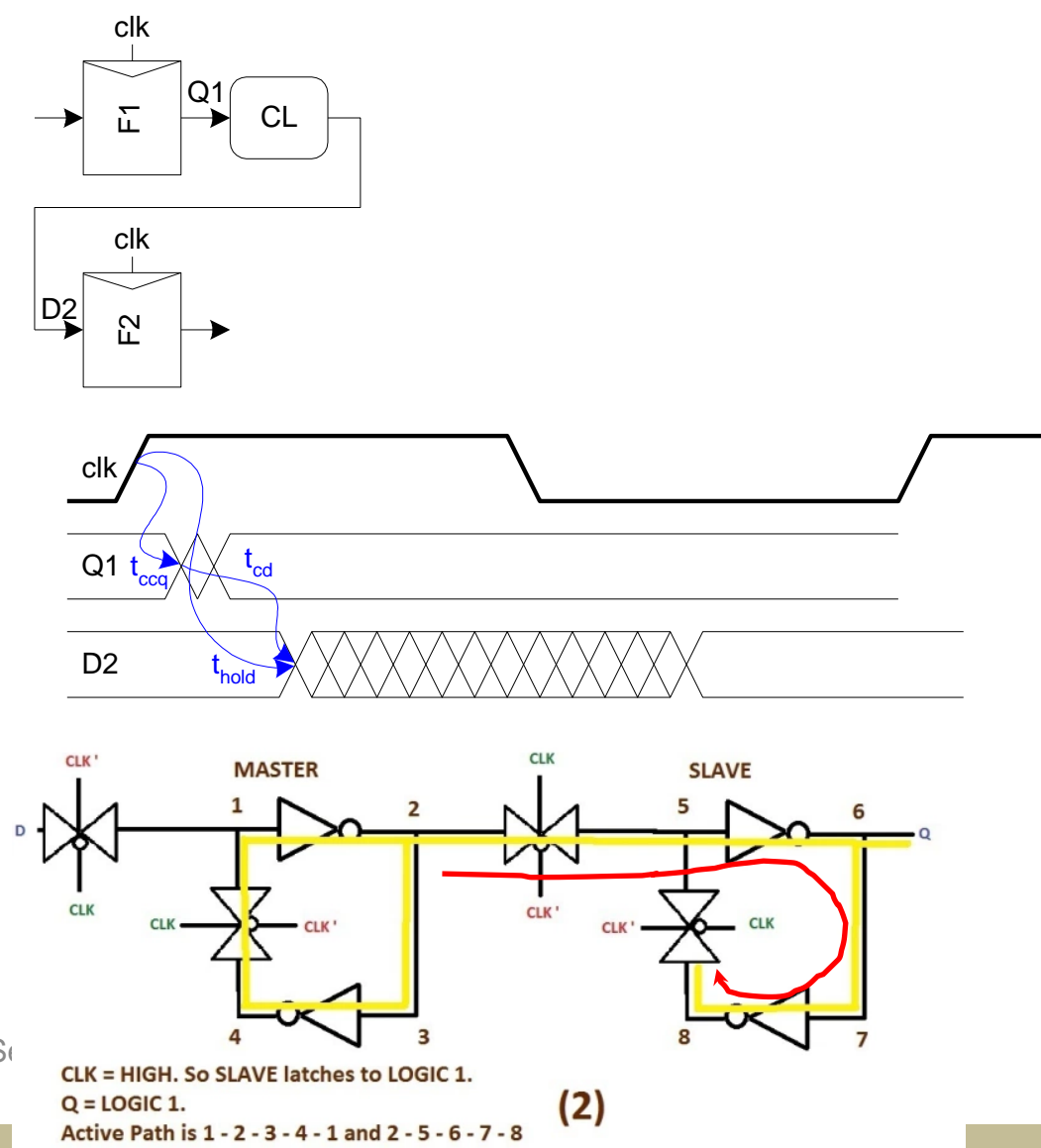
1. clock run slower

T_c become larger

2. comb. Logic faster

T_{pd} smaller by pipeline or
algorithm change

Min-Delay: Flip-Flops



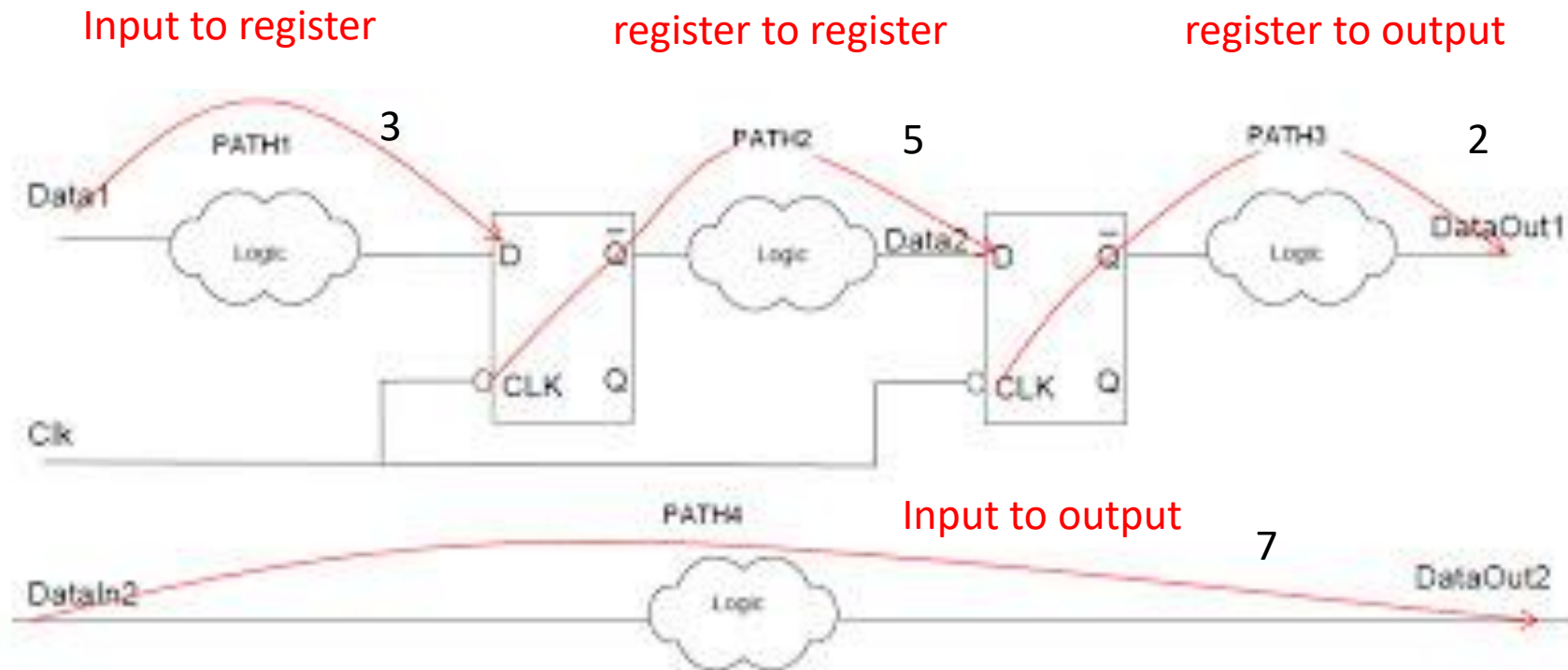
$$t_{cd} + t_{ccq} \geq t_{hold}$$

$$t_{cd} \geq t_{hold} - t_{ccq}$$

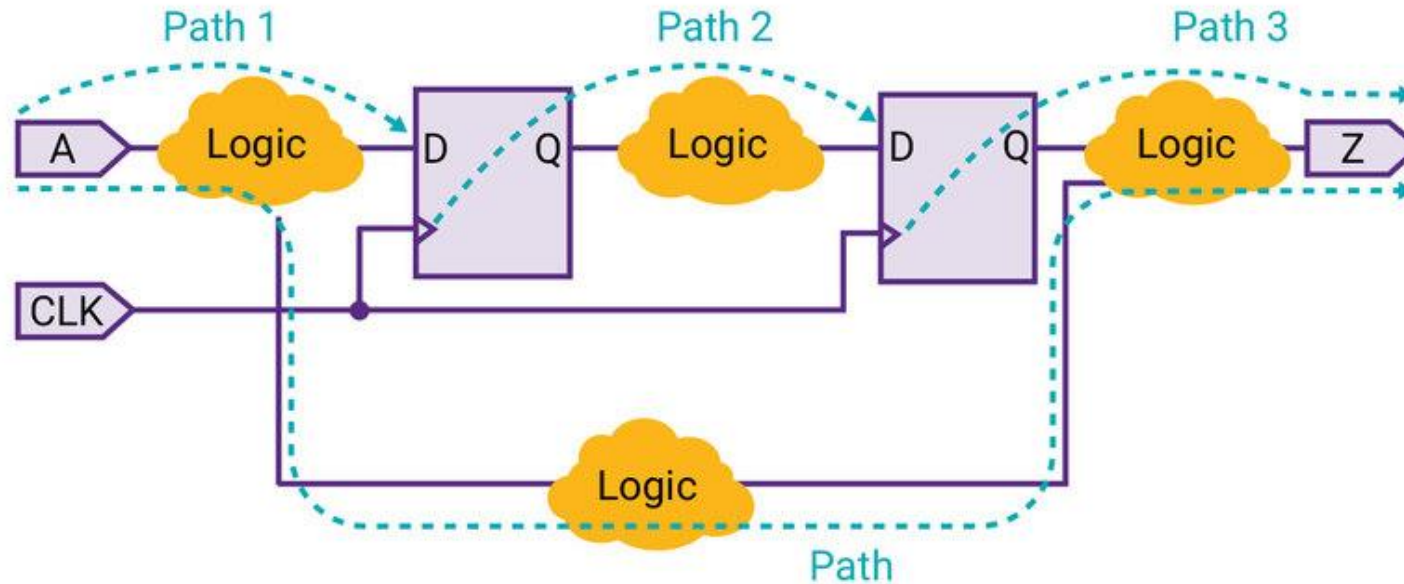
If not hold,
(comb. Logic delay is too short)
⇒ **hold time violation**
⇒ DFF will catch the wrong value
1. Decreasing clock rate does not work
2. Increase tcd (e.g. add delay, buffer)

Timing Paths

- Input to register, register to register, register to output
 - Start from or end to DFFs
- Input to output

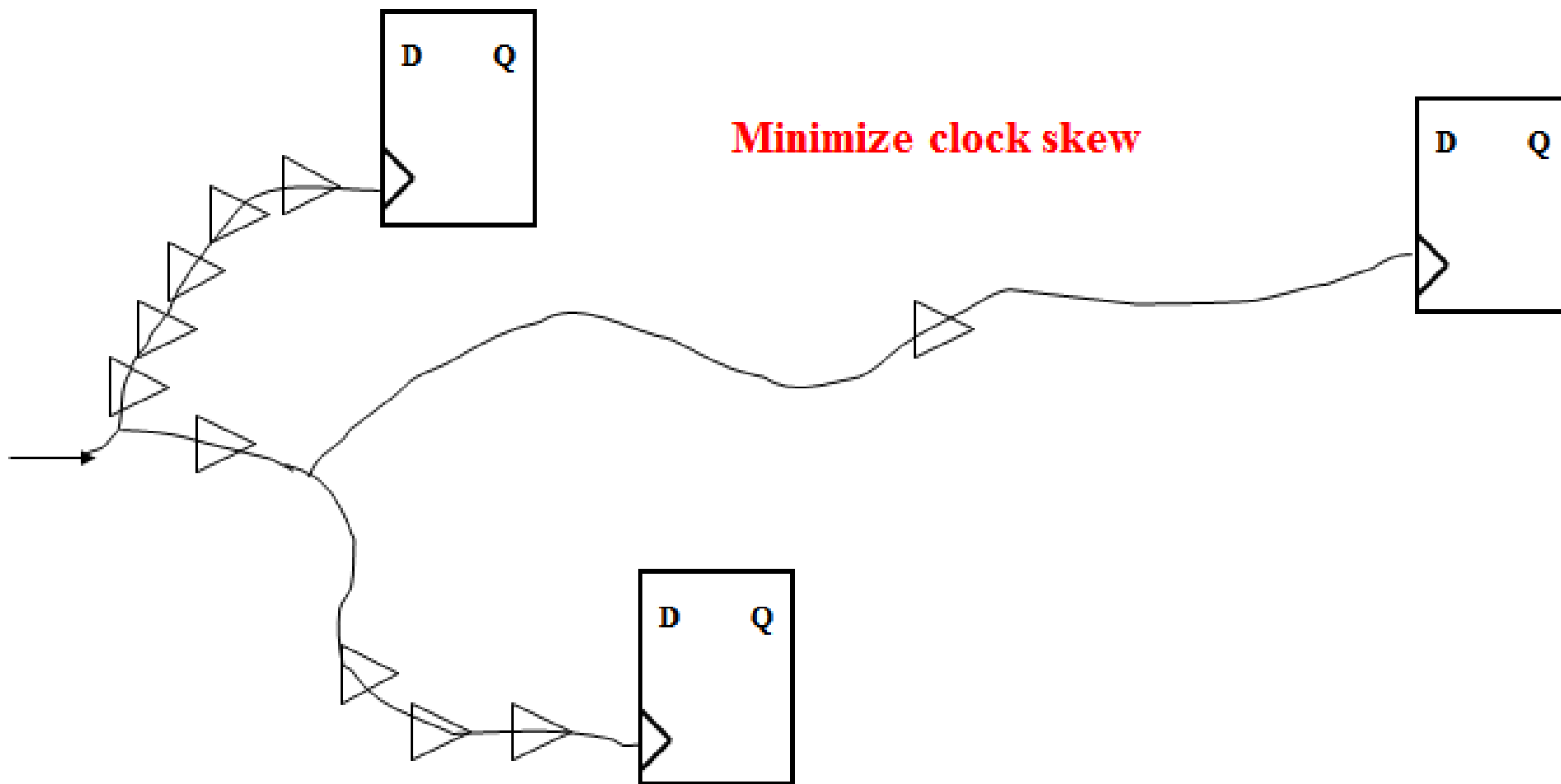


Timing paths



In the example, each logic cloud represents a combinational logic network. Each path starts at a data launch point, passes through some combinational logic, and ends at a data capture point.

Path	Startpoint	Endpoint
Path 1	Input port	Data input of a sequential element
Path 2	Clock pin of a sequential element	Data input of a sequential element
Path 3	Clock pin of a sequential element	Output port
Path 4	Input port	Output port



Example

$$t_{dCQ} = t_{cCQ} = t_s = 150\text{ps}$$

$$t_h = 250\text{ps}$$

$$t_{dMax} = 850\text{ps}$$

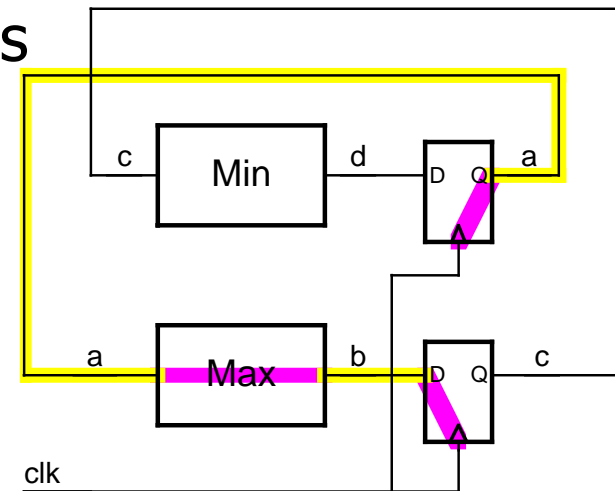
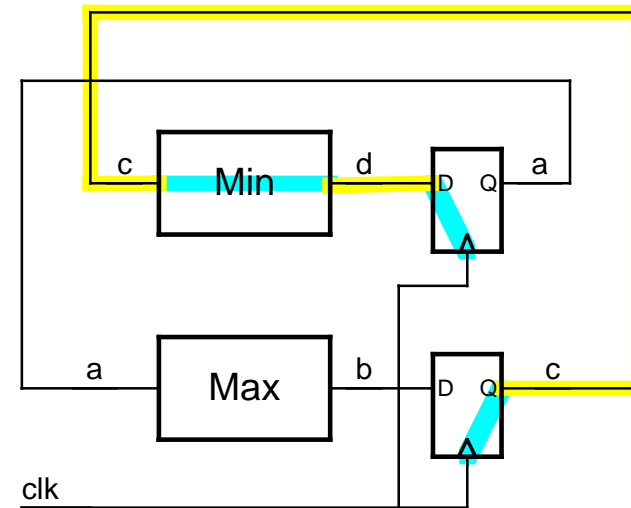
$$t_{cMin} = 100\text{ps}$$

Is hold time constraint met?

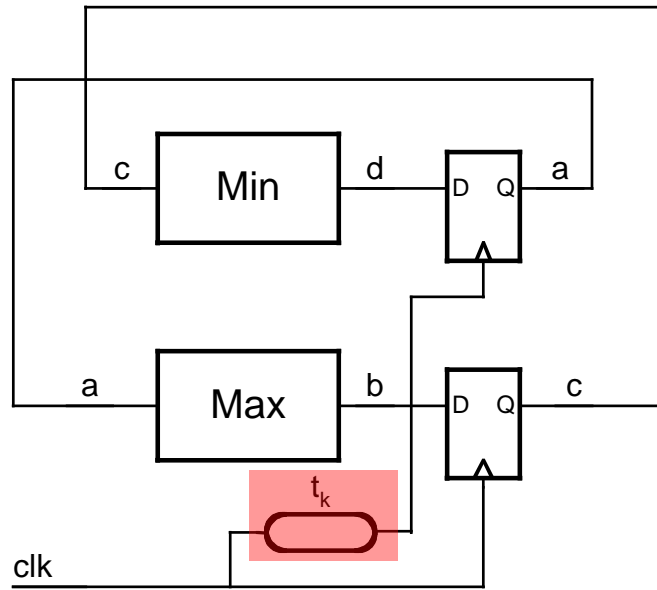
$$t_h \leq t_{cCQ} + t_{cMin} \quad 250\text{ps} \leq 100 + 150\text{ps}$$

What is the minimum cycle time?

$$t_{cy} \geq t_{dCQ} + t_{dMax} + t_s \quad t_{cy} \geq 1150\text{ps}$$



Add Clock Skew t_k

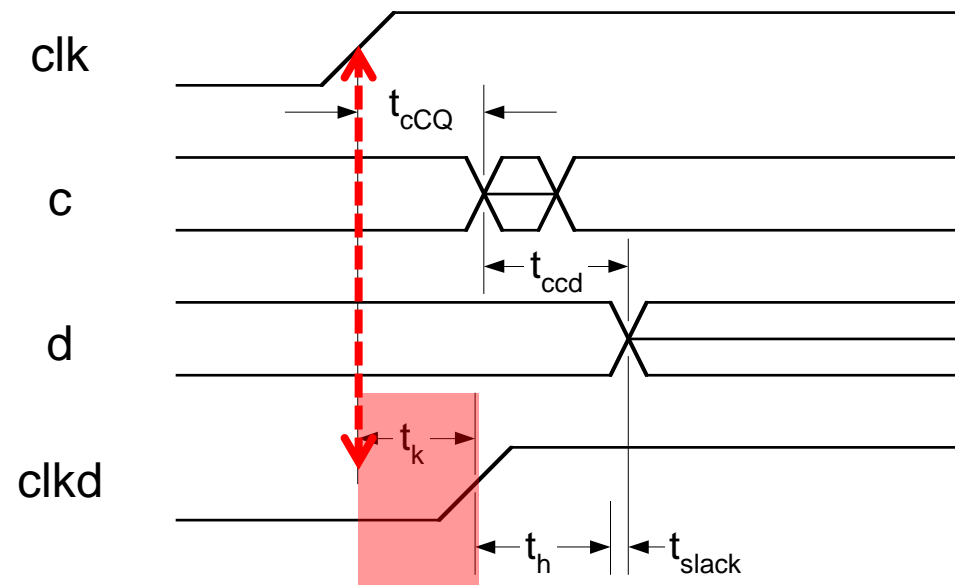


Clock skew: arrival time of clock signal difference

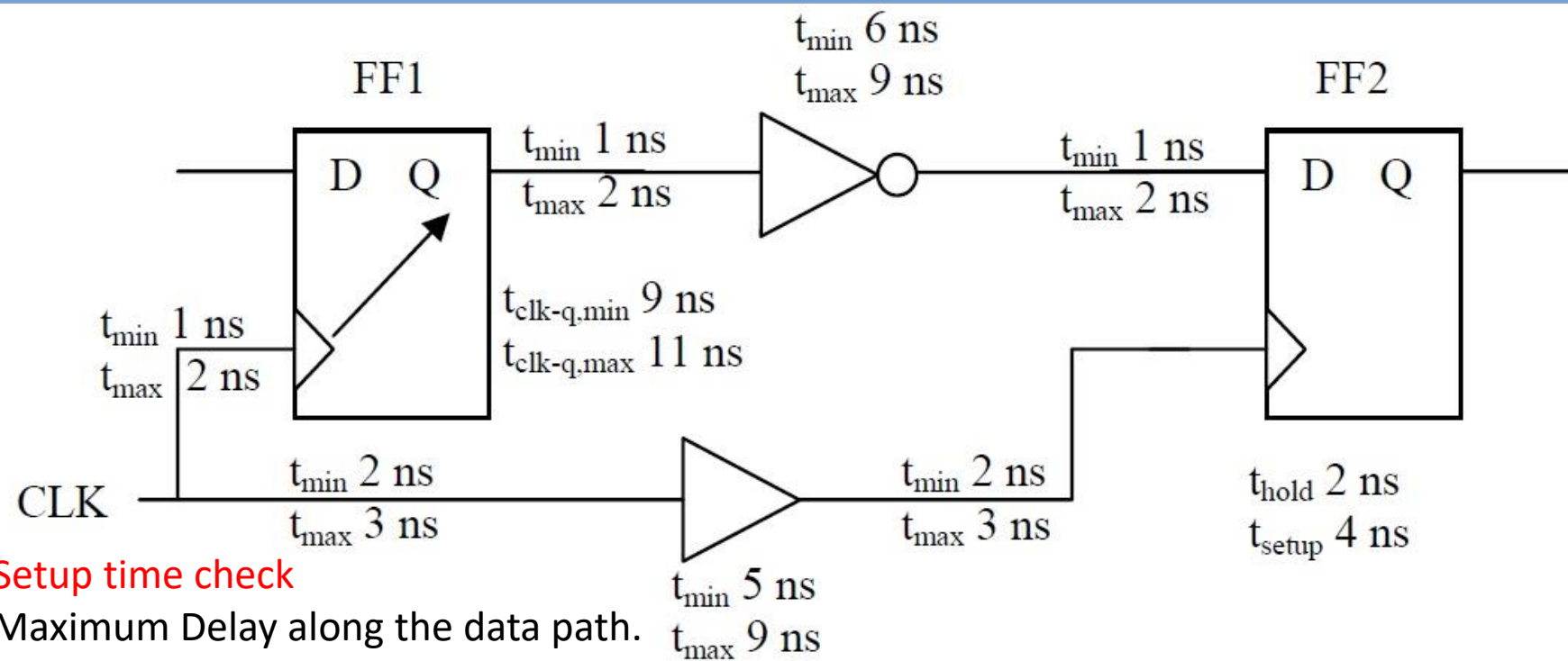
$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k \quad \text{Cycle get larger}$$

$$t_h < t_{cCQ} + t_{cMin} - t_k \quad \text{Hold time tighter}$$

Skew always reduces slack (margin)



check timing path as in timing report



Setup time check

Maximum Delay along the data path.

Minimum Delay along the clock path.

Delay in Data path

= max(wire delay to the clock input of FF1) + max(Clk-to-Q delay of FF1) + max(cell delay of inverter) + max(2 wire delay- "Q of FF1-to-inverter" and "inverter-to-D of FF2")

$$= T_d = 2 + 11 + 9 + (2 + 2) = 26 \text{ ns}$$

Clock path Delay

= (Clock period) + min(wire delay from CLK to Buffer input) + min(cell delay of Buffer) + min(wire delay from Buffer output to FF2/CLK pin) - (Setup time of FF2)

$$= T_{clk} = 15 + 2 + 5 + 2 - 4 = 20 \text{ ns}$$

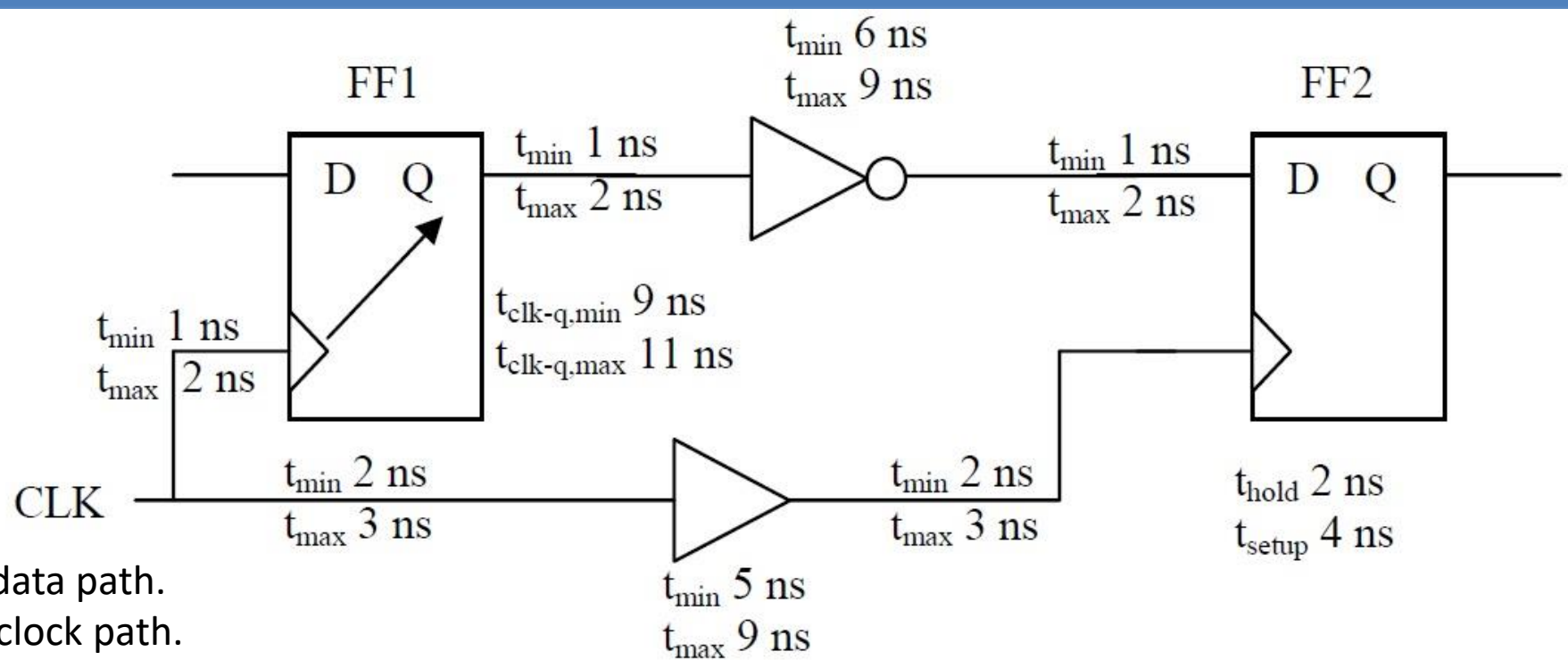
$$\text{Setup Slack} = T_{clk} - T_d = 20 \text{ ns} - 26 \text{ ns} = -6 \text{ ns}.$$

Since Setup Slack is negative \rightarrow Setup violation.

If Clock period is 22 ns then

$$T_{clk} = 22 + 2 + 5 + 2 - 4 = 27 \text{ ns AND } T_d = 26 \text{ ns}$$

$$\text{Setup Slack} = T_{clk} - T_d = 27 - 26 = 1 \text{ ns (No Violation)}$$



Hold Analysis

Minimum Delay along the data path.

Maximum Delay along the clock path.

Delay in Data path

= min(wire delay to the clock input of FF1) + min(Clk-to-Q delay of FF1) + min(cell delay of inverter) + min(2 wire delay- "Q of FF1-to-inverter" and "inverter-to-D of FF2")

$$= T_d = 1 + 9 + 6 + (1 + 1) = 18 \text{ ns}$$

Clock path Delay

= max(wire delay from CLK to Buffer input) + max(cell delay of Buffer) + max(wire delay from Buffer output to FF2/CLK pin) + (hold time of FF2)

$$= T_{clk} = 3 + 9 + 3 + 2 = 17 \text{ ns}$$

$$\text{Hold Slack} = T_d - T_{clk} = 18 \text{ ns} - 17 \text{ ns} = 1 \text{ ns}$$

Since Hold Slack is positive \rightarrow No hold Violation.

Note:

If the hold time had been 4 ns instead of 2 ns, then there would have been a hold violation.

$$T_d = 18 \text{ ns} \text{ and } T_{clk} = 3 + 9 + 3 + 4 = 19 \text{ ns}$$

$$\text{So Hold Slack} = T_d - T_{clk} = 18 \text{ ns} - 19 \text{ ns} = -1 \text{ ns (Violation)}$$

Summary

- Delays in digital systems
 - Propagation delay
 - Contamination delay
- Flip-flop timing constraints
 - Setup time (t_s)
 - Hold time (t_h)
- Cycle time determined by maximum delay

$$t_{cy} > t_{dCQ} + t_{dMax} + t_s$$

- Correct operation depends on minimum delay

$$t_h < t_{cCQ} + t_{cMin}$$

- Clock skew affects both

$$t_{cy} > t_{dCQ} + t_{dMax} + t_s + t_k$$

$$t_h < t_{cCQ} + t_{cMin} - t_k$$

HOW TO READ YOUR TIMING REPORT

How to Read and Interpret Timing Report

report_timing

Header

Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Data arrival

Point	Incr	Path
clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.10 *	1.10
FF1/CLK (fdef1a15)	0.00	1.10 r
FF1/Q (fdef1a15)	0.50 *	1.60 r
U2/Y (buf1a27)	0.11 *	1.71 r
U3/Y (buf1a27)	0.11 *	1.82 r
FF2/D (fdef1a15)	0.05 *	1.87 r
data arrival time		1.87

Data required

clock Clk (rise edge)	4.00	4.00
clock network delay (propagated)	1.00 *	5.00
FF2/CLK (fdef1a15)		5.00 r
library setup time	-0.21 *	4.79
data required time		4.79

Slack

data required time	4.79
data arrival time	-1.87
slack (MET)	2.92

Constraint File (note. These numbers may not match the following slides)

```
//設定clock, I/O 限制  
create_clock "clk" -name clk -period 2 -waveform {0 1.7}  
set_clock_uncertainty 0.2 clk  
set_fix_hold all_clocks()  
set_input_delay 0.5 -clock clk {in}  
set_output_delay -max 0.8 -clock clk {isprime}  
//設定 loading  
set_load -pin_load 5 {isprime}
```

**//Note: these commands are for practical applications to include
// clock jitter, input/output loading capacitances**

Global

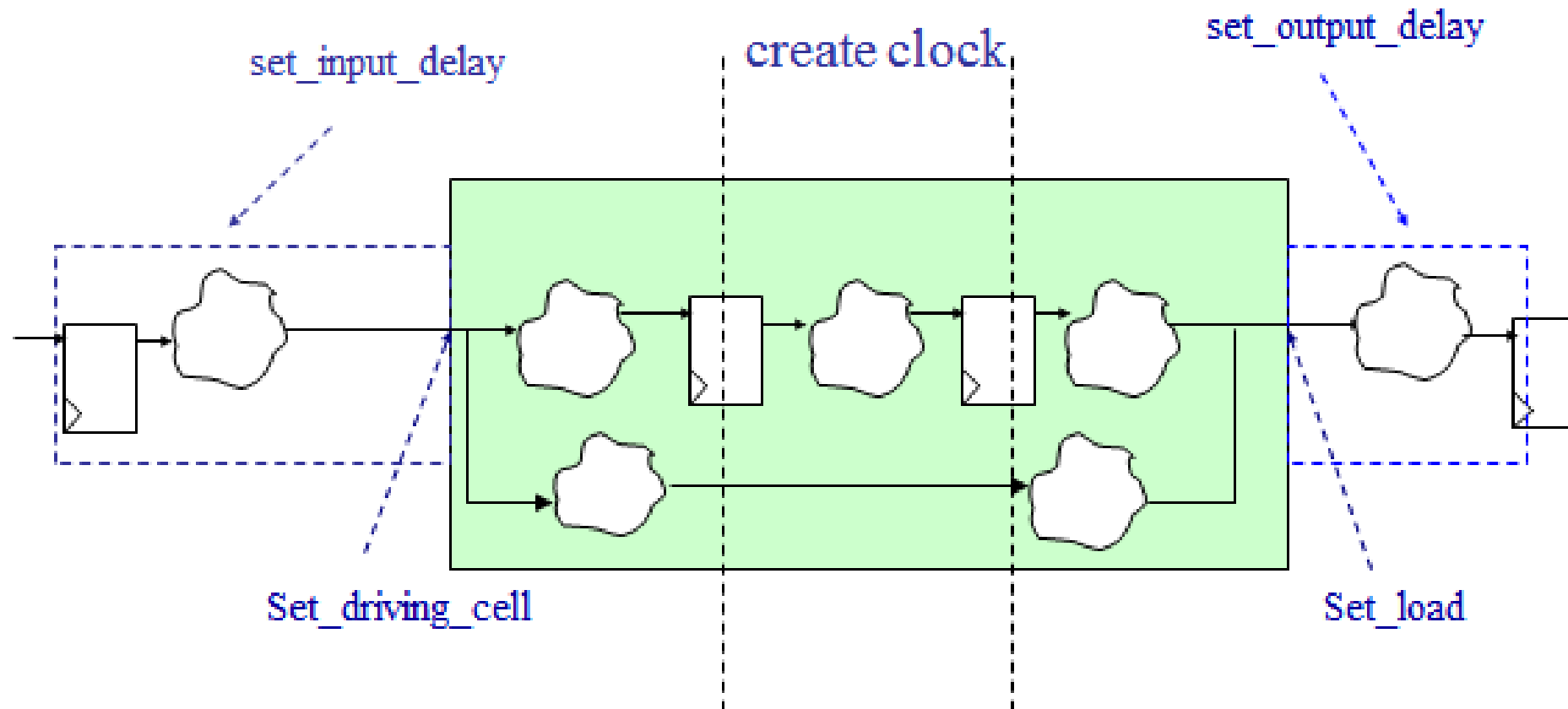
Target_library
Set_operating_conditions
Set_wire_load
Set_max_transition

Clock

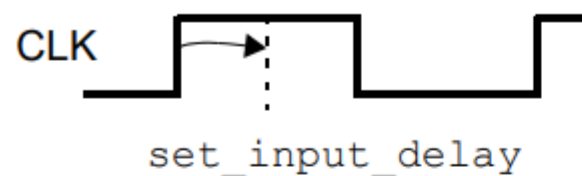
Create_clock
Set_dont_touch_network
Set_ideal_net (for sdf)
Set_clock_uncertainty

Timing Exception

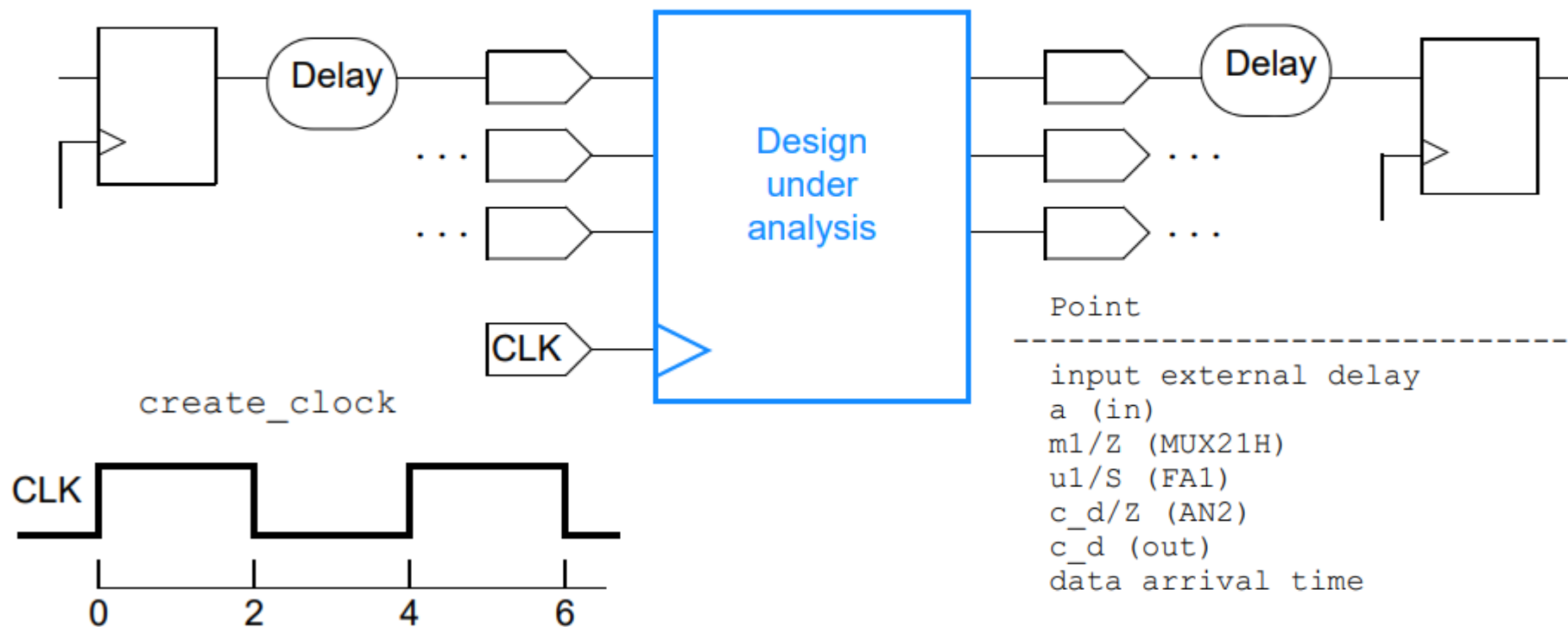
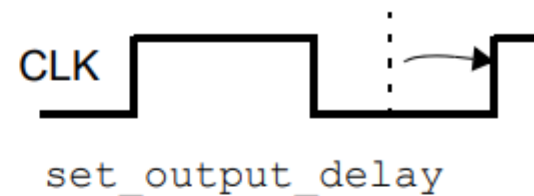
Set_false_path
Set_multicycle_path



Data arrival times



Data required times

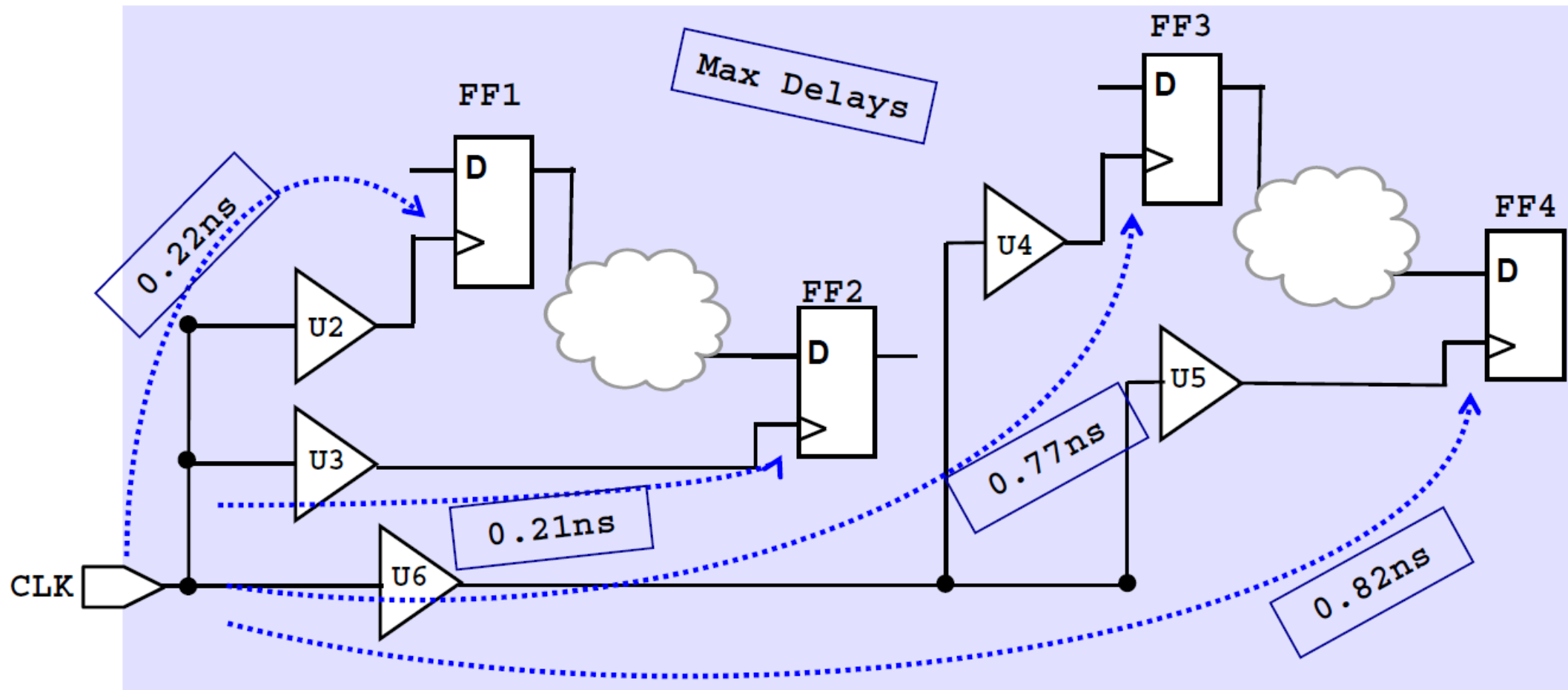


Point	Incr	Path
input external delay	10.00	10.00 r
a (in)	0.00	10.00 r
m1/Z (MUX21H)	1.00	11.00 r
u1/S (FA1)	1.00	12.00 r
c_d/Z (AN2)	1.00	13.00 r
c_d (out)	0.00	13.00 r
data arrival time		13.00
max_delay	15.00	15.00
output external delay	-10.00	5.00
data required time		5.00
data required time		5.00
data arrival time		-13.00
slack (VIOLATED)	-8.00	

Clock Network and Clock Skew

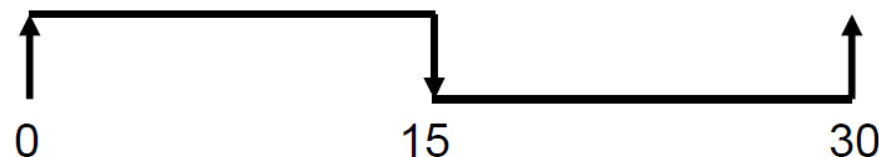
```
report_clock_timing -type skew
```

For each clock, report
REAL skew

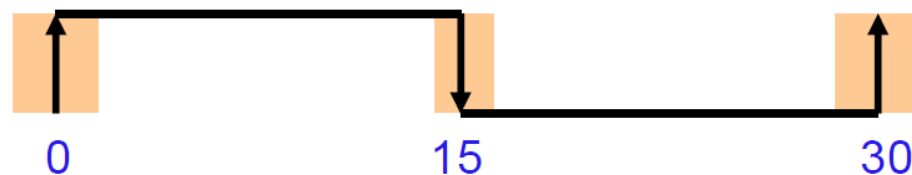


Specify Timing Assertions

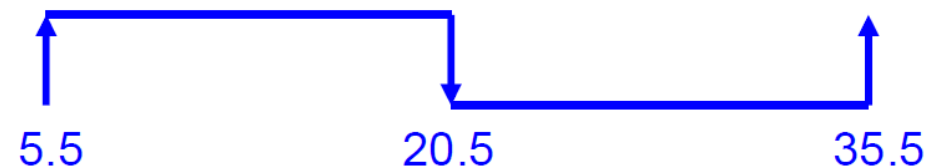
Reference clock waveform



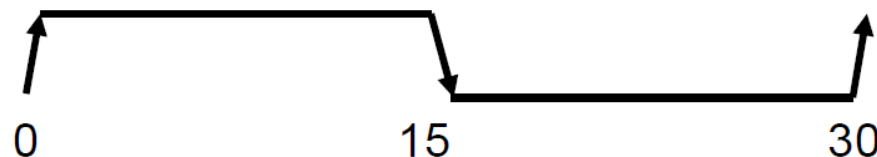
Reference clock waveform with uncertainty



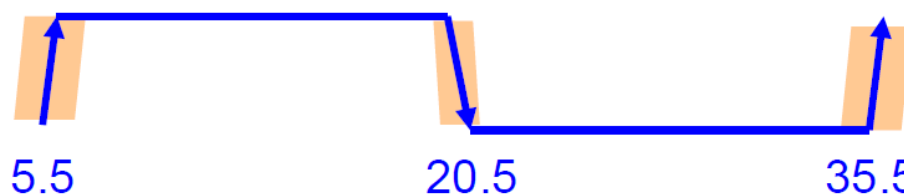
Reference clock waveform with latency



Reference clock waveform with transition

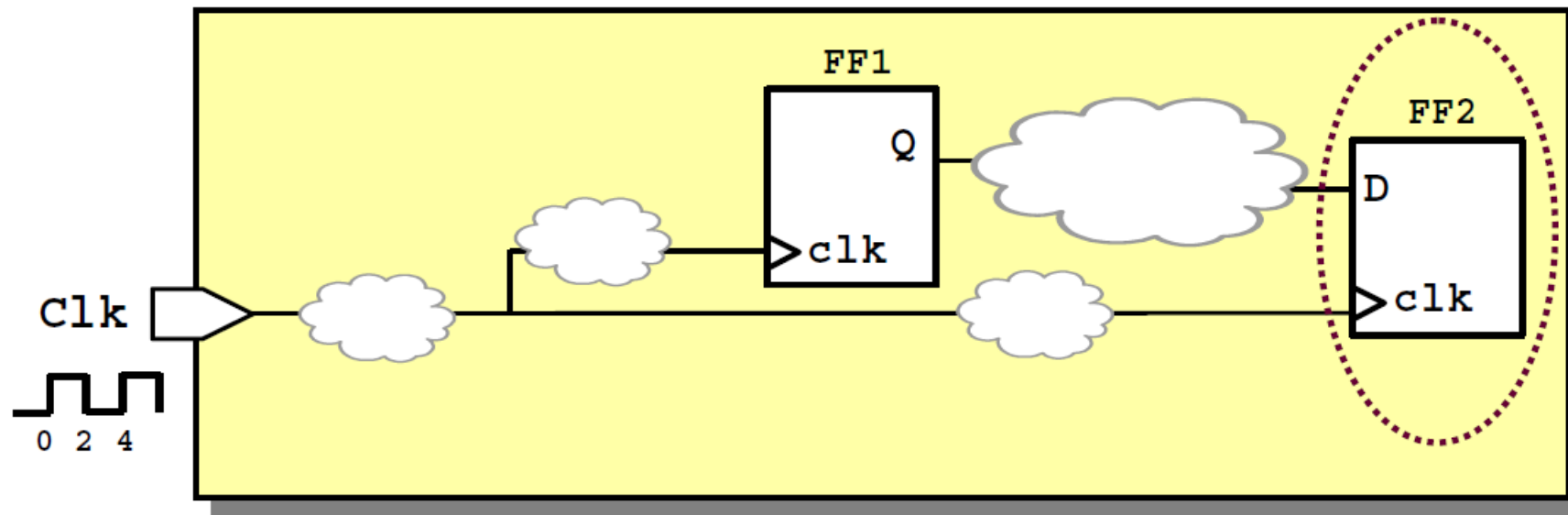


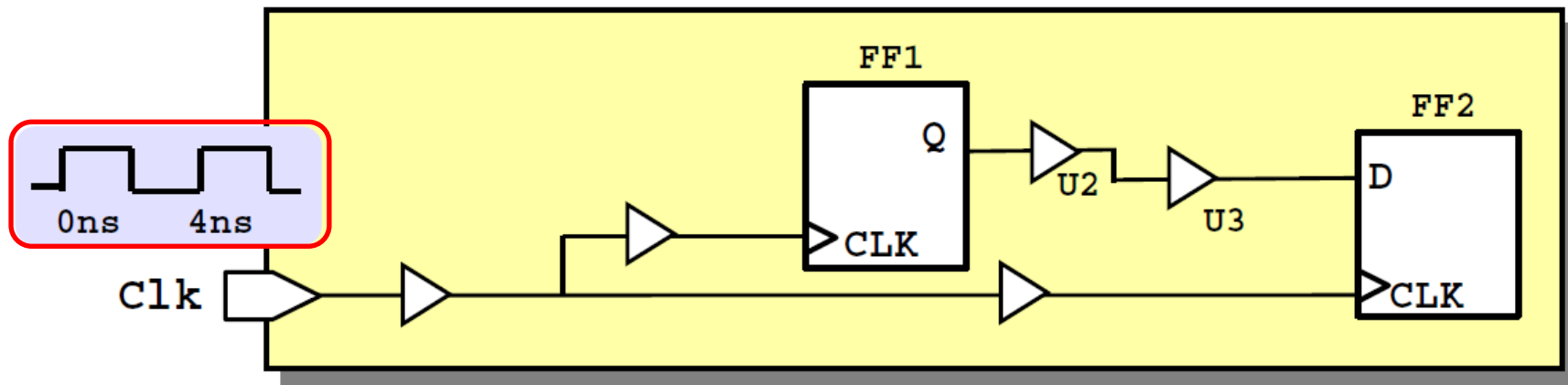
Reference clock waveform with uncertainty, latency, and transition



Timing Verification of Synchronous Designs

All “registers” must reliably capture data at the desired clock edges.

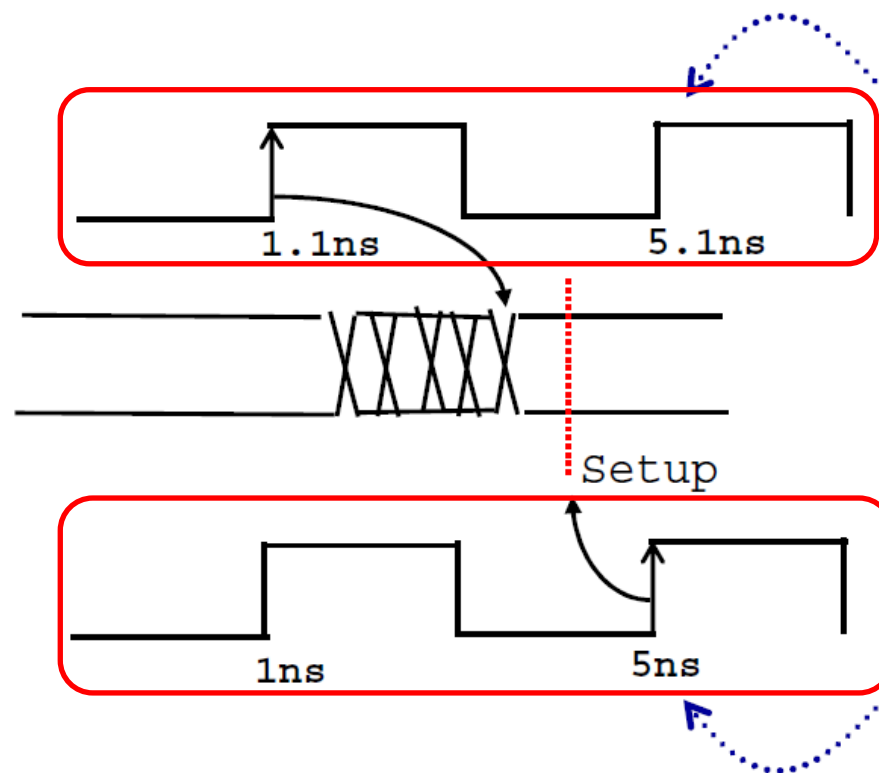




FF1/clk

FF2/D

FF2/clk

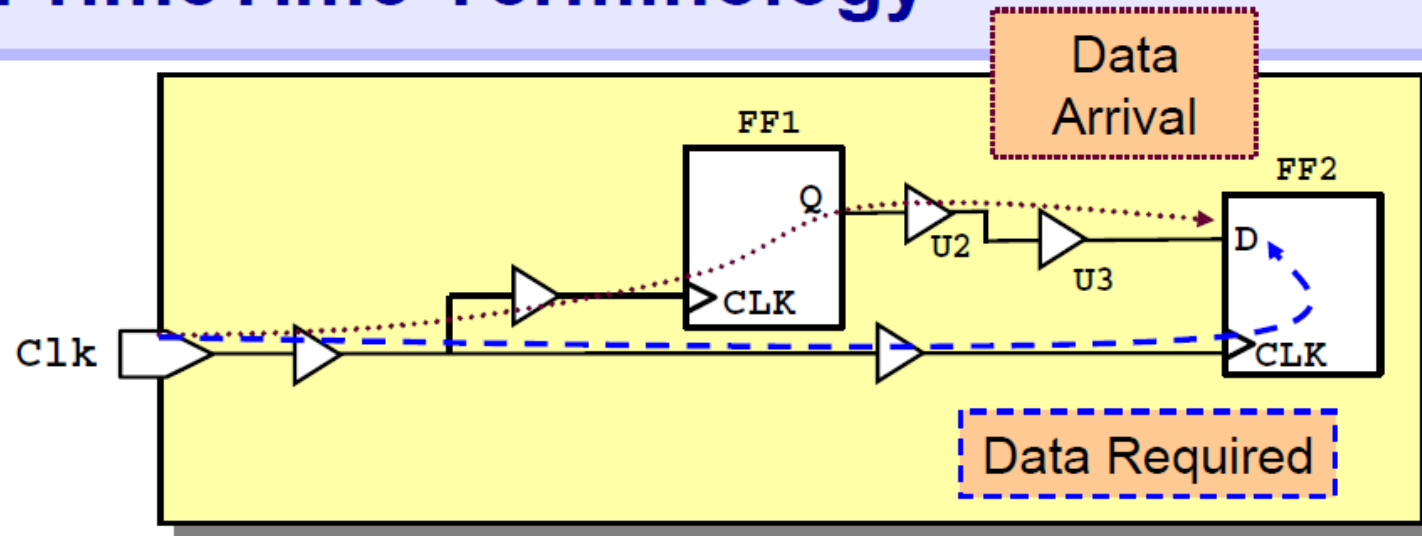


Where does this 1.1ns shift come from?

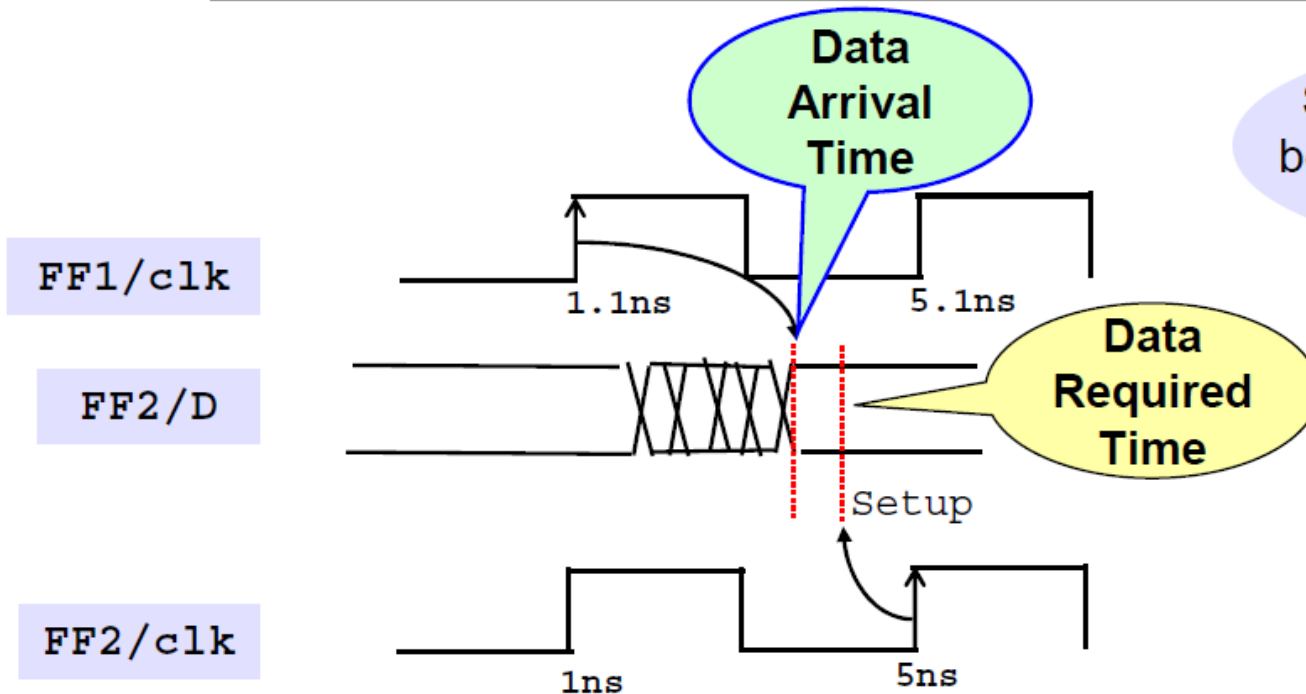
Why is the shift different here?

Clock skew

PrimeTime Terminology



Slack is the difference between data arrival and data required.



Four Sections in a Timing Report

report_timing

Header

Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Data arrival

Point	Incr	Path
clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.10 *	1.10
FF1/CLK (fdef1a15)	0.00	1.10 r
FF1/Q (fdef1a15)	0.50 *	1.60 r
U2/Y (buf1a27)	0.11 *	1.71 r
U3/Y (buf1a27)	0.11 *	1.82 r
FF2/D (fdef1a15)	0.05 *	1.87 r
data arrival time		1.87

Data required

clock Clk (rise edge)	4.00	4.00
clock network delay (propagated)	1.00 *	5.00
FF2/CLK (fdef1a15)		5.00 r
library setup time	-0.21 *	4.79
data required time		4.79

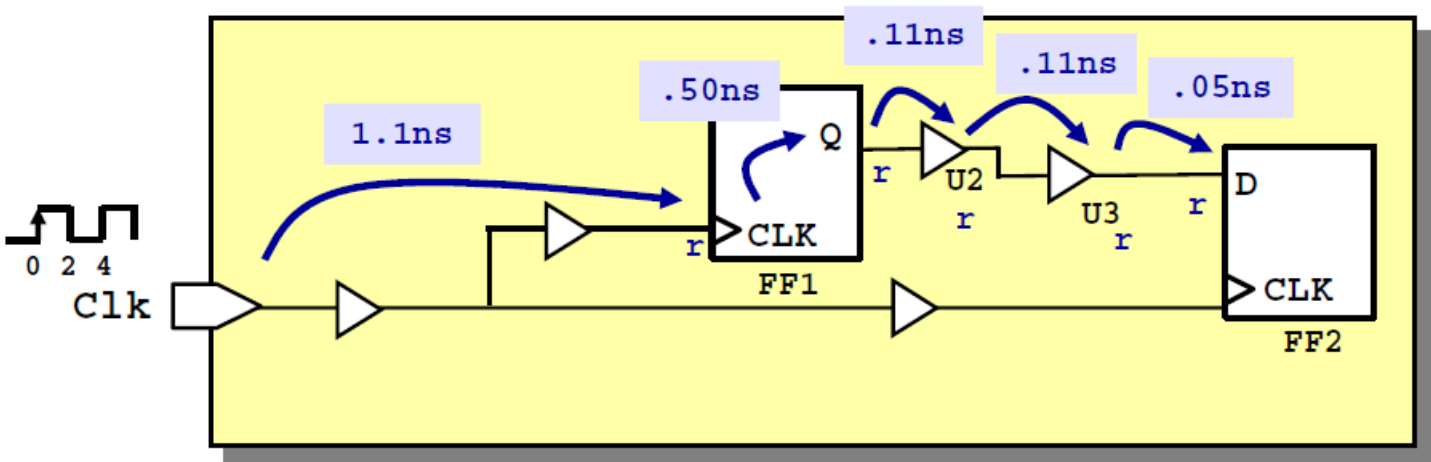
Slack

data required time	4.79
data arrival time	-1.87
slack (MET)	2.92

Data Arrival Section

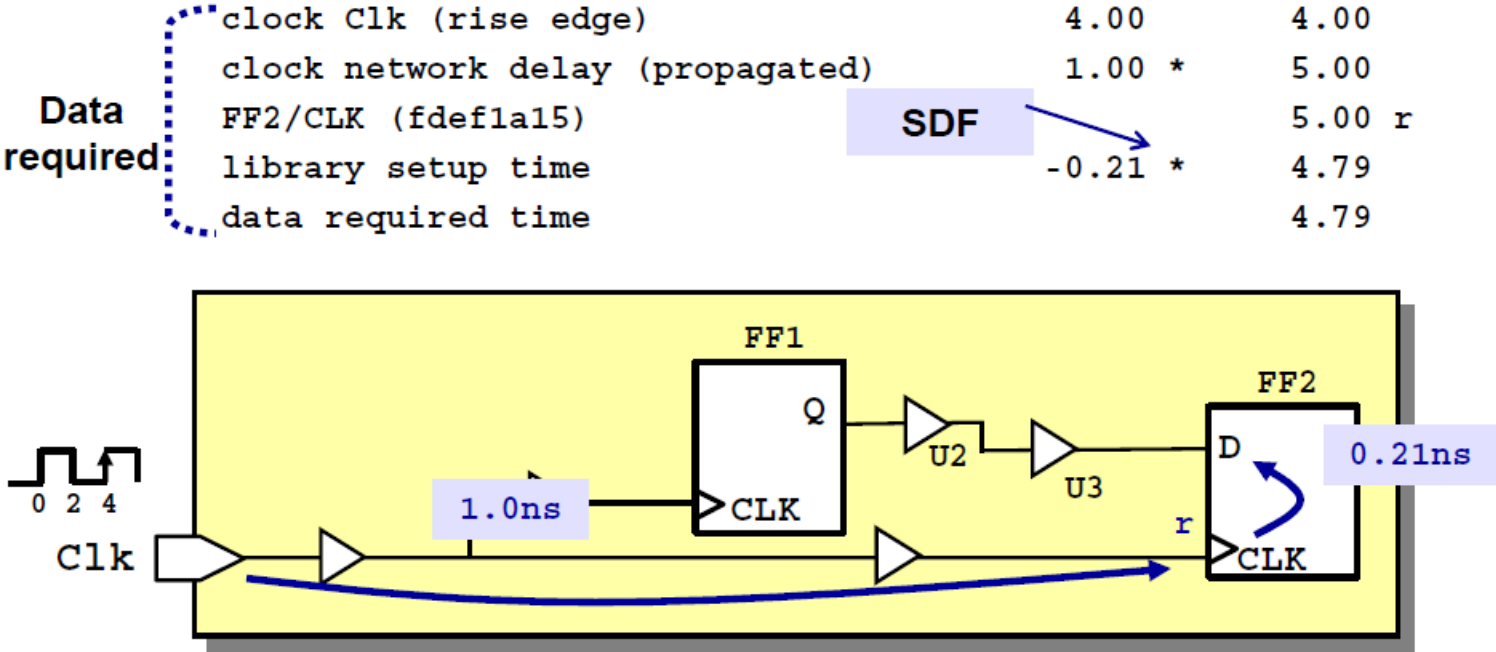
Data arrival

Point	Calculated latency	Incr	SDF	Path
clock Clk (rise edge)		0.00		0.00
clock network delay (propagated)		1.10 *		1.10
FF1/CLK (fdef1a15)		0.00		1.10 r
FF1/Q (fdef1a15)		0.50 *		1.60 r
U2/Y (buf1a27)	Library reference names	0.11 *		1.71 r
U3/Y (buf1a27)		0.11 *		1.82 r
FF2/D (fdef1a15)		0.05 *		1.87 r
data arrival time				1.87



Data Required Section

Point	Incr	Path
-----	-----	-----
clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.10 *	1.10
FF1/CLK (fdef1a15)	0.00	1.10 r
FF1/Q (fdef1a15)	0.50 *	1.60 r
U2/Y (buf1a27)	0.11 *	1.71 r
U3/Y (buf1a27)	0.11 *	1.82 r
FF2/D (fdef1a15)	0.05 *	1.87 r
data arrival time		1.87
clock Clk (rise edge)	4.00	4.00
clock network delay (propagated)	1.00 *	5.00
FF2/CLK (fdef1a15)		5.00 r
library setup time	-0.21 *	4.79
data required time		4.79



Summary - Slack

report_timing

Startpoint: FF1 (rising edge-triggered flip-flop clocked by Clk)
Endpoint: FF2 (rising edge-triggered flip-flop clocked by Clk)
Path Group: Clk
Path Type: max

Point	Incr	Path

clock Clk (rise edge)	0.00	0.00
clock network delay (propagated)	1.10 *	1.10
FF1/CLK (fdef1a15)	0.00	1.10 r
FF1/Q (fdef1a15)	0.50 *	1.60 r
U2/Y (buf1a27)	0.11 *	1.71 r
U3/Y (buf1a27)	0.11 *	1.82 r
FF2/D (fdef1a15)	0.05 *	1.87 r
data arrival time		1.87
clock Clk (rise edge)	4.00	4.00
clock network delay (propagated)	1.00 *	5.00
FF2/CLK (fdef1a15)		5.00 r
library setup time	-0.21 *	4.79
data required time		4.79

data required time		4.79
data arrival time		-1.87

slack (MET)		2.92

Slack