NYCU-ECE DCS-2023

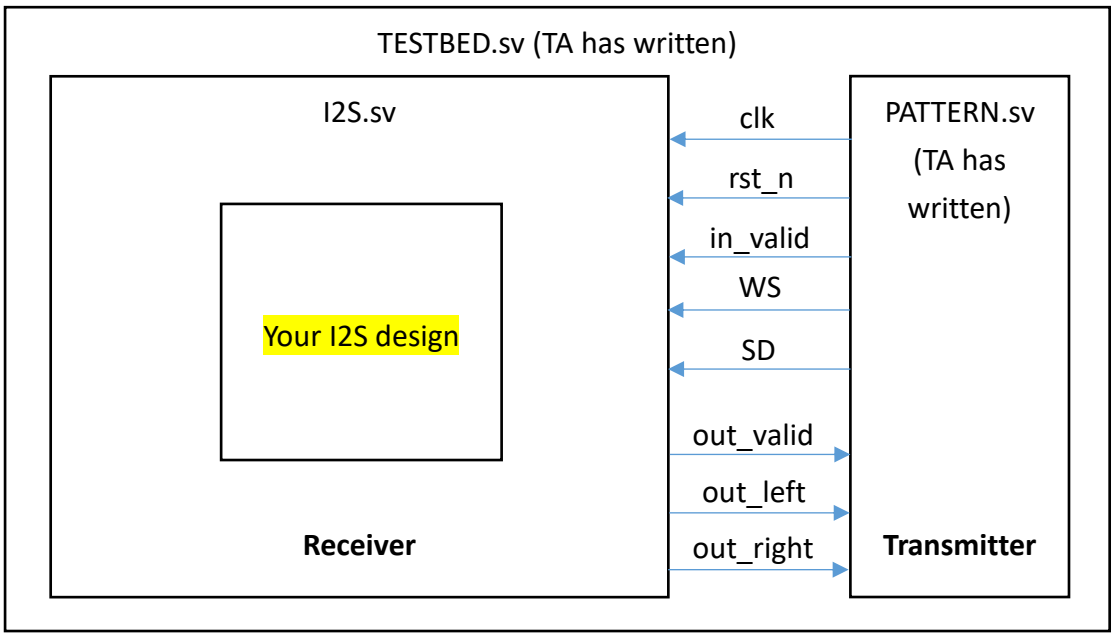
HW02

Design：Simplified I2S

Data Preparation

1. Extract the files needed from TA's directory.
   % tar xvf ~dcsta01/HW02.tar
2. The extracted files contain：
   A. 00_TESTBED/
   B. 01_RTL/
   C. 02_SYN/
   D. 03_GATE/
   E. 09_UPLOAD/

Block Diagram

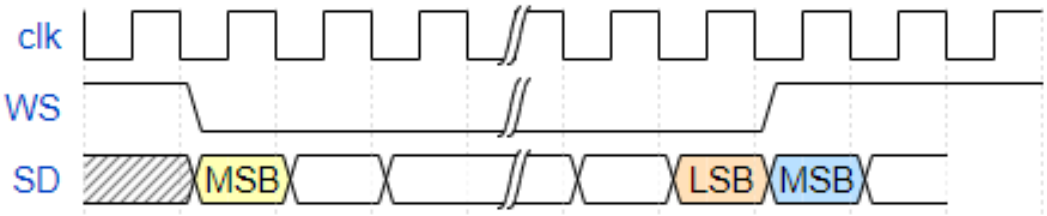


Design Description

The inter-IC sound (I2S) bus is a standardized communication structure designed for digital audio transmission. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus consisting of a clock line, a word select line and a serial data line is used. The transmitter as the controller has to generate the bit clock, word-select signal and data signal, and send these signals to the receiver.

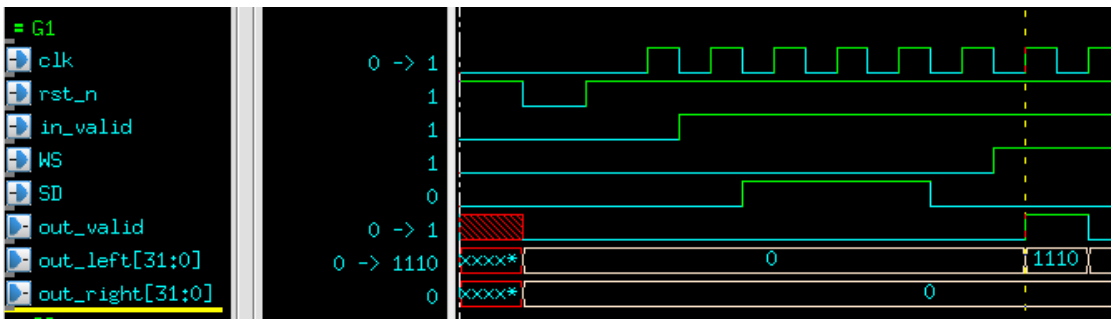
In this homework, you are required to design a I2S receiver. For design purposes, some specs of the standard I2S have been modified.

When in_valid is high, both WS and SD are valid. The word select line (WS) indicates the channel being transmitted. WS = 0 means the left channel, WS = 1 means the right channel. Serial data (SD) is transmitted in binary with the MSB first. Input data length depends on how long WS retains its state. (WS will remain unchanged for at least 5 cycles.) When WS transitions, you should raise out_valid and output the data according to the selected channel. Serial data is received first-in-first-out. If SD inputs more than 32 bits, only the last 32 bits are stored. If SD inputs less than 32 bits, the remaining bits should be 0.



Example：

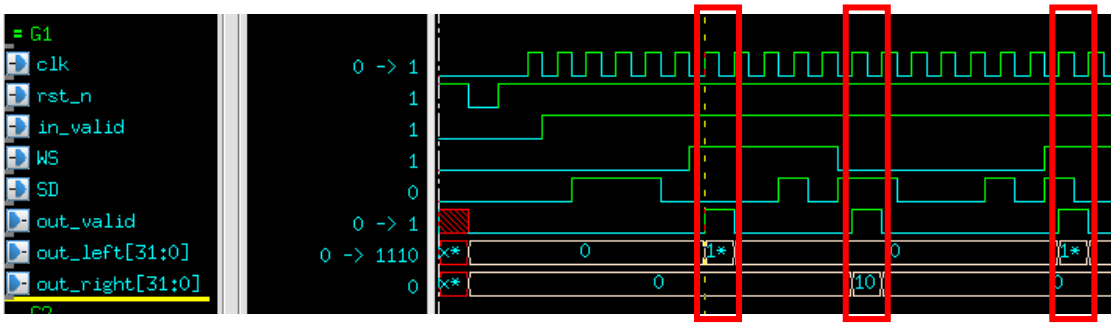
1. SD inputs：01110 (from left to right)
   WS = 0：Left channel.
   WS will retain its state for at least 5 cycles.



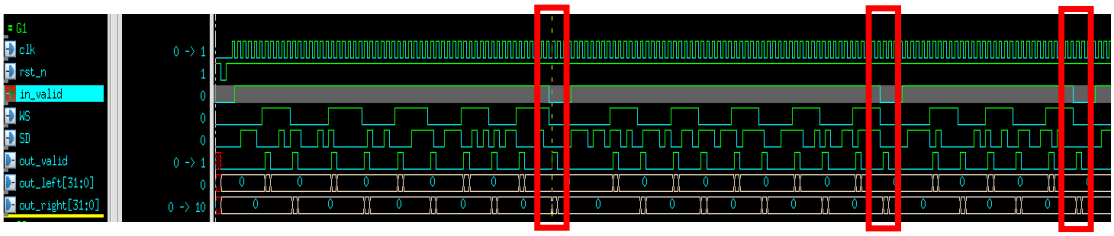
   Rise out_valid when WS changes to 1. (When WS transitions)
   out_left = 32'b0000_0000_0000_0000_0000_0000_0000_1110
   out_right = 32'd0

2. SD inputs：1011_0011_1111_1111_0010_1010_1111_0010_1101
   (Input order：1,0,1,1,0,0,1,1,1,1,1....)
   If SD inputs more than 32 bits, only the highlighted area should be valid.

3. You should raise out_valid and give the correct results when WS transitions. At the same time, WS and SD will not stop giving data unless in_valid falls. All output signals can only raise for 1 cycle.



4. in_valid might fall for a few cycles, you should still output the last result before in_valid falls.



Inputs and Outputs

Input Signals	Bit Width	Description
clk	1 bit	Clock.
rst_n	1 bit	Asynchronous active-low reset.
in_valid	1 bit	High when input is valid. (WS and SD)
WS	1 bit	Word select. 0：Left channel. 1：Right channel
SD	1 bit	Serial data.

Output Signals	Bit Width	Description
out_valid	1 bit	High when WS transitions. (Still has to rise once after in_valid falls) Out_valid should only be high for 1 cycle.
out_left	32 bits	Output data to the left channel if selected, otherwise output 0.

out_right	32 bits	Output data to the right channel if selected, otherwise output 0.

Specifications

1. Top module name : I2S (File name: I2S.sv)
2. Please use Systemverilog to complete your homework.
3. It is an asynchronous active-low reset architecture, and reset would be given only once at the beginning of the simulation.
4. All output signals should be reset after the reset signal is asserted.
5. Output results should be correct when out_valid is high.
6. 02_SYN results cannot include errors and latches.
7. 03_GATE results cannot include any timing violations.
8. Slack should be non-negative(MET) at the end of the timing report.
9. Performance is determined by area, the lower the better.
10. Combinational blocks and sequential blocks should be separated.
11. For loops are forbidden. TA will check your code.

Upload file

1. Please use 09_UPLOAD to upload your code. (**% ./01_upload**)
2. Please upload your report to new E3.
   (File name：report_dcsXXX.pdf, XXX is your server account.)
3. Deadline：
   DEMO1：3/30 23:59:59
   DEMO2：4/6 23:59:59

Grading Policy

1. Pass RTL & Synthesis & Gate simulation：70%
2. Area：15%
3. Report：15%

****NOTE****

Report should be less than 2 pages. You should describe your design, how you optimize it and show your block diagram. Finally, give a summary regarding this homework or any comments about this class.