

NAME; KAYODE PETER TEMITDPE  
MATRIC NUMBER ; 208077

DEPARTMENT : COMPUTER SCIENCE (200 LEVEL)

COURSE ; DIGITAL LOGIC DESIGN (CSC 213)

### Assignment

Figure 1;

A	B	A	P = $\overline{AA}$	B	R = $\overline{BB}$	Q = $\overline{Pr}$
0	0	0	1	0	1	0
0	1	0	1	1	0	1
1	0	1	0	0	1	1
1	1	1	0	1	0	1

The OR gate is implemented.

Figure 2;

A	B	C = $\overline{AB}$	D = $\overline{AC}$	E = $\overline{CB}$	Q = $\overline{DE}$
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	0	0

The XOR gate is implemented.

Figure 3;

A	A	$Q = \overline{A+B}$
0	0	1
1	1	0

The NOT gate is implemented.

Figure 4;

A	B	$M = \overline{A+B}$	$N = \overline{A+B}$	$Q = \overline{M+N}$
0	0	1	1	0
0	1	0	0	1
1	0	0	0	1
1	1	0	0	1

The OR gate is implemented.

Figure 5;

A	B	A	$M = \overline{A+A}$	B	$N = \overline{B+B}$	$Q = \overline{M+N}$
0	0	0	1	0	1	0
0	1	0	1	1	0	0
1	0	1	0	0	1	0
1	1	1	0	1	0	1

The AND gate is implemented.