Lab 1 Basic SPICE Simulations ECE334

Objective:

The purpose of this lab is to use SUE design manager its graphical waveform viewer (*NST*) to simulate some basic circuits. We start by doing transient simulations for a simple RC circuit, then we use SUE to characterize a CMOS inverter. Following that we will use the CMOS inverter and a NAND gate to design a pulse generator circuit.

Preparation:

P1) Consider the circuit shown in figure 1.
(a) Sketch the expected voltages at nodes 1 and 2 for the first 15ns.
(b) Defining rise and fall times to be the time it takes for the signal to go from 0 to 70 percent of its final value, calculate the rise and fall times at V_o.

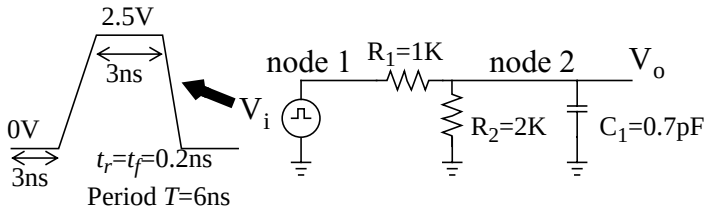

Figure 1: R-C circuit

P2) Draw the CMOS inverter of figure 2 in SUE, and setup your simulation to find its transfer characteristics and transient response satisfying the conditions below.

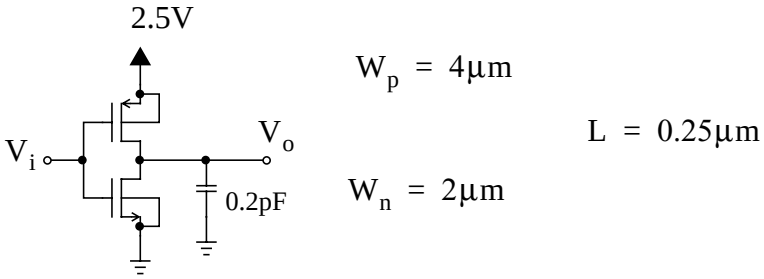

Figure 2: CMOS inverter

— For the transient response, setup your simulation to plot of the output, V_o, when the input, V_i, is an input pulse of height 2.5 volts for a duration of 3ns with rise and fall times of 0.2ns, and a period of 6ns. Set the channel length for both transistors to ln_min and lp_min.

— For the transfer characteristics, **make sure you remove the load capacitor**. Setup your simulation to plot of V_o vs. V_i when V_i is an input pulse of height 2.5 volts with rise and fall times of 16ns, a delay time of 0ns, and a period of 100ns. To plot the transfer characteristics of the CMOS inverter in *NST*, change the X-axis from "Time" to the input node (V_i). You can do this by clicking "*yourfilename*.tr0" under "File" menu. Make sure you choose the loaded data file and not the copied one. A menu will popup with all the node names for plotting. Choose your input node (V_i) and click on "X", then choose your output node (V_o) and click "Plot".

P3) Estimate the transient times of the CMOS inverter with the load capacitor, if a transistor (when it is conducting) can be approximated by a resistor of the value

$$R_{eq} = \frac{2}{\mu_i C_{ox}(W/L)_i(|V_{GS_i}| - |V_{ti}|)}$$

where subscript 'i' represents either 'n' or 'p' for an N- and P-MOSFET respectively and $C_{ox} = \varepsilon_{ox}/t_{ox}$. (Note: in Spice μ_i = UO [$cm^2/(V \cdot s)$], and t_{ox} = TOX [m]). You can find the values of the transistor parameters in the 0.25μm CMOS process model file "/cad2/mmi_local/sue/g25.mod".

Lab Work:

L1) Use SUE to simulate the circuit of figure 1. Plot the voltage at V_i and V_o using the graphical waveform viewer (*NST*) and compare your results with your sketches in part P1.

L2) Use SUE to perform the simulations in part P2. Plot the CMOS inverter transfer characteristic and transient response. Compare the transient times to your estimate in part P3.

L3) a) Perform a transistor level simulation for the pulse generator circuit of Lab 0. This is done by using the transistor level implementation for each logic gate. Use the same transistor sizes for the inverters as part L2), while for the NAND gate use Wp=Wn=4μm. Plot the output and input waveforms, and measure the pulse width you obtain from the circuit.

b) Insert a 0.25pF capacitor at the output of the third inverter and repeat part a). Provide a plot for the output waveform and compare the pulse width with part a).

c) Modify the circuit to achieve a pulse width of 1.5ns?

Expected Results:

For all the previous experiments, provide print-outs of the circuit diagrams and the required plots/waveforms.

Extra Notes:

- A brief SPICE tutorial from University of Pennsylvania - http://www.seas.upenn.edu/~jan/spice/spice.overview.html.

- In P3, transient times mean the rise and fall times.

- In P3, the value of Vti can be obtained from the parameter VTHO [measured in V] in the 0.25 m CMOS process model file.

- In L3,

Transistor level simulation should be performed. That means you have to redraw the pulse generator schematic in Lab 0 with all logic gates constructed with transistors.

In all simulations, which is from part (a) to part (c), you should use the same input pulse parameters as in the pulse generator circuit in Lab 0.

The pulse width is defined to be the interval between the 50% points of the pulse. Be careful that the pulse from your circuit is low-going (refer to p.22 of the SUE tutorial), so you should measure the pulse width from the 50% of the falling edge to the 50% of the rising edge of the pulse.

- The following summarizes what you will need to demonstrate to your TAs in lab:

L1

- schematic of the RC circuit in SUE

- Vi/Vo vs. time plot

- measure the rise and fall times from the plot and compare with your calculated results in part P1.

L2

- schematic of the CMOS inverter in SUE

- transfer characteristics - Vo vs. Vi plot

- transient response - Vo vs. time

- measure the rise and fall times from the transient response plot and compare with your estimated results in part P3.

L3a

- schematic of the pulse generator circuit in transistor-level implementation

- output/input vs. time plot

- measure the pulse width

L3b

- same as L3a with a 0.25pF capacitor inserted at the output of the 3rd inverter

L3c

- same as L3a with your circuit modified to achieve a pulse width of 1.5ns

- give a brief explanation about why your modification can achieve the target pulse width

FAQ:

1. I got the following error messages when doing HSPICE simulation in part P2.

BSIM3 Fatal **error** Effective channel width <= 0

BSIM3 Fatal **error** Effective channel width for C-V <= 0

BSIM3 Fatal **error** Effective channel width <= 0

BSIM3 Fatal **error** Effective channel width for C-V <= 0

You probably set the wrong properties values in the PMOS and NMOS icons. When editing the properties, you don't have to change the L value, just leave it as ln_min or lp_min. If you push into the view of the PMOS or NMOS icon, you will find that the width is measured by micrometers (W='$W*1u') in the SPICE property line. So, you should set the W value to be 4 and 2 for PMOS and NMOS respectively. You can verify your value setting from the output SPICE file (e.g. lab1_p2.sp), you should find that L=lp_min and L=ln_min for PMOS and NMOS respectively, and both lp_min and ln_min are set to be 0.25u. For the widths, you should find W='4*1u' and W='2*1u' respectively.