Problem 1; Hazards in pipelined Processes

a) Data Hazard (**RAW**)
DADD requires the value of R1(Register 1) being loaded by the LD instruction which takes cycles to complete.

b) Data Hazard (**WAW**)
DADD instruction modifies the Values of R1 after a write by the MULT instruction

c) Structural Hazard
Both instructions are using the multiplier unit those the latter will have to wait for the first to be executed.

d) Data Hazard (**RAW**)
SD requires the value of R1 computed by DADD still in MEM stage

e) Data Hazard (**RAW**)
SD requires value in R1computed by DADD thus cannot proceed until the R! value is updated

Problem 2; 2-Bit Saturating Counter Branch Predictor

a) A 2- bit saturating counter branch predictor uses a 2-bit counter to predict the outcome of a branch instruction
The counter can be in one of four states: 00, 01, 10, or 11. The states and transitions are as follows:
State 00: Strongly not taken
State 01: Weakly not taken
State 10: Weakly taken
State 11: Strongly taken

Current State	**Branch Outcome**	**Next State**	**Prediction**	**Misprediction**
00	Not Taken	00	Not Taken	No
00	Taken	01	Not Taken	Yes
01	Not Taken	00	Not Taken	No
01	Taken	10	Not Taken	Yes

Current State	Branch Outcome	Next State	Prediction	Misprediction
10	Not Taken	01	Taken	Yes
10	Taken	11	Taken	No
11	Not Taken	10	Taken	Yes
11	Taken	11	Taken	No

b) Outcome of predictions

Iteration	Current State	Next State	Branch Outcome	Prediction	Misprediction
1	00	00	Not Taken	Not Taken	No
2	00	01	Taken	Not Taken	Yes
3	01	00	Not Taken	Not Taken	No
4	00	01	Taken	Not Taken	Yes
5	01	00	Not Taken	Not Taken	No
6	00	01	Taken	Not Taken	Yes