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Lab 5

Design of a UART receiver

Introduction

In this lab you will design the receiver part of a simple UART, that is designed to receive one data byte at a time at 9600 Baud with no parity and one stop bit.

Assignment

A proposed design for your UART receiver would include:

- A clock step-down counter to divide your input clock (100 MHz) to a roughly symmetrical clock that is 16 times the serial baud rate
- A state machine that does the following
    1. Detect the rising edge of the start bit
    2. Sample the input waveform at the center of each of the 8 data bits
    3. Send the data bits to an 8-bit shift register
    4. Latch the shift register output at the end of the data byte
- Send the 8 output bits to a 7-segment LED display. You can use the same four-digit LED hex display (disp4.vhd) that you used in Lab 4. Since you only want to display two digits, set the higher 8 bits of the display component to a constant "00000000".

Simulating your design

Simulate the design in Vivado. Your test bench stimulus should produce a valid RS232 data frame with correct 9600 baud timing. The simulation clock frequency should match the 100 MHz board clock on the BASYS3.

Implementing the design

After you have sucessfully simulated the UART receiver, implement it on the Basys3 developer board. Choose one of the available PMOD ports for the RS232 interface module, and assign the appropriate I/O pins in your user constraints.

Connect the RS232 interface module to your computer's serial port through the provided null modem cable. Open a terminal and type "minicom" from the command line for a text-based serial terminal emulator. You may ask the instructor for help configuring and using Minicom

From Minicom, you can transmit individual characters to the UART receiver, and verify that the correct ASCII values of those characters are correctly received.