System Design Document for the Sequential Up/Down Counter

University at Buffalo, The State University at New York
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1. Introduction

1.1 Overview

A sequential up/down counter is a device which counts up or down by integer increments of one. This up/down counter increments or decrements the output once per second and features clamping. Clamping is a function that the limits the possible values of an output, in this case when the counter reaches a maximum or minimum value it stops counting rather than overflowing. The inputs to this counter are provided by a slider switch which controls the direction of counting and a pushbutton which resets the counter to zero. This circuit was designed on paper and then implemented and tested on a Xilinx FPGA using the Xilinx Vivado CAD tool. The output is displayed on the board using the four LEDs located on the board.

1.2 Document Scope

This document has been written to provide information regarding the counter circuit developed in Lab 3 of EE478. The inputs, outputs, and operation of this device are described below as well as details regarding implementation on an FPGA and testing using a simulated test bench.

1.3 Intended Audience

This document is intended for use by the EE478 TAs and professors for use in grading as well as by the members of group 1L in the Monday 9am lab session.

2. System Design Overview

2.1   System Block Diagram and Description

The counter takes three 1-bit inputs UD, R, and clk and produces a 4-bit output Y. The UD input controls the direction of the counter, with the counter incrementing when UD=1 and decrementing when UD=0. This input is connected to the first slider switch on the Xilinx board. The input R is connected to a pushbutton on the Xilinx board and rests the count to 0 when pressed. The clk input is connected to a 100MHz clock and controls the rate of the counting. The output Y is connected to the four LEDs on the Xilinx board and displays the current count value in 2's complement binary. This is shown in the block diagram below
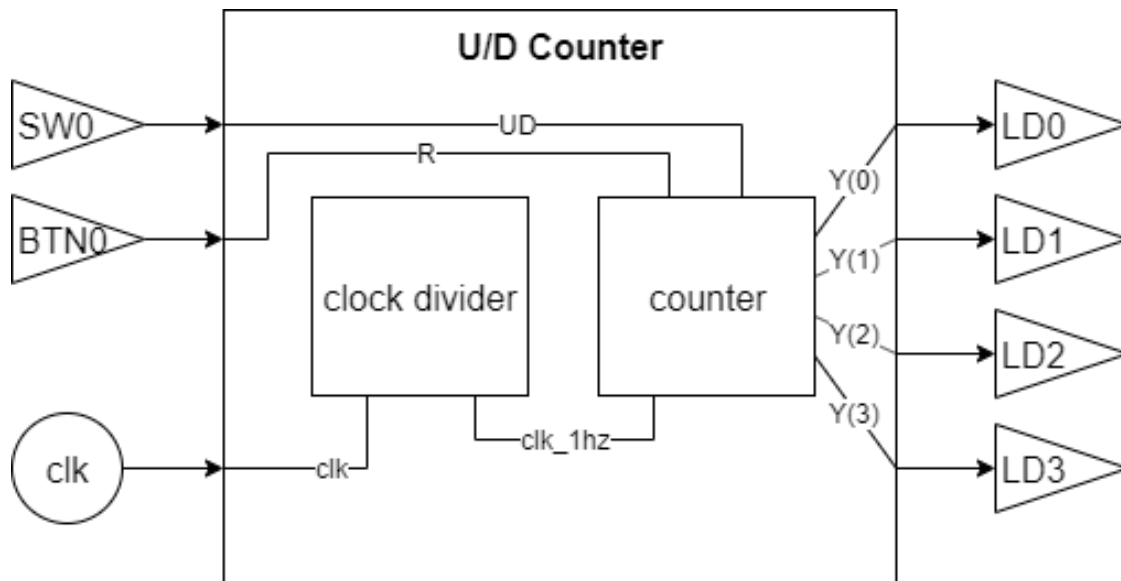

Figure 1: U/D Counter System Diagram

The clock input 125 MHz clock is fed to a clock divider process which generates a 1Hz clock signal. This slower clock signal and the switch and button inputs are connected to a counter module which implements the U/D counter functionality to produce the 4-bit output Y that is displayed on the LEDs.

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2.2 Clock Divider

This process implements a simple clock divider which takes the 1-bit 150MHz clock input and produces a 1-bit 1Hz clock signal clk_1hz. This is done by counting 150,000,000 clock cycles of the 150 MHz clock with clk_1hz being low for the first half of this period and high for the remainder. This circuit is implemented as shown in the following diagram

Figure 2: Clock Divider Circuit

2.3   Counter

This process takes three inputs: the 1-bit clk_1hz signal generated by the clock divider, the 1-bit UD value, and a 1-bit reset signal R. Every 1Hz clock cycle +1 or -1 is added to the current count value, until the value reaches -8 or 7. At this point the value 0 is added instead such that the output stops at the maximum values. If the reset button is pushed the counter value is reset to 0. This circuit is implemented as shown in the following diagram
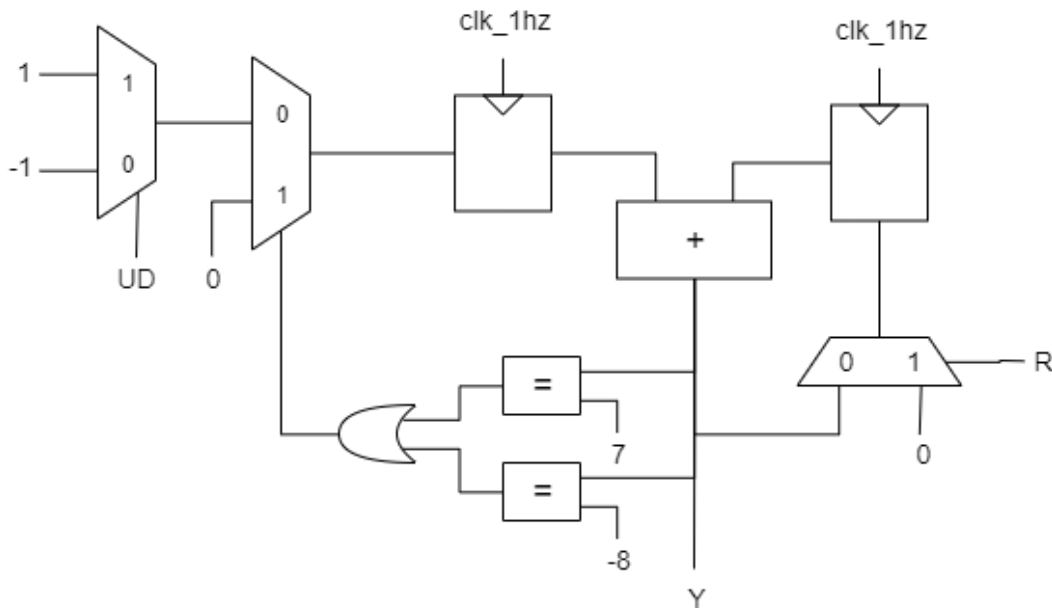

Figure 3: U/D Counter with Clamp

3. Testing and Verification

To ensure that our circuit functioned as intended we performed two forms of testing. First we simulated the designed using Xilinx Vivado and examined the simulated response to different inputs. After debugging and iterating, we synthesized our design and loaded it onto an FPGA where we performed testing of the physical circuit.

3.1   Testbench and Simulation

To test our design in simulation we developed a test bench which tests the full range of functionality of the circuit. Our simulation first creates an U/D sequential counter module, then drives the inputs to important test values. We then visualized these circuits using the ISim tool in Xilinx Vivado and compared the output to the expected values. Simulation was performed for 3 conditions with the period of counting reduced to much below 1Hz for ease of testing

3.1.1 Counting Up

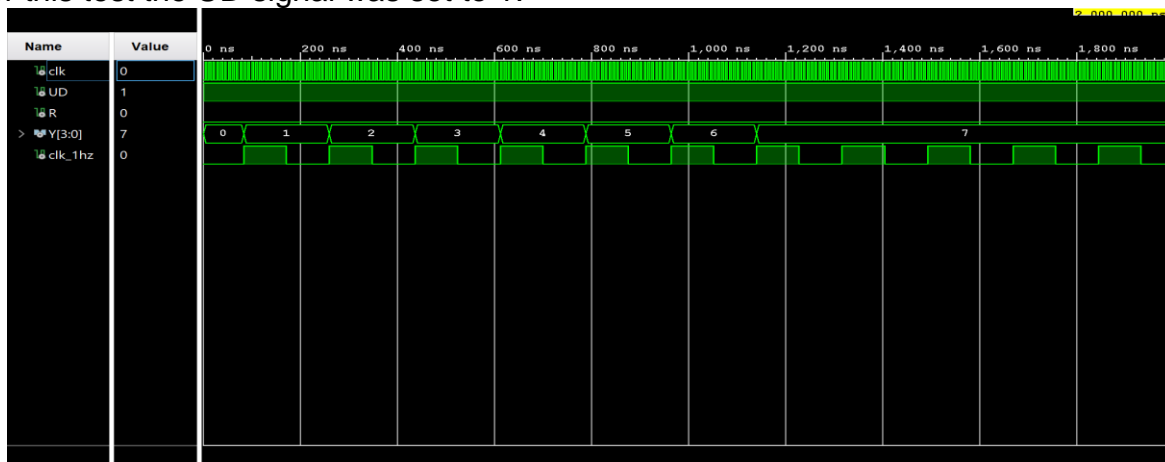For this test the UD signal was set to 1.

Figure 4: Counter Increasing

Here we see that starting from zero the output Y increases by 1 on every rising edge of the clk_1hz until it reaches the value 7, at this point it clamps to the value 7 and stops counting

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3.1.2 Counting Down

For this test the UD signal was set to 0.

Figure 5: Counter Decreasing

Here we see that starting from zero the output Y decreases by 1 on every rising edge of the clk_1hz until it reaches the value -8, at this point it clamps to the value -8 and stops counting

3.1.3 Resetting the Count

For this test we set the value of UD to 1, then configured the simulation to trigger the inset R as a one shot every 100 clk cycles. This pulsed the reset line to simulate a user pushing the reset button
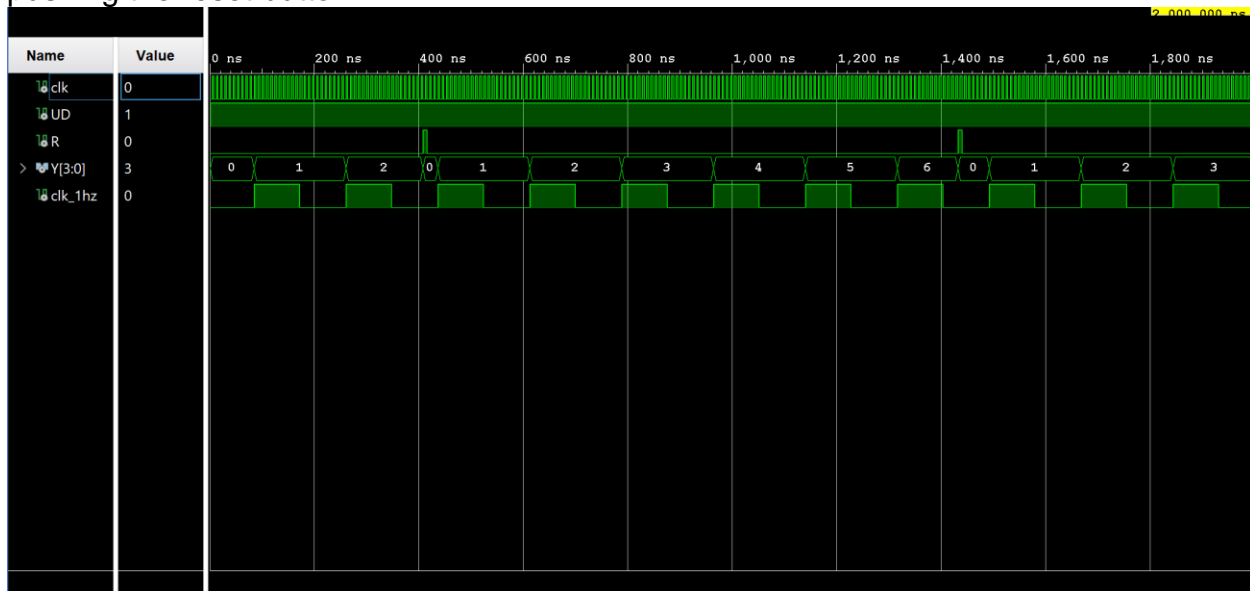

Figure 6: Counter Resetting

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3.2 Objective Verification

Once we constrained and synthesized our design we loaded it onto the FPGA and tested the circuit by manipulating the slider switch built into the Xilinx board. This controlled the UD input and selected the direction of counting. Once we observed that the output incremented and decremented appropriately while stopping at the maximum and minimum clamp values, we used the pushbutton to check that the output could be reset to zero. We also compared the frequency of incrementing/decrementing to a wall clock to ensure that the appropriate period was being observed.

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Glossary

This section includes helpful supplemental information to aid in understanding the content of this report.

List of Abbreviations

Below are selected abbreviations used in this document

- VHDL: VHSIC Hardware Description Language
- VHISC: Very High Speed Integrated Circuit
- FPGA: Field Programmable Gate Array
- LED: Light Emitting Diode
- CAD: Computer Aided Design
- MUX: Multiplexor
- XOR: Exclusive Or
- ALU: Arithmetic Logic Unit
- ASR: Arithmetic Shift Right
- U/D: Up/Down

Hardware References

- Zybo Z7 Manual (DigitalInc)
- Xilinx Vivado CAD tool (Xilinx)