Freescale Semiconductor, Inc.
Application Note

Document Number: AN5220
Rev. 0, 03/2016

MPC5748G Hardware Design Guidelines

By: **Masato Oshima**
Armin Winter
Jesus Sanchez
Chris Platt

Contents

1 Introduction

1.1 Purpose and Scope

The MPC5748G and MPC5746C microcontrollers are members of a 32-bit microcontroller family built on the Power Architecture® technology. This family of devices is designed to address a wide variety of automotive applications including but not limited to high end gateway, combined body controller and gateway, central body, vehicle body controllers, smart junction box and front module applications.

The purpose of this document is to describe hardware design considerations when developing hardware for the MPC5748G microcontrollers but is also mostly valid for the MPC5746C device. (Refer to NXP Application note AN5114 for details of differences between the two devices on www.nxp.com). It will cover topics such as voltage regulator and power considerations, clock generation, decoupling, etc. Detailed reference design schematics and descriptions of the main components, as well as some general hardware recommendations are provided within this document. Comparisons to earlier NXP devices targeted at similar applications are also provided where appropriate.

2 Power Supply

The MPC5748G device has multiple supply pins for the core, I/O (Input/output), flash and analog supplies. All such pins must be connected to the proper supply voltage for proper operation. All VSS pins need to be connected to the external power supply ground. Table 1 shows the power supply pins associated with the device and the required conditions applied to them.

NOTE

Do not leave any of the supply pins unconnected!

Table 1. Power supply pins

Supply Pin	Voltage	Description
VDD_LV	1.25V	Core logic low voltage supply
VSS_LV	0V	Core logic low ground voltage supply
VRC_CTRL	Output	PMC (Power Management Controller) Voltage Regulator Ctrl Output. The VRC_CTRL pin controls the base of the ballast transistor, while the VDD_LV pins of the device connect to the emitter of this pass device.
VDD_LP_DEC	Decoupling pin	Attach a low power decoupling capacitor (1uF)
VDD_HV_A	3.3V / 5V	I/O segment A supply voltage
VDD_HV_B	3.3V (FEC) 5V (non FEC)	I/O segment B supply voltage
VDD_HV_C	3.3V (MLB) 5V (non MLB)	I/O segment C supply voltage
VSS_HV	0V	I/O ground voltage supply
VDD_HV_FLA	Decoupling 3.3V	Flash regulator bypass capacitor in 5V mode. 3.3V Need to be supplied when in 3.3V mode.
VDD_HV_ADC0	3.3V / 5V	ADC0 supply voltage
VDD_HV_ADC1	3.3V / 5V	ADC1 supply voltage
VSS_HV_ADC0	0V	ADC0 ground voltage supply
VSS_HV_ADC1	0V	ADC1 ground voltage supply
VDD_HV_ADC1_REF	3.0V …5.5V	ADC1 reference voltage supply
VIN1_CMP_REF	3.15V…3.6V	Analog Comparator reference voltage supply
VSS_HV_VPP	0V	Tie to VSS_HV

VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3 V or 5 V. VDD_HV_A is the main I/O supply voltage, VDD_HV_B is the supply for the FEC (Fast Ethernet Controller) and VDD_HV_C is the supply for the MLB (Media Local Bus). If desired, this allows the user to have different I/O voltage operation in parallel. This means some I/O segments can operate in 5 V mode, whereas the other(s) run at 3.3 V. However, care must be taken with ADC inputs that operate across the I/O segments. The core supply voltage (VDD_LV) is typically 1.25 V. For more information, see the Electrical Specifications section within the data sheet.

2.1 Power Management Unit (PMU) Overview

The Power Management Unit (PMU) implements a linear voltage regulator to generate the internal VDD_LV digital supply from an external 3 V to 5.5 V supply. This voltage regulator is called FPREG (Full Power Regulator) which is used during full operating modes.

It also contains an option to bypass this regulator and instead use an externally supplied 1.25 V input. In addition there are two low power regulators, ULPREG (Ultra Low Power Regulator), used in STANDBY modes and LPREG (Low Power Regulator) used in low power modes except STANDBY, both of which can be active regardless of how the main 1.25 V is being supplied.

An additional regulator (FLASHREG) for the flash block is also within the PMU and is active when the device is in the 5 V mode, with a bypass option at lower voltages. It is highly recommended that users use the FLASHREG regulator rather than an external supply. Various voltage monitors also reside within the PMU, allowing the visibility of internal regulating points and external supplies.

Figure 1 shows the block diagram of the power scheme on the device.

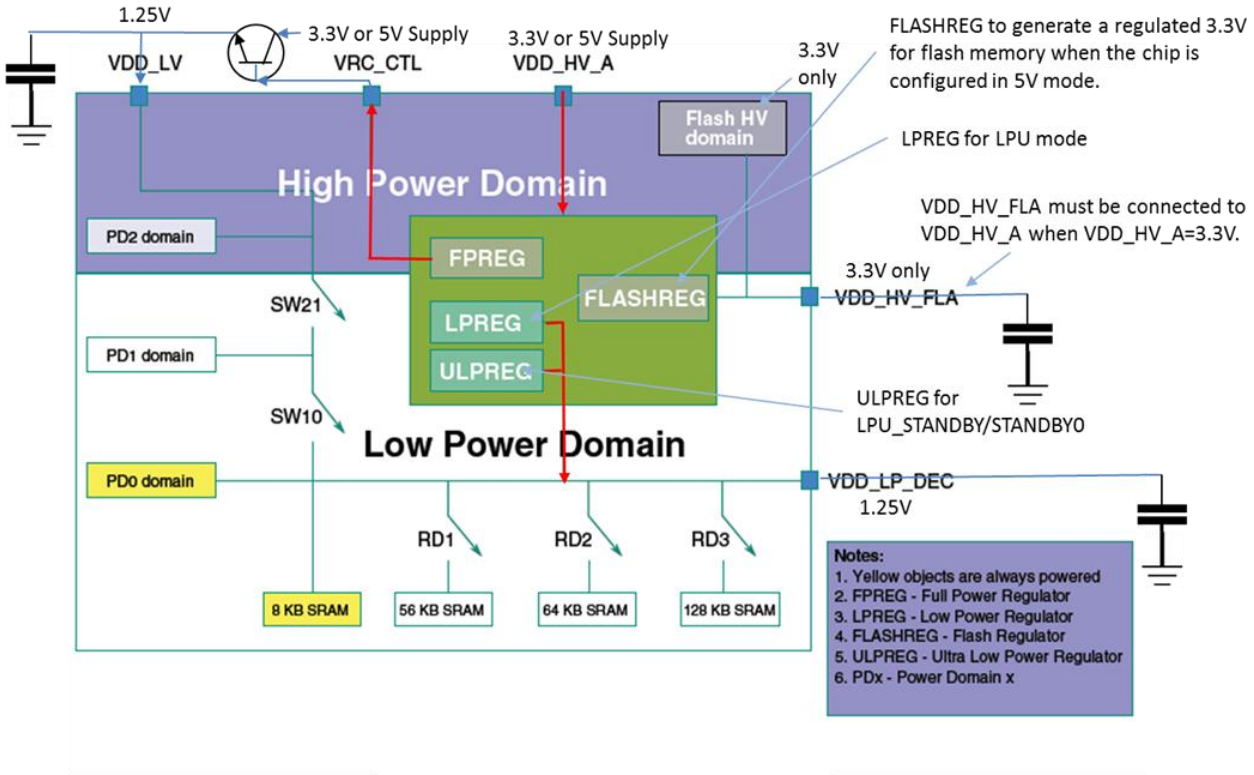


Figure 1. Power block diagram

2.2 Power Control Unit (PCU)

The Power Control Unit is used to reduce the overall device power consumption. Power can be saved by literally disconnecting parts of the device from the power supply via an on-chip power switching device. The device is grouped into multiple parts having this capability which are called Power Domains (PDx).

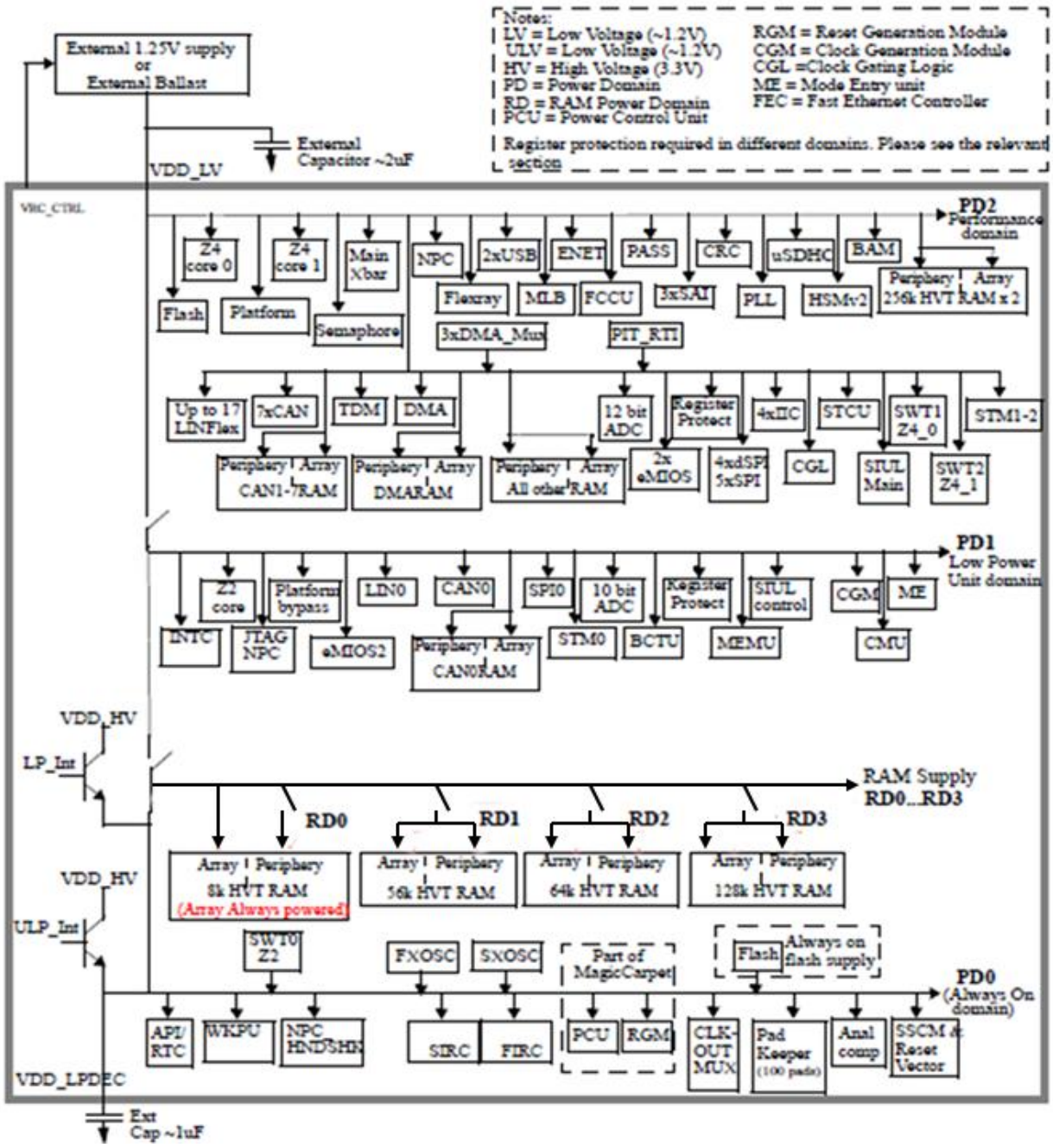


Figure 2. Power domains

Power Domain 0 (PD0)

PD0 is the 'always ON' power domain on the device. This domain plays an important role in maintaining the device configuration as well as providing basic autonomous functionality with very low power. This domain allows the SWT0 (Software Watchdog Timer) to continue running even when in the lowest power state.

Power Domain 1 (PD1)

PD1 contains the computational blocks that comprise the LPU (Low Power Unit) domain, and helps provide the SMS (Small Microcontroller System) configuration for applications which do not need maximum performance but are sensitive to power consumption. This domain is power gated OFF in STANDBY and LPU_STANDBY modes. This is basically a full small microcontroller system, aimed at handling the low power profiles and also emerging standards such as pretended networking.

Power Domain 2 (PD2)

PD2 consists of various high performance blocks. This domain is power gated off in STANDBY mode and all LPU modes and includes the cores and main platform.

Flash HV Power Domain

The Flash HV power domain consists of high voltage devices inside the flash memory module and is not listed in Figure 2. This domain must be kept powered at all times while the chip is not in the 'power on reset' state. The domain is supplied by the Flash Regulator.

SRAM (Static RAM) Domains

The MPC5748G microcontroller has a total of 768 KB SRAM, which is divided among the SRAM domains (known as RDx, where x is from 0 to 3) as follows:

- The **RD0** domain contains 8KB SRAM that is always available, and resides in the PD0 power domain. The RD0 SRAM domain together with the ULPREG regulator helps provide brownout protection.
- The **RD1** (56k), **RD2** (64k), and **RD3** (128k) SRAM domains, can be independently configured to be available during STANDBY.
- The remaining 512 KB SRAM resides in the **PD2** power domain. This SRAM is completely powered off in STANDBY and LPU modes, but is always powered on (available) in RUN, HALT and STOP modes.

NOTE

All SRAM is available in RUN, HALT, and STOP modes.

When a power domain is disconnected from the supply, the power consumption is reduced to zero in that domain. One effect of this is that status information or register settings contained in a disconnected power domain are lost. When re-connecting a power domain to the supply voltage, SW needs to ensure corresponding SRAM gets re-initialized along with any registers.

Power domains are controlled on a device mode basis. For each mode, the user can configure whether a particular power domain is connected to the supply voltage (power-up state) or disconnected (power-down state).

Maximum power saving is reached by entering the *STANDBY* mode. Exiting *STANDBY* mode can only be done via a system wakeup event or reset as all power domains other than power domain #0 are in the power-down state.

A detailed description of device modes and wake-up events is provided within the reference manual but a summary is shown in figure 3.

Operating Mode	Powered Domains	Chip Features						Clock Sources					Wake up Options
		Z2 core (PD1)	Z4 cores (PD2)	Powered SRAM Domains	Flash (PD2)	LPU Peripherals (PD1)	Main Peripherals (PD2)	16 MHz IRC	8MHz-40MHz FXOSC	Phase Locked Loop (PLL)	128 kHz IRC	32 kHz SXOSC	
RUN	PD0 PD1 PD2	OPT	OPT	All	OPT	OPT	OPT	OPT	OPT	OPT	OPT	OPT	N/A
WAIT/HALT	PD0 PD1 PD2	CG	CG	All	OPT	OPT	OPT	OPT	OPT	OPT	OPT	OPT	EIRQ WKPU RTC / API PIT Anal Comp Anal trig
STOP	PD0 PD1 PD2	CG	CG	All	CG	OPT	OPT	OPT	OPT	CG	OPT	OPT	
LPU_RUN	PD0 PD1	OPT	Off	RD0 RD1 RD2 RD3	Off	OPT	Off	OPT	OPT	Off	OPT	OPT	
LPU_STOP	PD0 PD1	CG	Off	RD0 RD1 RD2 RD3	Off	OPT	Off	OPT	OPT	Off	OPT	OPT	
STANDBY/ LPU_STANDBY	PD0	Off	Off	RD0 RD1 RD2 RD3	Off	Off	Off	OPT	OPT	Off	OPT	OPT	WKPU RTC/ API Anal Comp

Figure 3. User operating mode settings and options

Key:

- OPT – Optionally configured (enabled or disabled)
- CG – Clock Gated (Power still applied but clock gated)
- Off – Powered off

Please note that PD0 is always powered during normal device operation. Also note that depending on the specific device configuration there are from 1 to 3 on-chip RAM arrays. Array 0 contains multiple blocks of RAM of varying sizes and each is defined by an SRAM domain (RD0-3) which can be independently configured to be available or not during STANDBY modes. Any on chip RAM which is not assigned to one of the specific SRAM domains is part of the PD2 domain and will then only be available when PD2 is powered.

2.3 VDD_LV Power Supply Strategies

For RUN modes, the device supports two different power supply strategies, internal regulation mode and external regulation mode.

2.3.1 Internal Regulation Mode

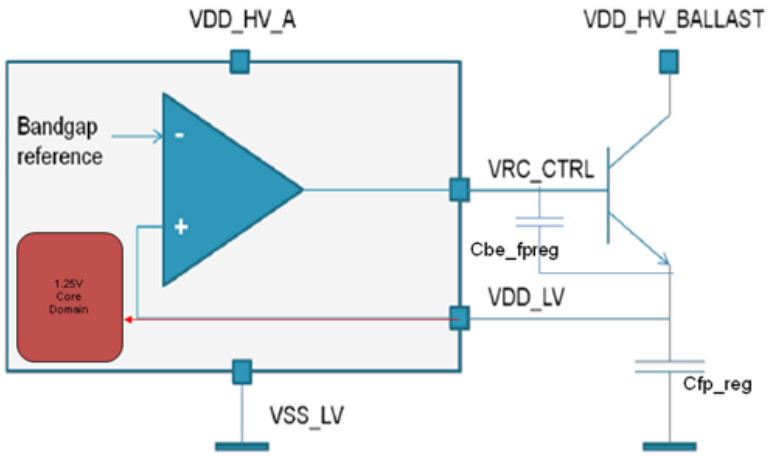


Figure 4. Internal regulation mode

Figure 4 shows the power supply in internal regulation mode. The 1.25V core logic voltage (VDD_LV) is generated by an external ballast transistor.

Table 2 shows the currently supported bipolar transistors, which should be chosen depending on the device performance requirements. Please see the current consumption section of the data sheet for recommended usage:

Table 2. Supported bipolar transistors

PART	MANUFACTURER	RECOMMENDED DERIVATIVE
BCP68	ONsemi	BCP68
	NXP	BCP68-10; BCP68-25
	Fairchild	BCP68-10; BCP68-25
BCP56	ONsemi	BCP56-10
	NXP	BCP56-10; BCP56-16
	Fairchild	BCP56
	ST	BCP56-16
MJD31	ONsemi	MJD31; MJD31C
	Fairchild	MJD31; MJD31C

For the Cfp_reg capacitor, a value of around 2.2 µF is recommended. This capacitance should not exceed 3 µF when accounting for variation over temperature, tolerance and drift.

For the Cbe_fpreg capacitor, an X7R type unit with a 10% tolerance is recommended. This should be a 3.3 nF value when using BCP68 and BCP56 ballast transistors, and a value of 4.7 nF when using an MJD31 transistor.

2.3.1.1 Selecting the NPN External Ballast Transistor

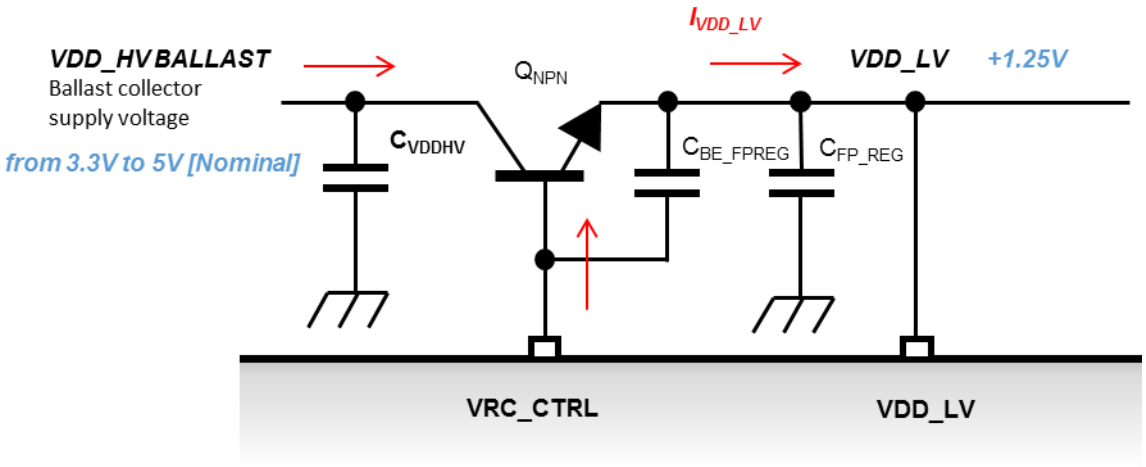


Figure 5. NPN Ballast transistor circuit

The maximum VDD_LV current capability [I_{VDD_LV}] (refer to figure 5) using a NPN External Ballast transistor [Q_{NPN}], is determined by the maximum allowed power of the device. The designer should consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- Package type
- Dissipation mounting pad area on the PCB
- Ambient temperature

Like maximum power supply voltages, the maximum junction temperature is a worst case limitation which should not be exceeded. This is a very important point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistors packages, the maximum power dissipation is specified at +25 °C; and above this temperature, the power derates to the maximum Junction Temperature (+150 °C). The Rth_{JA} depends considerably of the transistor package and the mounting pad area. The final product thermal limits should be tested and quantified in order to ensure acceptable performance and reliability.

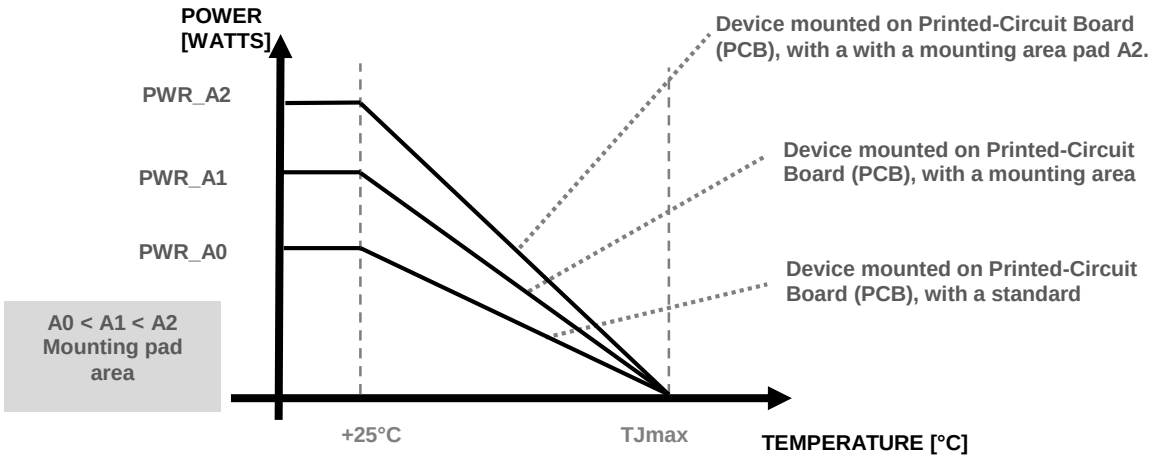


Figure 6. Maximum power dissipation versus temperature

Figure 6 shows how the maximum power dissipation is affected by temperature. The maximum power dissipation PWR_{MAX} by the device is given by:

Equation 1.

$$PWR_{MAX} = \frac{TJ_{MAX} - T_{AMB}}{Rth_{JA}}$$

where T_{AMB} is ambient temperature, TJ_{MAX} is maximum junction temperature and RthJA is the Junction to Ambient Thermal Resistance of the Ballast transistor mounted on the specific PCB.

2.3.1.2 Static Thermal Analysis

It is extremely important to consider the derating of the power device above of +25 °C (typical value for transistors). This guarantees that the junction temperature will be lower than the maximum operating junction temperature allowed by the device supplier. The following static thermal analysis demonstrates how the maximum power dissipation and the maximum supply current can be estimated for different voltage levels of VDD_LV.

NOTE

The data used in the next examples are purely for demonstration purposes and should not be taken as specifications for particular systems. For specific calculations, please refer to the device datasheet.

Example: Design parameters:

- $VDD\_HV\_BALLAST_1 = 5\ V$
- $VDD\_LV\ = 1.25\ V$
- $Rth_{JA}\ = 80\ °C/W$
- $T_J\ = +150\ °C$
- $Tamb_{MAX}\ = +85\ °C$

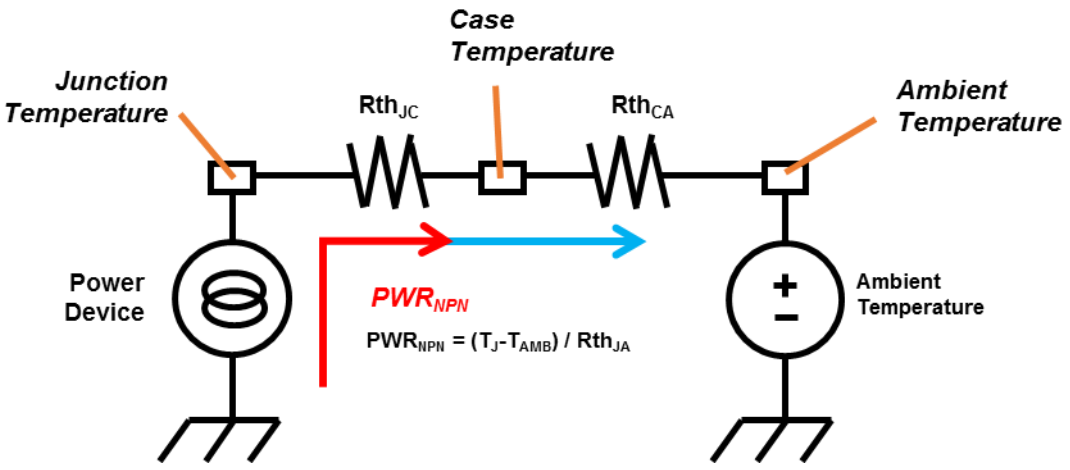


Figure 7. Static thermal analysis

As per figure 7 the analysis is as follows:

Equation 2.

$$Pwr_{NPN} = \frac{T_J - Tamb_{MAX}}{Rth_{JA}} = \frac{150°C - 85°C}{80°C/W} = 812.5\ mW$$

Thus, the maximum supply current at $VDD\_HV\_BALLAST_1$=5 V, is determined as:

Equation 3.

$$I_{VDD\_LV} = \frac{Pwr_{NPN}}{VDD\_HV\_BALLAST_1 - VDD\_LV} = \frac{812.5mW}{5V - 1.25V} = 216.66\ mA$$

For $VDD\_HV\_BALLAST_1 = 3.3\ V$, the maximum supply current is:

Equation 4.

$$I_{VDD\_LV} = \frac{Pwr_{NPN}}{VDD\_HV\_BALLAST_1 - VDD\_LV} = \frac{812.5mW}{3.3V - 1.25V} = 396.341\ mA$$

As a result of these examples, the maximum power dissipation of the ballast transistor is 812.5 mW. At this value, the transistor will reach its maximum operating temperature rating of 150 °C.

Transistor specifications generally give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C). The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature. The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.

2.3.2 External Regulation Mode

Fig 8 shows the regulator in external regulation mode.

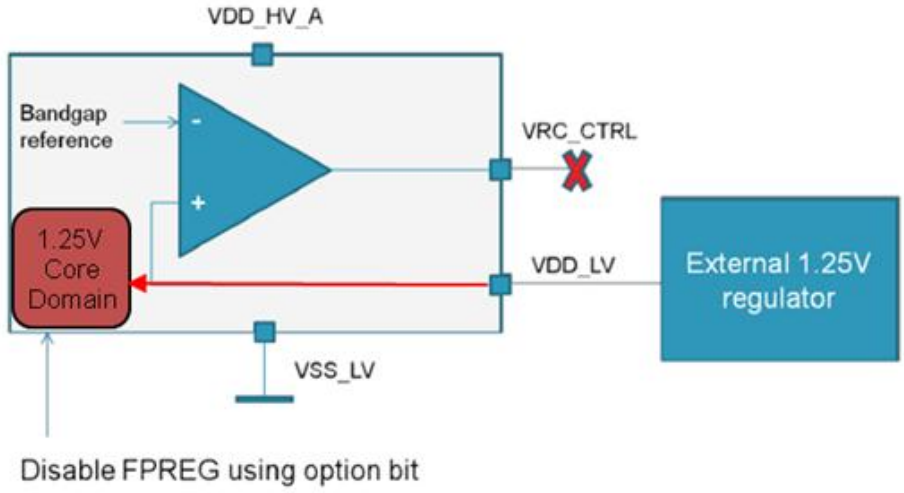


Figure 8. External regulation mode

In this configuration, the 1.25 V core logic voltage (VDD_LV) is generated by an external power supply. When using an externally supplied core logic power supply, it is acceptable to leave the VRC_CTRL pin floating.

If the application is using this mode, then that 1.25 V supply will continue to be connected to the PD2 domain unless the customer application takes steps to remove it. Hence, depending on the application configuration there may be leakage from the PD2 area in STANDBY or LPU modes. This can be avoided by disconnecting the external supply when the device has entered the low power states, although it must be re-applied to enable exit from the low power states.

NOTE

Since the default configuration at boot-up is internal regulation mode, when external regulation is used, the user option bit UTEST_MISC[REG_TYPE] must be set to disable the FPREG regulator.

2.4 Analog Power Supply

The MPC5748G microcontroller family contains two Successive Approximation Register (SAR) Analog-to-Digital Converters. There is one 10bit ADC (ADC0), as well as a 12bit ADC (ADC1) which operate completely independently of each other. Since each ADC has its own digital interface and analog unit they also require independent power supplies.

The ADC channels are independent and no channels are shared between the ADC modules. This is in an enhancement compared to the MPC56xxB/C/D family.

ADC1 supports the option to interface a high precision ADC reference on VDD_HV_ADC1_REF. It is possible to directly connect VDD_HV_ADC1_REF to VDD_HV_ADC1 without impacting device performance.

The ADC reference (VDD_HV_ADC1_REF) is also capable of being lower than the ADC analog supply (VDD_HV_ADC1). Hence VDD_HV_ADC1_REF is independent to VDD_HV_ADC1.

For example, it is possible to allow VDD_HV_ADC1_REF to be 3.3 V whilst VDD_HV_ADC1 is 5 V.

On some smaller packages, those VDD_HV_ADC1_REF pads are bonded internally to remove the requirement for physical device pins. This, to minimize the number of power / ground pins and maximize the number of I/Os on the smaller package options.

Due to the requirement to be compatible with MPC564xB/C, there are four pins as a minimum for the analog connections:

- VDD_HV_ADC0
- VSS_HV_ADC0
- VDD_HV_ADC1
- VSS_HV_ADC1

The 12 bit ADC will have its analog supply and reference bonded out individually, but this will be package dependent as mentioned above. For the 176LQFP they will be shared to maintain compatibility with the MPC564xB/C family. For the BGAs, a separate VDD_HV_ADC1_REF pin will be available.

NOTE

Do not have the VDD_HV_ADC1_REF pin floating.

It needs to be connected to a supply/reference voltage.

For proper operation of the Analog-to-Digital Converter, a noise-free analog supply is essential. Any noise on the analog supply and, or reference voltage rail severely degrades the performance of the converter, leading to inaccurate and, or unstable converted counts.

Special care has to be taken during PCB design to avoid noise on the analog supply and reference rail.

The user is able to switch in different references to the ADC for test conversions. This is to offer a possibility to verify that the ADC is working correctly.

Four references are offered:

- Vssa
- 1/3 Vdda
- 2/3 Vdda
- Vdda

Both ADCs will also have access to a number of internal diagnostic signals:

- Vrefh
- Internal Band gap
- ADC analog supply

In addition the 12 bit ADC (ADC1) is able to monitor various signals inside the PMC analog block.

2.5 External Decoupling Capacitor Connectivity

An external capacitor needs to be connected to VDD_LV. The MPC564xB/C derivatives used a slightly different scheme due to the size of the capacitor (~40 µF).

However, for MPC5748G, the external capacitance can be kept much smaller (~2.2 uF) for various customer requirements, such as cost, board space and inrush current. Figure 9 shows the required voltage regulator capacitances.

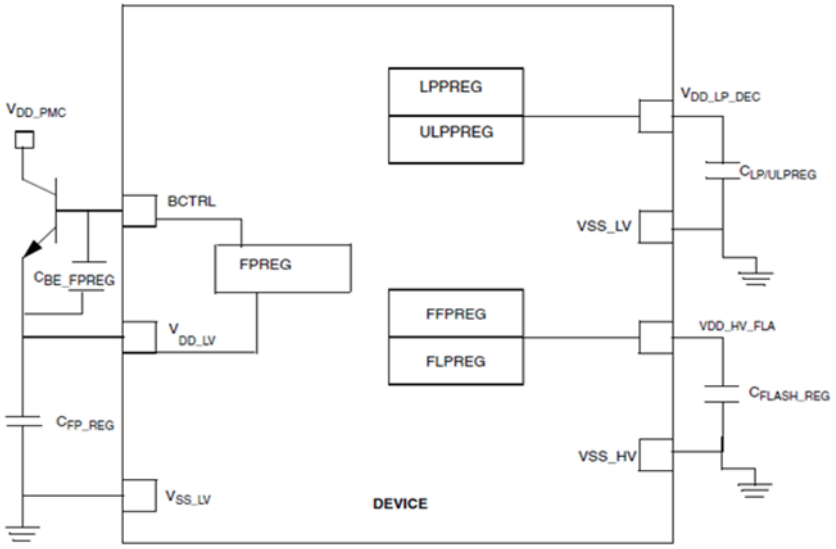


Figure 9. Voltage regulator capacitance connection

2.5.1 Decoupling/Bypass Capacitors

Users should always make sure that the traces for decoupling capacitors are as short as possible. Shortening the capacitor traces to/from the ground/power plane is THE MOST IMPORTANT concern for making a low inductance connection.

It is recommended to use the smallest package capacitor available for power supply bypassing near individual pins.

For tantalum and electrolytic capacitors, make sure to select a high enough voltage to take into account the derating over time. It is typical want to pick a voltage at least 2X higher than the voltage being applied to the cap. The derating curve can be found in the data sheet of the capacitor and should be verified that the voltage capacitor was selected is enough. Figure 10 shows the recommended decoupling scheme for the device.

The user must take great care not to place so much bulk/bypass capacitance that the power rail will get out of the correct power-up or power-down sequence (this is the order of power supplies starting-up and powering-down).

In order to design a good decoupling scheme, especially for very fast switching interfaces like ETHERNET, and USB, FLEXRay, etc., care must be taken to pair power and ground planes as close as possible to each other (<10 mils). This creates an effective interplane capacitance. This greatly reduces noise and increases power supply stability at the pins because of the extremely low inductance of this kind

of capacitance in these layers. The number of discrete capacitance can also actually be reduced because the effective capacitance is greatly increased and the impedance of the power distribution network is reduced across a very broad frequency range.

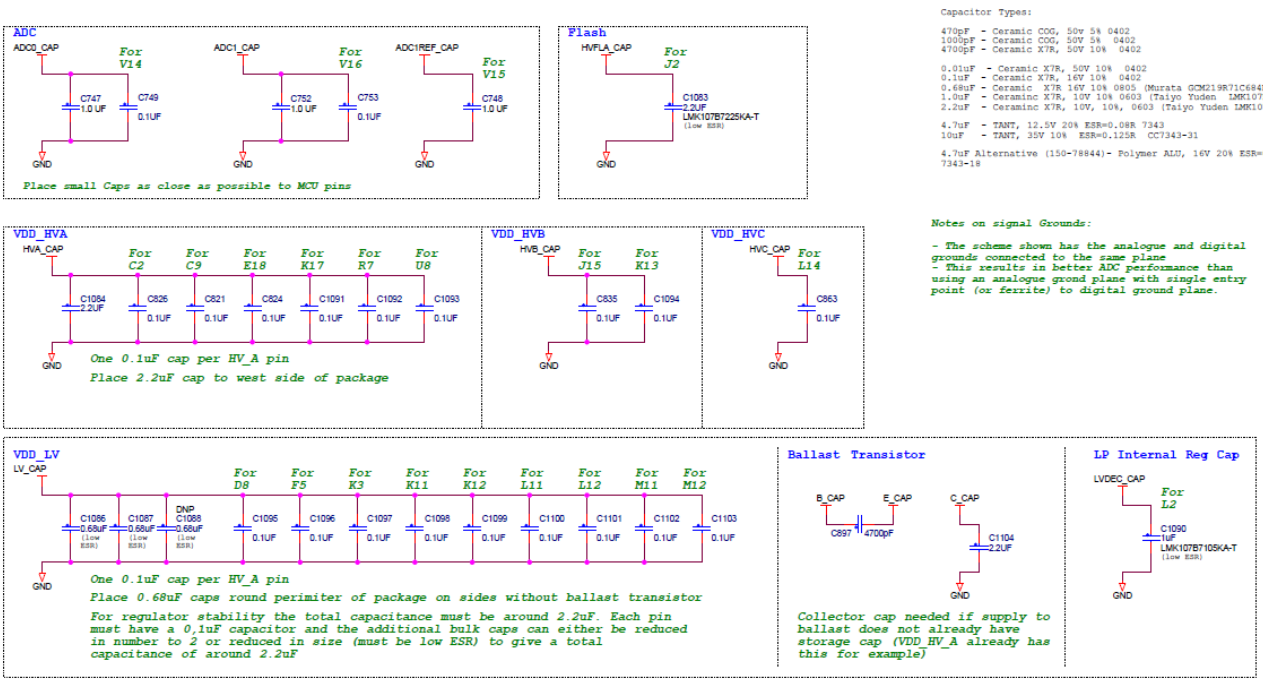


Figure 10. Recommended Decoupling Capacitors

2.6 Power Sequencing

For all MPC5748G derivatives, no requirements are placed on the power up/down sequence of the various power pins to ensure the correct reset state for all the modules.

However, it is recommended that no voltage larger than a diode drop (~0.7 V) should be applied to any input pin prior to powering up the device. Voltages applied to pins of an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results. The user should also ensure that:

- Internal pull resistors implemented on all independent IO domains.
- All I/O domains effectively pulled (level shifted) to a safe state in all conditions.
- When using the internal regulator to control an external ballast then the PORST can be pulled to a safe state.
- When using an external 1.2 V supply then the external PORST pin must be driven to keep the device in reset during the power-up process.
- For pins that are powered prior to device power up a series resistor should be used to limit the current and to keep the voltage below 0.7 V. (See injection Current Application note AN4731).

2.7 Voltage Monitoring

The MPC5748G microcontroller features internal voltage monitoring to ensure supplies are within their correct operating ranges. If any ‘essential’ supply falls outside of its correct operating range, the voltage monitors take the device into a ‘safe, power on reset’ state. The following diagram describes the various voltage monitors and what supplies (and what point on supply) they monitor. Refer to the data sheet for details on electrical specifications for these voltage monitors.

The Brownout (BO) detector monitoring 8 kb standby SRAM supply ensures the voltage on the SRAM supply is good enough to retain its array content and, if voltage drops too low, this detector is set and software can read this upon reset recovery as explained in the PMCDIG SGSR[BROWNOUT].

There is no voltage monitoring on the VDD_HV_B and VDD_HV_C I/O segments. In most cases those segments will be connected VDD_HV_A at the PCB level.

For applications not following this approach, external precautions have to be taken when splitting the I/O domains.

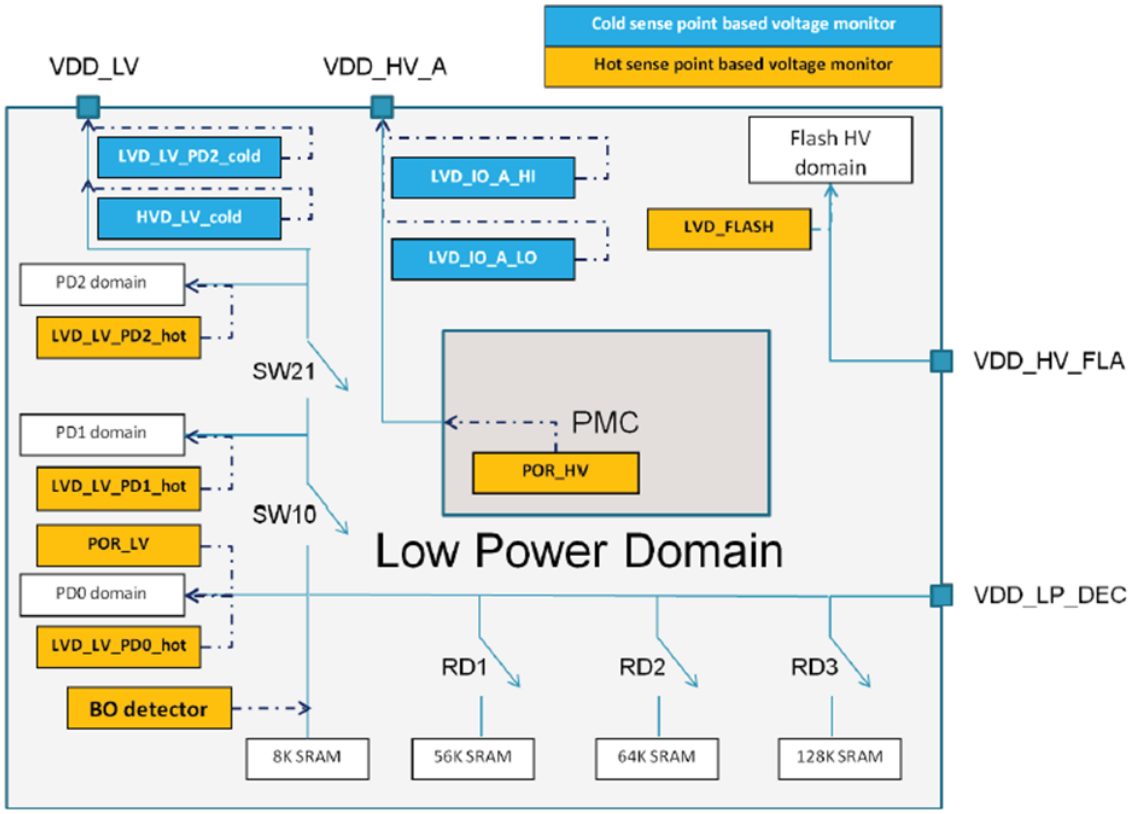


Figure 11. Voltage Monitoring

3 Clocking

The main differences of the clocking architecture of the MPC5748G family compared to the MPC560xB family is the ability to reduce the cores and platform clocks during low computational activity periods, while maintaining the majority of the peripheral operation (timer, comms, adc, etc.).

The MPC5748G allows the LPU and associated peripherals (in LPU domain) clock frequency to be scaled to optimize power consumption when operating in LPU mode.

As is the case with MPC5646, the MPC5748G boots from the Z4 core with the internal 16 MHz RC oscillator (FIRC), and uses this as a backup clock in the event of a PLL or oscillator failure. The microcontroller also supplies a method to ramp the clock frequencies and activate logic at controlled rates to avoid transient power spikes that exceed the capabilities of the external power supply.

The MPC5748G clocking architecture allows MBIST (Memory Built in Self-Test) and LBIST (Logic Built in Self-Test – Not present on MPC5746C) to complete execution (and power up) in less than 10 ms.

3.1 System Clock Generation

The top-level system clock generation architecture is shown in figure 12 below. It gives the clock distribution to the cores and peripheral modules on the MPC5748G. All clock dividers and muxes are located and programmed in the CGM (Clock Generation Module) on the device, with the exception of the HSM (hardware Security Module) clock divider, FlexCANs, and FlexRay.

The MPC5748G supports seven synchronous clock nodes to support DFS (Dynamic Frequency Scaling). These groups can be classified into 3 categories:

- Fixed Frequency Group (F160, F80, F40, F20): This group will not scale down during DFS operation. It implies all the modules will continue receiving the same frequency (for example, PIT timers are operating at F40MHz and would not scale down).
- Scalable Frequency Group (S160, S40, S80): This group will scale down during DFS operation (for example, Z4a core is operating at S160 and would scale down as per configuration in MC_CGM_SC_DCn registers.
- Flexible Group (FS80): This group is configured to scale down along with the Scalable group during Linear DFS and is kept at a fixed frequency during Non-Linear DFS

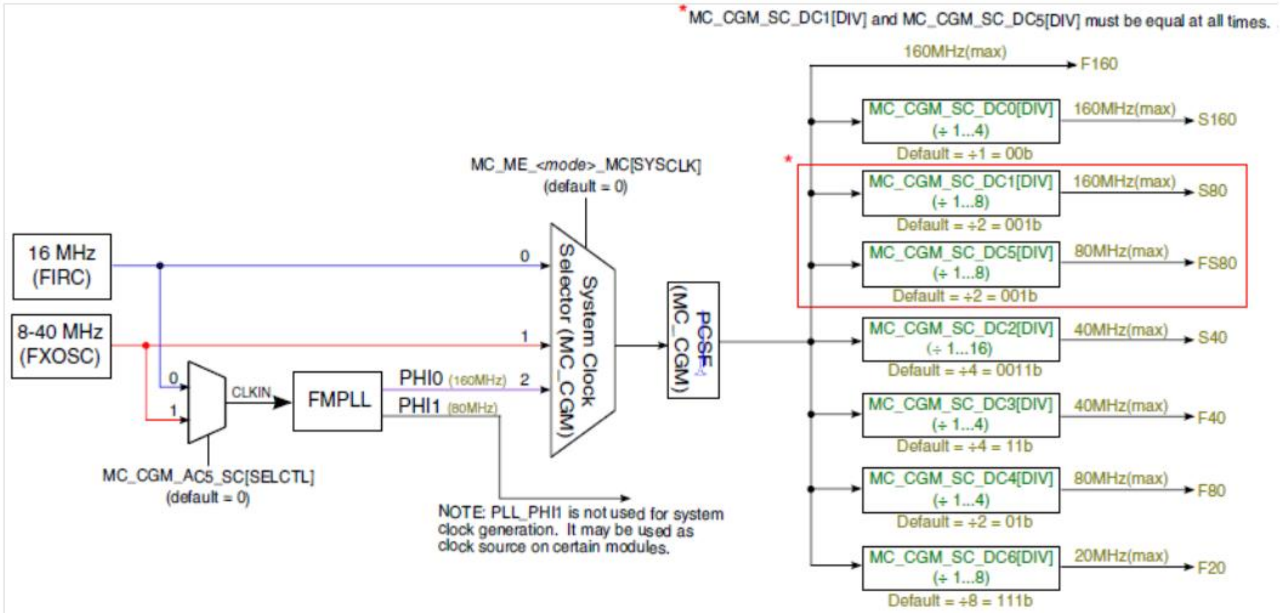


Figure 12. System Clock Generation

Chapter 8 of the reference manual contains tables detailing maximum clocks allowed per master/slave and peripherals.

3.2 HSM (Hardware Security Module) Clock Divider

The clock dividers for the HSM core and random number generator (TRNG) are located outside the HSM in the CGL (Clock Gating Logic). These dividers are controlled by the HSM.

The HSM contains an internal PIT/RTI block, which is clocked by the 16MIRC (FIRC) on the device. Again the divider is in the CGL and controlled from the HSM. The HSM has an internal clock monitor on its input clock, so there is no Clock Monitoring Unit (CMU) on the device for the HSM clock.

3.3 Ethernet Clocking

MPC5748G supports external clock sources for both MII and RMII Ethernet interface modes. The MII 100 clocks (TXCLK/RXCLK) are 25 MHz, and the RMII clock (REF_CLK) is 50 MHz .

MII and RMII clocking summary:

- MII 10 - 2.5 MHz on the Ethernet bus side (supplied by the PHY)
- MII 100 - 25 MHz on the Ethernet bus side (supplied by the PHY)
- Both RMII 10 & 100 - 50 MHz reference clock to ENET. Note that this 50 MHz clock should be provided to the RMII PHY.

The RXCLK pin is an input, used in MII mode only, and ignored in RMII mode. The TXCLK pin is an input, used in MII mode only and is shared with the REF_CLK input which is needed in RMII mode.

The REF_CLK is an input to the device and used in RMII mode. It is always fed into the device.

3.4 FlexRay Clocking

The Flexray protocol clock has an option to be sourced from either PLL_PHI_1 clock or the external oscillator (FXOSC). Clock selection is done in the Flexray block itself and the selection is output from the Flexray block to the CGL, where the actual clock mux is located. When the system clock is 80 MHz it also possible to drive FlexRay peripheral from the PLL clock.

3.5 FlexCAN Clocking

The FlexCAN protocol clock has an option to be sourced from either the FS80 or the external oscillator (FXOSC). Clock selection is done in the FlexCAN block itself and the selection is output from the FlexCAN block to the CGL, where the actual clock mux is located.

3.6 USB (Universal Serial Bus) Clocking

The 60MHz ULPI clock is generated by the USB PHY and used to drive the on chip USB2.0 modules (USBSPH and USBOTG).

3.7 uSDHC (Secure Digital High Capacity) Clocking

The uSDHCV2 controller is clocked from the divided system clock (80 MHz) and further divide the card clock (SD_CLK) down to 40 MHz as it has a max value of 52 MHz.

3.8 SAI (Synchronous Audio Interface) Clocking

The SAI's run on dedicated frequencies that are different from the system clock and this clock can be supplied internally or externally. In both cases the frequency of the audio bit clock needs to be closed loop controlled to remove long term drift.

In case the audio bit clock is provided from internal, the fractional clock divider is required to generate

22.57 MHz (44.1 KHz sample rate) or 24.57 MHz (sample rate of 48 KHz). As the peak jitter from the fractional divider is /2 x input clock, the input clock for the FCD (Fractional Clock Divider) needs to be selected with a frequency as high as possible to meet audio jitter requirements . Thus, the 160 MHz clock is used as an input into the FCD.

For high quality audio an external audio clock should be used with a jitter of about 100 ps RMS. In this case the clock is supplied externally via the external pins. Note that the SAI and FCD are implemented as separate modules.

The SAI has a register to control the FCD. It is capable to derive the SAI ACLK from the MLBCLK. MLBCLK is fed into the FCD module. This is required to synchronize the ACLK to MLBCLK.

3.9 Peripheral Clocking

The MPC5748G family allows the core and platform clocks to be scaled independently from the peripheral (master and slave peripherals) clocks allowing the user to reduce power consumption, by reducing core and platform clocks, but keeping peripheral clocks fixed.

Table 3 below details the peripherals that need to stay at a fixed frequency when core and XBAR (Cross bar) clocks are scaled.

Table 3. Peripheral clocking

Peripheral	Scales with frequency	Fixed output frequency
HSM	Yes	No
FlexRay	No	Yes
Ethernet	No	Yes
USB	No	Yes
uSDHC	No	Yes
MLB	No	Yes
eDMA	No	Yes
FlexCAN	No	Yes
eMIOS	No	Yes
ADC	No	Yes
DSPI	No	Yes
LINFlex	No	Yes

Peripheral	Scales with frequency	Fixed output frequency
I²C	No	Yes
SAI	No	Yes
BCTU	No	Yes
PIT_RTI	No	Yes
RTC_API	No	Yes
STM	No	Yes

3.10 e200Z2 Clocking

The e200Z2 core is limited to a max frequency of 80 MHz. It has a flexible divider that allows it to run at an integer multiple of the e200Z4 CPUs. The divider supports divide by 1-2-4 (Reset default div 1).

3.11 LPU Clocking

It is possible to run the Low Power Unit (LPU) from the FXOSC and FIRC and further divide down the frequency to the peripherals in the low power domain (e.g. LIN, SPI, ADC,…). See LPU reference manual chapter for details for specific peripherals in LPU mode.

3.12 External Clocks

There are two external clock output pins on MPC5748G, CLKOUT[1:0]. The output from CLKOUT[0] can be individually selected from the FXOSC, FIRC, PLL_PHI_0, S160, RTC_CLK and PLL_PHI_1. This is identical to MPC5646G and can be divided down by an output divider.

It is not available in standby mode.

The output from CLKOUT[1] can be individually selected from the FXOSC, FIRC, SXOSC, SIRC and is available in all modes including standby. For CLKOUT[1] the output of the external selector mux has a divider to enable the generation of 2 MHz and 24.6 KHz to 102.4 KHz from FXOSC. CLK_OUT pins are recommended to have a test point on PCB for debugging purpose.

3.13 Clock Sources

The following sub-sections define the clock sources on the MPC5748G. All members of the MPC5748G family might not support all the clock sources listed below:

- PLL0 (SSCG - Spread Spectrum Clock Generator (FM))
- 8-40 MHz External Oscillator (FXOSC)
- External Clock (EXTAL Bypass)
- 16 MHz Internal RC Oscillator (FIRC)
- 128 KHz Internal RC Oscillator (SIRC)
- 32 KHz External Oscillator (SXOSC)

Please note, the PLL0 clock source is out of the scope of this document, and is hence not described in detail.

3.14 Fast External Oscillator (FXOSC)

The FXOSC supports an external high frequency oscillator in the range of 4 MHz to 40 MHz.

This device provides a driver for an oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, and a way of reducing the radiated emissions.

This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and the MCU such as minimizing trace lengths.

Full Swing Pierce (FSP mode) operation is also available in the case that parasitic capacitances cannot easily be reduced, by using a crystal with high equivalent series resistance. For this mode, special care needs to be taken regarding the serial resistance used to avoid crystal overdrive.

Two other modes, External (EXT Wave) and disable (OFF mode) are also provided. For EXT Wave, the drive is disabled and an external source of clock of CMOS levels

Based on the analog oscillator supply can be used. The maximum input clock frequency is 40 MHz. The bypass clock is input on the EXTAL package pin and passed by the FXOSC when bypass clock mode is selected in the clock control logic. The bypass clock can be used as a reference for PLL0 or as a system and peripheral clock source.

When OFF, EXTAL is pulled down by a 240K resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

Enabling and disabling of the oscillator at startup is determined by a bit in the UTest row of the flash. The default value is disabled. There is also a bit in UTest to determine if the FXOSC should be configured for crystal or Bypass. The default value is crystal.

In addition, the Loop Controlled Pierce (LCP) mode is disabled when the device comes out of Power On Reset. This is not user configurable, as it should always start in full power mode and then be configured by software for low power mode (LCP mode) if desired.

The FXOSC is able to start without software intervention when MBIST and/or LBIST is enabled and when oscillator lock information is provided to indicate that FXOSC is stable and ready to be used. This status bit can be found in the FXOSC digital interface.

The device can also detect an invalid oscillator clock. This applies to both loss of clock and operating at the wrong frequency.

A clock monitoring unit (CMU) is used to track the oscillator clock using the 16MIRC as the reference clock. The FXOSC monitor is always enabled when the FXOSC and FIRC are valid. For further details, please refer to the Clock Monitor chapter within the reference manual.

Figure 13 shows the connection scheme.

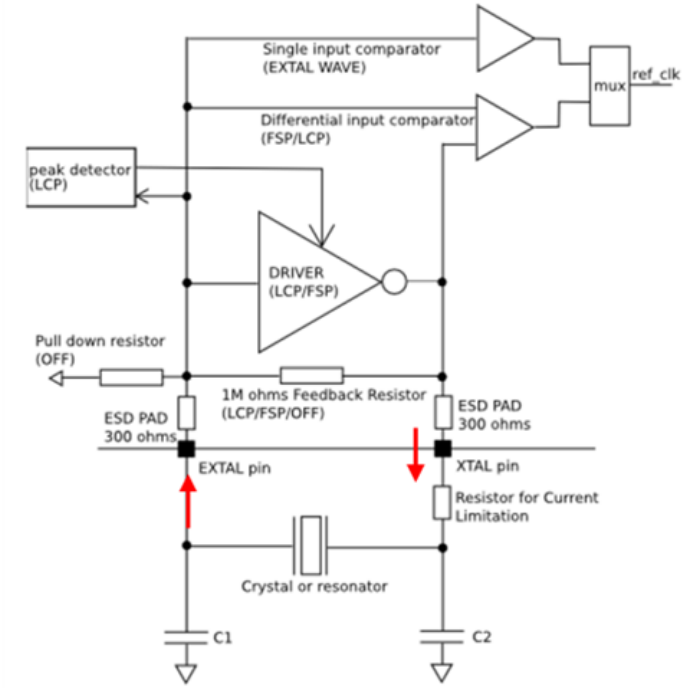


Figure 13. Oscillator Connection scheme

Oscillator recommendations:

- An external feedback resistor is not needed because it's already integrated into the device.
- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum value of the C1 and C2 capacitors. The data sheet includes recommendations for the tank capacitors C1 and C2. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point
- To reduce EMC emission, use the lowest crystal frequency possible and use FMPLL for system clock generation.
- Keep the oscillator circuit as compact as possible to minimize emissions.
- VSS _HV should be connected directly to the ground plane so that return currents can flow easily between VSS _HV and the two capacitors (C1 and C2).
- Avoid other high frequency signals near the oscillator circuitry. These can influence the oscillator.
- Layout/configure the ground supply on the basis of low impedance.
- Shield the crystal with an additional ground plane underneath the crystal.
- Do not lay out sensitive signals near the oscillator. Analyze cross-talk between different layers.
- The VSS pin close to the XTAL pins must be connected to the ground plane and decoupled to the closest VDD pin.
- Capacitors should be placed at both ends of the crystal, directly connected to the ground plane while keeping the overall loop as small as possible.

- The crystal package, when metallic, is directly connected to the ground.
- To isolate the noise from or to a special area of the PCB, a guard ring cab be used. That will almost surround this area with ground (except in one point) and thus there will be no current flowing through this guard ring in normal operation.

NOTE

Guard rings add capacitance to the PCB.

Figure 14 shows the recommended placement and routing for the oscillator layout.

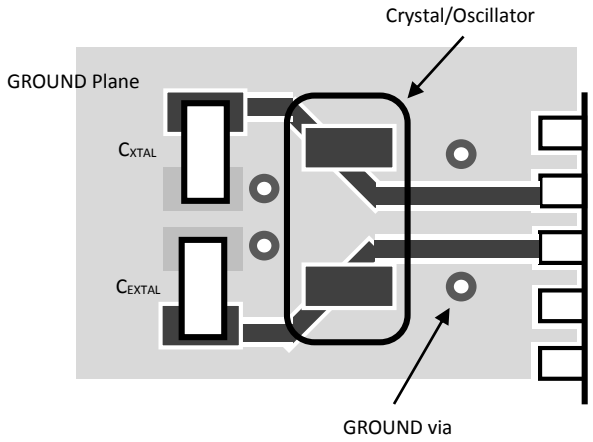


Figure 14. Suggested Crystal Oscillator Layout

3.15 16 MHz Internal RC Oscillator (FIRC)

The 16MIRC clock is the default clock during device boot up, and is always enabled on boot-up exit. For power saving reasons there is an option to disable the FIRC when entering STANDBY mode. During the STANDBY mode entry process, the FIRC is controlled based on ME_STANDBY_MC[RCON] bit. This is the last step in the standby entry sequence.

On any system wake-up event, the device exits STANDBY mode and switches on the FIRC. The actual power down status of the FIRC when the device is in standby is provided by RC_CTL[FIRCON_STDBY] bit.

To help achieve the improved trim options the number of trim bits has been extended versus the MPC560xB family implementation. There are 12 trimming bits for this new version of the FIRC and these will be required to be loaded from flash during boot up.

The start-up time is in line with what was achieved on the MPC560xB family.

The frequency of the FIRC clock is monitored by the frequency meter in CMU_0. There is no automated trigger of an FCCU error condition if the FIRC fails.

3.16 32 KHz External Oscillator (SXOSC)

The MPC5748G offers an on-chip 32 KHz RC oscillator (SIRC). In principal, it offers the same functionality as implemented on the MPC560xB/C family, but enhanced by a new LCP (Loop Controlled

Pierce) feature. This feature is disabled by default from reset, but there will be a user option to allow it to be enabled. When moving into LCP mode, this will greatly reduce the power consumption.

3.17 128 KHz Internal RC Oscillator (SIRC)

An on-chip 128 KHz RC oscillator (SIRC) is supported. The SWT will always be clocked by the 128 KHz IRC (SIRC). Also The RTC_API use this time base e.g. for periodic low power wake-up.

3.18 Progressive Clock Switching

The MPC5748G supplies a method to ramp the clock frequencies and active logic such that each frequency step produces less than a 50mA current change on the core supply over a 20 µs period. This applies both to the powering up and down of the device and entry and exit of low power modes.

Since ramping the clock rates in the application with application SW by adjusting the PLL output dividers is not adequate, this feature is supported in hardware.

The integrated progressive clock switching feature can be optionally enabled by SW. The default state is disabled.

4 RESET

The different reset sources on the device are organized into two families: 'destructive' and 'functional'. The reference manual contains a detailed definition of functional and destructive RESETs.

When a reset is triggered, the MC_RGM (Reset Generation Module) state machine is activated and proceeds through the different phases (i.e., PHASEn states) as shown in figure 15. Each phase is associated with a particular chip reset being provided to the system. A phase is completed when all corresponding phase completion gates from either the system or internal to the MC_RGM are acknowledged. The chip reset associated with the phase is then released, and the state machine proceeds to the next phase up to entering the IDLE phase. During this entire process, the MC_ME state machine is held in RESET mode. Only at the end of the reset sequence, when the IDLE phase is reached, does the MC_ME (Mode Entry Module) enter the DRUN mode.

On a side note, it is worth noting that there is an alternative possibility for software to configure some reset source events to be converted from a reset to either a SAFE mode request issued to the MC_ME or to an interrupt issued to the core.

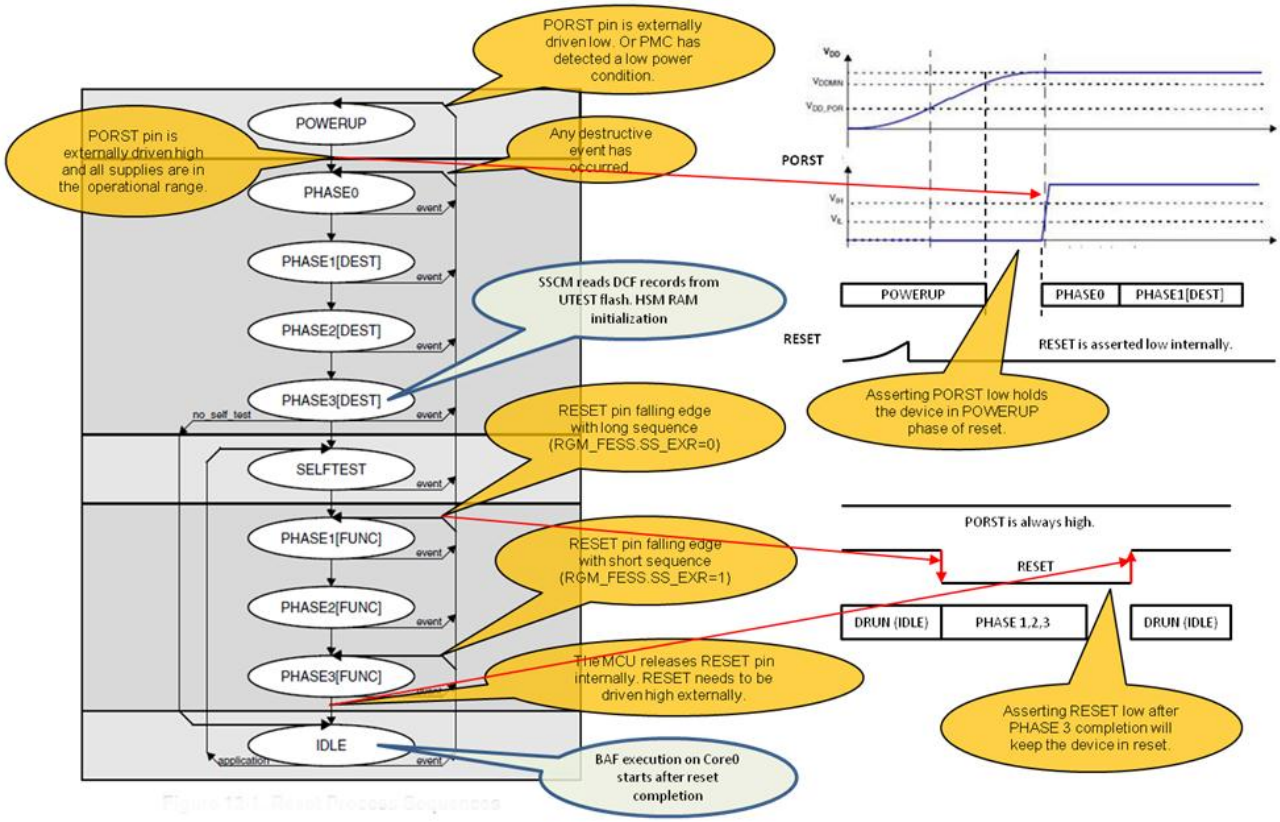


Figure 15. Reset process sequences

The Reset and Generation Module (RGM) which forms the heart of the reset flow has largely been reused from the MPC564xG/B.

During the initial part of the reset phase the only clock available will be the FIRC clock, which will be ~16MHz. and this will be used to clock the various state machine elements. This is the fail-safe clock and the default out-of-reset

The external oscillator is optionally enabled during start up (dependent on the DCF (Device Configuration)).

4.1 PORST (Power on Reset) Pin

The PORST pin facilitates the device reset signal. The PORST and the RESET pins should NOT be connected together.

The PORST on MPC5748G is an input only pin, unlike other MPC57xx devices which have an open drain output driver.

For both, internal and external regulation mode, an external pull up resister is necessary on PORST as shown is figure 16.

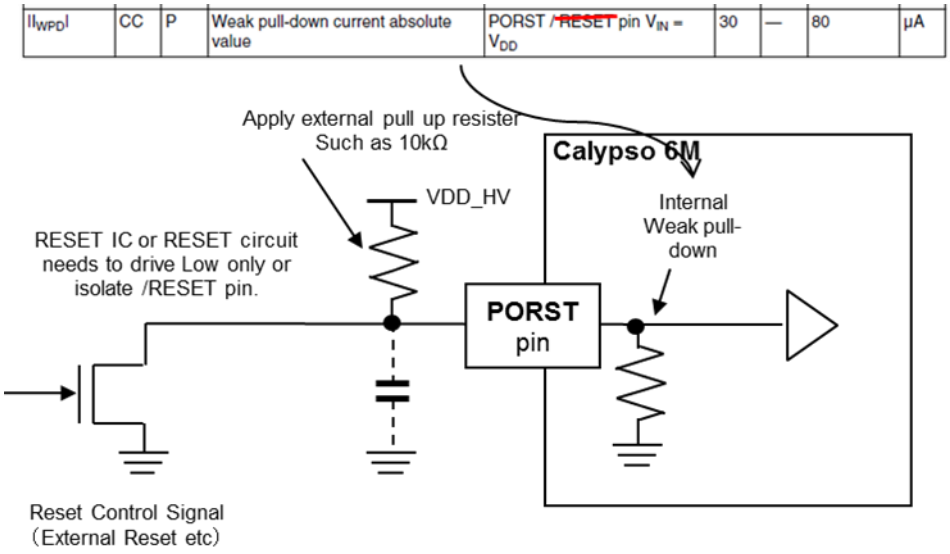


Figure 16. Pin configuration

For normal mode of operation utilizing the internal core voltage regulator and external ballast transistor, i.e. in Internal Regulation mode, the PORST should be pulled high externally (10K resistor recommended).

If the core voltage is being supplied externally, i.e. in External Regulation mode, the customer must ensure that the PORST is held low (including during the power-up phase) in the event that the core voltage is below the operational threshold specified in the datasheet. See figure 17.

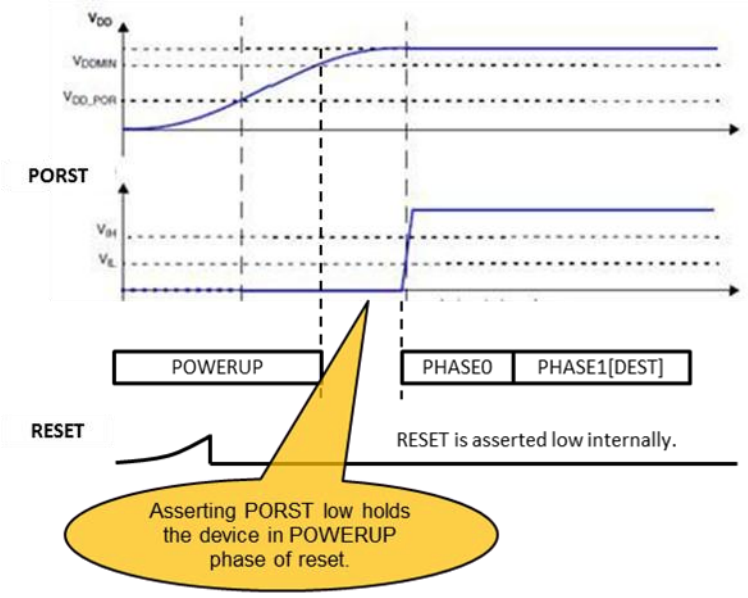
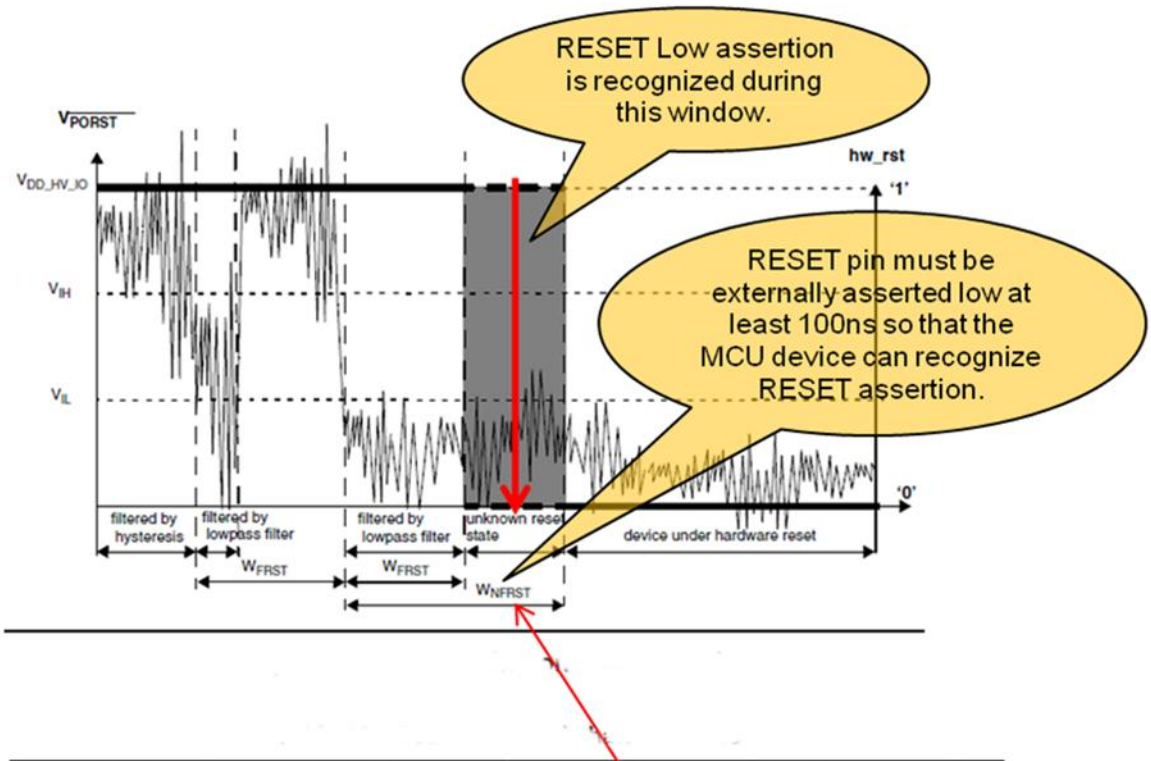


Figure 17. Holding PORST low

4.2 Noise Filtering on PORST and RESET

Figure 18 outlines the care which must be taken with respect to noise filtering on the reset signal.



Symbol			Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	—	Input high level TTL (Schmitt Trigger)	—	2.0	—	V_{DDIO}+0.4	V
V_{IL}	SR	—	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}[3]	CC	C	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
W_{FRST}	SR	P	PORST and RESET input filtered pulse	—	—	—	10	ns
W_{NFRST}	SR	P	PORST and RESET input not filtered pulse	—	100	—	—	ns

Figure 18. Noise filtering on reset signal

5 Boot Assist Flash (BAF)

Figure 19 shows the operation on the BAF on this device.

NOTE

There are no longer any FAB or ABS pins on these devices as there were on previous families so Serial Boot Mode is only entered if no valid RCHW (Reset Configuration Half Word) is found.

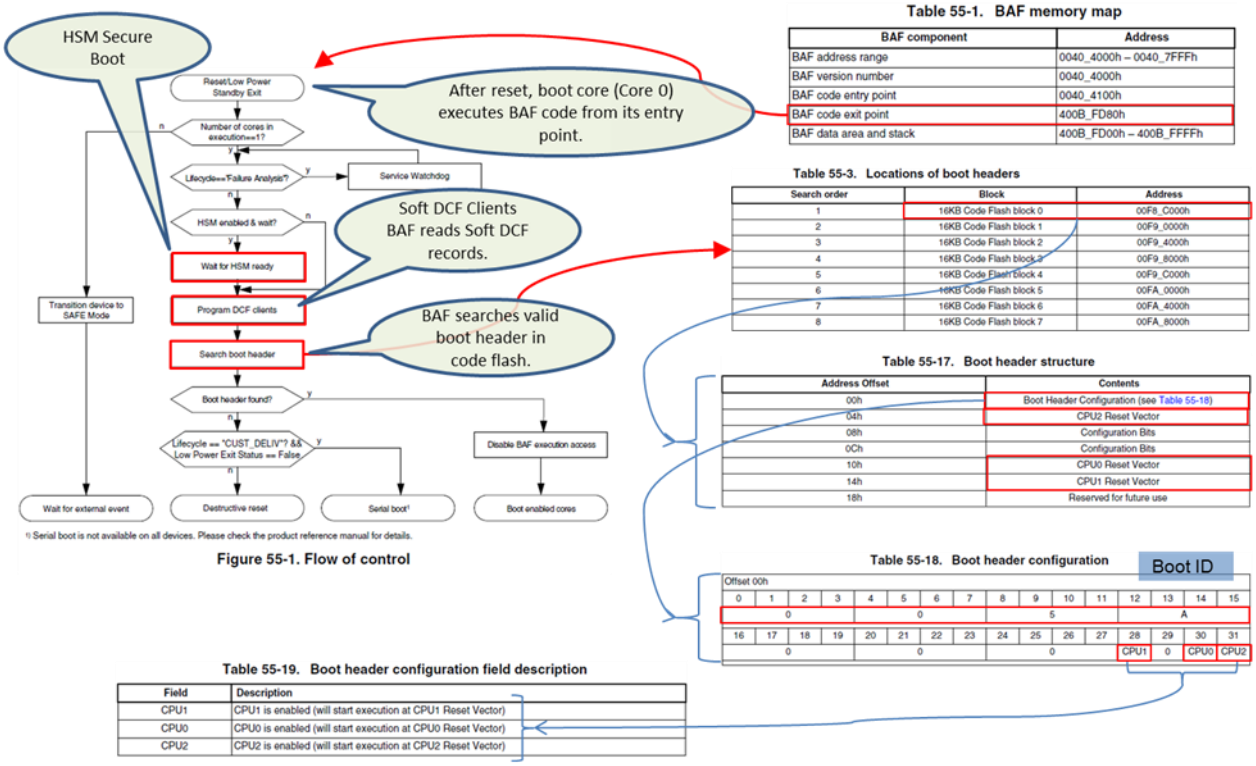


Figure 55-1. Flow of control

Table 55-1. BAF memory map

BAF component	Address
BAF address range	0040_4000h – 0040_7FFFh
BAF version number	0040_4000h
BAF code entry point	0040_4100h
BAF code exit point	400B_FD80h
BAF data area and stack	400B_FD00h – 400B_FFFFh

Table 55-3. Locations of boot headers

Search order	Block	Address
1	16KB Code Flash block 0	00F8_C000h
2	16KB Code Flash block 1	00F9_0000h
3	16KB Code Flash block 2	00F9_4000h
4	16KB Code Flash block 3	00F9_8000h
5	16KB Code Flash block 4	00F9_C000h
6	16KB Code Flash block 5	00FA_0000h
7	16KB Code Flash block 6	00FA_4000h
8	16KB Code Flash block 7	00FA_8000h

Table 55-17. Boot header structure

Address Offset	Contents
00h	Boot Header Configuration (see Table 55-18)
04h	CPU2 Reset Vector
08h	Configuration Bits
0Ch	Configuration Bits
10h	CPU0 Reset Vector
14h	CPU1 Reset Vector
18h	Reserved for future use

Table 55-18. Boot header configuration

Boot ID

Offset 00h															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0				0				5				A			
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0				0				0				CPU1	0	CPU0	CPU2

Table 55-19. Boot header configuration field description

Field	Description
CPU1	CPU1 is enabled (will start execution at CPU1 Reset Vector)
CPU0	CPU0 is enabled (will start execution at CPU0 Reset Vector)
CPU2	CPU2 is enabled (will start execution at CPU2 Reset Vector)

Figure 19. BAF Operation

6 Input/Output Pin's

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a VDD_HV/VSS_HV supply pair. In order to ensure device reliability, the average current of the I/O on a single segment should remain below the IAVGSEG maximum value as defined in the data sheet.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the IDYNSEG maximum value.

If there is a need to source/sink current through some I/Os, care should be taken to spread the amount of current between the segments. This is to ensure the design does not exceed the max IDYNSEG current.

The MPC560xB Family has some dedicated ADC pads, but MPC5748G doesn't have any dedicated ADC channels. Most I/O pins are GPI or GPIO muxed with an ADC channel. All of them have a weak pull up/down feature.

6.1 I/O Pad Block Diagram (GPIO & Module Mux Port)

Figure 20 shows an I/O pad block diagram without analog inputs.

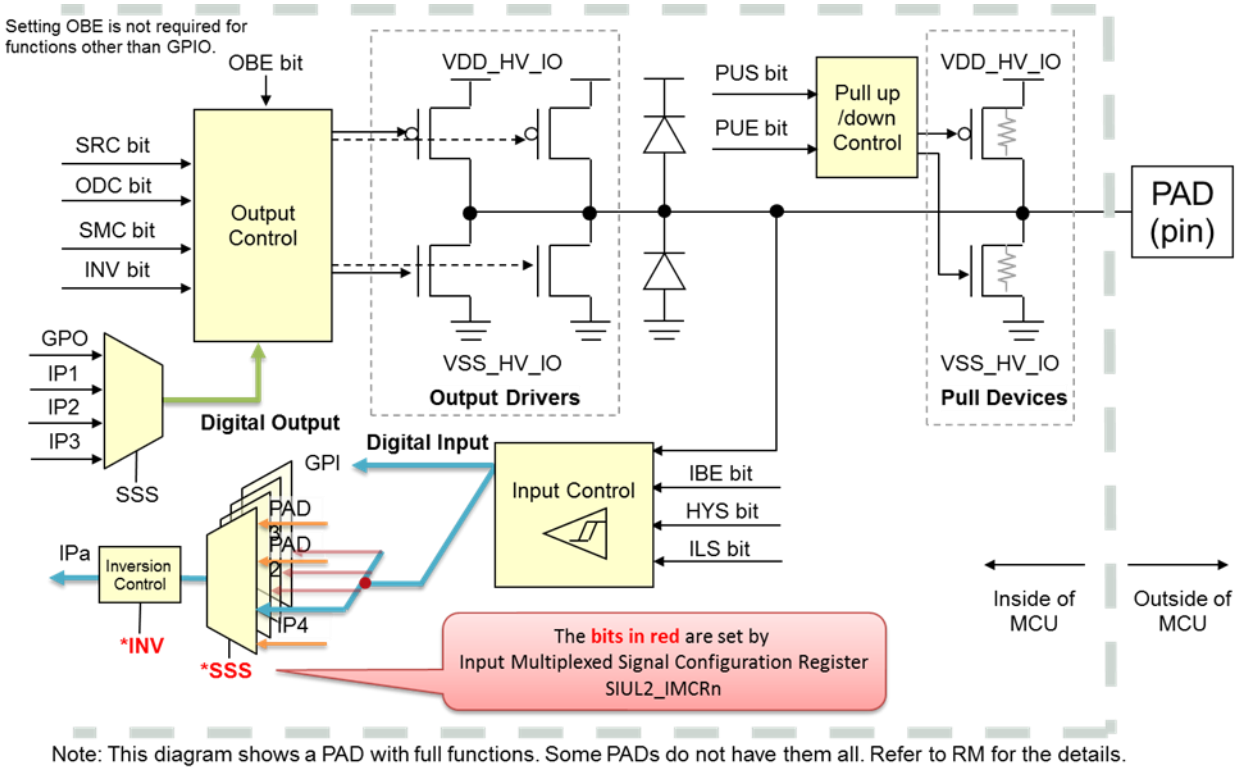


Figure 20. I/O pad block diagram without analog inputs

6.2 I/O Pad Block Diagram with Analog Input (GPIO & Module MUX Port)

Figure 21 shows the I/O pad block diagram with analog inputs

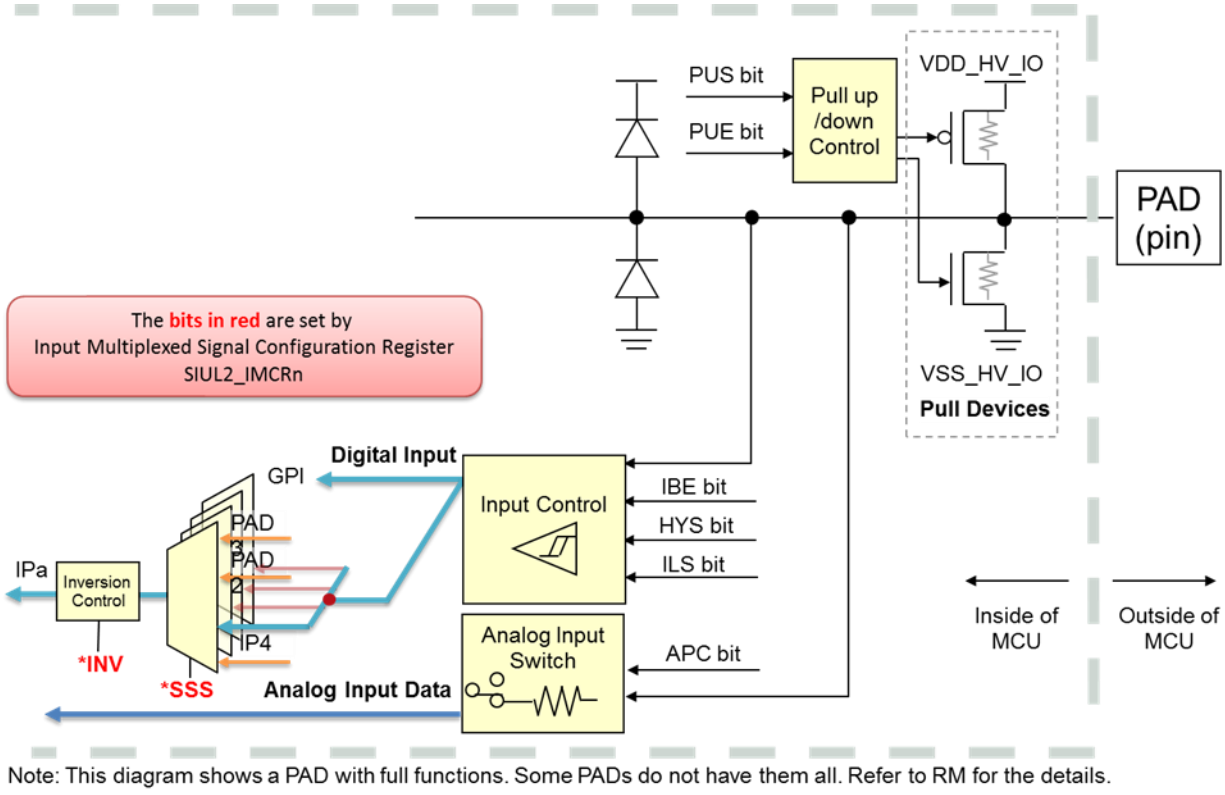


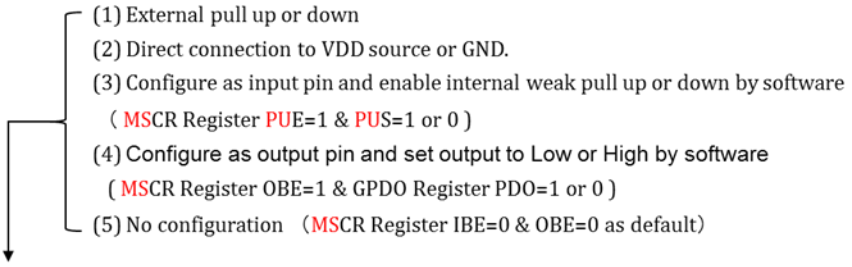
Figure 21. I/O pad block diagram with analog inputs

6.3 Unused GPIO Pin Termination

Most microcontrollers are designed to be used in a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, unused clocks, counters or I/Os, should never be left floating or unconnected.

Figure 22 shows the recommended terminations for all pin types.



Pin Type	Termination	Note
Pin which is exposed to IO pad on the package.	(1)	Recommended. Benefit of this option is to ensure the termination during Power-On. But this option costs more.
	(2)	Take care for output collision toward external driver due to software mishandling.
	(3)	Recommended. But take care for long wiring to external device without external pull up or down.
	(4)	Recommended. Don't apply for input pin. Take care for output collision toward external driver due to software mishandling.
	(5)	
Pin which is not exposed out of the package	(3)	Recommended.
	(4)	Recommended. Don't apply for input pin.
	(5)	

Figure 22. Recommended terminations for all pin types

6.4 Pad Keeper

The pad keeper supports the state retention of GPIO in all low power modes. State retention is controlled by pad keeper logic.

NOTE

Not all I/O will support state retention in Power Domain0 (PD0) and Power Domain1 (PD1).

- The Pad Keeper reduces external termination with pull up/down register.
- 75 pad keeper on 176LQFP
- 99 pad keeper on 256BGA

Supported pins:

Red pins are only available on 256BGA.

PA 0,1,2,4,12,13,14,15

PB 0,1,3,4,5,6,7,8,9,10,11,12

PC 0,1,6,7,8,9,10,11

PD 0,1,2,3,4,5,6,7,8,9,10,11,12,13

PE 0,3,5,9,11

PF 0,1,2,3,4,5,6,7,8,9,10,11,12,13

PG 3,5,6,7,8,9

PH 9,10

PI 1,3,9,10,14,15

PJ 0,1,2,3,5,6,7,8,9,10,11,12,13,14,15

PK 0,1,2,3,4,5,6,7,8

6.5 Injection Current

The following guidelines should be followed with respect to injection currents.

- Max. Injected input current on any pin during overload condition: +-5 mA
- Absolute sum of all injected input currents during overload condition: +-50 mA
- Note that ADC input pad must never exceed its own IO segment supply voltage where the input pad resides. If ADC input pin is higher than IO supply where the pin resides, then this will cause ESD diodes in pads to forward bias. Figure 23 shows the effect of injection current on performance.
- Applying signals to pins (~3.3 V) during power-off (VDD ~0V) must be considered as a kind of overload condition. Series resistors between signal sources and pins may be needed to limit injection current IINJ.
- In general, any overload conditions (positive or negative voltage out of VIH and VIL spec applied to the pins) should be avoided. Injection current leads to increased leakage current on the pins next to the injected pin.

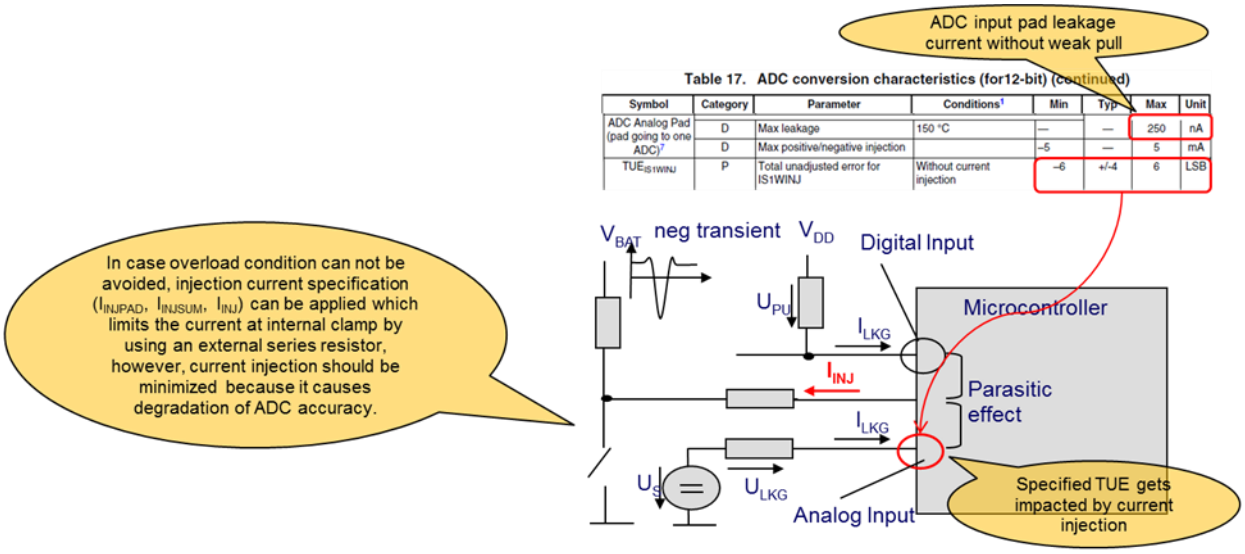


Figure 23. Effect of injection current on ADC performance

6.6 Internal Weak Pull-Up/Down

The Internal weak pull feature is a feature primarily for device protection. Because of that, the actual minimum weak pull current specification doesn't really matter to an end user.

On the other hand, the maximum weak pull current specification is important for the case that the application requires the internal weak pull up to oppose a voltage level caused by an external pull up/down resistor before software changes the internal weak pull configuration. Figure 24 shows an example of configuration.

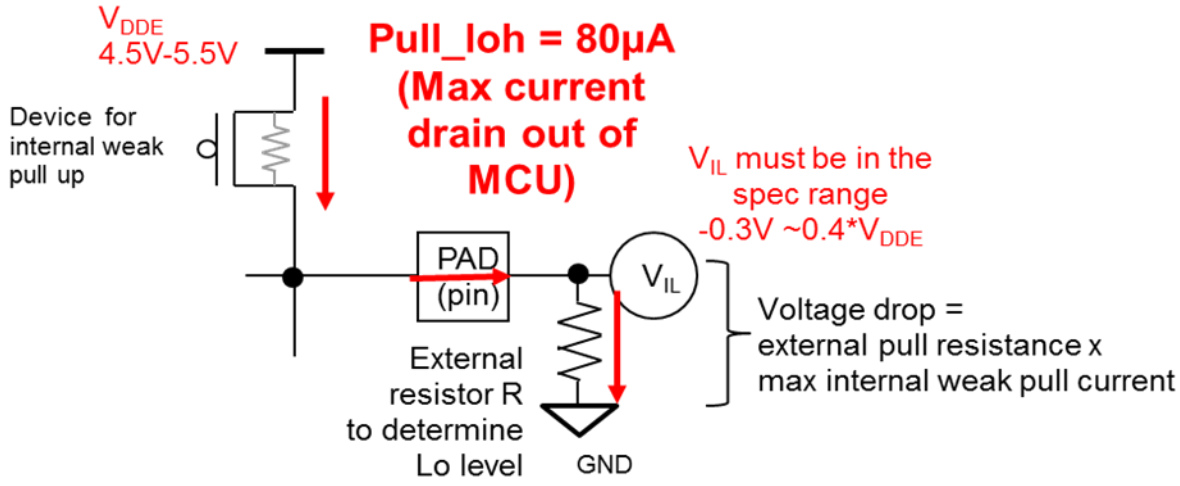


Figure 24. Example Weak pull up/down configuration

Example:

External resistor R=10 kΩ

80uA max weak pull up current as specified in the data sheet.

Voltage drop (VIL) = 10 kΩ x 80 µA = 0.8 V

The voltage above pin is less than VIL max= 0.40x4.5V = 1.8 V at VDD=4.5 V

Therefore R=10 kΩ is suitable.

The same principal applies for internal weak pull down scenarios.

7 JTAG Connector

Figure 25 shows the standard 14 bit JTAG connection signals available on the MPC5748G.

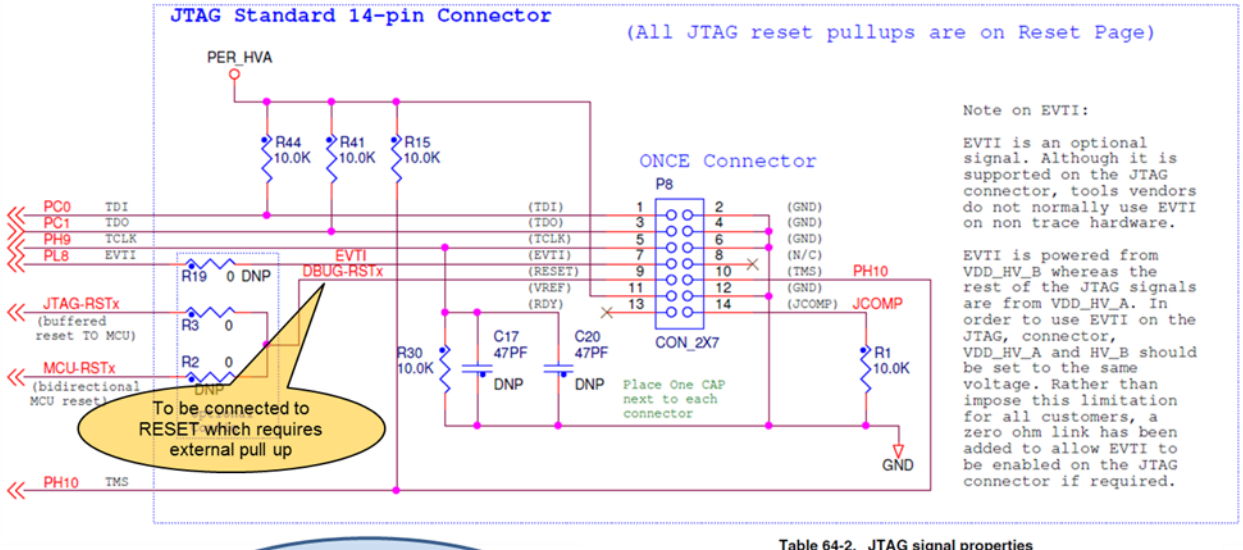


Table 64-2 shows correct default pull setting for JTAG pins. Note that TCK is now pulled-down by default which is opposite from Bolero.

Table 64-2. JTAG signal properties

Name	I/O	Function	Reset State	Pull
TCK	Input	Test Clock	—	Down
TDI	Input	Test Data In	—	Up
TDO	Output	Test Data Out	High Z[1]	—
TMS	Input	Test Mode Select	—	Up

1. TDO output buffer enable is negated when the JTAGC is not in the Shift-IR or Shift-DR states. A weak pull may be implemented at the TDO pad for use when JTAGC is inactive.

Figure 25. JTAG connector

8 Basics of Static Thermal Analysis

Principle of thermal analysis are similar to those in the electrical domain. Understanding one domain simplifies the task of becoming proficient in the other. This is especially clear when we consider thermal conduction.

Each domain has a “through” and an “across” variable, as shown in Figure 26 and Table 4. The through variable can be thought of as the parameter that flows from one reference point to another. Current is the through variable for the electrical domain and power is the through variable in the thermal domain

The across variable can be thought of as the variable that forces the flow of current or heat. In each domain the forcing function is a difference in potential; in one domain it's temperature and in the other it's voltage. Both systems have a resistance that impedes the flow of the through variable.

Given the duality of the two systems, it is no surprise that the fundamental equations of the domains are similar. This is illustrated most clearly when we see that each system has an "Ohm's Law", as is shown in Figure 26.

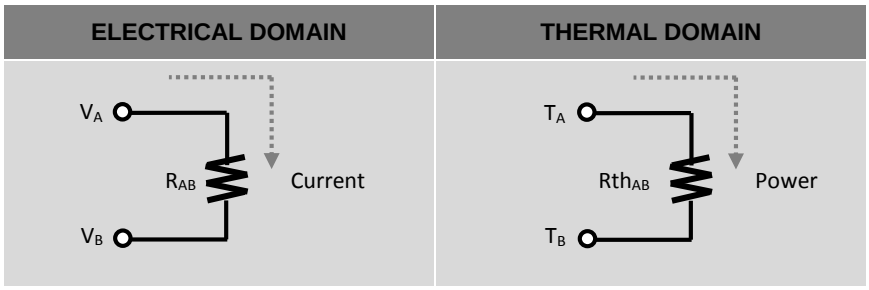


Figure 26. Electrical and thermal domains

Table 4 shows the basic relationships in the Electrical and thermal domains.

Table 4. Electrical and thermal domain relationships.

	ELECTRICAL DOMAIN			THERMAL DOMAIN		
	VARIABLE	**SYMBOL**	**UNITS**	**VARIABLE**	**SYMBOL**	**UNITS**
Through Variable	Current	I	Amperes	Power	P_D	Watts
Across Variable	Voltage	V	Volts	Temperature	T	°C or °K
Resistance	Electrical Resistance	R	Ohms	Thermal Resistance	Rth_{AB} / $R_{\theta AB}$	°C/W or °K/W
Capacitance	Electrical Capacitance	C	Farads	Thermal Capacitance	C_θ	Jouls/°C
Ohms Law	$\Delta V_{AB} = V_A - V_B = I \times R_{AB}$			$\Delta T_{AB} = T_A - T_B = P_D \times R_{\theta AB}$		

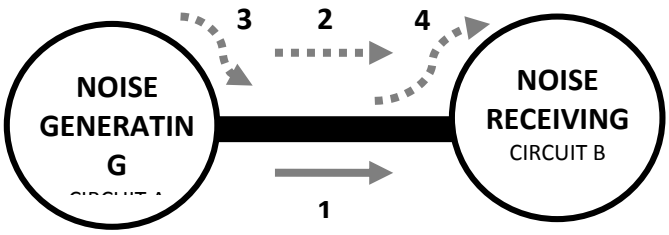
9 EMI/EMC (Electromagnetic Interference/Compatibility and ESD (Electrostatic Discharge) Considerations for Layout

These considerations are important for all system and board designs. Though the theory behind this is well understood, each board and system experiences this in its own way. There are many PCB and component related variables involved.

9.1 EMI/EMC

This document will not go into the details of electromagnetic theory or explain the different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits.

EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: conduction and radiation. See figure 27.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 27. EMI/EMC basics

The design considerations narrow down to:

- The radiated & conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables, etc.

The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test.

This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

9.2 EMI

Every board or system is different as far as EMI/EMC issues are concerned, requiring its own solution. However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Use multiple decoupling capacitors with different values and appropriate power supply decoupling techniques. Be aware that every capacitor has a self-resonant frequency.
- Provide adequate filter capacitors on the power supply source. These capacitors and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.
- Apply current return rules to connect the grounds together while isolating the ground plane for the analog portion. If the project does not use ADC and there are no analog circuits do not isolate grounds.
- Avoid connecting the ground splits with a ferrite bead. At high frequencies, a ferrite bead has high impedance and creates a large ground potential difference between the planes.

9.3 ESD

A supply voltage glitch or ESD will put the device in an unknown state. Therefore, it is important to have a good PCB layout for optimum noise and ESD performance. The similar ESD protection diodes can be utilized for CANphy (CANH and CANL) pins as well. Keep the loop area of critical traces as short as possible. If your design needs to bring any pin like GPIO to a connector (for external connectivity) you need to take special ESD care by adding ESD protection parts. For additional information and guidelines for the PCB design for reduction of EMI/EMC issues.

10 Example Communication Peripheral Connections

There are a wide range of peripheral pins available on the MCUs. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, CAN, Ethernet, and RS-232 communication interfaces.

The table below summarizes the maximum communication speed and general overview information of the different types of interfaces.

Table 5. Communication module comparison

Common name	Standard	Distributed timebase	Speed (maximum Kbits/second)	Channels	Time triggered	Arbitration
RS-232D	EIA RS-232 revision D	No	115.2	Single	No	None (optional flow control)
K Line	ISO 9141	No	150[1]	Single	No	None
LIN	LIN 1.0, LIN 2.0, and LIN 2.1[2]	No	100[3]	Single	No	None (master/slave)

Common name	Standard	Distributed timebase	Speed (maximum Kbits/second)	Channels	Time triggered	Arbitration
CAN	Bosch 2.0B ISO11898	No	1000[4]	Single	No (additional function)	CSMA[5]
FlexRay	FlexRay	Yes	10000	Dual	Yes	TDMA6
Ethernet	IEEE® 802.3	No	10,000/100,000	Single	No	CSMA

1. Typical speed is 10.4Kbits/s.

2. Many NXP devices only support the LIN 1.0 and 2.0 standards. LIN2.1 requires a different sampling scheme covered by an erratum to the LIN standard..

3. Typical speed is 10 or 20 Kbits/s, but supports a fast mode of 100 Kbits/s.

4. Two different speed classes are supported by CAN, a fast (250K to 1Mbits/s) and a low speed CAN (5K to 125Kbits/s).

5. Carrier Sense Multiple Access

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system. The below figure shows a typical protection circuit.

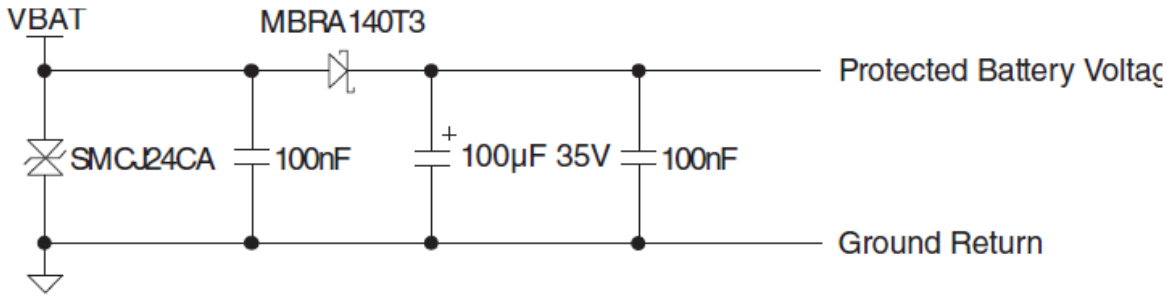


Figure 28. Typical Protection Circuit

10.1 Example LIN Interface for eSCI

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node

communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

On many of the NXP automotive MCUs, the enhanced Serial Communication Interface (eSCI) module implements Local Interconnect Network (LIN) interface. This same module (eSCI) also supports the standard Universal Asynchronous Receiver/Transmitter (UART) functions (with a different physical layer device).

The following figure shows a typical interface implemented using the NXP LIN transceiver.

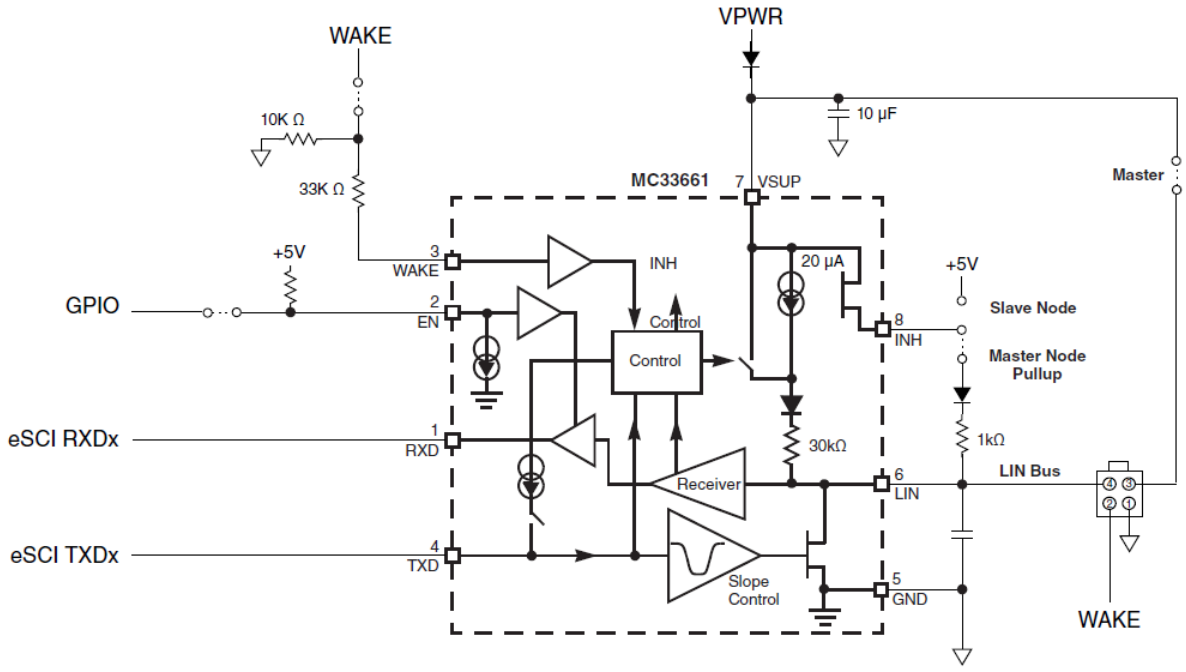


Figure 29. Typical eSCI to LIN connections

The table below shows the pins of the MC33661 and their typical connections to an MCU.

Table 6. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU.
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device.
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode.
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU.
5	GND	Input	Ground	System Ground Reference	Device ground reference.
6	LIN	Input/ Output	LIN Bus	LIN bus	Bidirectional pin that represents the single-wire transmit and receiver.
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V.
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes.

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There is no standard industry-defined LIN connector. NXP uses a 4-pin Molex that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. The NXP Molex connector definition is shown in the following table.

Table 7. LIN connector pin-out recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- **LIN Bus** - This is the single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- **VPWR** - This connector input can be used as the power input to a slave node. Care should be taken that sufficient
- current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- **Wake** - The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, turn on the MCU that controls a function inside the vehicle, such as power a smart dome light or enable the controls of a smart seat.
- **Ground** - Ground reference for the module.

Part numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in the table below.

Table 8. Recommended 4-pin Molex mini-fit Jr connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

10.2 Example RS-323 Interface for eSCI

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals though other interfaces, such as USB. RS-232 was intended to be a very low-cost, low-performance interface. This interface was originally specified with signal voltages of +12 V and -12 V typically. However, this has been lowered to a typical minimum voltage of +5 V and -5 V in recent years.

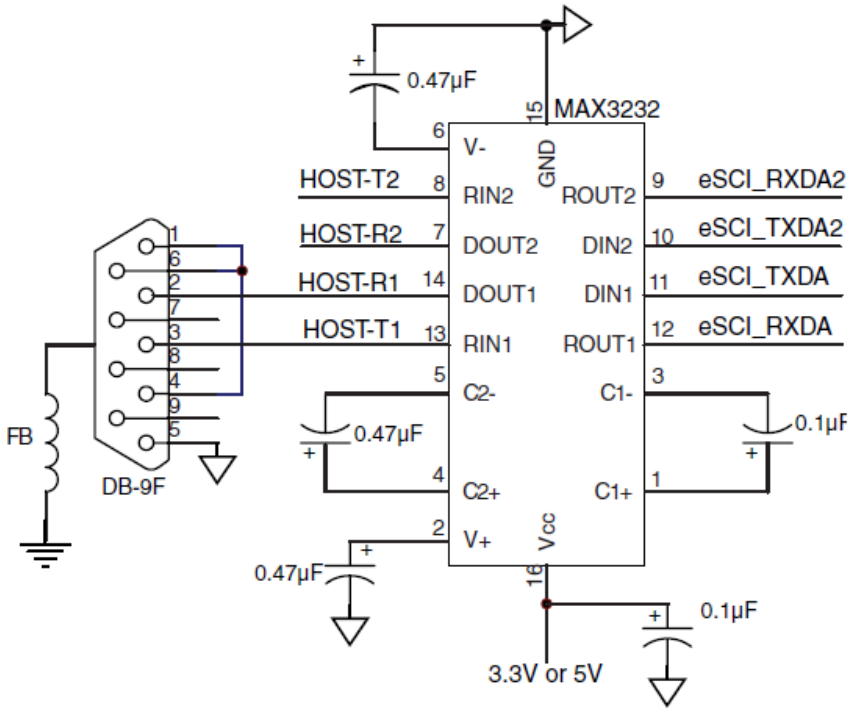
On many of the NXP automotive MCUs, the enhanced Serial Communication Interface (eSCI) module implements the standard Universal Asynchronous Receiver/Transmitter (UART) functions. This same module (eSCI) also supports the Local Interconnect Network (LIN) interface (with a different physical layer device).

The figure below shows the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature range of -40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore the commercial device can be used for prototyping purposes. TI does offer a device option with an operating temperature range of -40 to +85° C. TI has an enhanced version of the device, MAX3232-EP, which is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of -55 to +125° C.

Figure 30. Typical eSCI to RS-232D circuit



The following table shows the standard connection of the RS-232 connector, as used on the NXP evaluation boards.

Table 9. Typical RS-232D connector definition

6 Connect to pin 1 and 4	**1** Connect to pin 4 and 6
7 N/C	**2** RS-232 TX (Transmit)
8 N/C	**3** RS-232 RX (Receive)
9	**4** Connect to pin 1 and 6
	5 GND

NOTE

N/C Pins are not connected. Shell of connector should be connected through a ferrite bead to ground.

10.3 Example K LINE interface for eSCI

ISO9141, also known as K Line, is a low-speed diagnostic interface that provides a bi-directional half-duplex single-wire communication channel. A K Line interface can be implemented with a standard UART type function, such as is implemented in the eSCI module of the devices in NXP's MPC5500 and MPC5600 families. The K Line interface is used primarily for a low cost on-board diagnostic interface.

The MC33200 implements a K line interface in an 8-pin SOICN package. Features of the MC33290 are:

- Operation over wide supply voltage of 8.0 V to 18 V
- Operating temperature of -40 to 125 °C
- Interface directly to standard CMOS microprocessors
- ISO K Line pin protected against shorts to ground
- Thermal shutdown with hysteresis
- ISO K Line pin capable of high currents
- ISO K Line can be driven with up to 10 nF of parasitic capacitance
- 8.0 kV ESD protection attainable with few additional components
- Standby mode: no battery current drain with VDD at 5.0 V
- Low current drain during operation with VDD at 5.0 V

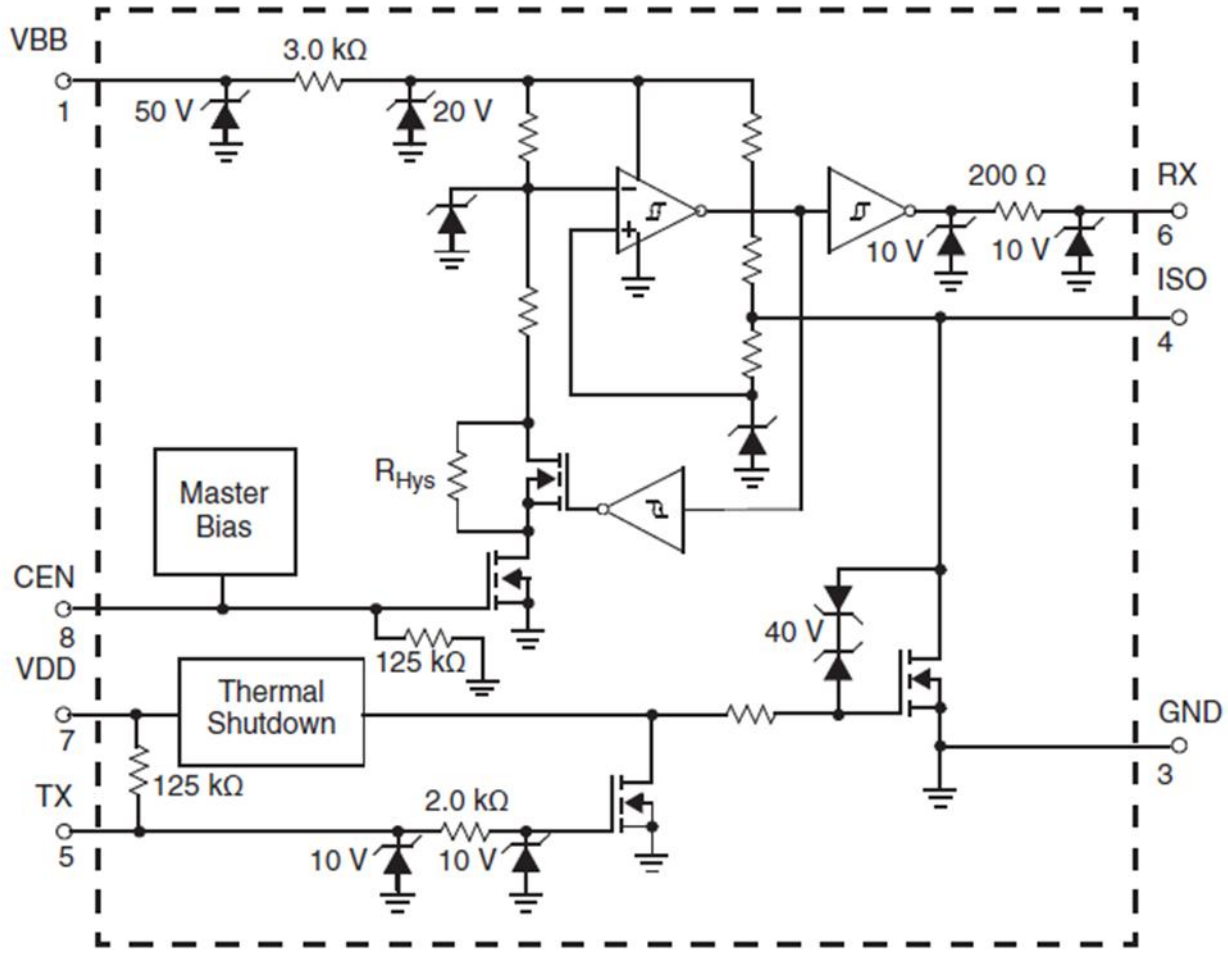


Figure 31. MC33290 block diagram

The following figure shows a typical interface between the MCU and the MC33290.

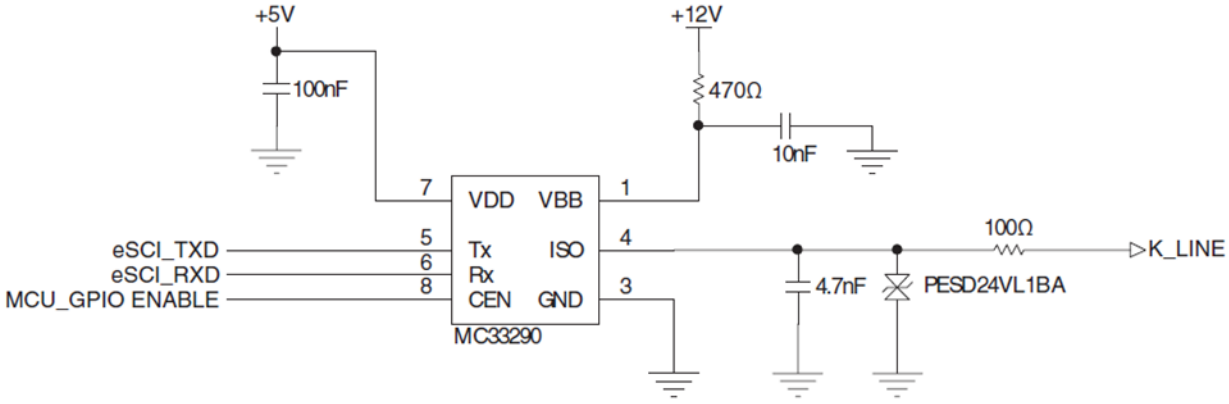


Figure 32. Typical eSCI to K Line connections

The following table shows the pins of the MC33290 and the typical connection in a target system.

Table 10. MC33290 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	VBB	Input	Battery Voltage	Protected battery voltage	VBB is the protected battery voltage supply for the device. It should have a reverse bias protection diode and a series resistor to the over-voltage protected battery.
2	NC	—	—	None	This pin should have no connection in the system.
3	GND	Input	Ground	Ground	Ground reference and power return for the device.
4	ISO	Input/ Output	ISO9141 bus	K-Line connector	ISO9141 bus connection.
5	TX	Input	Transmit data input	eSCI TXD	Input data to be transmitted on the ISO bus.
6	RX	Output	Receive Data Output	eSCI RXD	Output of the data received on the ISO bus.
7	VDD	Input	Digital Interface logic supply	5 V supply	Logic power source.
8	CEN	Input	Chip Enable	MCU GPIO (output)	Chip enable for the MC33290.

NOTE

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system.

Typically NXP does not include a K Line connector; therefore no standard connector is defined.

10.4 CAN Interface Circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip varies from device to device. A separate CAN transceiver is required for each CANmodule, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

NXP CAN modules conform to CAN protocol specification version 2.0 B, and the transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks. Some devices support the updated ISO11898-2 specification with support for CAN with flexible data-rate (CAN FD).

Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 11. NXP CAN Transceiver comparison

Frame data rate (Kbit/s)	1000	125	1000	1000	5000
Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep	Normal, Listen-only

10.4.1 High-Speed CAN TJA1050 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

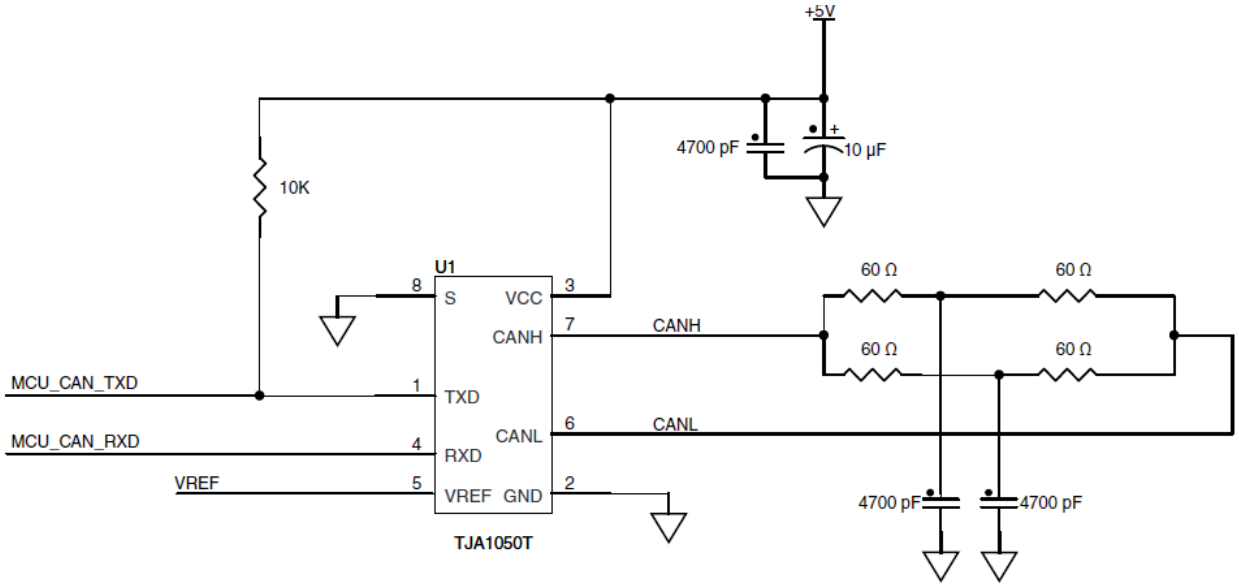


Figure 33. Typical high-speed CAN circuit using TJA1050

NOTE

Decoupling shown as an example only.

TXD/RXD pullup/pulldown may be required depending on device implementation.

The table below describes the TJA1050 pin and system connections.

Table 12. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in case of an error condition.

10.4.2 Low-Speed CAN TJA1054 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

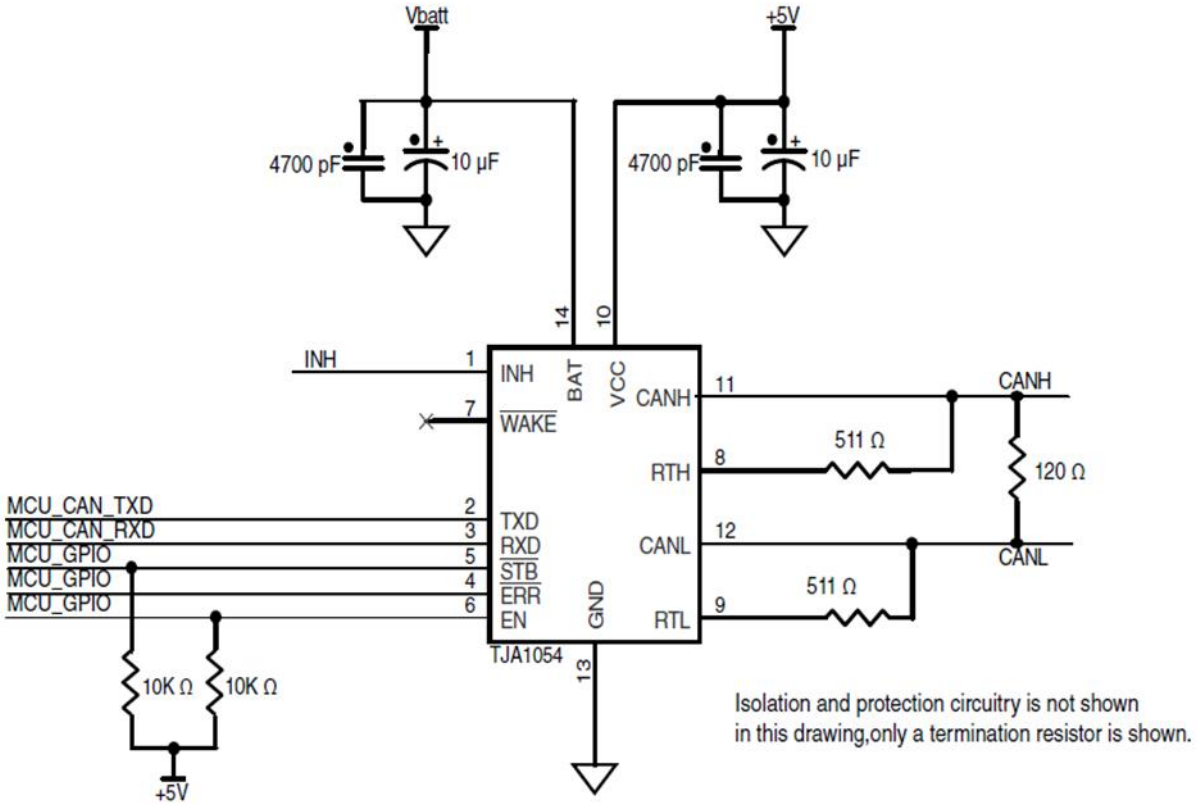


Figure 34. Typical low-speed CAN circuit using TJA1054

NOTE

Decoupling shown as an example only.

STB and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 13. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
4	ERR	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake-up is detected in Standby or Sleep modes.
5	STB	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	WAKE	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high[1] [This allows the transceiver to control the CAN bus impedance under an error condition.]
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low [This allows the transceiver to control the CAN bus impedance under an error condition.]
10	VCC	Input	Voltage Supply	5 V	Digital IO supply voltage, 5 V
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

1. This allows the transceiver to control the CAN bus impedance under an error condition.

10.4.3 Recommended CAN connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket is used on the evaluation board and a cable with a connector connects with it.

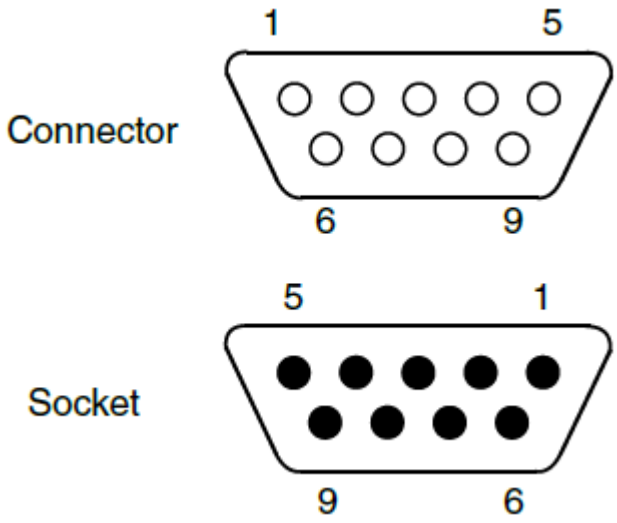


Figure 35. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 14. DB-9 pin signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

10.5 Ethernet Interface

Ethernet is a communication technology that was originally developed for creating local area networks (LANs) between computers. Over time, it has become the standard wired communications network for the PC and is widely used within telecommunications and industrial applications. In recent years, Ethernet has found its way into automotive electronics with deployment in diagnostic and camera applications.

The Ethernet Controller (ENET) implemented on the MPC5748G devices is a communication controller that supports 10 and 100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and

transceiver function are required to complete the connection to the physical interface. The figure below shows a typical set up of the complete interface to the network. Here a TJA1100 from NXP is used as the Ethernet PHY.

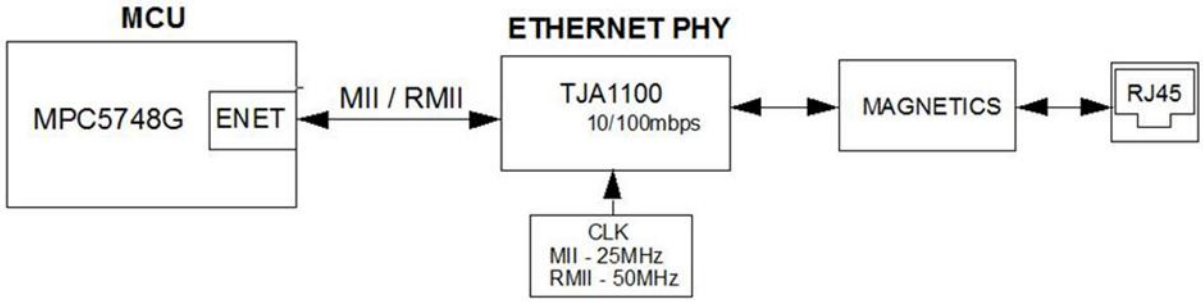


Figure 36. MCU connections to TJA1100 ethernet PHY

As shown in Fig 36 the ENET can interface to a PHY using either the 10/100 Mbit/s MII or RMII or the 10 Mbit/s only 7-wire interface. The ENET signals are summarized in Table X and their use in each interface type is highlighted. Note that the signals required by different PHYs will vary in some cases for each interface option; see the Data Sheet for your selected PHY.

Table 15. ENET signal overview

MII	RMII	Description	I/O
MII_COL	—	Asserted upon detection of a collision and remains asserted while the collision persists. This signal is not defined for full-duplex mode.	I
MII_CRS	—	Carrier sense. When asserted, indicates transmit or receive medium is not idle. In RMII mode, this signal is present on the RMII_CRS_DV pin.	I
MII_MDC	RMII_MDC	Output clock provides a timing reference to the PHY for data transfers on the MDIO signal.	O
MII_MDIO	RMII_MDIO	Transfers control information between the external PHY and the media-access controller. Data is synchronous to MDC. This signal is an input after reset.	I/O
MII_RXCLK	—	In MII mode, provides a timing reference for RXDV, RXD[3:0], and RXER	I
MII_RXDV	RMII_CRS_DV	Asserting this input indicates the PHY has valid nibbles present on the MII. RXDV must remain asserted from the first recovered nibble of the frame through to the last nibble. Asserting RXDV must start no later than the SFD and exclude any EOF. In RMII mode, this pin also generates the CRS signal.	I
MII_RXD[3:0]	RMII_RXD[1:0]	Contains the Ethernet input data transferred from the PHY to the media-access controller when RXDV is asserted.	I
MII_RXER	RMII_RXER	When asserted with RXDV, indicates the PHY detects an error in the current frame.	I
MII_TXCLK	—	Input clock, which provides a timing reference for TXEN, TXD[3:0], and TXER.	I

MII	RMII	Description	I/O
MII_TXD[3:0]	RMII_TXD[1:0]	Serial output Ethernet data. Only valid during TXEN assertion.	O
MII_TXEN	RMII_TXEN	Indicates when valid nibbles are present on the MII. This signal is asserted with the first nibble of a preamble and is deasserted before the first TXCLK following the final nibble of the frame.	O
MII_TXER	—	When asserted for one or more clock cycles while TXEN is also asserted, PHY sends one or more illegal symbols.	O
—	RMII_REF_CLK	In RMII mode, this signal is the reference clock for receive, transmit, and the control interface.	I
1588_TMRn	1588_TMRn	Capture/Compare block input/output event signal.bus. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn ENET_TCCR0 register for inspection by software. When configured for compare, 1588_TMR the corresponding signal 1588_TMRn is asserted for one cycle1 to 32 cycles when the timer reaches the compare value programmed in ENET_TCCRn. An interrupt can be triggered if ENET_TCSRn[TIE] is set. A DMA request can be triggered if ENET_TCSRn[TDRE] is set.	I/O
ENET_1588_CLKIN	ENET_1588_CLKIN	Alternate IEEE 1588 Ethernet clock input; Clock period should be an integer number of nanoseconds	I

11 References

- AN2727
- AN3208
- AN3335
- AN4219
- AN2536
- BasicThermalWP
- MPC5748G Reference Manual
- MPC5748G Data Sheet
- MPC5748G EVB Design Specification and Schematics

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AN5220
Rev. 0
03/2016